VIDEO ICs DATABOOK

1st EDITION

JULY 1989

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

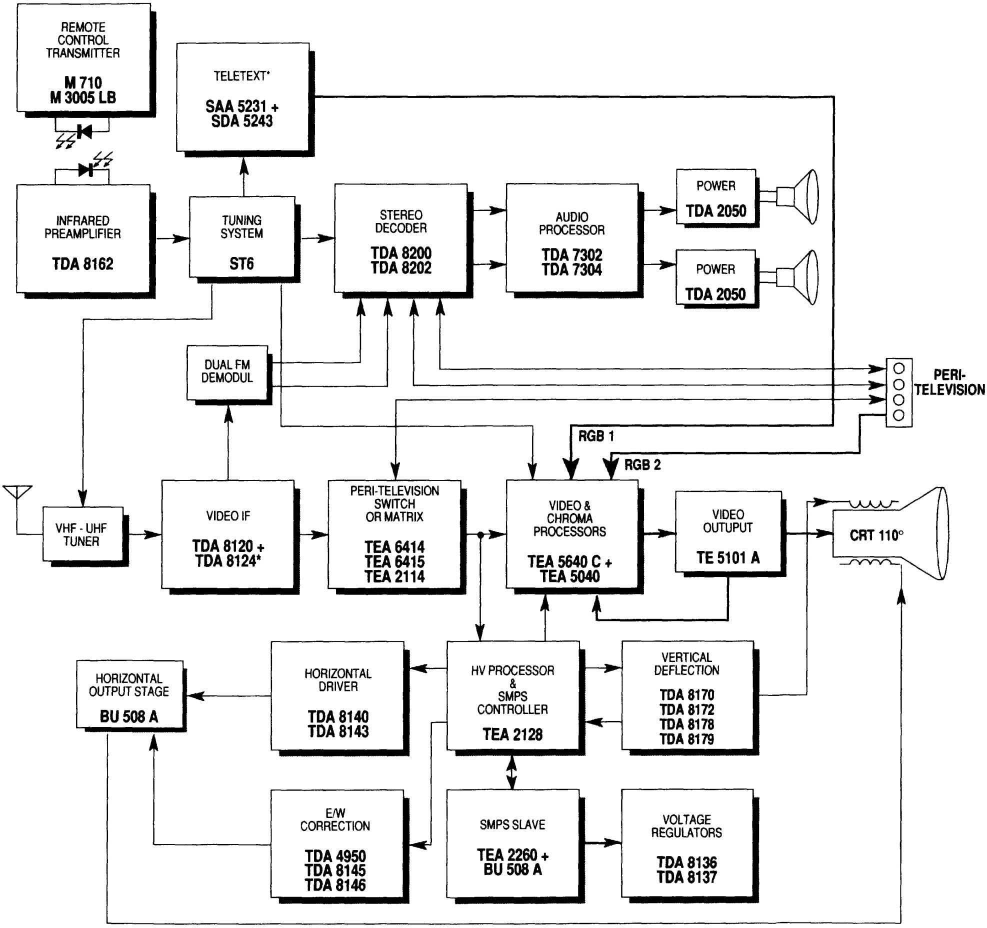
1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

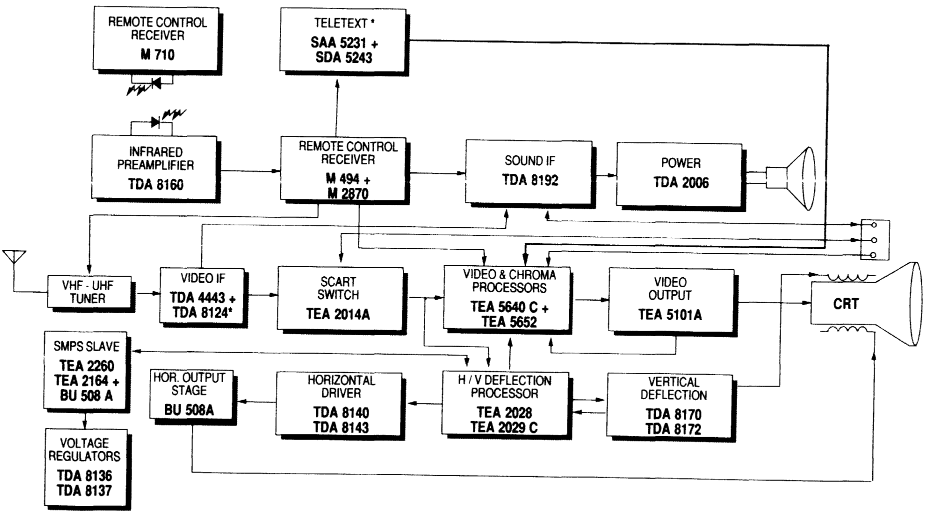
TYPICAL CONFIGURATION BLOCK DIAGRAMS

MULTISTANDARD HIGH-END CTV
(FREQUENCY SYNTHESIS - STEREO SOUND)



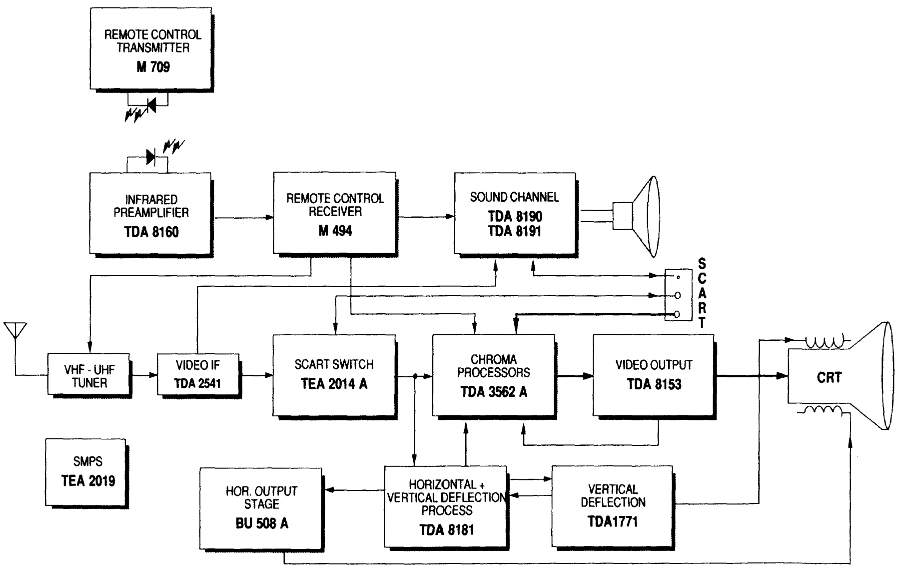
* TO BE ANNOUNCED

MULTISTANDARD COLOR TV
(VOLTAGE SYNTHESIS - AM/FM MONO SOUND)

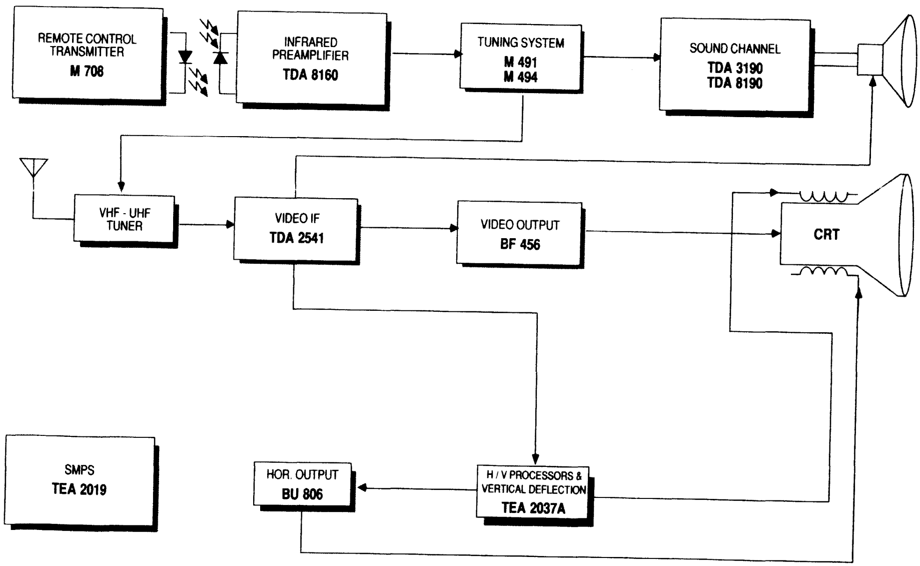


* to be announced

LOW COST PAL / NTSC COLOR TV
(VOLTAGE SYNTHESIS - FM SOUND)

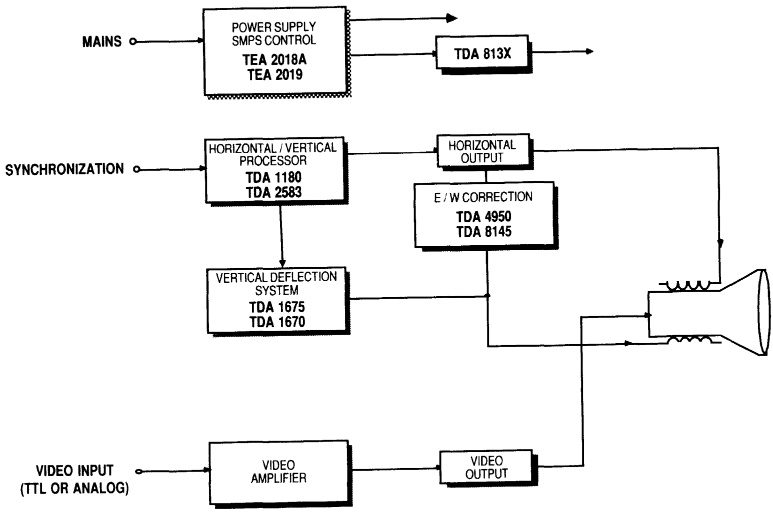


BLACK & WHITE TV



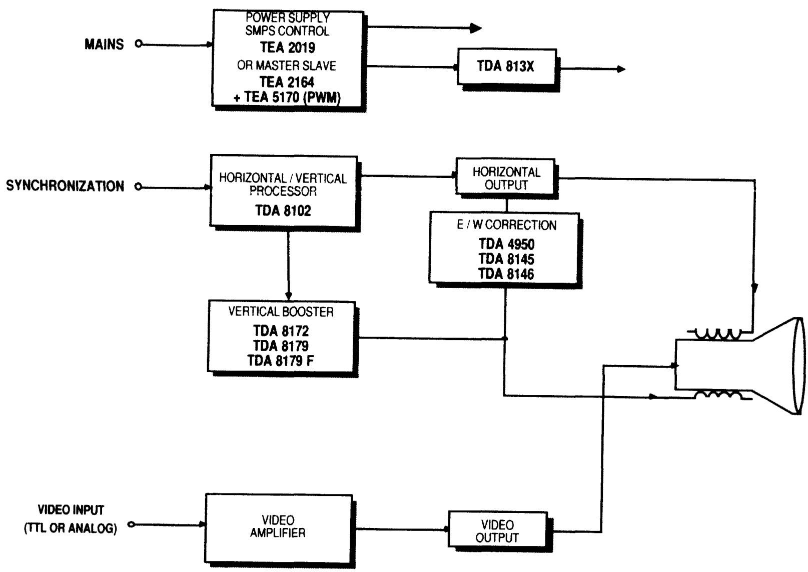
FLEXIBLE MEDIUM PERFORMANCE MONITOR

15 - 22 kHz



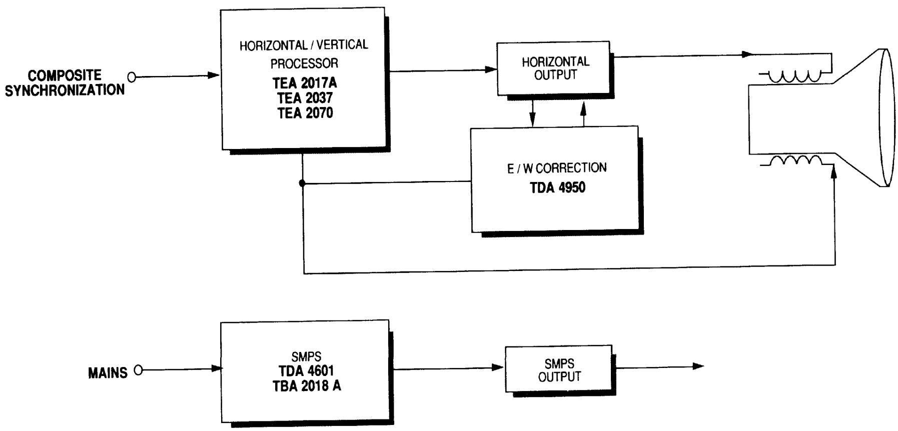
HIGH PERFORMANCE MONITOR

14 - 20" / 22 - 32 kHz
14" / 46 kHz

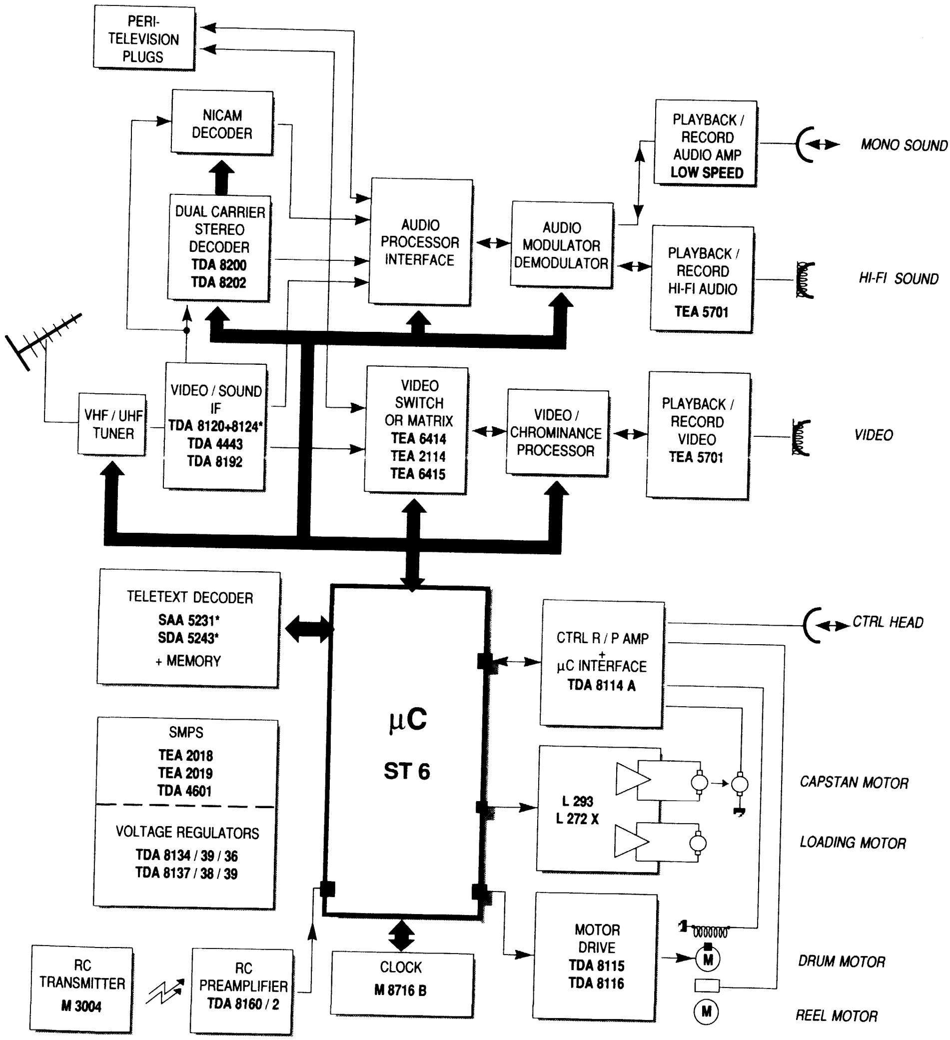


LOW COST MEDIUM PERFORMANCE MONITOR

15 - 22 kHz



MID- & HIGH-END VTR



* TO BE ANNOUCED

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

ALPHANUMERICAL INDEX

DATASHEETS

SGS-THOMSON MICROELECTRONICS

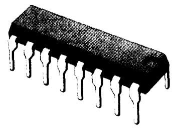
L272
L272M

DUAL POWER OPERATIONAL AMPLIFIERS

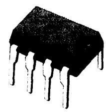
- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

The L272 and L272M are monolithic integrated circuits in powerdip and minidip packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



Powerdip (8 + 8)



Minidip Plastic

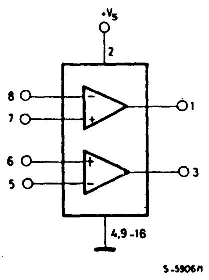
ORDERING NUMBERS:

L272 L272M

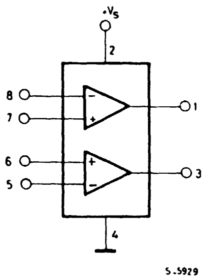
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at $T_{amb} = 80°C$ (**L272**), $T_{amb} = 50°C$ (**L272M**)	1	W
	$T_{case} = 75°C$ (**L272**)	5	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

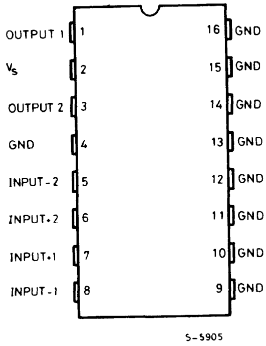


L272

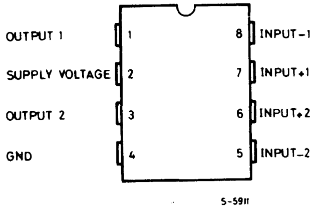


L272M

CONNECTION DIAGRAM
(Top view)

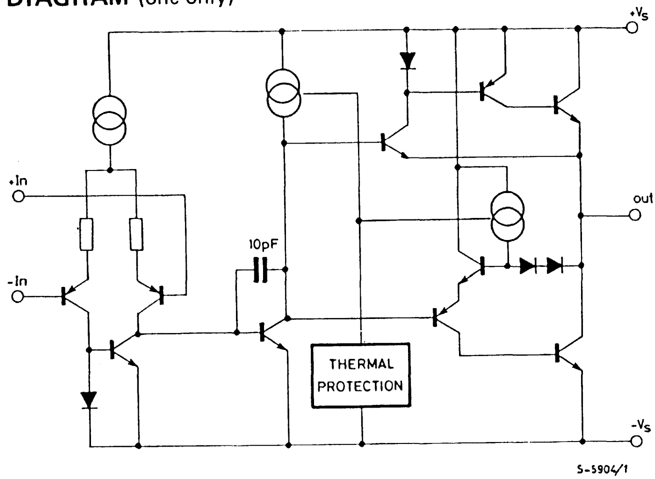


L272



L272M

SCHEMATIC DIAGRAM (one only)



THERMAL DATA

			Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	15°C/W	* 70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	70°C/W	100°C/W

* Thermal resistance junction-pin 4

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		4		28	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$; V_s = 24V		8	12	mA
		$V_o = \frac{V_s}{2}$; V_s = 12V		7.5	11	mA
I_b	Input bias current			0.3	2.5	μA
V_{os}	Input offset voltage			15	60	mV
I_{os}	Input offset current			50	250	nA
SR	Slew rate			1		V/μs
B	Gain-bandwidth product			350		KHz
R_i	Input resistance		500			KΩ
G_v	O.L. voltage gain	f = 100Hz	60	70		dB
		f = 1KHz		50		dB
e_N	Input noise voltage	B = 20KHz		10		μV
I_N	Input noise current	B = 20KHz		200		pA
CRR	Common Mode rejection	f = 1KHz	60	75		dB
SVR	Supply voltage rejection	f = 100Hz, R_G = 10KΩ, V_R = 0.5V; V_s = 24V		70		dB
		V_s = ±12V	54	62		dB
		V_s = ± 6V		56		dB
V_o	Output voltage swing	I_p = 0.1A		23		V
		I_p = 0.5A	21	22.5		V
C_s	Channel separation	f = 1KHz; R_L = 10Ω; G_v = 30dB; V_s = 24V		60		dB
		V_s = ± 6V		60		dB
d	Distortion	f = 1KHz, V_s = 24V, G_v = 30dB, R_L = ∞		0.5		%
T_{sd}	Thermal shutdown junction temperature			145		°C

Fig. 1 - Quiescent current vs. supply voltage

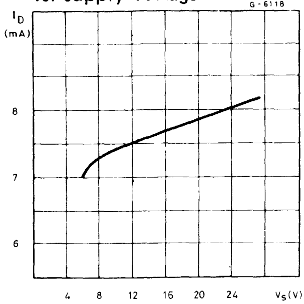


Fig. 2 -- Quiescent drain current vs. temperature

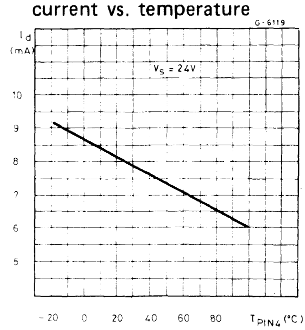


Fig. 3 - Open loop voltage gain

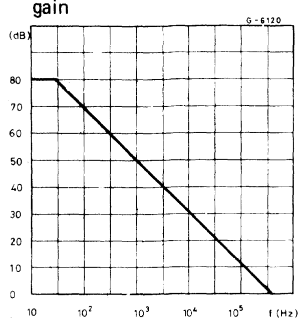


Fig. 4 - Output voltage swing vs. load current

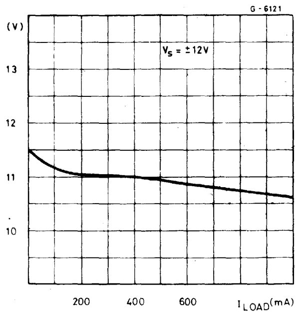


Fig. 5 -- Output voltage swing vs. load current

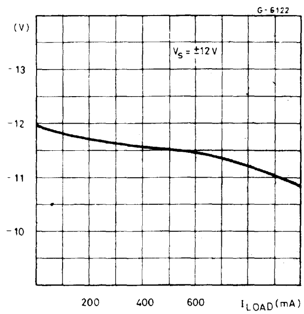


Fig. 6 - Supply voltage rejection vs. frequency

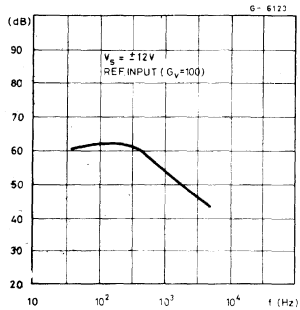


Fig. 7 - Channel separation vs. frequency

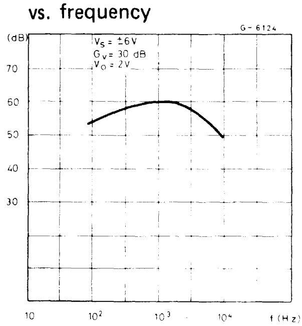
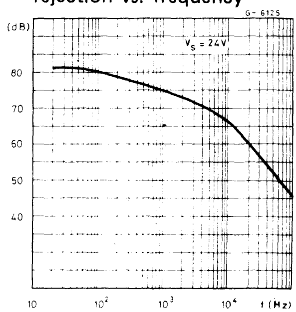


Fig. 8 -- Common mode rejection vs. frequency



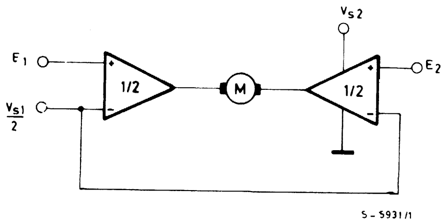
APPLICATION SUGGESTION

NOTE

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as or instance:

- layout accuracy;
- A 100nF capacitor corrected between supply pins and ground;
- boucherot cell (0.1 to 0.2μF + 1Ω series) between outputs and ground or across the load.

Fig. 9 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 10 - Servocontrol for compact-disc

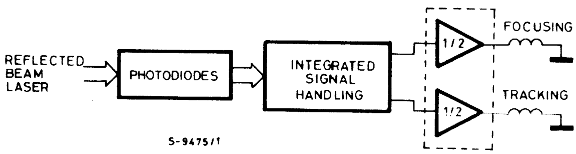


Fig. 11 - Capstan motor control in video recorders

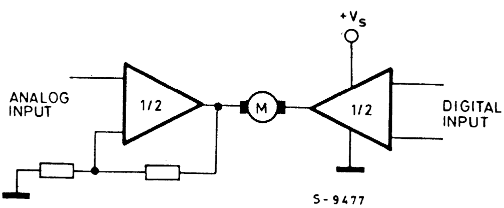
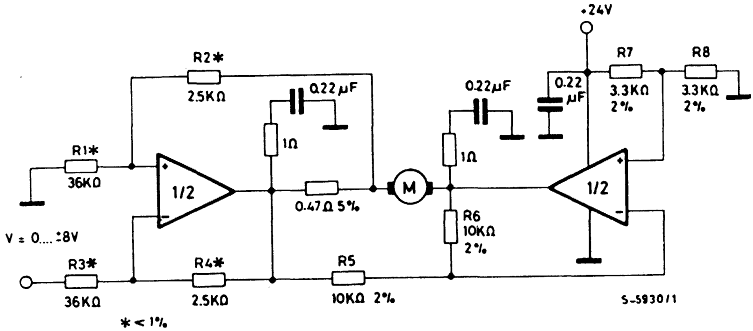


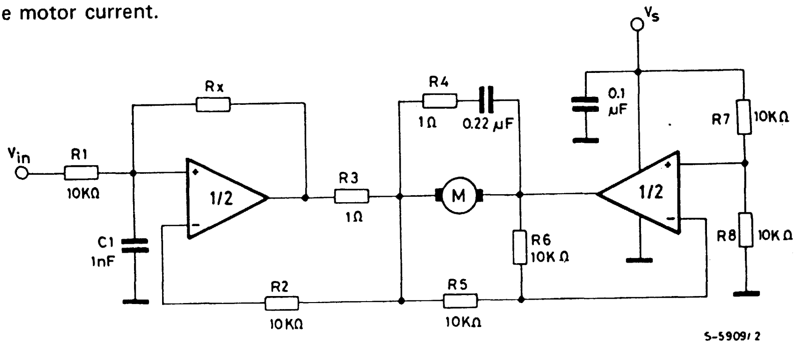
Fig. 12 - Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 13 - Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\ (V_i - \frac{V_s}{2}) + |R_o| \cdot I_M$ where $|R_o| = \frac{2R3 \circ R1}{R_X}$ and I_M is the motor current.



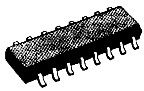
SGS-THOMSON
MICROELECTRONICS

L272D

DUAL POWER OPERATIONAL AMPLIFIERS

ADVANCE DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN



SO-16J

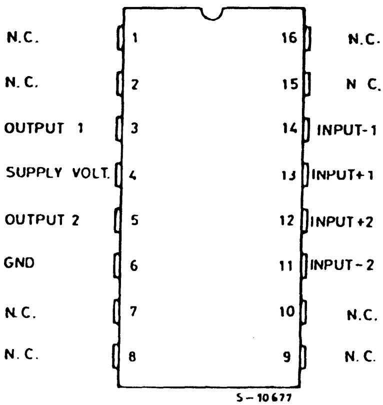
ORDER CODE : L272D

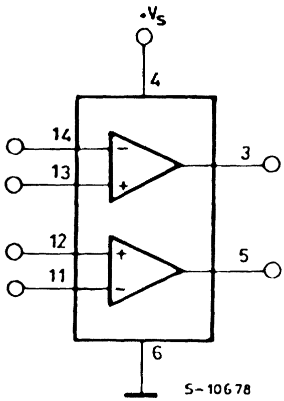
DESCRIPTION

The L272D is a monolithic integrated circuit in SO-16 packages intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies, compact disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

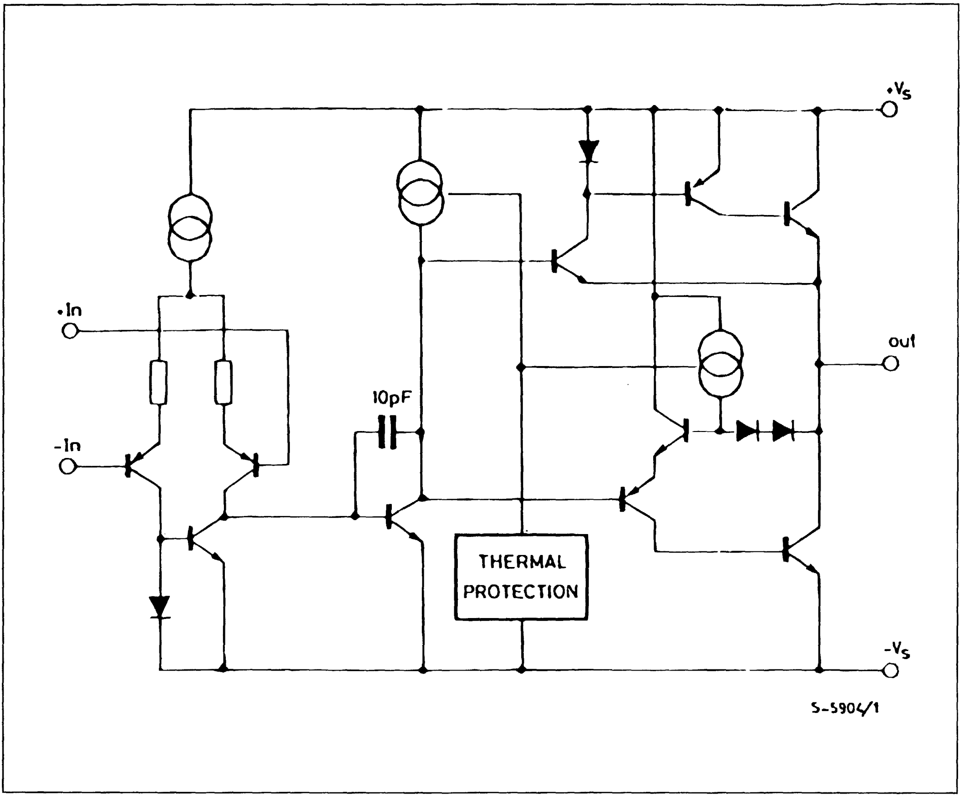
PIN CONNECTION AND BLOCK DIAGRAM





This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SCHEMATIC DIAGRAM (one only)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	$\pm V_s$	
I_o	DC Output Current	1	A
I_p	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Power Dissipation at T_{case} = 90°C	1.2	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{thj\text{-}alumina}$(*)	Thermal Resistance Junction-alumina	Max.	50	°C/W

(*) Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15 x 20 mm ; 0.65 mm thickness and infinite heathsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		4		28	V
I_s	Quiescent Drain Current	$V_o = \frac{V_s}{2}$ V_s = 24V		8	12	mA
		$V_o = \frac{V_s}{2}$ V_s = 12V		7.5	11	mA
I_b	Input Bias Current			0.3	2.5	µA
V_{os}	Input Offset Voltage			15	60	mV
I_{os}	Input Offset Current			50	250	nA
SR	Slew Rate			1		V/µs
B	Gain-bandwidth Product			350		KHz
R_i	Input Resistance		500			KΩ
G_v	O. L. Voltage Gain	f = 100Hz	60	70		dB
		f = 1KHz		50		dB
e_N	Input Noise Voltage	B = 20KHz		10		µV
I_N	Input Noise Current	B = 20KHz		200		pA
CRR	Common Mode Rejection	f = 1KHz	60	75		dB
SVR	Supply Voltage Rejection	f = 100Hz V_s = 24V R_G = 10KΩ V_s = ± 12V V_R = 0.5V V_s = ± 6V	 54 	70 62 56		dB dB dB
V_o	Output Voltage Swing	I_p = 0.1A I_p = 0.5A	 21	23 22.5		V V
C_s	Channel Separation	f = 1KHz ; R_L = 10Ω ; G_v = 30dB V_s = 24V V_s = ± 6V		 60 60		 dB dB
d	Distortion	f = 1KHz G_v = 30dB V_s = 24V R_L = ∞		0.5		%
T_{sd}	Thermal Shutdown Junction Temperature			145		°C

Figure 1 : Quiescent Current vs. Supply Voltage.

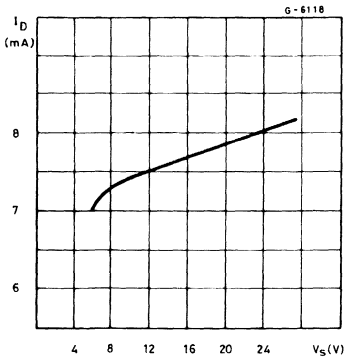


Figure 2 : Quiescent Drain Current vs. Temperature.

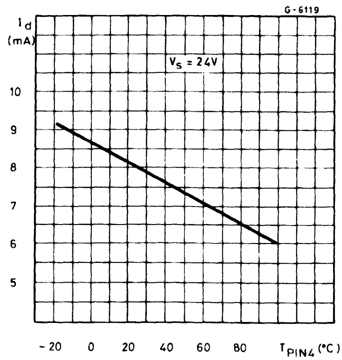


Figure 3 : Open Loop Voltage Gain.

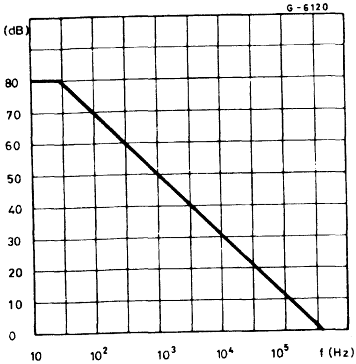


Figure 4 : Output Voltage Swing vs.Load Current.

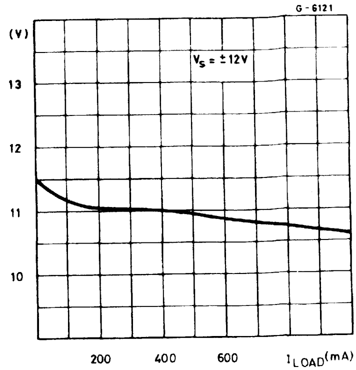


Figure 5 : Output Voltage Swing vs. Load Current.

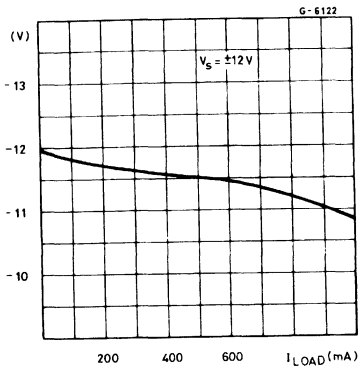


Figure 6 : Supply Voltage Rejection vs. Frequency.

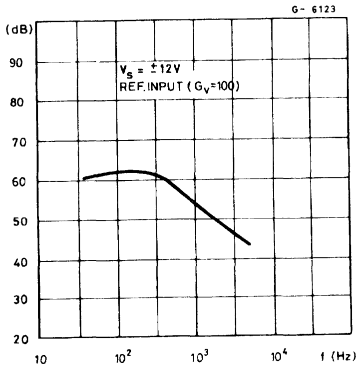


Figure 7 : Channel Separation vs. Frequency.

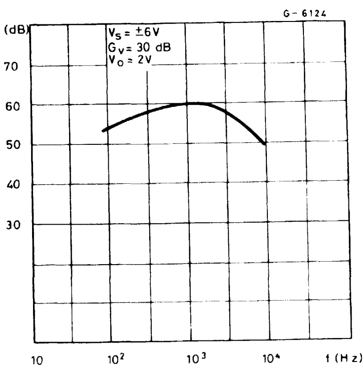
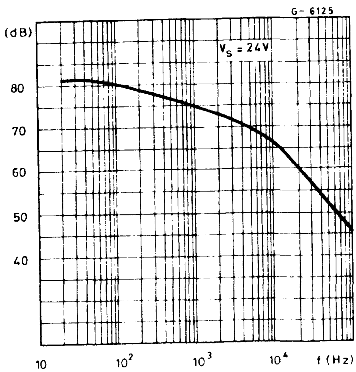


Figure 8 : Common Mode Rejection vs. Frequency.



SGS-THOMSON MICROELECTRONICS

L2720/2/4

LOW DROP DUAL POWER OPERATIONAL AMPLIFIERS

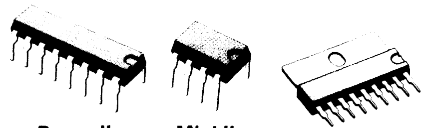
PRELIMINARY DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE

The L2720, L2722 and L2724 are monolithic integrated circuits in powerdip, minidip and SIP-9 packages, intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

They are particularly indicated for driving, inductive loads, as motor and finds applications in compact-disc VCR automotive, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.



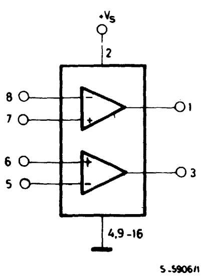
Powerdip (8 + 8) | **Minidip Plastic** | **SIP-9**

ORDERING NUMBERS:
L2720 L2722 L2724

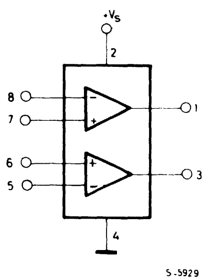
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	28	V
V_s	Peak supply voltage (50ms)	50	V
V_I	Input voltage	V_s	
V_I	Differential input voltage	$\pm V_s$	
I_o	DC output current	1	A
I_p	Peak output current (non repetitive)	1.5	A
P_{tot}	Power dissipation at T_{amb} = 80°C (L2720), T_{amb} = 50°C (L2722)	1	W
	T_{case} = 75°C (L2720)	5	W
	T_{case} = 50°C (L2724)	10	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAMS



L2720



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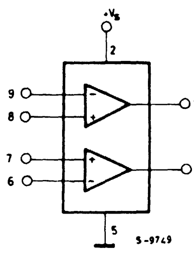
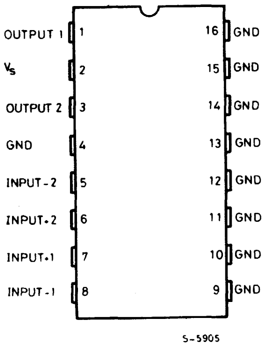


L2724

CONNECTION DIAGRAMS
(Top view)



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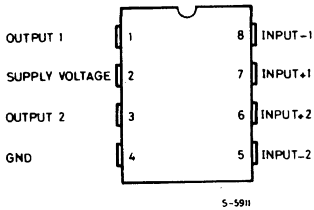

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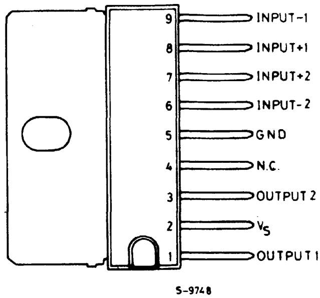
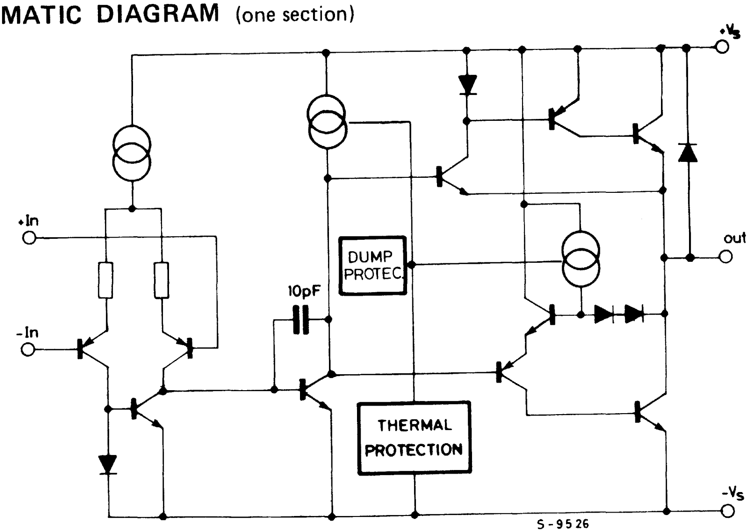


L2724

SCHEMATIC DIAGRAM (one section)



THERMAL DATA			SIP-9	Powerdip	Minidip
$R_{th\ j\text{-}case}$	Thermal resistance junction-pins	max	10°C/W	15°C/W	*70°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-albient	max	70°C/W	70°C/W	100°C/W

* Thermal resistance junction-pin 4.

ELECTRICAL CHARACTERISTICS ($V_s = 24V$, $T_{amb} = 25°C$ unless otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single supply voltage			4		28	V
V_s	Split supply voltage			± 2		± 14	V
I_s	Quiescent drain current	$V_o = \frac{V_s}{2}$	$V_s = 24V$		10	15	mA
			$V_s = 8V$		9	15	mA
I_b	Input bias current				0.2	1	μA
V_{os}	Input offset voltage					10	mV
I_{os}	Input offset current					100	nA
SR	Slew rate				2		V/μs
B	Gain-bandwidth product				1.2		MHz
R_i	Input resistance			500			KΩ
G_v	O.L. voltage gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input noise voltage	B = 22Hz to 22KHz			10		μV
I_N	Input noise current	B = 22Hz to 22KHz			200		pA
CMR	Common Mode rejection	f = 1KHz		66	84		dB
SVR	Supply voltage rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	$V_s = 24V$ $V_s = \pm 12V$ $V_s = \pm 6V$	60	70 75 80		dB dB dB
$V_{DROP\ (HIGH)}$		$V_s = \pm 2.5V$ to $\pm 12V$	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP\ (LOW)}$		$V_s = \pm 2.5V$ to $\pm 12V$	I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel separation	f = 1KHz R_L = 10Ω G_v = 30dB	$V_s = 24V$		60		dB
			$V_s = 6V$		60		dB
T_{sd}	Thermal shutdown junction temperature				145		°C

Fig. 1 - Quiescent current vs. supply voltage

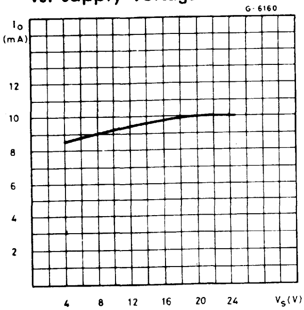


Fig. 2 - Open loop gain vs. frequency

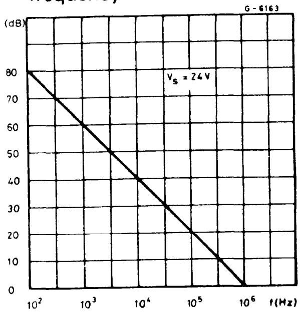


Fig. 3 - Common mode rejection vs. frequency

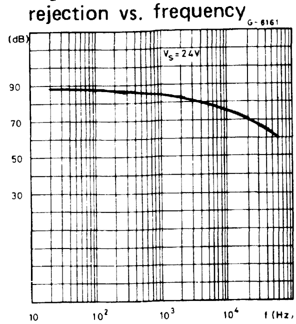


Fig. 4 - Output swing vs. load current (V_s = ± 5V)

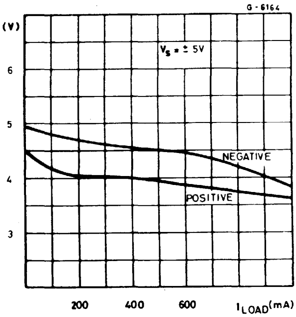


Fig. 5 - Output swing vs. load current (V_s = ± 12V)

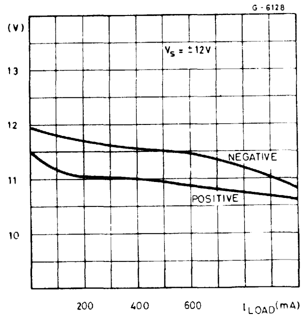


Fig. 6 - Supply voltage rejection vs. frequency

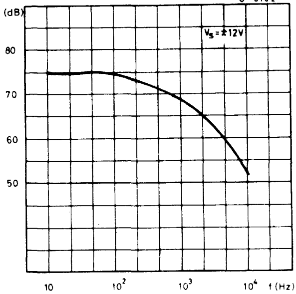
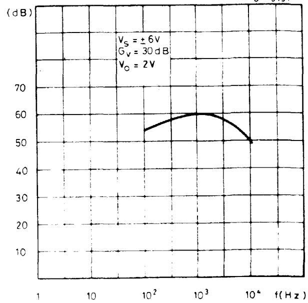


Fig. 7 - Channel separation vs. frequency



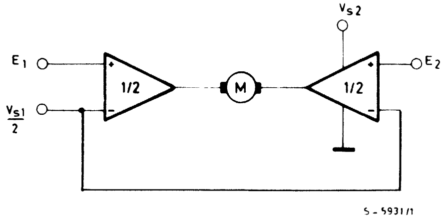
SGS-THOMSON MICROELECTRONICS

APPLICATION SUGGESTION

In order to avoid possible instability occurring into final stage the usual suggestions for the linear power stages are useful, as for instance:

- layout accuracy;
- A 100nF capacitor connected between supply pins and ground;
- boucherot cell (0.1 to 0.2 μF + 1Ω series) between outputs and ground or across the load. With single supply operation, a resistor (1KΩ) between the output and supply pin can be necessary for stability.

Fig. 8 - Bidirectional DC motor control with μP compatible inputs



V_{S1} = logic supply voltage

Must be $V_{S2} > V_{S1}$

E1, E2 = logic inputs

Fig. 9 - Servocontrol for compact-disc

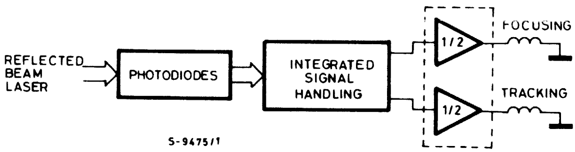


Fig. 10 - Capstan motor control in video recorders

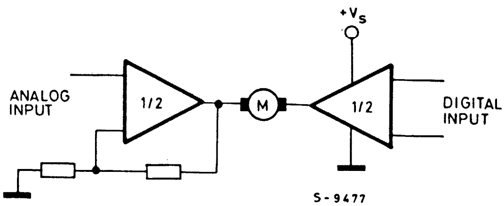
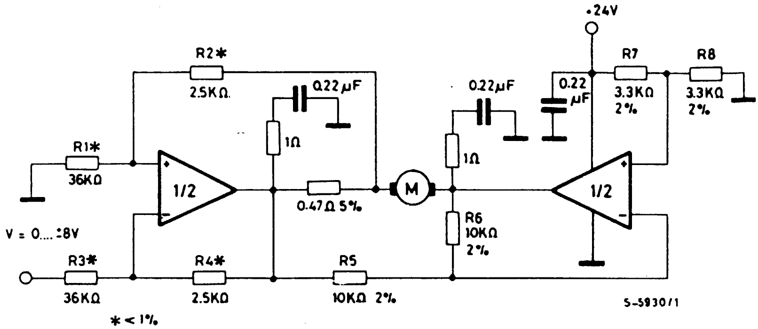


Fig. 11 – Motor current control circuit



Note: The input voltage level is compatible with L291 (5-BIT D/A converter)

Fig. 12 – Bidirectional speed control of DC motors.

For circuit stability ensure that $R_X > \frac{2R3 \circ R1}{R_M}$ where R_M = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\left(V_i - \frac{V_s}{2}\right) + |R_o| \cdot I_M$ where $|R_o| = \frac{2R \circ R1}{R_X}$ and I_M is the motor current.

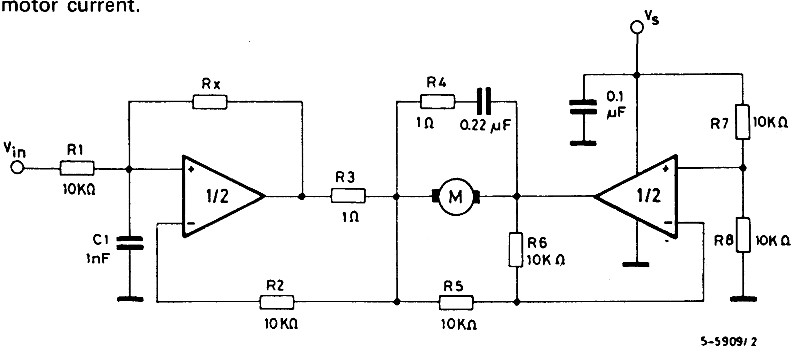
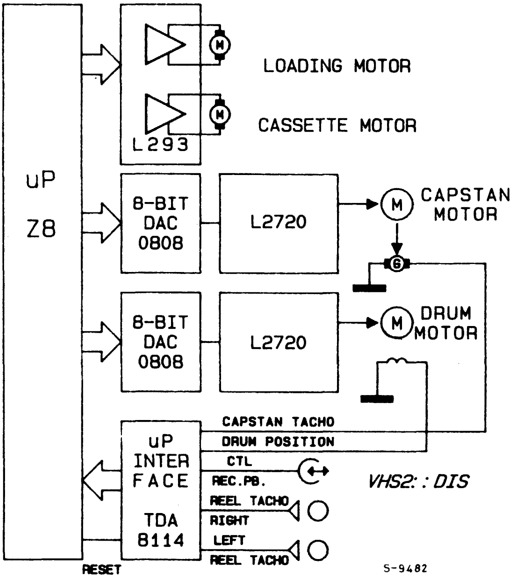


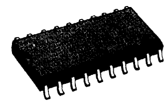
Fig. 13 - VHS-VCR Motor control circuit



LOW DROP DUAL POWER OPERATIONAL AMPLIFIER

ADVANCE DATA

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- LOW INPUT OFFSET VOLTAGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN
- CLAMP DIODE



SO-20
(12 + 4 + 4)

ORDER CODE : L2726

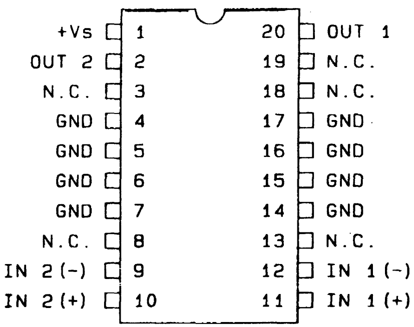
DESCRIPTION

The L2726 is a monolithic integrated circuit in SO-20 package intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies.

It is particularly indicated for driving inductive loads, as motor and finds applications in compact-disc VCR automative, etc.

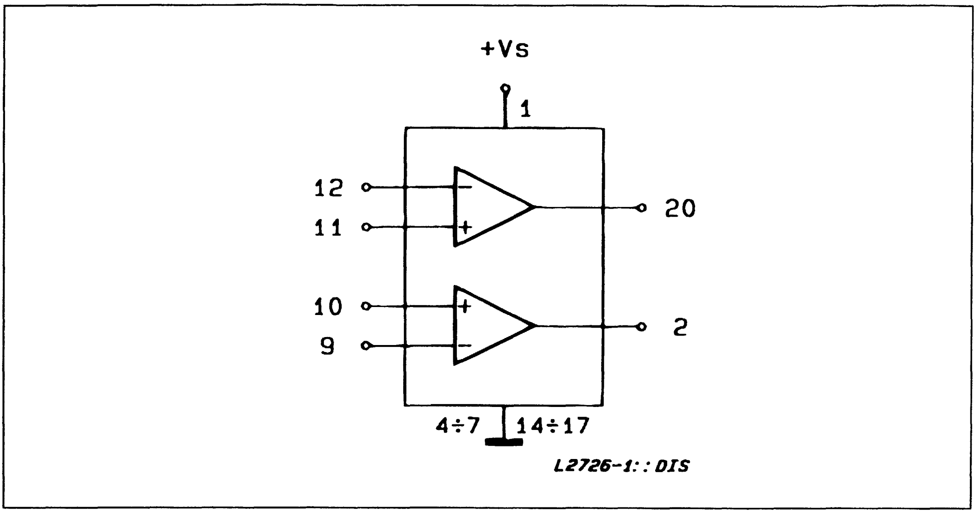
The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

PIN CONNECTION (top view)

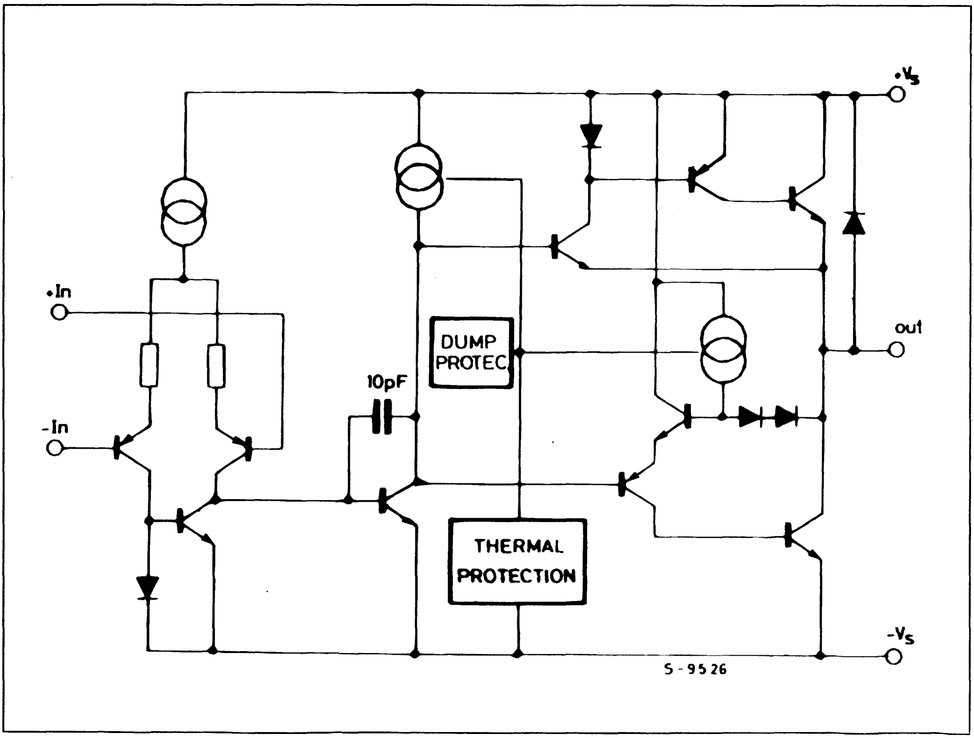


L2726-2: : DIS

BLOCK DIAGRAM



SCHEMATIC DIAGRAM (one section)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
V_s	Peak Supply Voltage (50ms)	50	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	$\pm V_s$	
I_O	DC Output Current	1	A
I_p	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Power Dissipation at T_{amb} = 85°C T_{case} = 75°C	1 5	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	15.0	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient (*)	Max	65	°C/W

(*) With 4 sq. cm copper area heatsink.

ELECTRICAL CHARACTERISTICS (V_s = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Single Supply Voltage			4		28	V
V_s	Split Supply Voltage			± 2		± 14	V
I_s	Quiescent Drain Current	$V_o = \frac{V_s}{2}$	V_s = 24V		10	15	mA
			V_s = 8V		9	15	mA
I_b	Input Bias Current				0.2	1	µA
V_{os}	Input Offset Voltage					10	mV
I_{os}	Input Offset Current					100	nA
SR	Slew Rate				2		V/µs
B	Gain-bandwidth Product				1.2		MHz
R_i	Input Resistance			500			KΩ
G_v	O. L. Voltage Gain	f = 100Hz		70	80		dB
		f = 1KHz			60		dB
e_N	Input Noise Voltage	B = 22Hz to 22KHz			10		µV
I_N	Input Noise Current	B = 22Hz to 22KHz			200		pA
CMR	Common Mode Rejection	f = 1KHz		66	84		dB
SVR •	Supply Voltage Rejection	f = 100Hz R_G = 10KΩ V_R = 0.5V	V_s = 24V V_s = ± 12V V_s = ± 6V	60	70 75 80		dB dB dB
$V_{DROP(HIGH)}$		V_s = ± 2.5V to ± 12V	I_p = 100mA		0.7		V
			I_p = 500mA		1.0	1.5	V
$V_{DROP(LOW)}$			I_p = 100mA		0.3		V
			I_p = 500mA		0.5	1.0	V
C_s	Channel Separation	f = 1KHz R_L = 10Ω G_v = 30dB	V_s = 24V		60		dB
			V_s = 6V		60		dB
T_{sd}	Thermal Shutdown Junction Temperature				145		°C

Figure 1 : Quiescent Current vs. Supply Voltage.

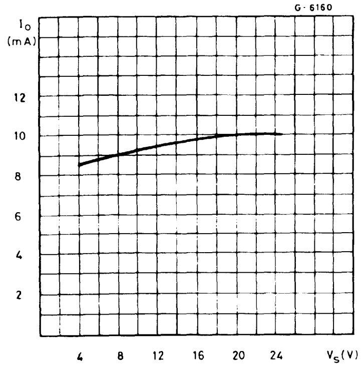


Figure 2 : Open Loop Gain vs. Frequency.

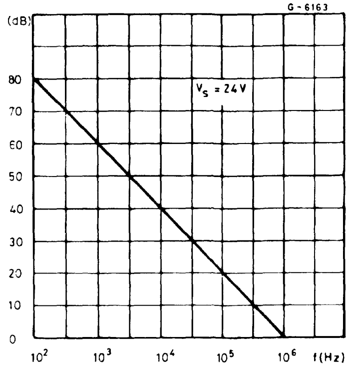


Figure 3 : Common Mode Rejection vs. Frequency.

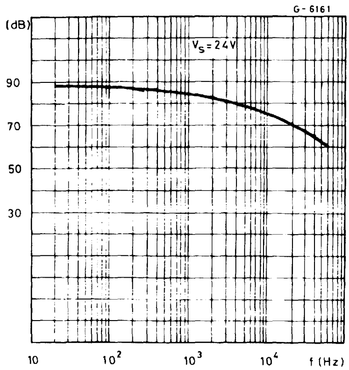


Figure 4 : Output Swing vs. Load Current ($V_S = \pm 5V$).

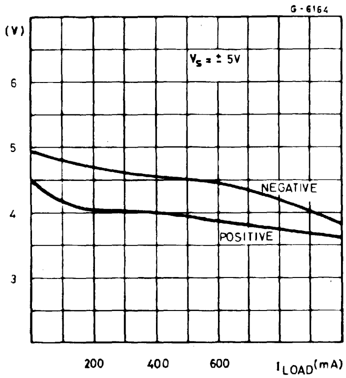


Figure 5 : Output Swing vs. Load Current ($V_S = \pm 12$ V).

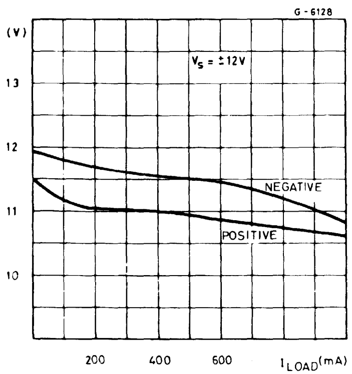


Figure 6 : Supply Voltage Rejection vs. Frequency.

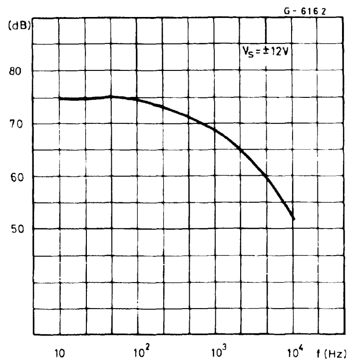
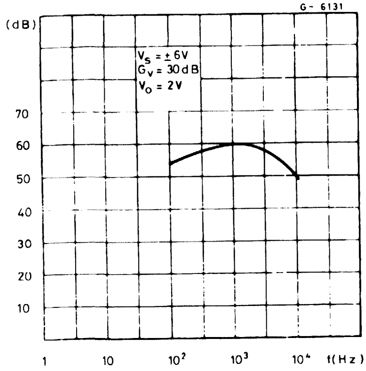


Figure 7 : Channel Separation vs. Frequency.



SGS-THOMSON
MICROELECTRONICS

L4901A

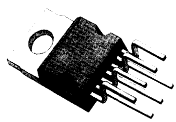
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 400mA
  I_{02} = 400mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4901A is a monolithic low drop dual 5V regulator designed mainly tor supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



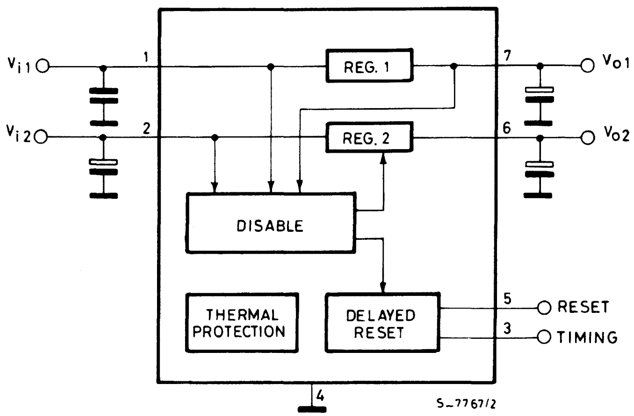
Heptawatt

ORDERING NUMBER: L4901A

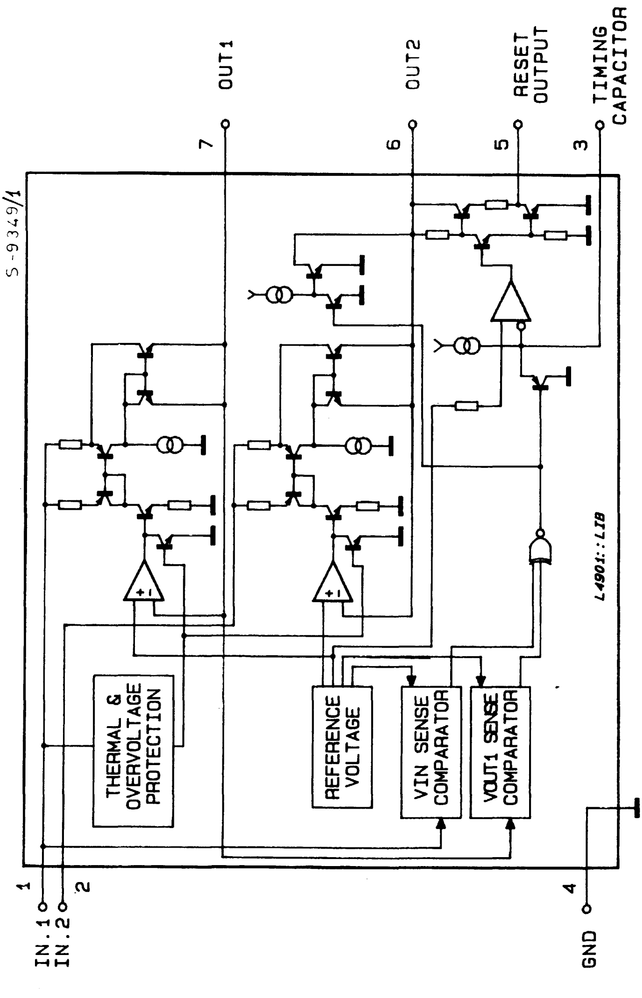
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

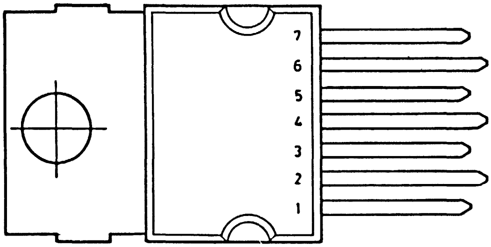
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



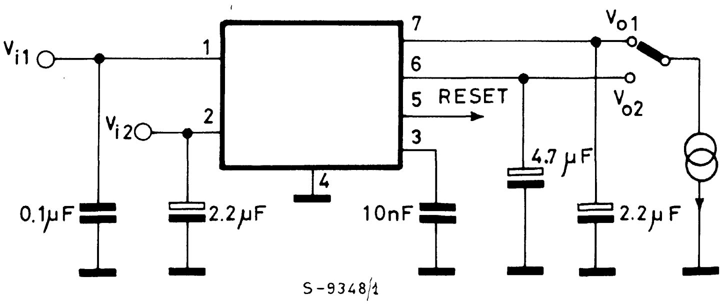
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 400mA regulator input.
2	INPUT 2	400mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) = C_t (nF)
6	OUTPUT 2	5V - 400mA regulator output. Enabled if $V_{O\,1} > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 400mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_{IN1} = V_{IN2}$ = 14,4V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	400			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	400			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+ 1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 400mA		50	100	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 400mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leq$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leq$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4901A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

- an input overvoltage
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator;
- very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

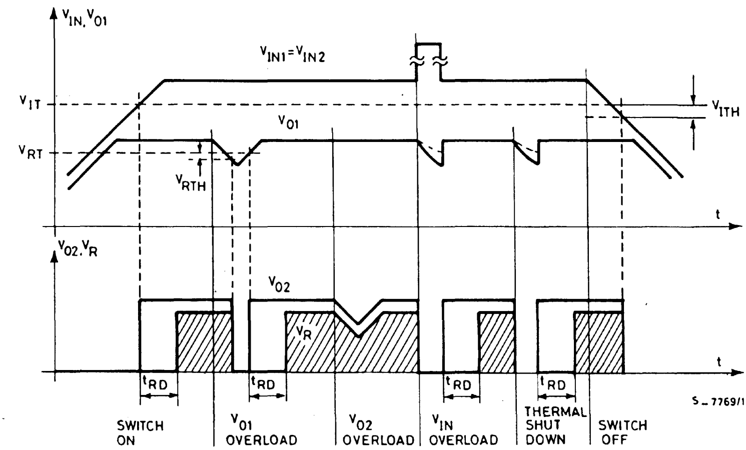
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4901A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

The L4901A is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in fig. 5 the reset output is used both to disable the μP and, through the address decoder M74HC138, to ensure that the RAMS are disabled as soon as the main supply starts to fall.

Another interesting application of the L4901A is in μP system with shadow memories. (see fig. 6)

When the input voltage goes below V_{IT}, the reset output enables the execution of a routine that saves the machine's state in the shadow RAM (xicor x 2201 for example).

Thanks to the low consumption of the Reg. 1 a 680μF capacitor on its input is sufficient to provide enough energy to complete the operation. The diode on the input guarantees the supply of the equipment even if a short circuit on V_I occurs.

APPLICATION SUGGESTION (continued)

Fig. 2

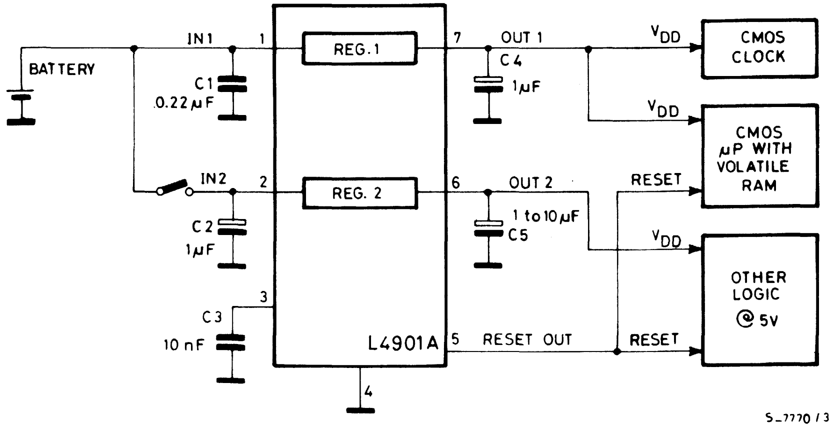
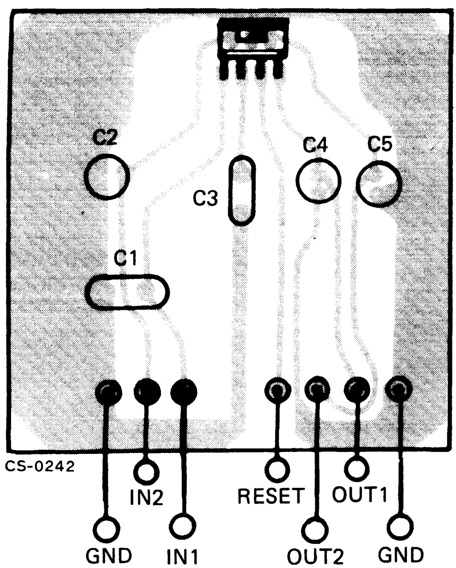


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

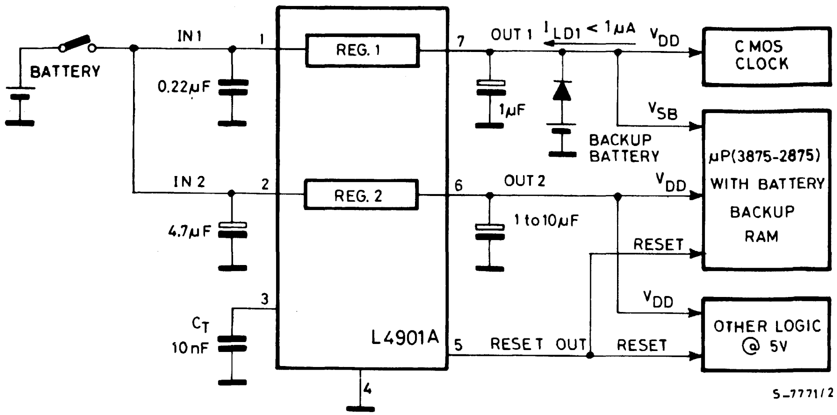
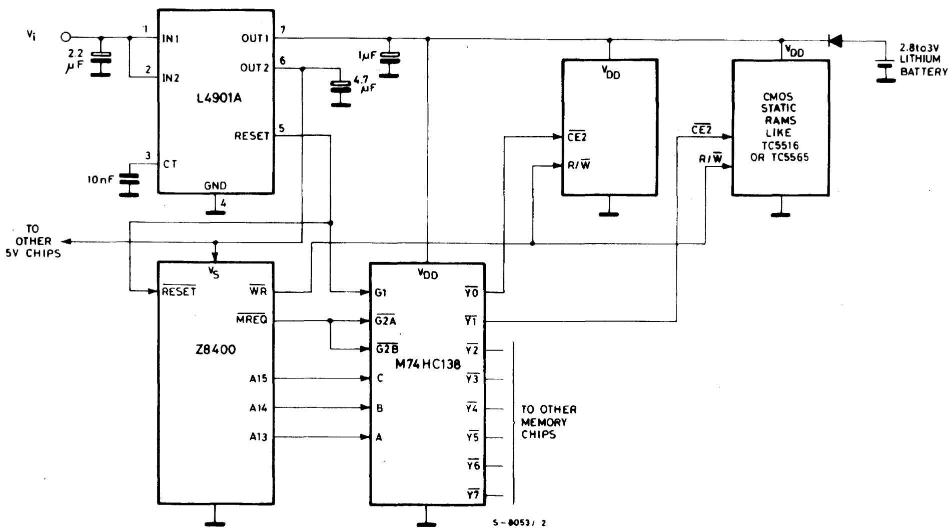


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6

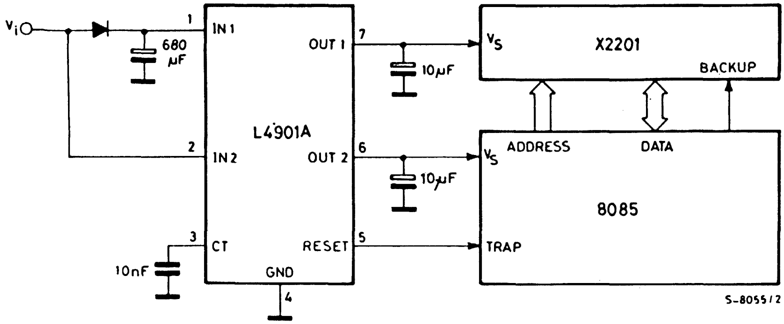


Fig. 7 - Quiescent current (Reg. 1) vs. output current

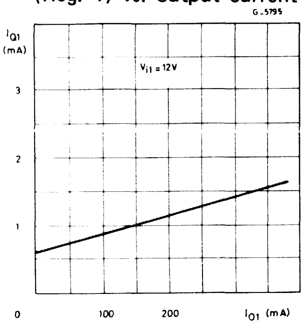


Fig. 8 - Quiescent current (Reg. 1) vs. input voltage

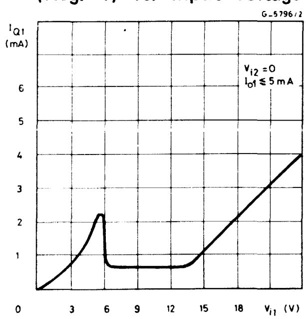


Fig. 9 - Total quiescent current vs. input voltage

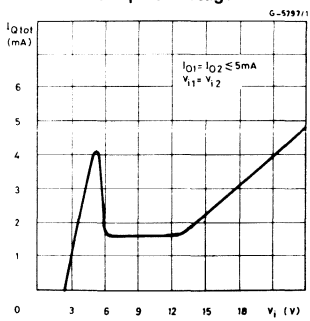


Fig. 10 - Regulator 1 output current and short circuit current vs. input voltage

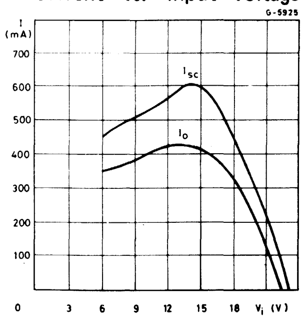


Fig. 11 - Regulator 2 output current and short circuit current vs. input voltage

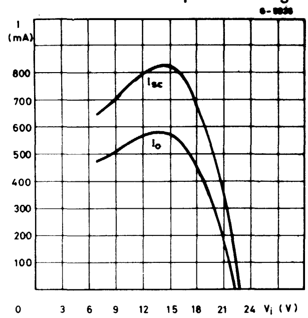
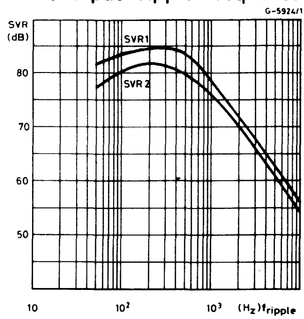


Fig. 12 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence

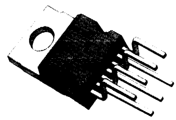


DUAL 5V REGULATOR WITH RESET AND DISABLE

PRELIMINARY DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: I_{01} = 300mA
  I_{02} = 300mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- RESET OUTPUT NORMALLY HIGH
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4902A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.
Reset and data save functions and remote switch on/off control can be realized.



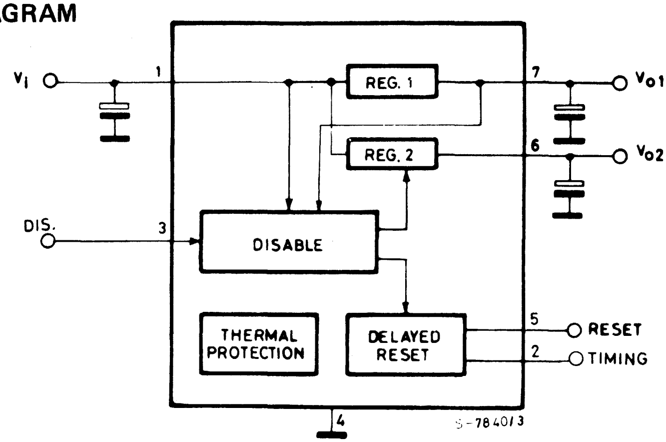
Heptawatt

ORDERING NUMBER: L4902A

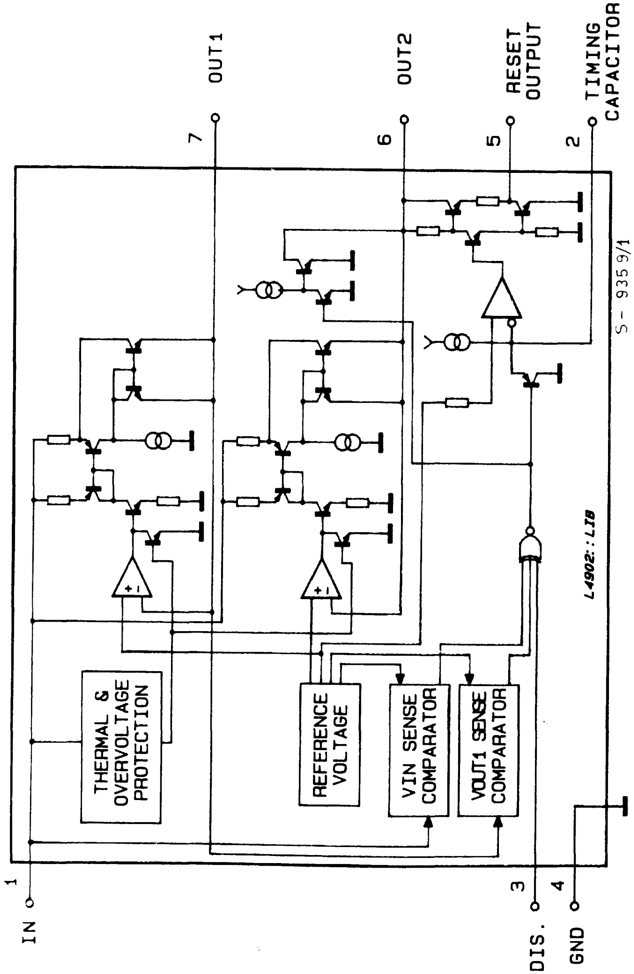
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

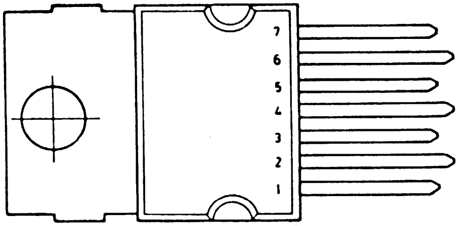
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



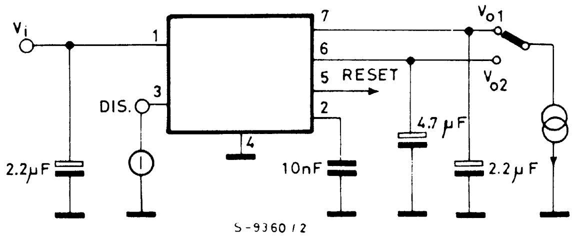
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Regulators common input.
2	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 5μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
3	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disable output Reg. 2.
4	GND	Common ground.
5	RESET OUTPUT	When pin 2 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) $= C_t$ (nF).
6	OUTPUT 2	5V - 300mA regulator output. Enabled if $V_O\ 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 300mA. Low leakage (in switch-OFF condition) output.

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max.	ΔV_{01} = -100mV	300			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	μA
I_{02}	Output current 2 max.	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 300mA		0.7 0.8 1.1	0.8 1 1.4	V V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 300mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	80	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = I_{02} $\leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -1mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 -30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R=0.5V I_o = 100mA	50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4902A makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with common inputs plus a reset output for the data save function and a Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:
- a high level ($> V_{DT}$) is applied on pin 3;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:
- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down condition.

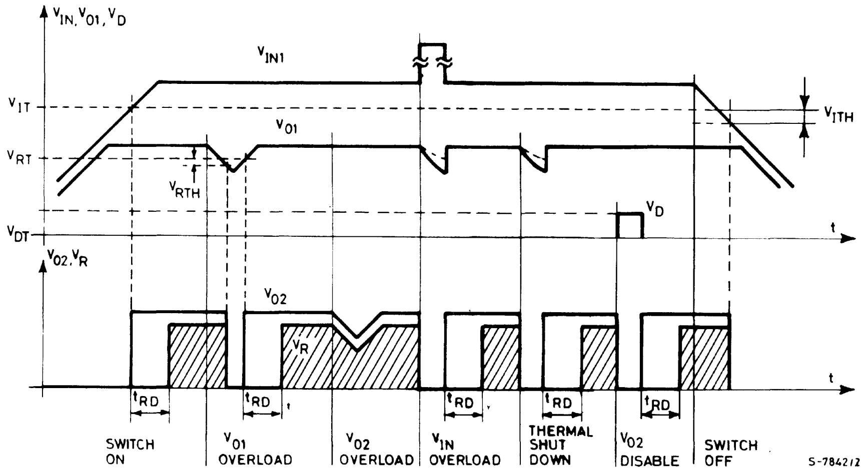
This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.
The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



APPLICATION SUGGESTION

Fig. 2 illustrate how the L4902A's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Another application for the L4902A is supplying a shadow-ram microcomputer chip (SGS M38SH72 for exemple) where a fast NV memory is backed up on chip by a EEPROM when a low level on the reset output occurs.

By adding two CMOS-SCHMIDT-TRIGGER and few external components, also a watch dog function may be realized (see fig. 5). During normal operation the microsystem supplies a periodical pulse waveform; if an anomalous condition occours (in the program or in the system), the pulses will be absent and the disable input will be activated after a settling time determined by R1 C1. In this condition all the circuitry connected to V_{02} will be disabled, the system will be restarted with a new reset front.

The disable of V_{02} prevent spurious operation during microprocessor malfunctioning.

APPLICATION SUGGESTION (continued)

Fig. 2

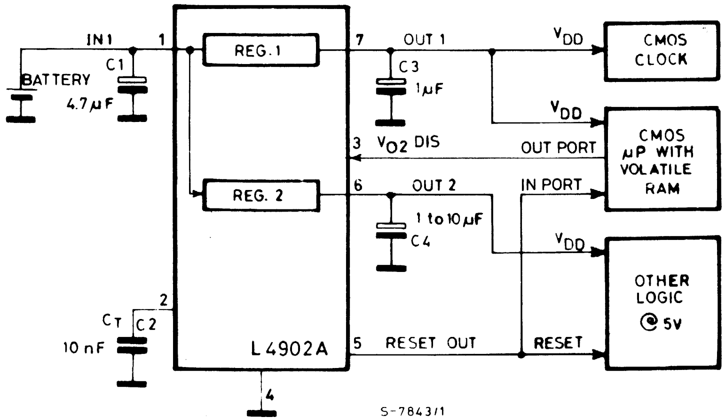
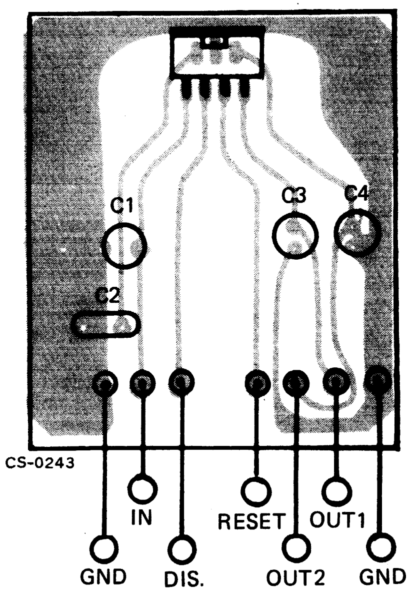


Fig. 3 - P.C. board and component layout of the circuit of Fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

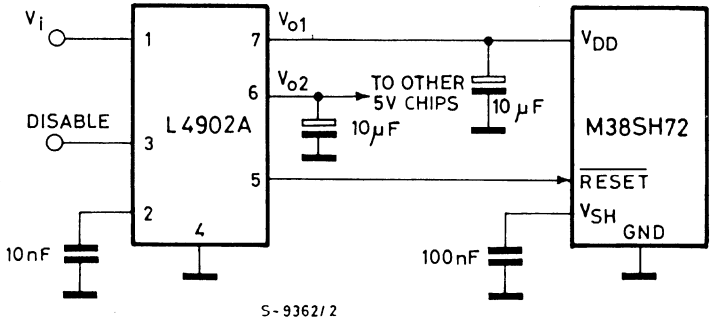
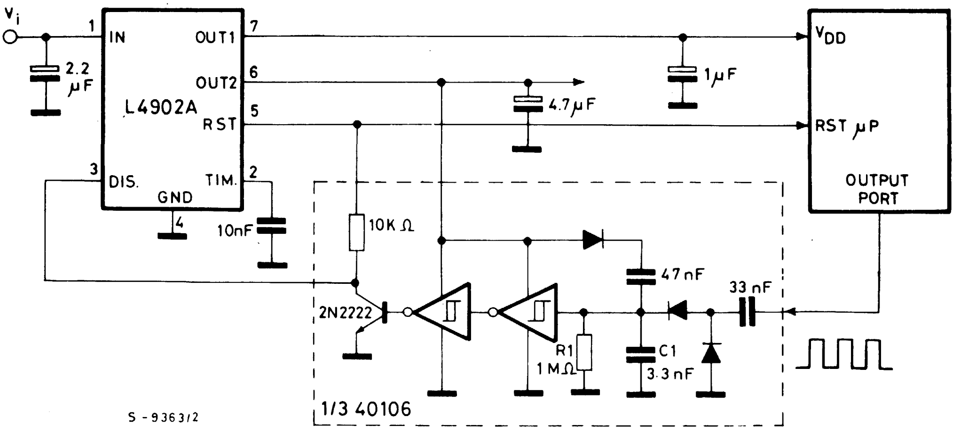


Fig. 5



APPLICATION SUGGESTION (continued)

Fig. 6 - Quiescent current vs. output current

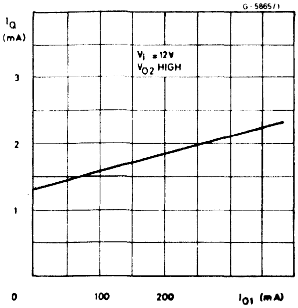


Fig. 7 - Quiescent current vs. input voltage

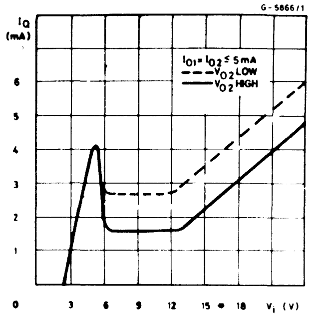
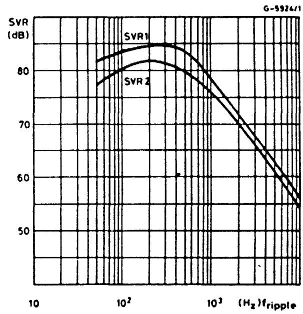


Fig. 8 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



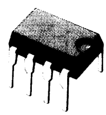
DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4903 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.



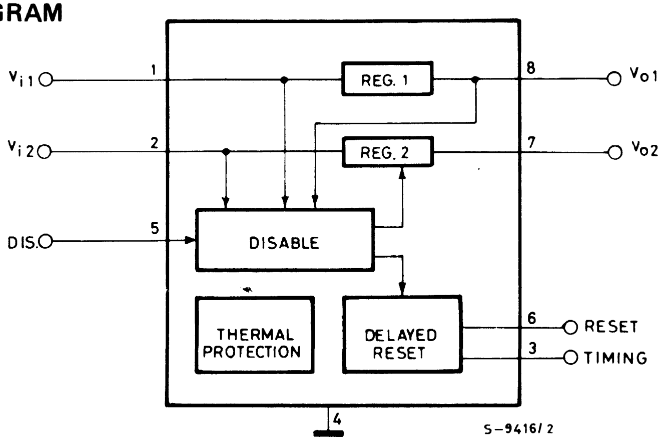
Minidip Plastic

ORDERING NUMBER: L4903

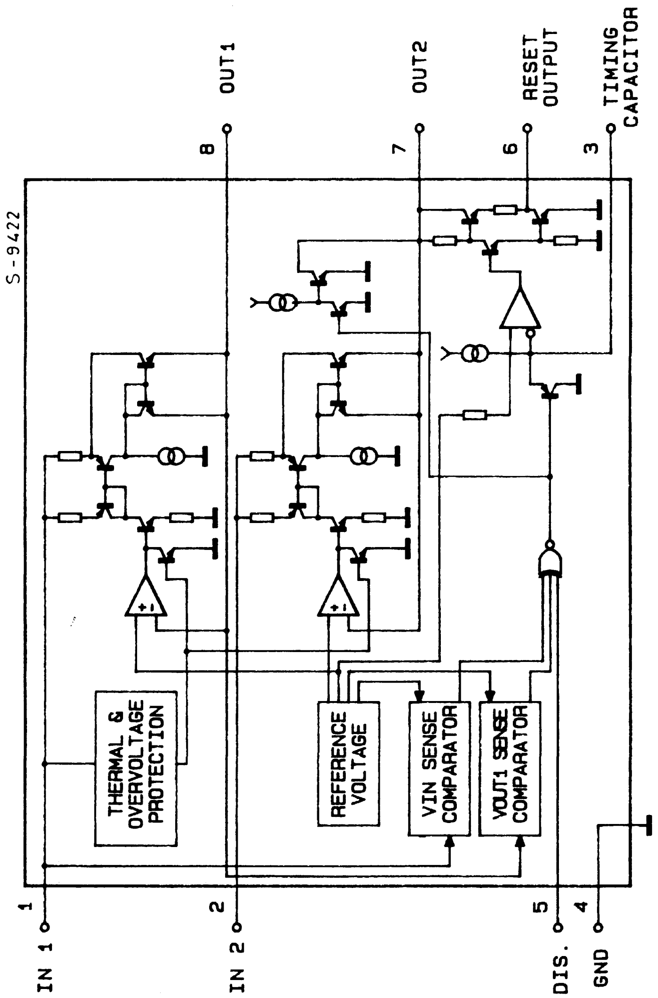
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
V_t	Transient input overvoltage (t = 40 ms)	60	V
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

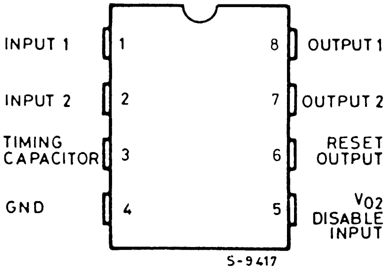


SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top view)



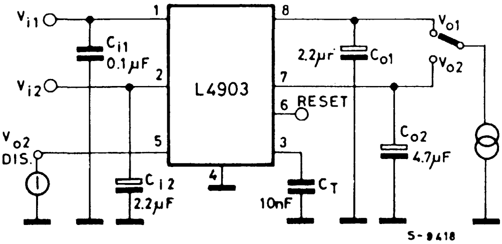
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	V_{02} DISABLE INPUT	A high level ($> V_{DT}$) disables output Reg. 2.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O\ 1 > V_{RT}$. DISABLE INPUT $< V_{DT}$ and $V_{IN\ 2} > V_{IT}$. If Reg. 2 is switched OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

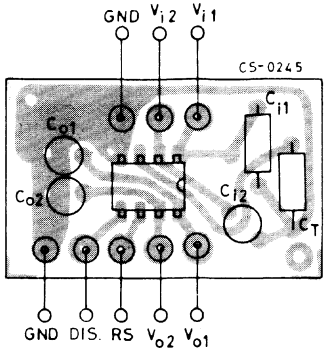
THERMAL DATA

$R_{th\ j\text{-}pin}$	Thermal resistance junction-pin 4	max	70	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1 max. (*)	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leq$ 3V			1	µA
I_{02}	Output current 2 max. (*)	ΔV_{02} = -100mV	100			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hysteresis			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	V_{IN1} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH I_{01} = $I_{02} \leq$ 5mA		4.5 2.7 1.6	6.5 4.5 3.5	mA mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 I_{01} < 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.4	4.7	V_{02}-0.2	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500μA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	μs
V_{DT}	V_{02} disable threshold voltage			1.25	2.4	V
I_D	V_{02} disable input current	$V_D \leq 0.4V$ $V_D \geq 2.4V$		-150 30		μA μA
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current conditions.

APPLICATION INFORMATION

In power supplies for μP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.
When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).
V_{02} is switched at low level and V_R at high level when one of the following conditions occurs:

- a high level (> V_{DT}) is applied on pin 5;
- an input overvoltage;
- an overload on the output 1 ($V_{01} < V_{RT}$);
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

- 5V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

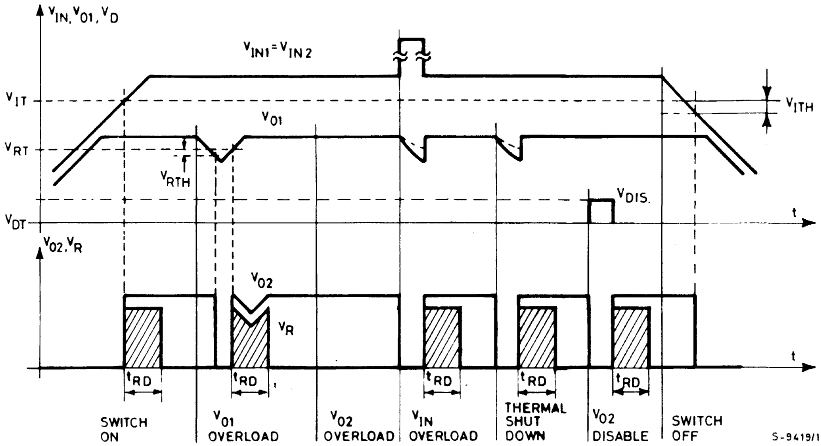
CIRCUIT OPERATION (continued)

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Fig. 1



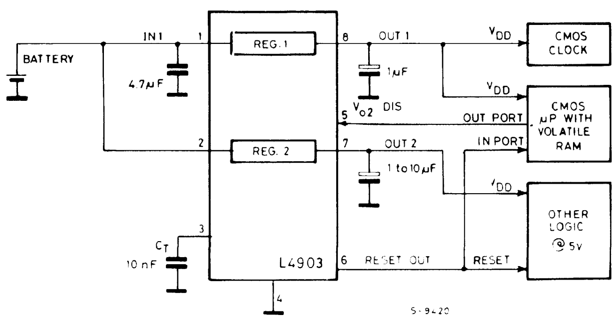
APPLICATION SUGGESTION

Fig. 2 illustrates how the L4903's disable input may be used in a CMOS μComputer application.

The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS μcomputer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a μP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Fig. 2



APPLICATION SUGGESTIONS (continued)

Fig. 3 - Quiescent current (Reg. 1) vs. output current

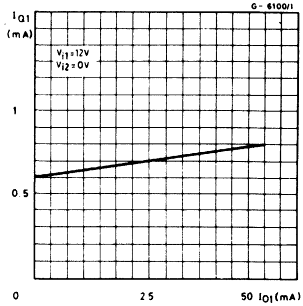


Fig. 4 - Quiescent current (Reg. 1) vs. input voltage

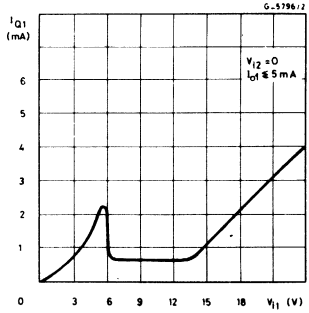


Fig. 5 - Total quiescent current vs. input voltage

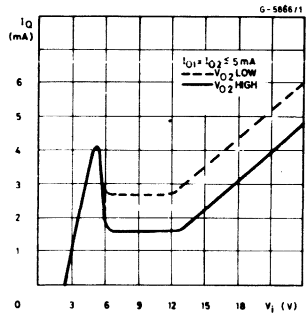
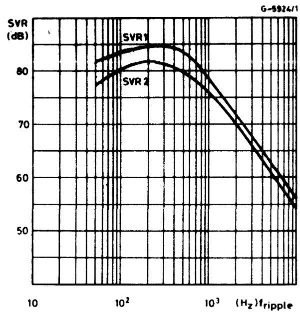


Fig. 6 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



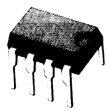
DUAL 5V REGULATOR WITH RESET

PRELIMINARY DATA

- OUTPUT CURRENTS: I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4904A is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



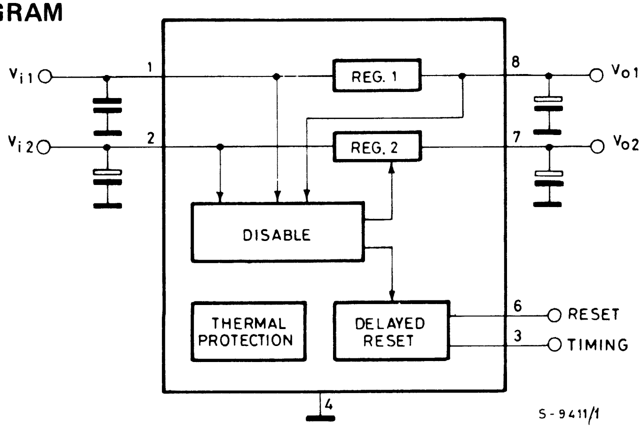
Minidip Plastic

ORDERING NUMBER: L4904A

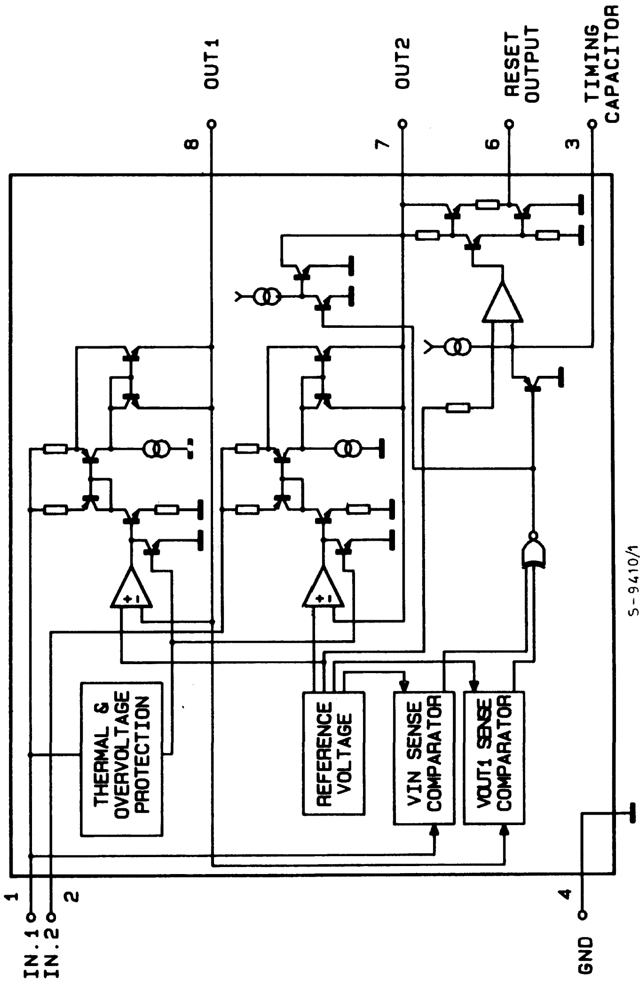
ABSOLUTE MAXIMUM RATINGS

V_{IN}	DC input voltage	24	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
P_{tot}	Power dissipation at T_{amb} = 50°C	1	W
T_j	Storage and junction temperature	-40 to 150	°C

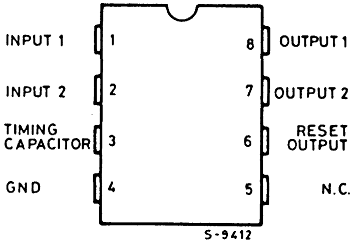
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



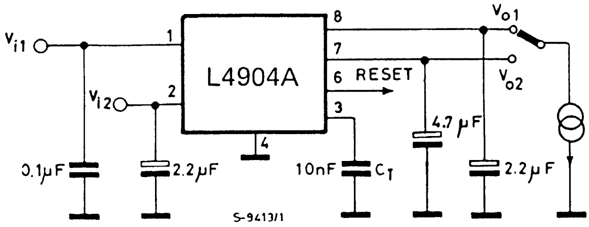
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 50mA regulator input.
2	INPUT 2	100mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
6	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A}\right)$; t_{RD} (ms) $= C_t$ (nF).
7	OUTPUT 2	5V - 100mA regulator output. Enabled if $V_O 1 > V_{RT}$ and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	OUTPUT 1	5V - 50mA regulator output with low leakage in switch-OFF condition.

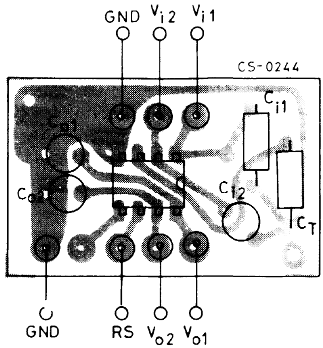
THERMAL DATA

$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	100	°C/W

TEST CIRCUIT



P.C. board and components layout of the test circuit (1 : 1 scale)



ELECTRICAL CHARACTERISTICS (V_{IN} = 14,4V, T_{amb} = 25°C unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				20	V
V_{01}	Output voltage 1	R load 1KΩ	4.95	5.05	5.15	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01} -0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	50			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leqslant$ 3V			1	µA
I_{02}	Output current 2	ΔV_{02} = -100mV	100			mA
V_{I01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input threshold voltage		V_{01} +1.2	6.4	V_{01} +1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation	7V < V_{IN} < 18V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	
ΔV_{01}	Load regulation 1	V_{IN} = 8V 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 100mA		10	50	
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leqslant$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leqslant$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{O2}-0.15	4.9	V_{O2}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500µA	V_{O2} - 1	4.12	V_{O2}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3		11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	µs
$\frac{\Delta V_{O1}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
$\frac{\Delta V_{O2}}{\Delta T}$	Thermal drift	$-20°C \leq T_{amb} \leq 125°C$		0.3 -0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 50mA	50	84		dB
SVR2	Supply voltage rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4904A makes it very easy to supply such equipments; it provides two voltage regulators (booth 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{O1} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{O2}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{O2} and V_R are switched together at low level when one of the following conditions occurs:

– an input overvoltage
– an overload on the output 1 ($V_{O1} < V_{RT}$);
– a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{O1} output features:

– 5V internal reference without voltage divider between the output and the error comparator;
– very low drop series regulator element utilizing current mirrors;

permit high output impedance and then very low leakage current even in power down conditions.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{O1} regulator also features low consumption (0.6mA

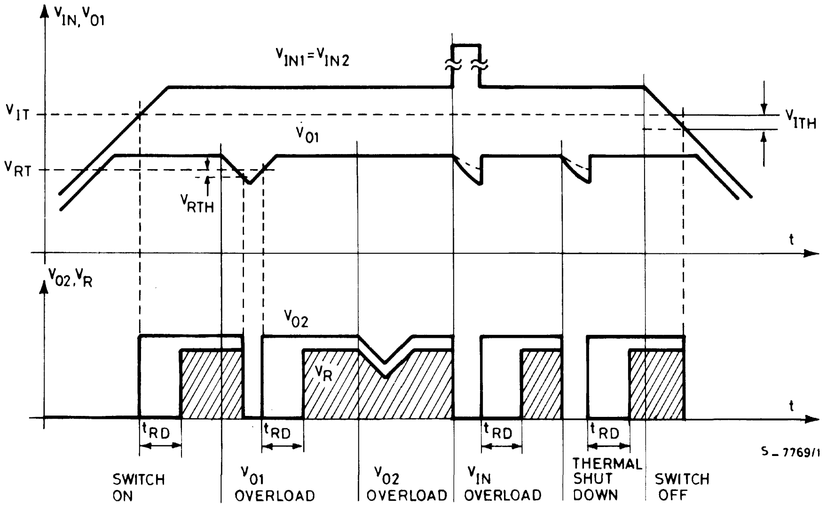
CIRCUIT OPERATION (continued)

typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-dav clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 3 shows the L4904A with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type C-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTIONS (continued)

Application Circuits of a Microprocessor system (Fig. 2) or with data save battery (Fig. 3). The reset output provide delayed rising front at the turn-off of the regulator 2.

Fig. 2

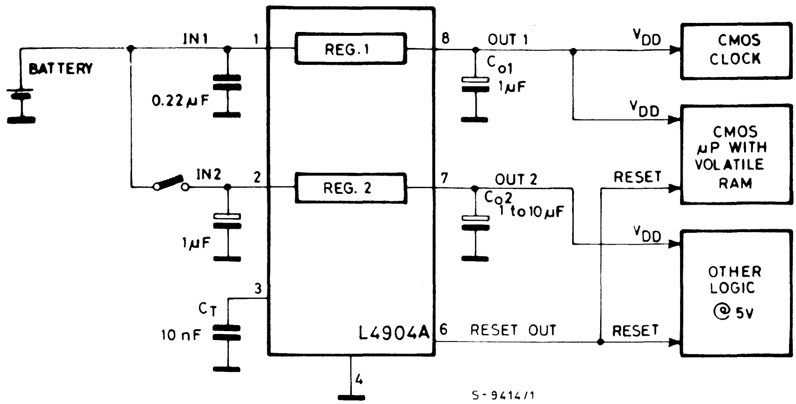
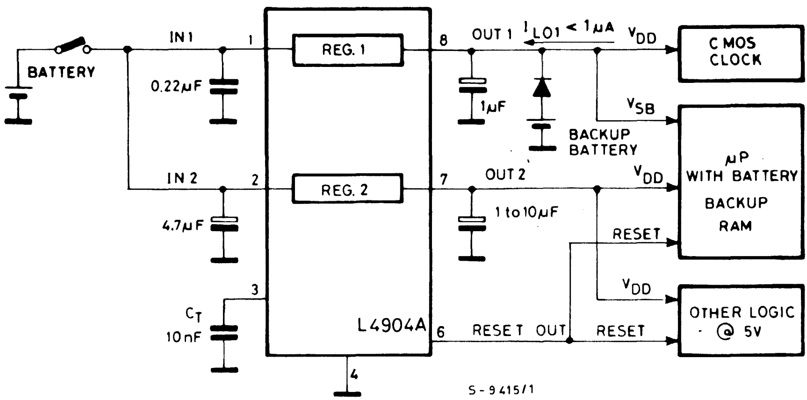


Fig. 3



APPLICATION SUGGESTIONS (continued)

Fig. 4 - Quiescent current (Reg. 1) vs. output current

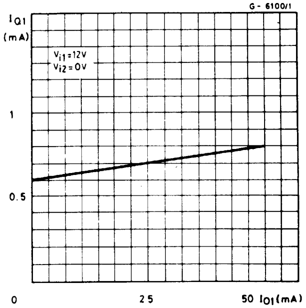


Fig. 5 - Quiescent current (Reg. 1) vs. input voltage

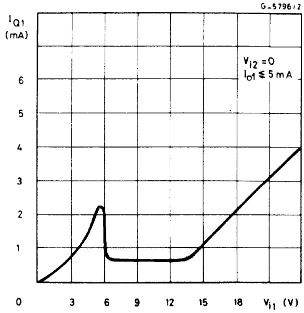


Fig. 6 - Total quiescent current vs. input voltage

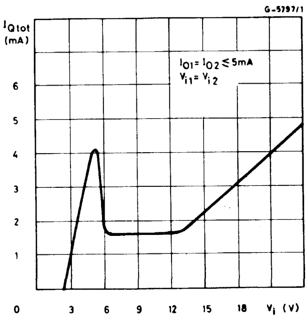
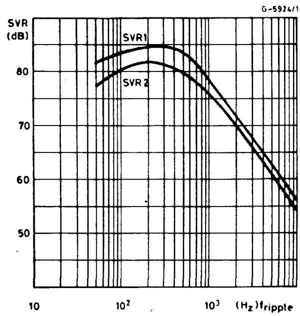


Fig. 7 - Supply voltage rejection regulators 1 and 2 vs. input ripple frequence



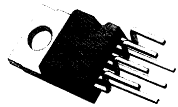
DUAL 5V REGULATOR WITH RESET

ADVANCE DATA

- DOUBLE BATTERY OPERATING
- OUTPUT CURRENTS: $I_{01} = 200mA$
  $I_{02} = 300mA$
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 1%
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- LOW LEAKAGE CURRENT, LESS THAN 1μA AT OUTPUT 1
- LOW QUIESCIENT CURRENT (INPUT 1)
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT HIGH
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION

The L4905 is a monolithic low drop dual 5V regulator designed mainly for supplying microprocessor systems.

Reset and data save functions during switch on/off can be realized.



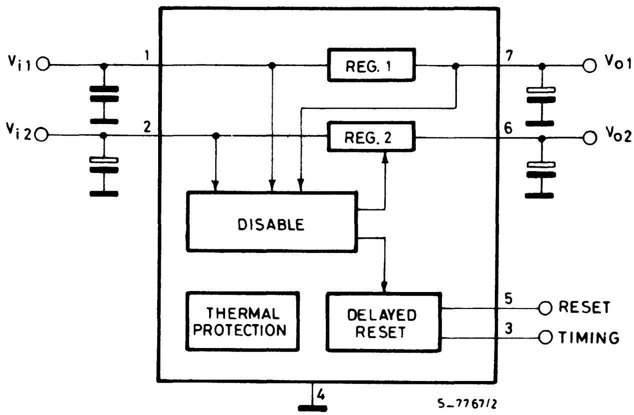
Heptawatt

ORDERING NUMBER: L4905

ABSOLUTE MAXIMUM RATINGS

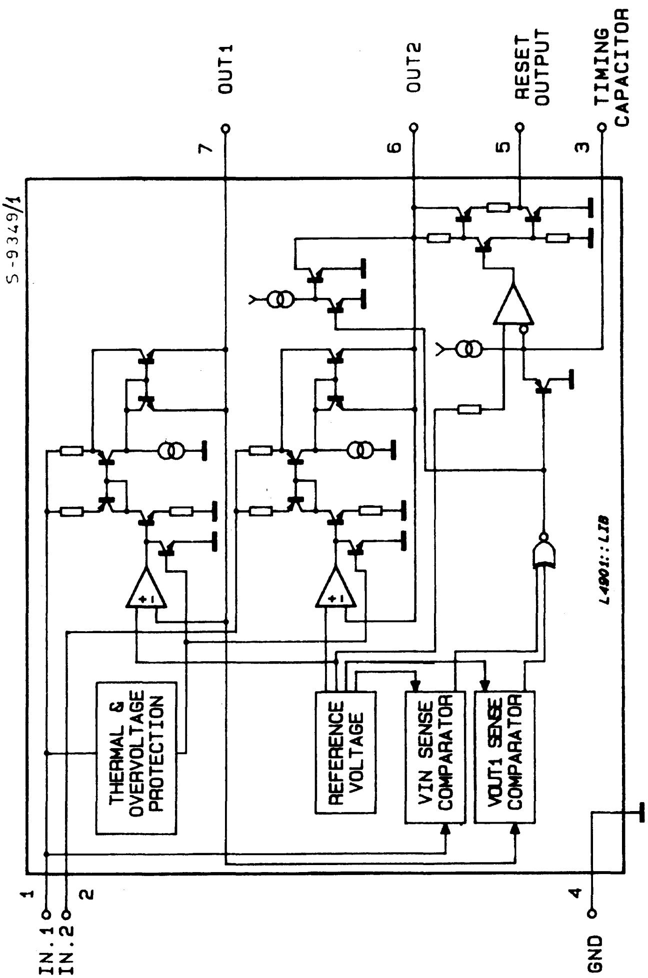
V_{IN}	DC input voltage	28	V
	Transient input overvoltage (t = 40 ms)	60	V
I_o	Output current	internally limited	
T_j	Storage and junction temperature	-40 to 150	°C

BLOCK DIAGRAM

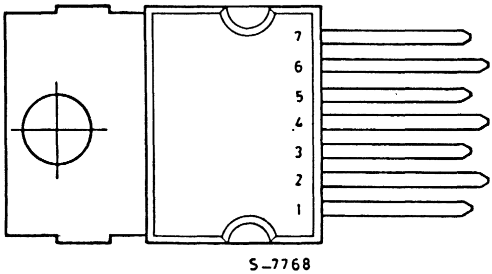


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top view)



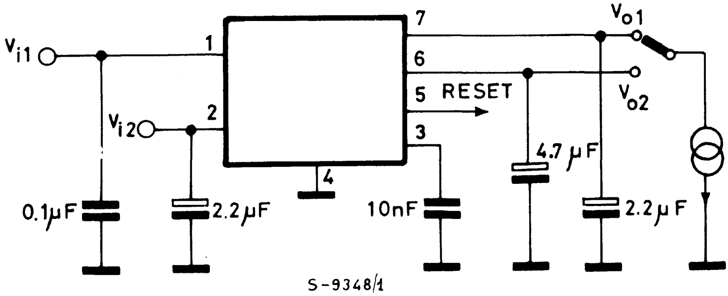
PIN FUNCTIONS

N°	NAME	FUNCTION
1	INPUT 1	Low quiescent current 200mA regulator input.
2	INPUT 2	300mA regulator input.
3	TIMING CAPACITOR	If Reg. 2 is switched-ON the delay capacitor is charged with a 10μA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common ground.
5	RESET OUTPUT	When pin 3 reaches 5V the reset output is switched high. Therefore $t_{RD} = C_t \left(\frac{5V}{10\mu A} \right)$; t_{RD} (ms) $= C_t$ (nF)
6	OUTPUT 2	5V - 300mA regulator output. Enabled if V_O 1 > V_{RT} and $V_{IN\,2} > V_{IT}$. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
7	OUTPUT 1	5V - 200mA regulator output with low leakage (in switch-OFF condition).

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	4	°C/W

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{IN1} = V_{IN2} = 14,4V, T_{amb} = 25° unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC operating input voltage				24	V
V_{01}	Output voltage 1	R load 1KΩ	5.0	5.05	5.1	V
V_{02H}	Output voltage 2 HIGH	R load 1KΩ	V_{01}-0.1	5	V_{01}	V
V_{02L}	Output voltage 2 LOW	I_{02} = -5mA		0.1		V
I_{01}	Output current 1	ΔV_{01} = -100mV	200			mA
I_{L01}	Leakage output 1 current	V_{IN} = 0 $V_{01} \leqslant$ 3V			1	μA
I_{02}	Output current 2	ΔV_{02} = -100mV	300			mA
V_{i01}	Output 1 dropout voltage (*)	I_{01} = 10mA I_{01} = 100mA I_{01} = 200mA		0.7 0.8 1.05	0.8 1 1.3	V V
V_{IT}	Input threshold voltage		V_{01}+1.2	6.4	V_{01}+1.7	V
V_{ITH}	Input threshold voltage hyst.			250		mV
ΔV_{01}	Line regulation 1	7V < V_{IN} < 24V I_{01} = 5mA		5	50	mV
ΔV_{02}	Line regulation 2	I_{02} = 5mA		5	50	mV
ΔV_{01}	Load regulation 1	5mA < I_{01} < 200mA		40	80	mV
ΔV_{02}	Load regulation 2	5mA < I_{02} < 300mA		50	100	mV
I_Q	Quiescent current	0 < V_{IN} < 13V 7V < V_{IN} < 13V I_{02} = $I_{01} \leqslant$ 5mA		4.5 1.6	6.5 3.5	mA mA
I_{Q1}	Quiescent current 1	6.3V < V_{IN1} < 13V V_{IN2} = 0 $I_{01} \leqslant$ 5mA I_{02} = 0		0.6	0.9	mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{RT}	Reset threshold voltage		V_{02}-0.15	4.9	V_{02}-0.05	V
V_{RTH}	Reset threshold hysteresis		30	50	80	mV
V_{RH}	Reset output voltage HIGH	I_R = 500µA	V_{02}-1	4.12	V_{02}	V
V_{RL}	Reset output voltage LOW	I_R = -5mA		0.25	0.4	V
t_{RD}	Reset pulse delay	C_t = 10nF	3	5	11	ms
t_d	Timing capacitor discharge time	C_t = 10nF			20	µs
$\frac{\Delta V_{01}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 - 0.8		mV/°C
$\frac{\Delta V_{02}}{\Delta T}$	Thermal drift	-20°C ≤ T_{amb} ≤ 125°C		0.3 - 0.8		mV/°C
SVR1	Supply voltage rejection	f = 100Hz V_R = 0.5V I_o = 100mA	54 50	84		dB
SVR2	Supply voltage rejection		50	80		dB
T_{JSD}	Thermal shut down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25mV under constant output current condition.

APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4905 makes it very easy to supply such equipments; it provides two voltage regulators (both 5V high precision) with separate inputs plus a reset output for the data save function.

CIRCUIT OPERATION (see Fig. 1)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02}) switches on and the reset output (V_R) also goes high after a programmable time T_{RD} (timing capacitor).

V_{02} and V_R are switched together at low level when one of the following conditions occurs:

– an input overvoltage
– an overload on the output 1 ($V_{01} < V_{RT}$);
– a switch off ($V_{IN} < V_{IT} - V_{ITH}$);

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features:

– 5V internal reference without voltage divider between the output and the error comparator;
– very low drop series regulator element utilizing current mirrors;
– permit high output impedance and then very low leakage current error even in power down condition.

This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery. The V_{01}

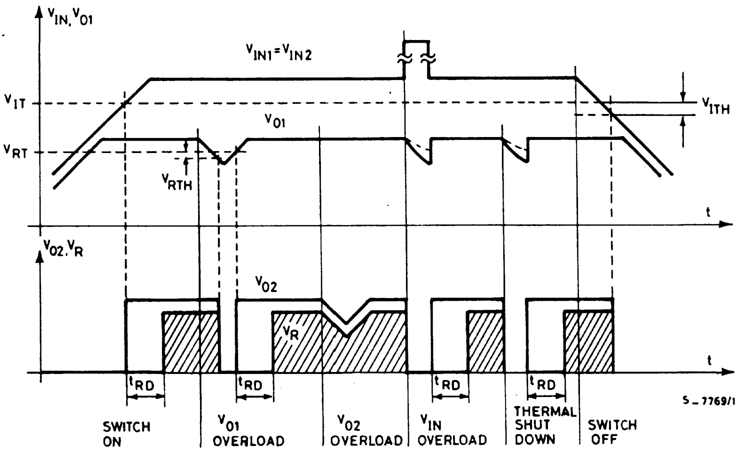
CIRCUIT OPERATION (continued)

regulator also features low consumption (0.6mA typ.) to minimize battery drain in applications where the V_1 regulator is permanently connected to a battery supply.

The V_{02} output can supply other non essential 5V circuits wich may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

Fig. 1



APPLICATION SUGGESTIONS

Fig. 2 shows an application circuit for a μP system typically used in trip computers or in car radios with programmable tuning.

Reg. 1 is permanently connected to a battery and supplies a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory.

Reg. 2 may be switched OFF when the system is inactive.

Fig. 4 shows the L4905 with a back up battery on the V_{01} output to maintain a CMOS time-of-day clock and a stand by type N-MOS μP. The reset output makes sure that the RAM is forced into the low consumption stand by state, so the access to memory is inhibit and the back up battery voltage cannot drop so low that memory contents are corrupted.

In this case the main on-off switch disconnects both regulators from the supply battery.

APPLICATION SUGGESTION (continued)

Fig. 2

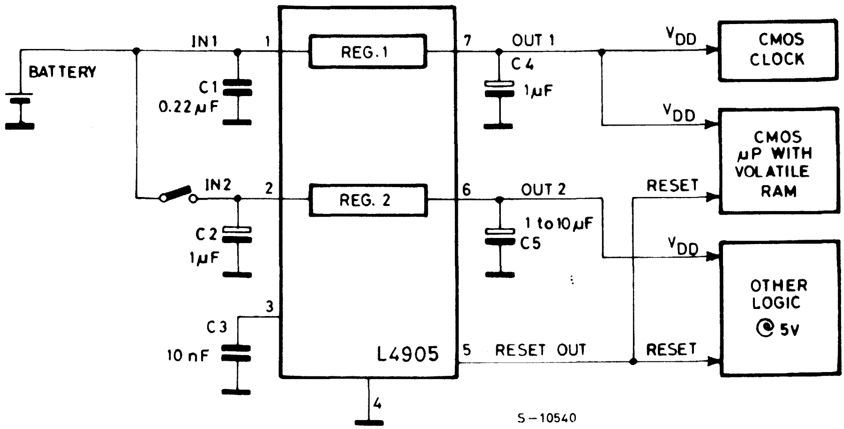
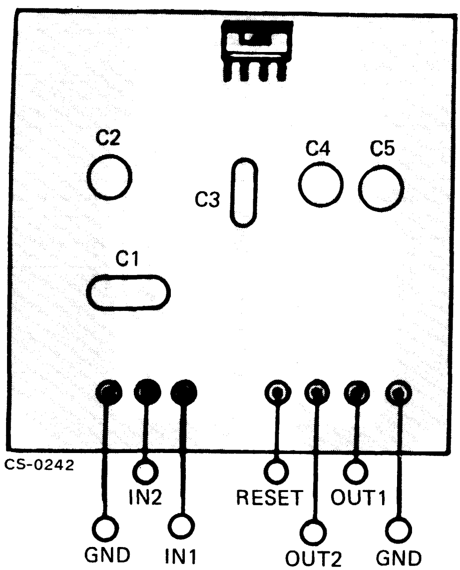


Fig. 3 - P.C. board component layout of fig. 2 (1 : 1 scale)



APPLICATION SUGGESTION (continued)

Fig. 4

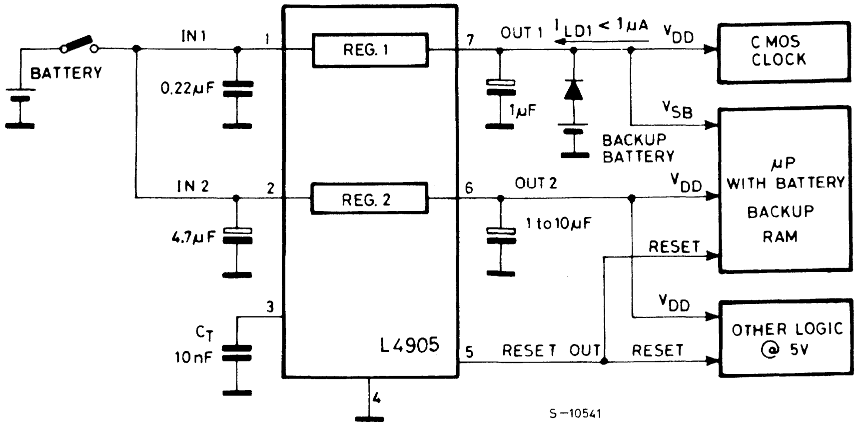


Fig. 5 - Quiescent current (Reg. 1) vs. output current

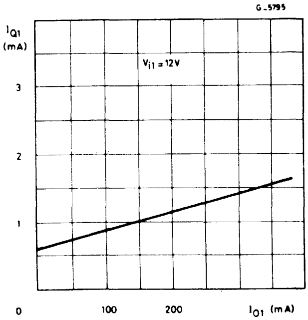


Fig. 6 - Quiescent current (Reg. 1) vs. input voltage

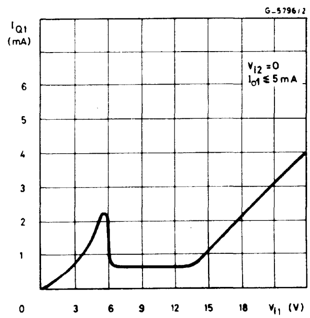
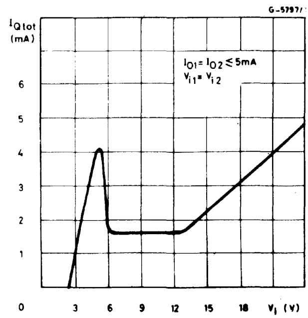


Fig. 7 - Total quiescent current vs. input voltage

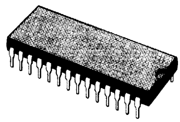


SGS-THOMSON MICROELECTRONICS

M104

PCM REMOTE CONTROL RECEIVER

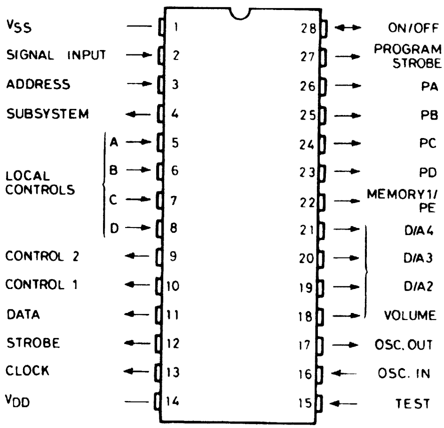
- 128 CHANNEL DECODING
- 5-BIT BINARY STATIC OUTPUTS (32 programs)
- 4 ANALOGUE CONTROLS/63 STEPS
- 445 TO 510 kHz REFERENCE OSCILLATOR
- 5 V SUPPLY VOLTAGE
- LOCAL CONTROLS AVAILABLE
- INTEGRATED DIGITAL POWER ON RESET
- SERIAL "I-BUS" OUTPUT FOR TELETEXT AND VIEWDATA
- TO BE USED IN CONJUNCTION WITH M709 OR M710 R.C. TRANSMITTERS (flash transmission mode)
- TECHNICAL NOTE TN 155 AVAILABLE



DIP28

ORDER CODE : M104B1

PIN CONNECTIONS



NOTE : THE TEST PIN MUST BE CONNECTED TO V_{SS}

S-4609/1

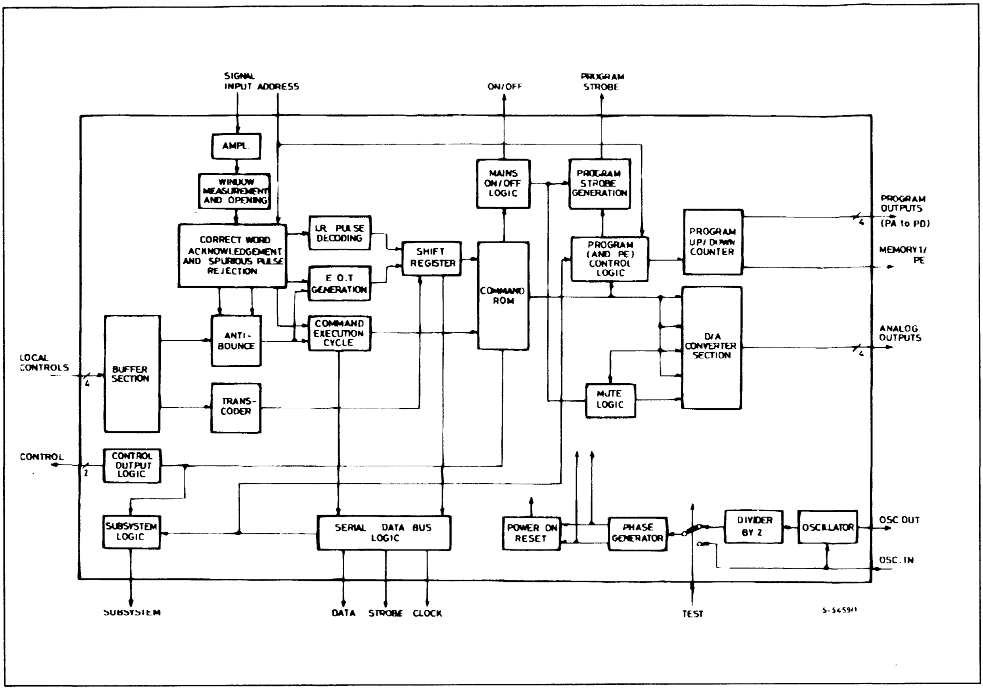
DESCRIPTION

The M104 has been developed for remote control of TV or radio sets in conjunction with M709/M710 R.C. transmitters. The receiver decodes the transmitted commands only if the transmitted address matches the address code selected at the receiver. 2 addresses are available for this purpose. The accepted command is afterwards released on the serial data bus.

When the M104 is operating in the subsystem mode (e.g. Teletext, Viewdata) and a command is continuously received, the Data Bus is disabled after the first signal has been released ; it is reenabled after the reception or the internal generation of the "end of transmission code". The frequency of the clock oscillator can be in the range 445 to 510 kHz and no synchronization is required with the transmitter clock.

The M104 is produced with N-channel silicon gate technology and is assembled in a 28 pin dual in-line plastic package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7	V
V_I	Input Voltage (except pin 2) Input voltage pin 2	– 0.3 to + 7 – 0.3 to + 14	V
$V_{O(off)}$	Off-state Output Voltage (pins 26, 25, 24, 23, 22, 27, 21, 20, 19, 18, 28) Off-state Output Voltage (pins 17, 10, 9, 4, 12, 11, 13)	14 7	V V

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage (except pin 2) Input Voltage pin 2	0 to 5.25 0 to 13.2	V V
$V_{O(off)}$	Off state Output Voltage (pins 26, 25, 24, 23, 22, 27, 21, 20, 19, 18, 28) Off state Output Voltage (pins 17, 10, 9, 4, 12, 11, 13)	Max 13.2 Max 5.5	V V

Note : Test pin and unused open drain outputs must be connected to V_{SS}.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)
Typical Values are at 5 V, T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions	Value			Unit
				Min.	Typ.	Max.	
V_{IL}	Input Low Voltage	3-28				0.8	V
		5-6-7-8				1.5	
V_{IH}	Input High Voltage	3-28		2.5			V
		5-6-7-8		4			
V_{IPP}	Peak to Peak Voltage	2		0.5		13.2	V
V_{OL}	Output Low Voltage	26-25-24-23-22 10-9-21-20 19-18-28-4	V_{DD} = 4.75 V I_{OL} = 0.8 mA			0.4	V
		27-12-11-13	V_{DD} = 4.75 V I_{OL} = 1.6 mA			0.4	
I_{IL}	Input Low Current	3-5-6-7-8	V_{DD} = 5.25 V V_{IL} = 0.4 V			– 0.4	mA
I_{IH}	Input High Current	28-3	V_{DD} = 5.25 V V_{IH} = 5.25 V			25	µA
$I_{O(off)}$	Output Leakage Current	26-25-24-23-22 27-21-20-19 18-28	V_{DD} = 5.25 V $V_{O(off)}$ = 13.2 V			50	µA
		10-9-4 12-11-13	V_{DD} = 5.25 V $V_{O(off)}$ = 5.25 V			25	
I_{DD}	Supply Current	14	V_{DD} = 5.25 V All Outputs Open			50	mA

DESCRIPTION

PIN 1 - V_{SS}.

The substrate of the ICs is connected to this pin. It is the reference pin for all parameters of the ICs.

PIN 2 - SIGNAL INPUT.

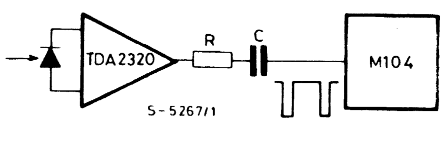
The minimum signal to be applied is 0.5 V peak to peak.

The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity :

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop-pulse
- check of noise level ; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored and decoded. The received coded word is also released on the serial data bus.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.



Supply Voltage of TDA 2320	R	C
5	2.2 K	4.7 nF
12	10 K	4.7 nF

The end of transmission code is also released on the Data Bus.

PIN 3 - ADDRESS INPUT.

The receiver decodes only signals transmitted with addresses 1 and 2. This input has integrated pull-up resistor of 50 K (max).

Address	Pin 3
1	Low
2	High

PIN 4 - SUBSYSTEM MODE INDICATION.

This open drain output is set high at power on reset and can be switched low with commands 56 to 62. It is repositioned high by commands 2, 12 and 63.

When the receiver is in the subsystem mode (output low) and a command is received continuously the data bus is disabled after the first signal has been released.

It is reenabled after the reception or the internal generation of the "end of transmission code".

No Program change command is executed when M104 is in subsystem mode.

PINS 5-6-7-8 - LOCAL CONTROL INPUTS LOC-A, LOC-B, LOC-C, LOC-D.

These inputs are provided for emergency operations. Therefore only a few controls are provided.

Local input commands and I.R. commands have the same priority.

If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.

Viceversa an I.R. signal cannot be decoded until an issued local command has been executed and the "end of transmission" released.

All these inputs have integrated pull-up resistor of 50 KΩ (max).

Each command is accepted after it has been present continuously for about 40 ms.

Inputs				**Data Bus Codes**						**Function**
A	**B**	**C**	**D**	**C1**	**C2**	**C3**	**C4**	**C5**	**C6**	
H	H	H	H							
L	H	H	H	L	L	L	H	L	L	Program +
H	L	H	H	H	L	L	H	L	L	Program –
L	L	H	H	H	L	L	L	L	H	Volume –
H	H	L	H	H	H	L	L	L	L	
L	H	L	H	L	L	L	L	L	H	Volume +
H	L	L	H	L	H	L	L	L	H	A 2 +
L	L	L	H	L	H	L	H	L	L	Normalization
H	H	H	L	L	H	H	H	L	L	Memory 1 H
L	H	H	L	H	H	L	L	L	H	A 2 –
H	L	H	L	L	L	H	L	L	H	A 3 +
L	L	H	L	H	L	H	L	L	H	A 3 –
H	H	L	L	H	L	H	H	L	L	Memory 1 L
L	H	L	L	L	H	H	L	L	H	A 4 +
H	L	L	L	H	H	H	L	L	H	A 4 –
L	L	L	L	L	H	L	L	L	L	Mains off

PINS 9-10 - CONTROL OUTPUT R2, R1.

These outputs consist of open drain transistors that are switched on when commands 6 and 7 are issued. The outputs remain switched on for a time variable between 144 and 173 ms after reception of the command (f_{ref} = 500 kHz). They can be used for example to control fine tuning or automatic search commands of M293 (Electronic Program Memory).

Command N°	**R1** (pin 10)	**R2** (pin 9)
6	L	H
7	H	L

PINS 11-12-13 - SERIAL DATA BUS.

DATA (pin 11)

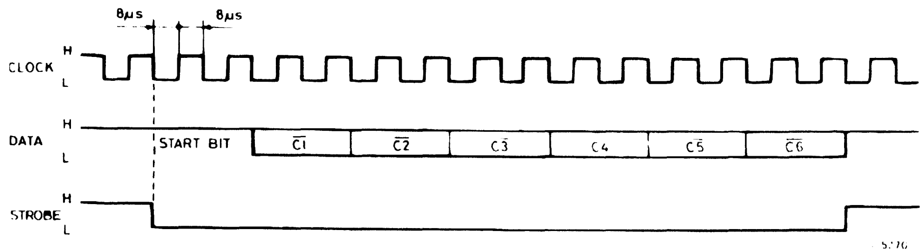
STROBE (pin 12)

CLOCK (pin 13)

Each signal, either remote or local, is released on this serial data bus to control external circuits (Teletext, Viewdata, Videorecorder, Hi-Fi, etc...).

The serial data bus has the following configuration :

All outputs have open drain configuration. See also description of pin 4 for subsystem mode operation.



PIN 14 - V_{DD}.

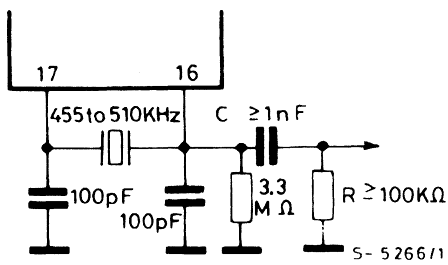
The supply voltage has to be 5 V ± 5 %. An internal power-on reset (lasting 125 ms) is generated when the 5 V is applied.

PIN 15 - TEST.

This pin is used for testing and has to be connected to V_{SS}.

PIN 16-17 - CLOCK OSCILLATOR.

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies. The clock signal can be used to drive the clock of other ICs through a capacitor connected at pin 16. The 3.3 MΩ resistor must be connected in any case to provide correct reset generation at power-on. If pin16 is temporanly connected to GND, a power-on reset is generated at release of this condition.



PIN 18 TO 21 - ANALOGUE CONTROL OUTPUTS.

These outputs are provided to control four analogue values (for example volume, brightness, colour saturation and contrast in TV sets).

The outputs deliver square wave signals of 7.8 kHz with a duty cycle variable in 63 steps.

In the case of a continuous command for varying the analogue information, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with f_{ref} = 500 kHz).

Local controls are varied every 115 ms (f_{ref} = 500 kHz).

The circuits is provided with underflow and overflow protection.

At supply on reset the volume output (pin 18) is set at duty cycle 21/64 (pulse = H). All other outputs are set at 31/64.

The normalization command sets all the outputs except volume to mid position (31/64).

The volume output can be switched to V_{SS} and reset to the previous level by means of command 2 (mute). It is also reset by means of the normalization command, volume + and mains off command.

The volume output is muted at each mains on and off command for approximately 0.5 sec.

It is also muted at supply on/off. The analogue outputs cannot be modified in the standby condition (mains off).

PIN 22 - MEMORY 1 (PE).

This output can be used as shift command for selection of up to 32 programs.

The output is set at power on to a low level. It can be controlled using commands 13 and 14. In the case of program +/– commands the output is automatically switched if the receiver operates with the address 1 (pin 3 = L) and if the program commands are accepted (see pins 23 to 26 and 4).

Otherwise this output is not affected by the program +/ – commands and can be used for general applications. It has open drain configuration.

PINS 23-24-25-26 - PD, PC, PB, PA PROGRAM OUTPUTS.

Open drain, binary coded, static outputs. At power on reset the outputs are set to program 1 (PA to PD = L L L L).

The program selection can be sequential or direct. If the TV set is in the standby condition the program step-by-step ± commands (8, 9) or the direct program selection commands (16 to 31) can be used to switch on the set.

In the first case the program can be stepped only if the command has been interrupted and a continuous sequential program change command causes program stepping in the up or down direction every 0.57 sec. (every 0.5 sec. if issued from R.C. transmitter).

Direct program selection is possible only by remote control.

The selection of up to 32 programs is possible using the memory 1 output (pin 22) that is put low and high by transmitting the commands 13 and 14 respectively.

All the program and shift commands are blocked when one of the commands from 56 to 62 is issued.

This "subsystem mode" condition is reset by commands 2, 12 and 63.

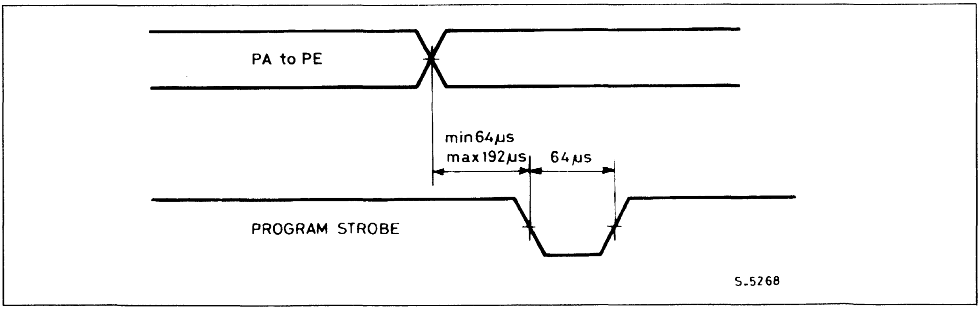
PIN 27 - PROGRAM STROBE OUTPUT.

The program strobe signal is generated each time the content of the memory has to be read and each time the mains output is switched off or on. It is therefore generated at direct program selection (16 to 31) program ± stepping (8, 9) and shift commands (13, 14) with address 1.

The strobe signal is not available when the M104 is in the subsystem mode ; the output has open drain configuration.

At direct program selection and shift commands, the strobe is available only one.

This output has open drain configuration.



PIN 28 - MAINS ON/OFF.

This active low output, is provided to control the on/off switching of the TV set via a transistor and a relay.

When the supply voltage is applied to the device, the output transistor is automatically biased off.

In this "standby" condition, only the mains on commands are accepted.

A mains on command can be given in one of the following ways :

- a) - by commands 8 , 9 (program +/–)
- - by command 12
- - by commands 16 to 31.

All these commands are accepted only when received 5 times (about 0.4 sec).

The "end of transmission" code resets the associated counter.

b) - connecting pin 28 to V_{SS} (GND) for at least 10μ s after the power-on reset time (125 ms).

This feature is provided for automatic switch on of the set using a temporarily active slide contact in parallel with the master power on switch.

The command is accepted only when the supply voltage V_{DD} has risen above approximately 4 V.

The set can be put in standby by means of command 2. This command also has to be received 5 times.

M104 TRUTH TABLE

Command N°	I.R. Code						Local Controls				Data Bus Code						Function
	C1	C2	C3	C4	C5	C6	A	B	C	D	C1	C2	C3	C4	C5	C6	
0	0	0	0	0	0	0					L	L	L	L	L	L	End of Transmission
1	1	0	0	0	0	0					H	L	L	L	L	L	Mute on off
2	0	1	0	0	0	0	L	L	L	L	L	H	L	L	L	L	Mains off Mute off Subsyst. off
3	1	1	0	0	0	0					H	H	L	L	L	L	(pin 4 H)
4	0	0	1	0	0	0					L	L	H	L	L	L	
5	1	0	1	0	0	0					H	L	H	L	L	L	
6	0	1	1	0	0	0					L	H	H	L	L	L	Control 1 L
7	1	1	1	0	0	0					H	H	H	L	L	L	Control 2 L
8	0	0	0	1	0	0	L	H	H	H	L	L	L	H	L	L	Program + / Mains on
9	1	0	0	1	0	0	H	L	H	H	H	L	L	H	L	L	Program – / Mains on
10	0	1	0	1	0	0	L	L	L	H	L	H	L	H	L	L	Normalization/Mute off
11	1	1	0	1	0	0					H	H	L	H	L	L	
12	0	0	1	1	0	0					L	L	H	H	L	L	Mains on/Subsystem off (pin 4 H)
13	1	0	1	1	0	0	H	H	L	L	H	L	H	H	L	L	Memory 1 L
14	0	1	1	1	0	0	H	H	H	L	L	H	H	H	L	L	Memory 1 H
15	1	1	1	1	0	0					H	H	H	H	L	L	
16	0	0	0	0	1	0					L	L	L	L	H	L	Program 16 / Mains on
17	1	0	0	0	1	0					H	L	L	L	H	L	program 1 / Mains on
18	0	1	0	0	1	0					L	H	L	L	H	L	Program 2 / Mains on
19	1	1	0	0	1	0					H	H	L	L	H	L	Program 3 / Mains on
20	0	0	1	0	1	0					L	L	H	L	H	L	Program 4 / Mains on
21	1	0	1	0	1	0					H	L	H	L	H	L	Program 5 / Mains on
22	0	1	1	0	1	0					L	H	H	L	H	L	Program 6 / Mains on
23	1	1	1	0	1	0					H	H	H	L	H	L	Program 7 / Mains on
24	0	0	0	1	1	0					L	L	L	H	H	L	Program 8 / Mains on
25	1	0	0	1	1	0					H	L	L	H	H	L	program 9 / Mains on
26	0	1	0	1	1	0					L	H	L	H	H	L	Program 10 / Mains on
27	1	1	0	1	1	0					H	H	L	H	H	L	Program 11 / Mains on
28	0	0	1	1	1	0					L	L	H	H	H	L	Program 12 / Mains on
29	1	0	1	1	1	0					H	L	H	H	H	L	Program 13 / Mains on
30	0	1	1	1	1	0					L	H	H	H	H	L	Program 14 / Mains on
31	1	1	1	1	1	0					H	H	H	H	H	L	Program 15 / Mains on
32	0	0	0	0	0	1	L	H	L	H	L	L	L	L	L	H	Volume + / Mute off
33	1	0	0	0	0	1	L	L	H	H	H	L	L	L	L	H	Volume –
34	0	1	0	0	0	1	H	L	L	H	L	H	L	L	L	H	Analog 2 +
35	1	1	0	0	0	1	L	H	H	L	H	H	L	L	L	H	Analog 2 –
36	0	0	1	0	0	1	H	L	H	L	L	L	H	L	L	H	Analog 3 +
37	1	0	1	0	0	1	L	L	H	L	H	L	H	L	L	H	Analog 3 –
38	0	1	1	0	0	1	L	H	L	L	L	H	H	L	L	H	Analog 4 +
39	1	1	1	0	0	1	H	L	L	L	H	H	H	L	L	H	Analog 4 –

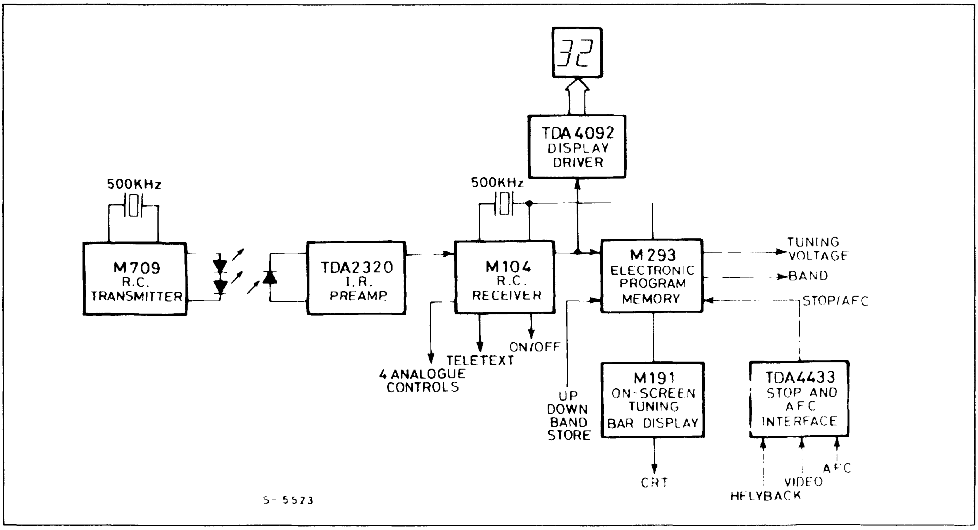
M104 TRUTH TABLE (continued)

Command N°	I.R. Code C1	C2	C3	C4	C5	C6	Local Controls A	B	C	D	Data Bus Code C1	C2	C3	C4	C5	C6	Function
40	0	0	0	1	0	1					L	L	L	H	L	H	
41	1	0	0	1	0	1					H	L	L	H	L	H	
42	0	1	0	1	0	1					L	H	L	H	L	H	
43	1	1	0	1	0	1					H	H	L	H	L	H	
44	0	0	1	1	0	1					L	L	H	H	L	H	
45	1	0	1	1	0	1					H	L	H	H	L	H	
46	0	1	1	1	0	1					L	H	H	H	L	H	
47	1	1	1	1	0	1					H	H	H	H	L	H	
48	0	0	0	0	1	1					L	L	L	L	H	H	
49	1	0	0	0	1	1					H	L	L	L	H	H	
50	0	1	0	0	1	1					L	H	L	L	H	H	
51	1	1	0	0	1	1					H	H	L	L	H	H	
52	0	0	1	0	1	1					L	L	H	L	H	H	
53	1	0	1	0	1	1					H	L	H	L	H	H	
54	0	1	1	0	1	1					L	H	H	L	H	H	
55	1	1	1	0	1	1					H	H	H	L	H	H	
56	0	0	0	1	1	1					L	L	L	H	H	H	Subsystem Mode on
57	1	0	0	1	1	1					H	L	L	H	H	H	Subsystem Mode on
58	0	1	0	1	1	1					L	H	L	H	H	H	Subsystem Mode on
59	1	1	0	1	1	1					H	H	L	H	H	H	Subsystem Mode on (pin 4 L)
60	0	0	1	1	1	1					L	L	H	H	H	H	Subsystem Mode on
61	1	0	1	1	1	1					H	L	H	H	H	H	Subsystem Mode on
62	0	1	1	1	1	1					L	H	H	H	H	H	Subsystem Mode on
63	1	1	1	1	1	1					H	H	H	H	H	H	Subsystem Mode off (pin 4 H)

Note : All the program and shift commands (13, 14) are blocked when one of the commands from 56 to 62 is issued. This condition is reset by commands 2, 12 and 63.

TYPICAL APPLICATION

Remote controlled voltage synthesizer (up to 32 stations) for TV and radio.



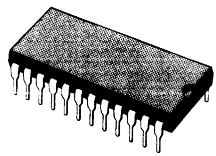
Note : For 16 program display, M192 can be used in place of TDA4092.

SGS-THOMSON MICROELECTRONICS

M105

PCM REMOTE CONTROL RECEIVER

- 5-BIT BINARY STATIC OUTPUTS (up to 32 programs)
- 4 ANALOG CONTROLS/63 STEPS
- 445 TO 510 kHz REFERENCE OSCILLATOR
- 5 V SUPPLY VOLTAGE
- LOCAL CONTROLS AVAILABLE
- INTEGRATED DIGITAL POWER ON RESET
- TO BE USED IN CONJUNCTION WITH M709 OR M710 R.C. TRANSMITTERS (flash transmission mode)
- TECHNICAL NOTE TN 155 AVAILABLE



DIP24

ORDER CODE : M105B1

DESCRIPTION

The M105 is a simplified version of the M104 (no serial data bus is provided) and it has been developed for remote control of TV or radio sets in conjunction with M709/M710 R.C. transmitters. The receiver decodes the transmitted commands only if the transmitted address matches the address code selected at the receiver. 2 addresses are available for this purpose.

The frequency of the clock oscillator can be in the range 445 to 510 kHz and no synchronization is required with the transmitter clock.

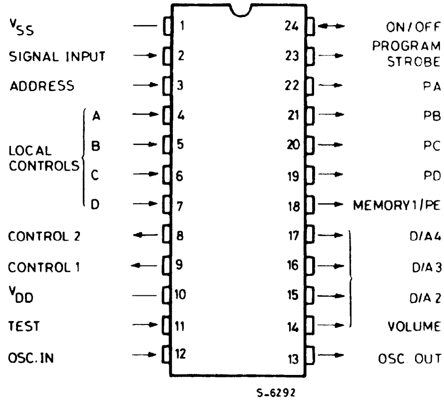
The M105 is produced with N-channel silicon gate technology and is assembled in a 24 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7	V
V_I	Input Voltage (except pin 2) Input Voltage pin 2	– 0.3 to 7 – 0.3 to 14	V V
$V_{O\ (off)}$	Off-state Input Voltage (except pin 10) (pins 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24) Off-state Output Voltage (pins 8, 9 13)	14 7	V V

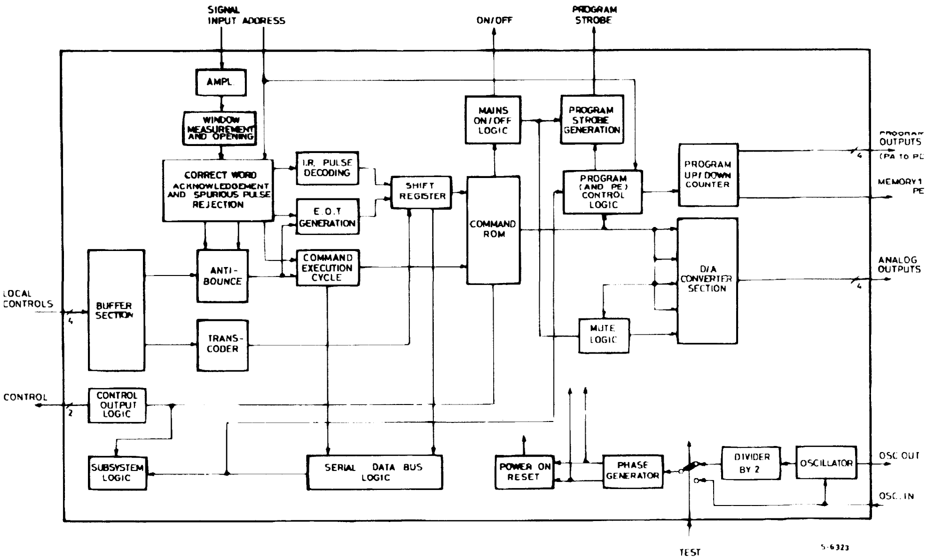
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



Note : The test pin must be connected to V_{SS}.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	4.75 to 5.25	V
V_I	Input Voltage (except pin 2) Input Voltage pin 2	0 to 5.25 0 to 13.2	V V
$V_{O\,(off)}$	Off-state Input Voltage (pins 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24) Off-state Output Voltage (pins 8, 9 13)	Max. 13.2 Max. 5.5	V V

Note : Test pin and unused open drain outputs must be connected to V_{SS}.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)
Typical Values are at 5 V, T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions	Value			Unit
				Min.	Typ.	Max.	
V_{IL}	Input Low Voltage	3–24				0.8	V
		4–5–6–7				1.5	
V_{IH}	Input High Voltage	3-24		2.5			V
		4–5–6–7		4			
V_{IPP}	Peak to Peak Voltage	2		0.5		13.2	V
V_{OL}	Output Low Voltage	8–9–14–15 16–17–18–19 20–21–22–24	V_{DD} = 4.75 V I_{OL} = 1.6 mA			0.4	V
		23	V_{DD} = 4.75 V I_{OL} = 1.6 mA			0.4	
I_{IL}	Input Low Current	3–4–5–6–7	V_{DD} = 5.25 V V_{IL} = 0.4 V			–0.4	mA
I_{IH}	Input High Current	3–24	V_{DD} = 5.25 V V_{IH} = 5.25 V			25	µA
$I_{O(off)}$	Output Leakage Curent	14–15–16–17 18–19–20–21 22–23–24	V_{DD} = 5.25 V $V_{O\,(off)}$ = 13.2 V			50	µA
		8–9	V_{DD} = 5.25 V $V_{O\,(off)}$ = 5.25 V			25	
I_{DD}	Supply Current	10	V_{DD} = 5.25 V All Outputs Open			50	mA

DESCRIPTION

PIN 1. V_{SS}

The substrate of the ICs is connected to this pin. It is the reference pin for all parameters of the ICs.

PIN 2. SIGNAL INPUT

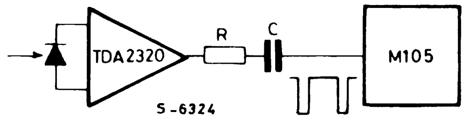
The minimum signal to be applied is 0.5 V peak to peak.

The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity :

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses betweeen the parity bit and the stop-pulse
- check of noise level ; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored and decoded. The received coded word is also released on the serial data bus.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.



Supply Voltage Of TDA 2320	R	C
5	2.2 K	4.7 nF
12	10 K	4.7 nF

PIN 3. ADDRESS INPUT

The receiver decodes only signals transmitted by M709/M710 with address 1 and 2. This input as an integrated pull-up resistor of 50 KΩ (max).

Address	pin 3
1	Low
2	High

PINS 4-5-6-7. LOCAL CONTROL INPUTS LOC-A, LOC-B, LOC-C, LOC-D (see table 1)

These inputs are provided for emergency operations. Therefore only a few controls are provided.

Local input commands and I.R. commands have the same priority.

If a complete I.R. command has been received, the local inputs are blocked until the commands has been executed and the "end of transmission code" generated.

Viceversa an I.R. signal cannot be decoded until an issued local command has been executed and the "end of transmission" released.

All these inputs have integrated pull-up resistor of 50 KΩ (max).

Each command is accepted after it has been present continuously for about 40 ms.

PINS 8-9. CONTROL OUTPUT R2, R1

These outputs consist of open drain transistors that are switched on when commands 6 and 7 are issued.

The outputs remain switched on for a time variable between 144 and 173 ms after reception of the command (f_{ref} = 500 kHz). They can be used for example to control fine tuning or automatic search commands of M293 (Electronic Program Memory).

Command N°	R1 (pin 9)	R2 (pin 8)
6	L	H
7	H	L

Table 1.

Inputs				Function
A	B	C	D	
H	H	H	H	
L	H	H	H	Progam +
H	L	H	H	Progam –
L	L	H	H	Volume –
H	H	L	H	
L	H	L	H	Volume +
H	L	L	H	A2 +
L	L	L	H	Nomalization
H	H	H	L	Memory 1 H
L	H	H	L	A2 –
H	L	H	L	A3 +
L	L	H	L	A3 –
H	H	L	L	Memory 1 L
L	H	L	L	A4 +
H	L	L	L	A4 –
L	L	L	L	Mains Off

PIN 10. V_{DD}

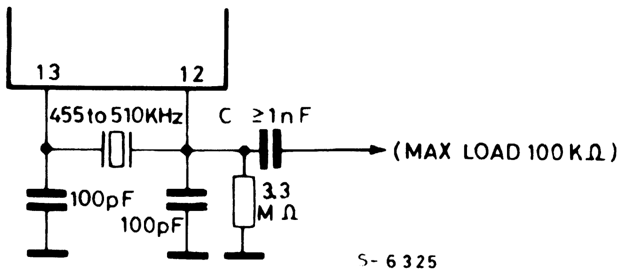
The supply voltage has to be 5 V ± 5 %. An internal power-on reset, having a duration of 125 ms, is generated when the 5 V is applied.

PIN 11. TEST

This pin is used for testing and has to be connected to V_{SS}.

PINS 12-13. CLOCK OSCILLATOR

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.



The clock signal can be used to drive the clock of other ICs through a capacitor connected at pin 12.

If pin 12 is temporanly connected to GND, a power-on reset is generated at release of this condition.

PINS 14 TO 17. ANALOGUE CONTROL OUTPUTS

These outputs are provided to control four analogue values (for example volume, brightness, colour saturation and contrast in TV sets).

The outputs deliver square wave signals of 7.8 kHz with a duty cycle variable in 63 steps.

In the case of a continuous command for varying the analogue information, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with f_{ref} = 500 kHz).

Local controls are varied every 115 ms (f_{ref} = 500 kHz).

The circuits is provided with underflow and overflow protection.

At supply on reset the volume output (pin 4) is set at duty cycle 21/64 (pulse = H). All other outputs are set at 31/64.

The normalization command sets all the outputs except volume to mid position (31/64).

The volume output can be switched to V_{SS} and reset to the previous level by means of command 2 (mute).

It is also reset by means of the normalization command, volume + and mains off command.

The volume output is muted at each mains on and off command for approximately 0.5 sec.

It is also muted at supply on/off. The analogue outputs cannot be modified in the standby condition (mains off).

PIN 18. MEMORY 1 (PE)

This output can be used as shift command for selection of up to 32 programs.

The output is set at power on to a low level. It can be controlled using commands 13 and 14. In the case of program ± commands the output is automatically switched if the receiver operates with the address 1 (pin 3 = L).

Otherwise this output is not affected by the program ± commands and can be used for general applications. It has open drain configuration.

PINS 19-20-21-22. PD, PC, PB, PA PROGRAM OUTPUTS

Open drain, binary coded, static outputs. At power on reset the outputs are set to program 1 (PA to PD = LLLL).

The program selection can be sequential or direct. If the TV set is in the standby condition the program step-by-step ± commands (8, 9) or the direct program selection commands (16 to 31) can be used to switch on the set.

In the first case the program can be stepped only if the command has been interrupted and a continuous sequential program change command causes program stepping in the up or down direction every 0.57 sec. (every 0.5 sec. if issued from R.C. transmitter).

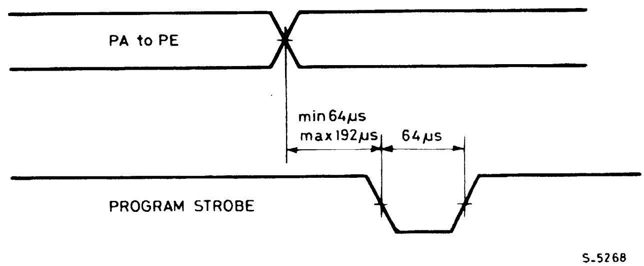
Direct program selection is possible only by remote control.

The selection of up to 32 programs is possible using the memory 1 output (pin 18) that is put low and high by transmitting the commands 13 and 14 respectively.

Note : All the program and shift commands are blocked when one of the commands from 56 to 62 is issued.
This condition is reset by commands 2, 12 and 63.

PIN 23. PROGRAM STROBE OUTPUT

The program strobe signal is generated each time the content of the memory has to be read and each time the mains output is switched off or on. It is therefore generated at direct program selection (16 to 31), program ± stepping (8, 9) and shift commands (13, 14) with address 1.



At direct program selection and shift commands, the strobe is available only once.

This output has open drain configuration.

Note : The strobe signal is not available when the M105 is in the subsystem mode ; the output has open drain configuration.

PIN 24. MAINS ON/OFF

This active low output, is provided to control the on/off switching of the TV set via a transistor and a relay.

When the supply voltage is applied to the device, the output transistor is automatically biased off.

In this "standby" condition, only the mains on commands are accepted.

A mains on command can be given in one of the following ways :

a) - by commands 8, 9 (program +/–)
   - by command 12
   - by commands 16 to 31

All these commands are accepted only when received 5 times (about 0.4 sec).

The "end of transmission" code resets the associated counter.

b) - connecting pin 24 to V_{SS} (GND) for at least 10 µs after the power-on reset time (125 ms).

This feature is provided for automatic switch on of the set using a temporarily active slide contact in parallel with the master power on switch.

The command is accepted only when the supply voltage V_{DD} has risen above approximately 4 V.

The set can be put in standby by means of command 2. This commands also has to be received 5 times.

M105 TRUTH TABLE

Command N°	I.R. Code						Local Controls				Function
	C1	C2	C3	C4	C5	C6	A	B	C	D	
0	0	0	0	0	0	0					End of Transmission.
1	1	0	0	0	0	0					Mute On/Off
2	0	1	0	0	0	0	L	L	L	L	Mains Off/Mute Off
3	1	1	0	0	0	0					
4	0	0	1	0	0	0					
5	1	0	1	0	0	0					
6	0	1	1	0	0	0					Control 1 L
7	1	1	1	0	0	0					Control 2 L
8	0	0	0	1	0	0	L	H	H	H	Program +/Mains On
9	1	0	0	1	0	0	H	L	H	H	Program –/Mains On
10	0	1	0	1	0	0	L	L	L	H	Normalization/Mute Off
11	1	1	0	1	0	0					
12	0	0	1	1	0	0					Mains On
13	1	0	1	1	0	0	H	H	L	L	Memory 1 L
14	0	1	1	1	0	0	H	H	H	L	Memory 1 H
15	1	1	1	1	0	0					
16	0	0	0	0	1	0					Program 16/Mains On
17	1	0	0	0	1	0					Program 1/Mains On
18	0	1	0	0	1	0					Program 2/Mains On
19	1	1	0	0	1	0					Program 3/Mains On
20	0	0	1	0	1	0					Program 4/Mains On
21	1	0	1	0	1	0					Program 5/Mains On
22	0	1	1	0	1	0					Program 6/Mains On
23	1	1	1	0	1	0					Program 7/Mains On
24	0	0	0	1	1	0					Program 8/Mains On
25	1	0	0	1	1	0					Program 9/Mains On
26	0	1	0	1	1	0					Program 10/Mains On
27	1	1	0	1	1	0					Program 11/Mains On
28	0	0	1	1	1	0					Program 12/Mains On
29	1	0	1	1	1	0					Program 13/Mains On
30	0	1	1	1	1	0					Program 14/Mains On
31	1	1	1	1	1	0					Program 15/Mains On
32	0	0	0	0	0	1	L	H	L	H	Volume +/Mute Off
33	1	0	0	0	0	1	L	L	H	H	Volume –
34	0	1	0	0	0	1	H	L	L	H	Analogue 2 +
35	1	1	0	0	0	1	L	H	H	L	Analogue 2 –
36	0	0	1	0	0	1	H	L	H	L	Analogue 3 +
37	1	0	1	0	0	1	L	L	H	L	Analogue 3 –
38	0	1	1	0	0	1	L	H	L	L	Analogue 4 +
39	1	1	1	0	0	1	H	L	L	L	Analogue 4 –
40	0	0	0	1	0	1					
41	1	0	0	1	0	1					
42	0	1	0	1	0	1					
43	1	1	0	1	0	1					
44	0	0	1	1	0	1					
45	1	0	1	1	0	1					
46	0	1	1	1	0	1					
47	1	1	1	1	0	1					

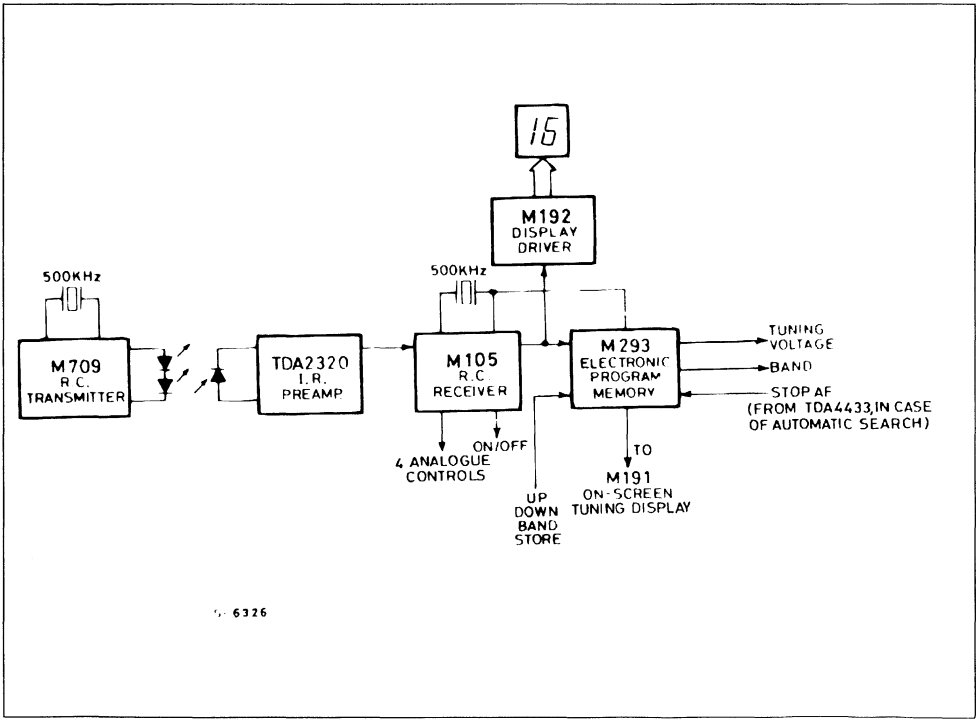
Note : All the program and shift commands (13, 14) are blocked when one of the commands from 56 to 62 is issued. This condition is reset by commands 2, 12 and 63.

M105 TRUTH TABLE

Command N°	I.R. Code						Local Controls				Function
	C1	C2	C3	C4	C5	C6	A	B	C	D	
48	0	0	0	0	1	1					
49	1	0	0	0	1	1					
50	0	1	0	0	1	1					
51	1	1	0	0	1	1					
52	0	0	1	0	1	1					
53	1	0	1	0	1	1					
54	0	1	1	0	1	1					
55	1	1	1	0	1	1					
56	0	0	0	1	1	1					
57	1	0	0	1	1	1					
58	0	1	0	1	1	1					
59	1	1	0	1	1	1					
60	0	0	1	1	1	1					
61	1	0	1	1	1	1					
62	0	1	1	1	1	1					
63	1	1	1	1	1	1					

TYPICAL APPLICATION

Remote controlled voltage synthetizer for TV.



Note : For 32 program display, TDA4092 can be used in place of M192.

SGS-THOMSON
MICROELECTRONICS

M206

PLL TV MICROCOMPUTER INTERFACE

- HIGHLY INTEGRATED SOLUTION INCLUDING PLL SYNTHESIZER, NV MEMORY, D/A CONVERTERS, BAND SELECT OUTPUTS, CLOCK OSCILLATOR, IR SIGNAL PRE-PROCESSOR AND SERIAL BUS INTERFACE
- 32 x 16 BITS OF NV MEMORY WITH LIFETIMES OF 10^4 CYCLES/WORD AND MINIMUM 10 YEARS RETENTION STORES TUNING DATA FOR 30 CHANNELS PLUS PRESET VALUES FOR THE SIX ANALOG OUTPUTS
- PRE-PROCESSOR FOR INFRARED REMOTE CONTROL SIGNALS REDUCES COMPONENT COUNT
- SIX PWM D/A CONVERTERS WITH 64-STEP RESOLUTION
- FOUR OPEN-DRAIN BAND SELECT OUTPUTS RATED TO 13.2 V
- ON-CHIP 4 MHz CLOCK OSCILLATOR WITH BUFFERED OUTPUT
- INTEGRATED DIGITAL POWER-ON RESET
- 3-WIRE SERIAL BUS TO LOAD/READ INTERNAL REGISTERS
- TECHNICAL NOTE TN 152 AVAILABLE

DESCRIPTION

The M206 is a highly integrated, programmable LSI integrated circuit for microcomputer controlled TV applications, realized using an advanced N-channel double polysilicon gate technology (NVMOS) that allows the integration of non-volatile memory and standard logic on the same chip.

It contains a phase-locked loop (PLL) synthesizer, six pulse-width modulation (PWM) digital/analog converters, a four-bit parallel output buffer, clock oscillator with buffered output, pre-processor for infrared remote control signals and a 3-wire serial bus interface.

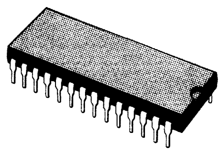
The M206 interfaces with a microcomputer through the three-wire serial bus and is programmed by loading thirteen internal registers - twelve of which are readable to simplify programming.

The PLL synthesizer requires an external 64 + 15/16 prescaler and divider and works with a phase comparator reference frequency of 0.9765 kHz. Outputs are provided to control the division ratio of the prescaler and to signal the out-of-lock condition to the microcomputer.

The infrared remote control signal pre-processor consists of a preamplifier, a squarer and a digital filter to separate noise from signals transmitted by the M708, M709 and M710 remote control transmitters. The output of this pre-processor is connected to the interrupt input of a microcomputer programmed to receive and decode the signal.

The M206 is supplied with two separate 5 V supply inputs, each provided with internal power-on reset circuits. The first, V_{DD1}, supplies the remote control and clock circuits in both standby and TV set operation. The second, V_{DD2}, supplies the rest of the circuits and is only active during TV operation.

The M206 is packaged in a 28-pin dual in-line plastic package.



DIP28

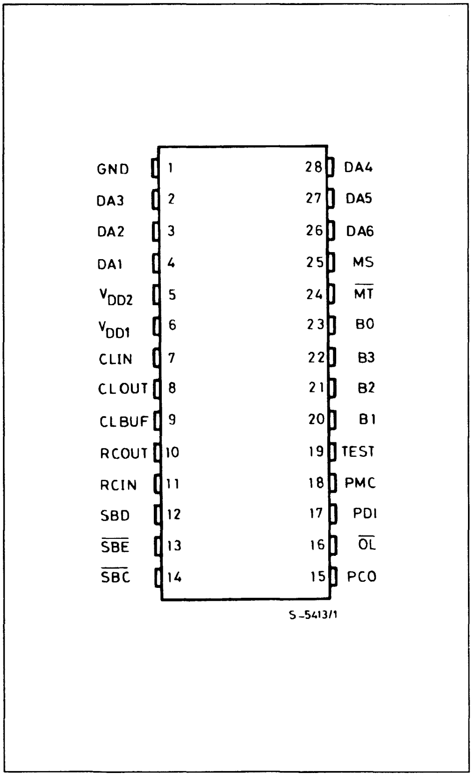
ORDER CODE : M206B1

ABSOLUTE MAXIMUM RATINGS

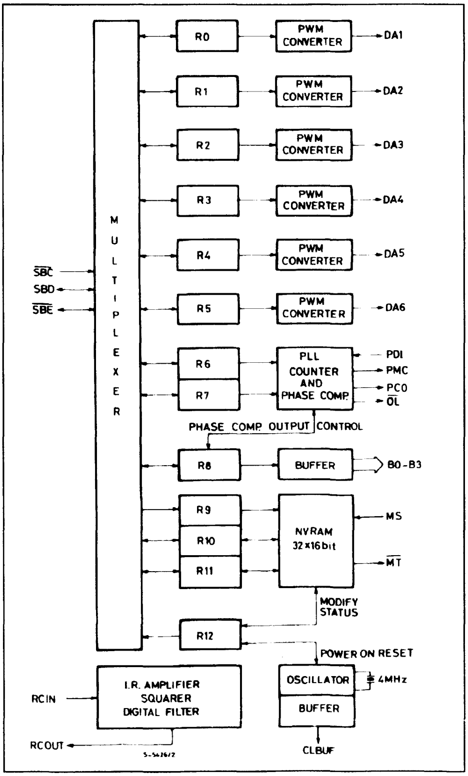
Symbol	Parameter	Value	Unit
V_{DD1}, V_{DD2}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 28	V
V_I	Input Voltage (except pin 11) Pin 11	– 0.3 to 7 – 0.3 to 15	V V
$V_{O\ (off)}$	Off State Output Voltage (except pins 2–3–4–26–27–28–20–21–22–23–24) Pins 2–3–4–20 to 23–26 to 28 Pin 24	7 15 28	 V V
I_{OL}	Output Current (except 2–3–4–26–27–28) Pins 2–3–4–26–27–28	5 10	mA mA
I_{OH}	Output Current (pins 15, 9)	– 5	mA
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Temperature	– 25 to 125	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

DA1-DA6 - *Digital/Analog converter outputs (open-drain outputs)*
Output from the six pulse-width modulation D/A converters.

B0-B3 - *Band drive outputs (open-drain outputs)*
Outputs from the four-bit buffer used for band selection.

SBD - *Serial Bus Data (bidirectional)*
Data line for serial communication with a microcomputer.

$\overline{\text{SBE}}$ - *Serial Bus Enable (bidirectional, active low)*
Enables serial bus transmissions.

$\overline{\text{SBC}}$ - *Serial Bus Clock (input, active low)*
Clock for serial bus transmissions.

RCIN - *Remote Control signal Input (analog input)*
Input to the infrared remote control signal preprocessor. Connected to the output of the IR preamplifier. Minimum input level 0.5 V peak-to-peak.

RCOUT - *Remote Control signal Output*
Output from the infrared remote control signal preprocessor. To be connected to the interrupt input of a microcomputer.

PDI - *Programmable Divider Input (input)*
This pin is the input of the programmable divider and is connected to the output of the prescaler.

PCM - *Prescaler Modulo Control (output)*
Control signal to set the prescaler division ratio (15 if high, 16 if low).

$\overline{\text{OL}}$ - *Out of Lock (output, active low)*
Signals an out of lock condition. This output is also active during the power on reset sequence.

PCO - *Phase Comparator Output*
The output of the phase comparator. Connected to the input of a low pass filter used to generate the tuning voltage.

TEST - *Test pin (input)*
The test pin is used only to test the device and is not specified for customer use. It must be connected to ground.

CLIN, CLOUT - *Clock oscillator connections*
A 4 MHz quartz crystal is connected between these pins.

V_{DD1}, V_{DD2}, GND - *Power Supply Connections*
V_{DD1} is the + 5 V standby supply input ; V_{DD2} is the main + 5 V supply input.

MS - *Memory Supply Input (input)*
Programming pulses for the NV memory are supplied to this pin during store cycles.

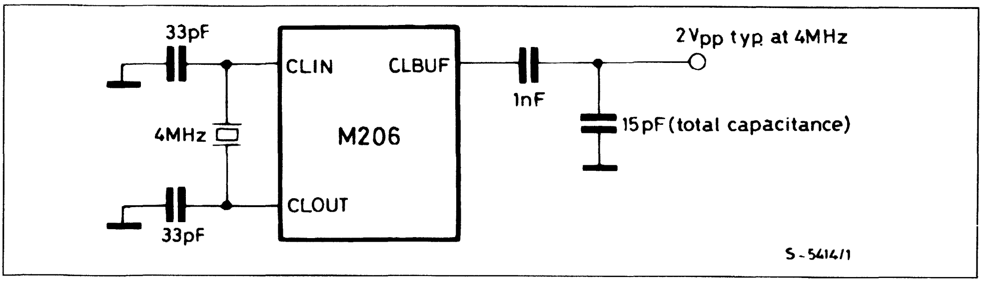
$\overline{\text{MT}}$ - *Memory Timing (output, active low)*
This output supplies the timing for the memory write pulses supplied to the MS input during store cycles.

CLBUF - *Clock Buffer (output)*
This is a buffered output from the on-chip clock oscillator and can be used to drive other components (for example the microcomputer).

FUNCTIONAL DESCRIPTION

CLOCK

To use the internal oscillator a 4 MHz quartz crystal is connected between the pins CLIN and CLOUT. If an external clock is used this must be connected to CLIN and CLOUT left unconnected or, if required as a clock output, loaded by a capacitor up to 15 pF. The minimum external clock amplitude is 2 V peak-to-peak. A buffered clock output, CLBUF, is provided which can drive up to three ± 100 μA loads.



LOADING AND READING INTERNAL REGISTERS

The M206 is programmed by loading a set of internal registers through a 3-wire serial bus. The functions of these registers are summarised in table 1.

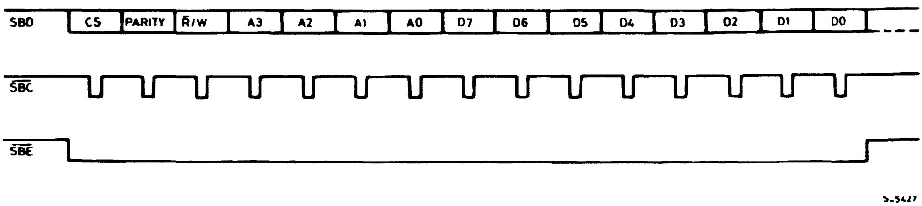
Table 1 : Summary of Internal Registers.

Register Number	Address				Number of Bits	Function
	A3	A2	A1	A0		
0	L	L	L	L	6	D/A Converter n° 1
1	L	L	L	H	6	D/A Converter n° 2
2	L	L	H	L	6	D/A Converter n° 3
3	L	L	H	H	6	D/A Converter n° 4
4	L	H	L	L	6	D/A Converter n° 5
5	L	H	L	H	6	D/A Converter n° 6
6	L	H	H	L	7	PLL Counter (MSB)
7	L	H	H	H	8	PLL Counter (LSB)
8	H	L	L	L	7	Buffer Outputs/Phase Comp. Output Control
9	H	L	L	H	5	NV Memory Address
10	H	L	H	L	8	NV Memory DATA
11	H	L	H	H	8	NV Memory DATA
12	H	H	L	L	2	NV Memory Modify Control/Reset Control

The 3-wire serial bus consists of the signals SBD (Serial Bus Data), SBE (Serial Bus Enable) and SBC (Serial Bus Clock). The enable and data pins, SBD and SBE, are bidirectional.

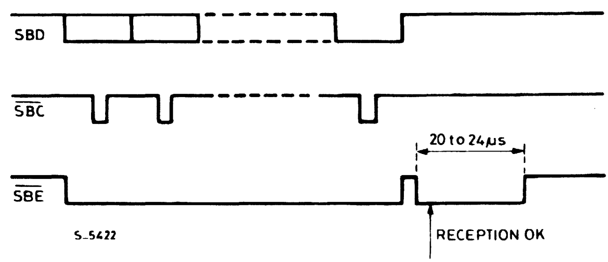
Data is accepted when the clock is low (active) and latched into the M206 on the low-high transition of the clock. All bus transfers are controlled by SBE.

REGISTER LOADING. Serial data transferred from the microprocessor to the M206 has the following format :



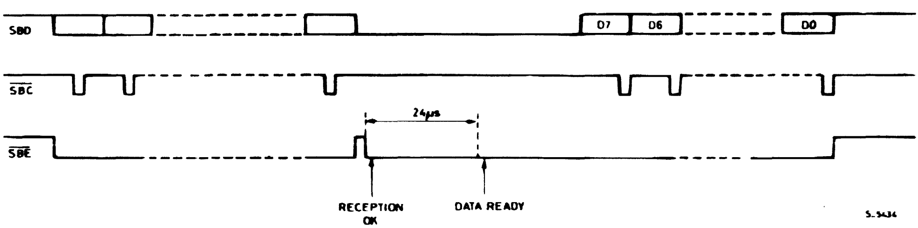
Bit	Description
CS	Chip Select (always low)
PARITY	Parity bit (the number of " H " bits transmitted is odd)
R/W	Read/Write. High for Register Load ; Low for Register Read
A0-A3	Register Address (see table 1)
D0-D7	Data to be loaded into register (load operation only).

The received data word is checked - length, CS and parity - immediately after the low-high transition of SBE. If the received word is valid this is signalled to the microprocessor by forcing the SBE line low for 20-24 s.



REGISTER READING. M206 registers are read by transmitting a 15 bit word as shown in fig. 4 with R/W low and the address of the register to be read in A0, A1, A2, A3. Bits D0-D7 can be high or low except when register 9 is addressed.

If this word is received correctly the SBE line is immediately pulled low by the M206 and after 24 µs the contents of the addressed register will be available to be read. The microprocessor reads this data by sending eight clock pulses. Data is output on the low-high transition of SBC and the first data bit is available before the first clock pulse.



LOADING THE NON-VOLATILE MEMORY. Data is stored in the 32 x 16-bit NV memory by loading the new contents into registers 10 and 11 then the address into register 9. The memory modify cycle begins when the address has been loaded and successful completion is indicated by a logic "1" in bit zero of register 12.

The time for a modify cycle varies from a few milliseconds to several hundred milliseconds during the device lifetime and is not internally limited. The storage operation should be aborted after one second if it proves unsuccessful. This is done by setting bit zero of register 12.

READING THE NON-VOLATILE MEMORY. The NV memory is read by loading the address into register 9. The contents of the addressed word are automatically loaded into registers 10 and 11 and can be read by two register read operations. The data is ready 200 µs after the address load.

PLL COUNTER

The PLL counter consists of a single counter that acts as the program counter (11 bit) and is swallow counter (4 bit) alternately. Data for the PLL counter is loaded into registers 6 and 7. Register 6 must be loaded first because the register 7 load operation initiates the data transfer to the PLL counter.

The reference frequency is produced by dividing the clock frequency by 4096. With a 4 MHz clock this gives a reference frequency of 976.5 Hz.

An out-of-lock signal is generated (output OL) when the phase error between the reference frequency and the input frequency exceeds 0.72 (2 µs).

The phase comparator output, PCO, has a three-state push pull configuration with a high level of 5 V and a low level of 0 V (with zero current sink or pump). The output impedance (both states) is typically 200 Ω (400 Ω maximum). The phase comparator output can be set to a high impedance state (both sink and pump transistors off) by setting bit 4 of register 8. The output is held in the high impedance state until this bit is reset. The phase comparator output should be set to high impedance when changing band.

RECOVERING LOCK. The phase comparator output can also be set to high and low levels to restore normal operation when the oscillator stops or the prescaler functions incorrectly at high frequency.

In the first condition (oscillator off) the prescaler sometimes oscillates, at high frequency. The loop reacts by reducing the varicap voltage in an attempt to reduce the frequency, thus worsening the situation. This out-of-lock condition is signalled to the microprocessor (by the $\overline{OL}$ output) which can set the phase comparator output to low level, forcing the varicap voltage up and restarting the oscillator. The phase comparator output is forced low by setting bit 5 of register 8. After about 1 ms this bit is automatically reset and the loop should lock again.

When the out-of-lock condition is caused by a failure of the prescaler to operate correctly at high frequencies the loop reacts by increasing the voltage, hence the frequency, again worsening the situation. To recover from this condition the phase comparator output is set high. This is done by setting bit 6 of register 8 which, as in the previous case, resets itself after 1 ms.

The out-of-lock condition could also be caused by unwanted changes in band or PLL counter contents provoked by external interference (spikes on supply etc.). For this reason it is always advisable to reload the band and PLL counter registers before attempting to recover lock as described above. If the phase comparator output is in the high impedance state, the $\overline{OL}$ output signals the reset condition but not the out-of-lock condition.

CALCULATING PLL COUNTER VALUES

a) F = video carrier

b) IF = 38.9 MHz

c) The frequency to be synthesized is Fs = F + IF

d) The Ref. frequency of the phase comparator is

$$F_{ref} = \frac{4.000\ \text{MHz}}{4096} = 0.97656\ \text{kHz}$$

e) Using the prescaler 64 + 15/16 the minimum frequency steps is

$$F_{ref} \times 64 = 62.5\ \text{kHz}$$

f) The modulo of division N is given by the ratio between the frequency to be synthesized and the reference frequency multiplied by 64. The result has to be rounded.

$$NS = \text{Integer rounded} \left[\frac{Fs}{F_{ref} \bullet 64} \right]$$

g) With the 64 + 15/16 prescaler and the particular counter of the M206 the division by N is given by

$$N_S = (I_S + 1) \,.\, 15 + (R_S + 1) \,.\, 16$$

where I (integer part) controls the division by 15 (program counter) and R (rest) controls the division by 16 (swallow counter). For ease of calculation we decrement N_S by one getting $N_C = N_S \;\; 1$.

The numbers I_C and R_C are given by :

$$N_C = (I_C + 1) \bullet 15 + (R_C + 1) \bullet 16$$

$$N_C - 31 = I_C \bullet 15 + R_C \bullet 16$$

using the formulas :

$$R_C = N_C - 31 - 15 \bullet \text{Integer} \left[\frac{N_C - 31}{15} \right]$$

$$IC = \frac{N_C - 31 - R_C \bullet 16}{15}$$

$R_S = R_C + 1$

$I_S = I_C \;\; 1$

Example :

Channel 21 — F = 471.25 MHz

$F_S = F + IF$ — $F_S = 471.25 + 38.9 = 510.15$ MHz

$$N_S = \text{Integer rounded} \left[\frac{510.15 \times 10^6}{62.5 \times 10^3} \right] = \text{Integer rounded } [8162.4] = 8162$$

$N_C = N_S - 1 = 8161$

$$R_C = N_C - 31 - 15 \bullet \text{Integer} \left[\frac{N_C - 31}{15} \right] = 8161 - 31 - 15 \bullet \text{Integer} \left[\frac{8161 - 31}{15} \right]$$

$$= 8130 - 15 \bullet \text{Integer } [542] = 8130 - 15 \bullet 542 = 8130 - 8130 = 0$$

$$I_C = \frac{N_C - 31 - R_C \bullet 16}{15} = \frac{8161 - 31}{15} = 542$$

$$R_S = R_C + 1 = 0 + 1 = 1$$

$$I_S = I_C - 1 = 542 - 1 = 541$$

R and I have to be translated into binary code.

DIGITAL/ANALOG CONVERTERS

The six pulse-width modulation (PWM) D/A converters have a resolution of 64 steps and an output frequency of 16 kHz (with 4 MHz clock). At power on reset they are set to a duty cycle of zero.

POWER ON RESET

The V_{DD1} and V_{DD2} supplies have an integrated digital power on reset with a duration of 250 ms.

The reset condition is signalled by a low level on the out-of-lock output, $\overline{OL}$. The microprocessor can test this condition by reading bit 1 of register 12. This bit is zero during power on reset and the $\overline{OL}$ output remains active until it is read. Reading this bit automatically restores it to a high state.

During power on reset time commands from the micoprocessor are not acknowledged. Power on reset also sets the phase comparator output to a high impedance, state. It is restored by resetting bit 4 of register 8.

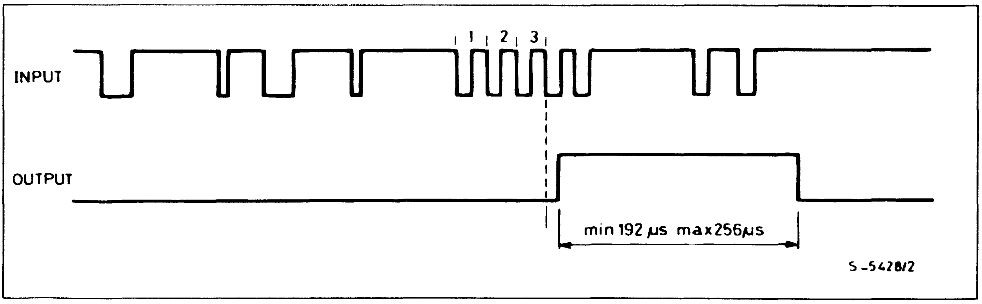
REMOTE CONTROL SIGNAL PRE-PROCESSOR

This section contains a preamplifier, squarer, digital filter and a pulse generator. The digital filter enables the pulse generator only if three successive negative going pulses (4 edges) are detected. The distance between these pulses must be in the range 24-27 µs (about 37-41 kHz with a 4 MHz clock). The input is not tested for the duration of the output pulse (192-256 µs).

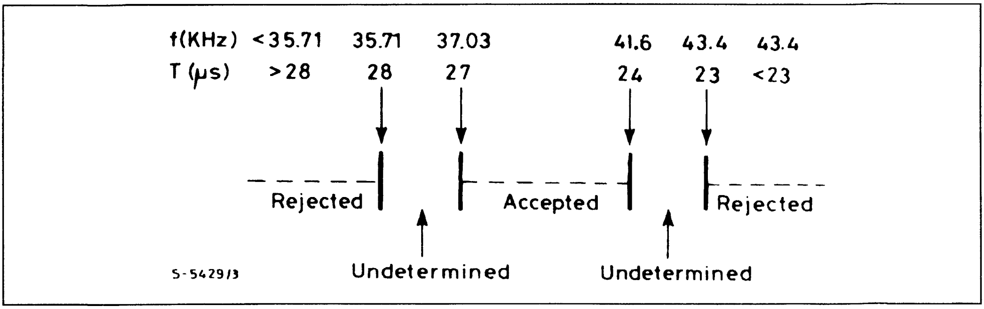
If this pre-processor is used in conjunction with M709 or M710 remote control transmitters valid signals can be recognized in the presence of extreme noise conditions. Separating the signals from the noise externally in this way reduces the number of interrupts that the microcomputer has to handle thus allowing it to concentrate on other takes. To take advantage of this section the M708, 709, 710 transmitters must operate with a clock frequency in the range 492-508 kHz.

The input can be DC or AC compled to the I.R. preamplifier.

In case of DC coupling the quiescent input level is suggested to be 1.5 V.



Response of the Digital Filter as a Function of the Input Frequency (in kHz).



M206 PROGRAMMING SUMMARY

Registers 0-5 – D/A Convertors 1-6

5 0	
BINARY CODED ANALOG VALUE	R0-R5 6 bits
MSB LSB	

Register 6 – PLL Program Counter.

6 0	
PROGRAM COUNT UPPER 7 BITS	7 bits
MSB	

Register 7 – PLL Program/Swallow Counter.

7	0	
PROGR. COUNT LOWER 4 BITS	SWALLOW COUNT	8 bits
LSB	MSB LSB	

Register 8 – Band Drive Outputs/Phase Comparator Output Control.

6						0
PCOH	PCOL	PCOZ	B3	B2	B1	B0

B0-B3 Band Drive outputs B0-B3
PCOZ Phase Comparator Output High Impedance
PCOL Phase Comparator Output Low Level
PCOH Phase Comparator Output High Level

PCOH	PCOL	PCOZ	Phase Comparator Output
L	L	L	Normal PLL Operation
L	L	H	High Impedance State
L	H	L	Low for 1 ms then returns automatically to normal PLL operation.
L	H	H	Low for 1 ms then returns to high impedance state.
H	L	L	High for 1 ms then returns to normal PLL operation.
H	L	H	High for 1 ms then returns to high impedance.
H	H	L	Normal Operation *
H	H	H	High Impedance *

* These combinations are not accepted and PCOL, PCOH are automatically reset low after 1 ms.

Register 9 – NV Memory Address.

4	0	
ADDRESS		5 bits
MSB	MSB	

Registers 10 & 11 – NV Memory Data.

7	0		7	0	
UPPER EIGHT DATA BITS		R10 8 bits	LOWER EIGHT DATA BITS		R11 8 bits
MSB				LSB	

Register 12 – NV Modify Status/Reset Status.

1	0	
RESET STATUS	MODIFY STATUS	2 bits

Flag	L	H
MODIFY STATUS RESET STATUS	Modify in progress. Reset actived.	Modify over. Reset not actived.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70 °C ; typical values are at T_{amb} = 25 °C)

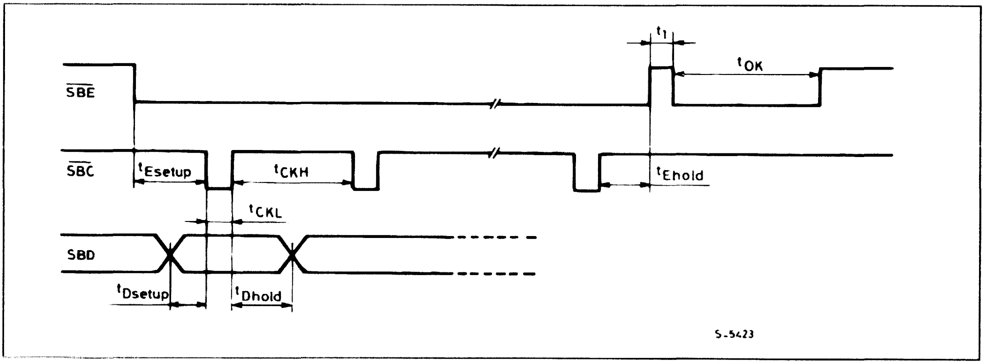
Symbol	Parameter	Pins	Test Conditions			Values Min.	Values Typ.	Values Max.	Unit
V_{DD1}, V_{DD2}	Supply Voltage	5–6				4.75	5	5.25	V
V_{PP}	Memory Supply Voltage	25				24	25	26	V
V_{IL}	Input Low Voltage	12–13–14–17				0		0.8	V
V_{IH}	Input High Voltage	12–13–14–17				2.4		5.25	V
V_{IPP}	Peak to Peak Signal	11	AC COUPLING			0.5		13.2	V
V_{TH}	Threshold Voltage	11	DC COUPLING				1.25		V
V_{OL}	Output Low Voltage	10–12–13 16–18–20 21–22–23	V_{DD} = 4.75 V I_{OL} = 1.6 mA					0.4	V
		9	V_{DD} = 4.75 V I_{OL} = 0.2 mA					0.4	
		15	V_{DD} = 4.75 V I_{OL} = 1 mA				0.2	0.4	
		2–3–4–26 27–28	V_{DD} = 4.75 V I_{OL} = 5 mA					1	
		24	V_{DD} = 4.75 V I_{OL} = 2.5 mA					8	
V_{OH}		9–18	V_{DD} = 4.75 V I_{OH} = – 0.2 mA					2.4	V
		15	I_{OH} = – 1 mA				V_{DD2} – 0.2	V_{DD2} – 0.4	
$I_{O(off)}$	Output Leakage Current	2–3–4–10–16 20–21–22–23 26–27–28	V_{DD} = 4.75 V $V_{O(off)}$ = 5.25 V					10	µA
		24	V_{DD} = 4.75 V $V_{O(off)}$ = 26 V					100	µA
I_{IL}	Input Low Current	12-13	V_{DD} = 5.25 V V_{OL} = 0.4 V				50	200	µA
I_{OZ}	High Impedance output Current	15	V_O = 0 to V_{DD2}				± 20		nA
I_{DD1}	Supply Current	6	V_{DD1} = 5.25 V					8	mA
I_{DD2}	Supply Current	5	V_{DD2} = 5.25 V					30	mA
I_{PP}	Memory Supply current	25	V_{PP} = 26 V	Write	Peak			40	mA
					Average			11	
				Erase	Pak			7	
					Average			4.5	
				Read	Peak			6	
					Average			2	

DYNAMIC ELECTRICAL CHARACTERISTICS

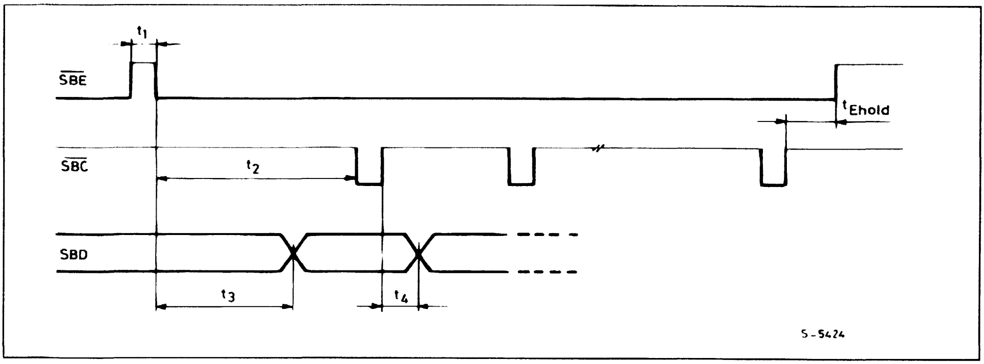
Symbol	Parameter	Test Conditions	Min.	Tup.	Max.	Unit
t_{CKL}	$\overline{SBC}$ LOW Time		2		50	µs
t_{CKH}	$\overline{SBC}$ HIGH Time		4			
$t_{E\ setup}$	$\overline{SBE}$ Set-up to $\overline{SBC}$ falling edge time		0.5			
$t_{E\ hold}$	$\overline{SBE}$ Hold Time from $\overline{SBC}$ rising edge		3			
$t_{D\ setup}$	Data Setup Time		1			
$t_{D\ hold}$	Data Hold time		1			
t_1	Time between $\overline{SBE}$ Rising Edge and OK of Reception				3	
t_{OK}	OK of Reception Time			22	26	
t_2	Minimum $\overline{SBC}$ Delay Time from OK of Reception		26			
t_3	Data Valid Time from OK of Reception			20	25	
t_4	Data Valid Time from $\overline{SBC}$ Pulse				4	
t_5	Propagation Delay of PMC				0.9	

TIMING WAVEFORMS

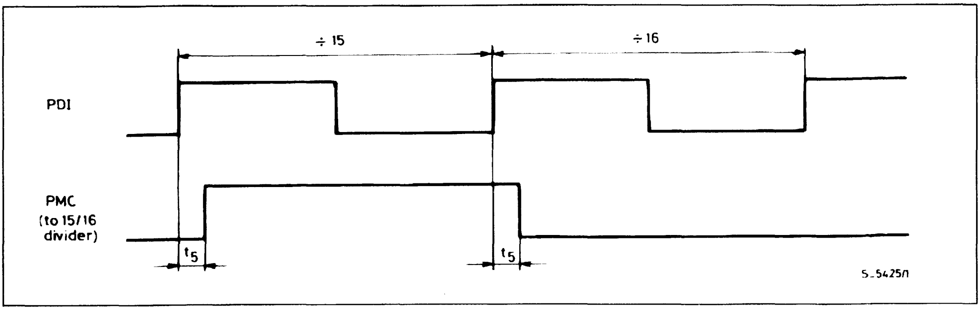
REGISTER LOAD



REGISTER READ

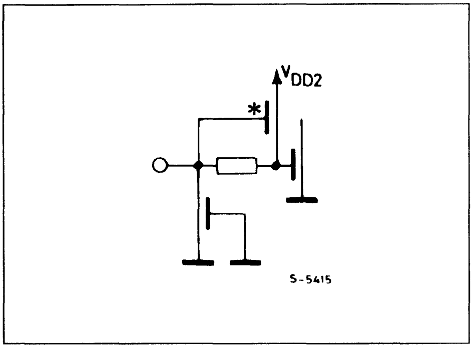


PRESCALER MODULO CONTROL TIMING

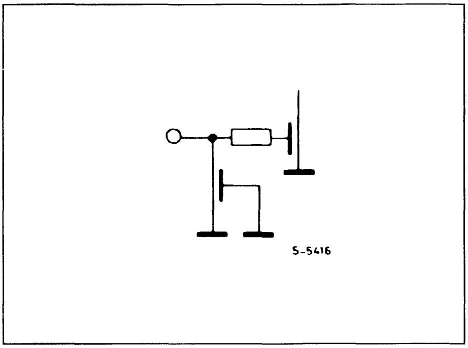


INPUT AND OUTPUT CONFIGURATIONS

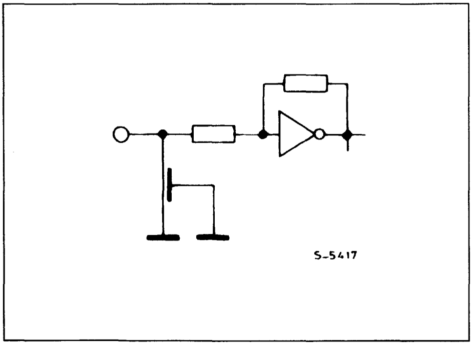
$\overline{SBC}$



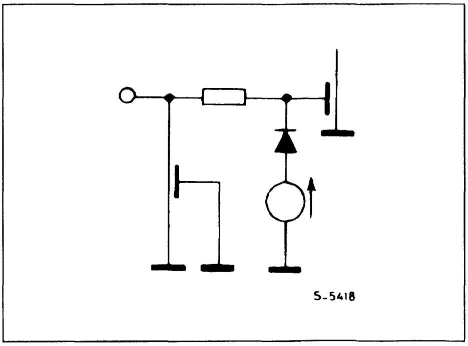
PDI



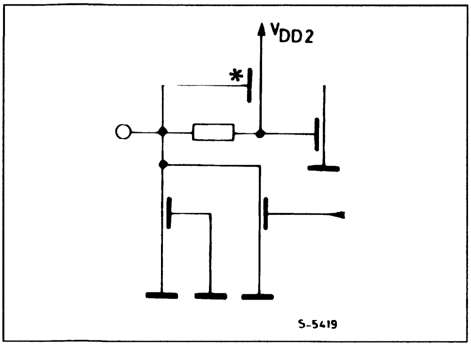
CLIN



RCIN

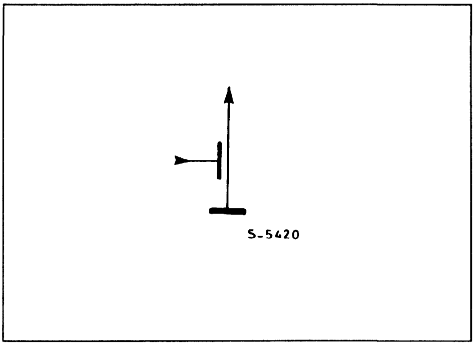


SBD, $\overline{SBE}$

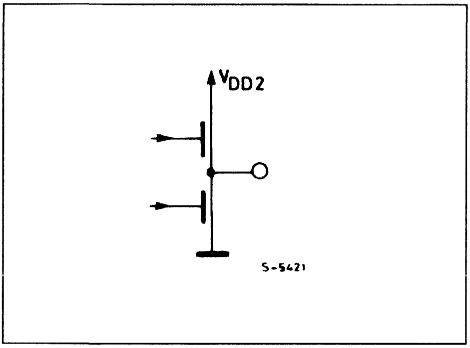


* Depletion transistors.

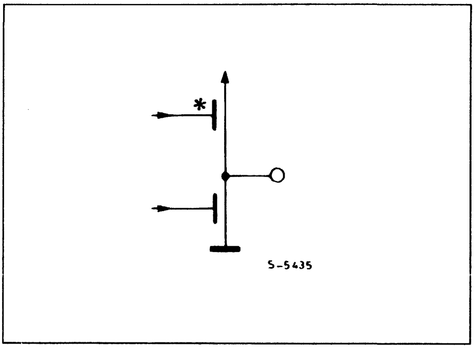
DA1-DA6, B0-B3, $\overline{OL}$, RCOUT



PCO

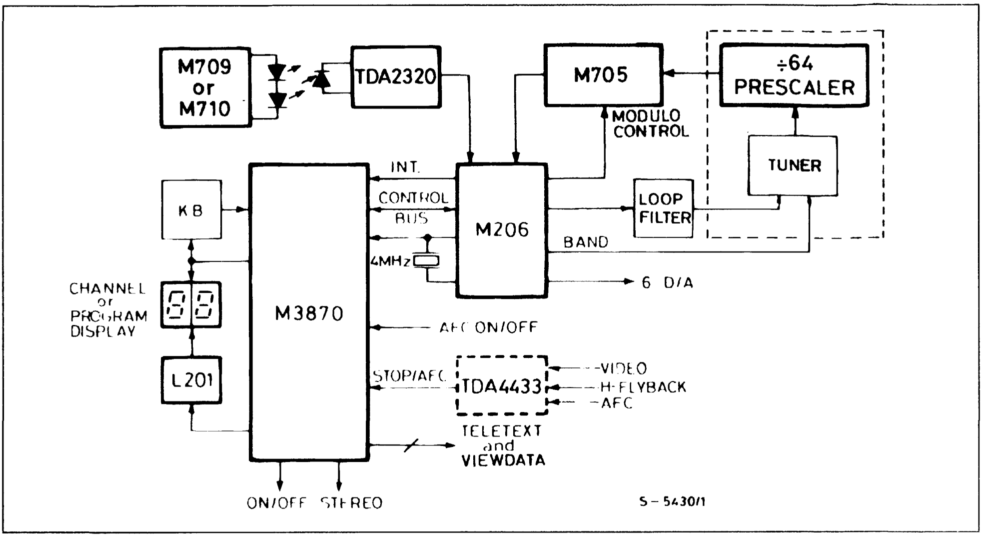


PMC, CLOUT, CLBUF



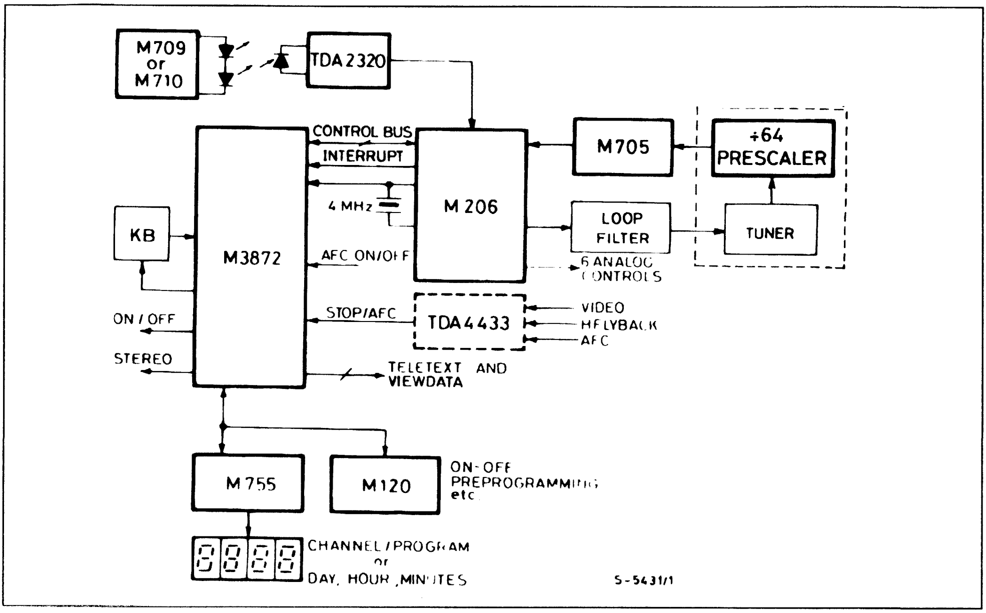
TYPICAL APPLICATIONS

Remote Controlled TV Frequency Synthetizer.



- Remote Control Decoding by Microprocessor.
- 32 Station Non-Volatile Memory or 30 Station
- Memory + Normalized D/A Positions
- Flexible System Operation
- Frequency Synthesis of all Standard and CATV Channels
- Direct Channel Selection
- ± 4 MHz Fine Tuning (62.5 kHz per Step)
- Automatic Search within Channel (using TDA4433)
- AFC Operation (using TDA4433)
- 6 D/A Converters
- Teletext and Viewdata Data Bus Conversion

Remote Controlled TV Frequency Synthetizer and Clock Timer.



Frequency Synthesis as described in the Basic Configuration with the addition of :
- Further Station Memory, using M120, 1 K NV MEMORY
- Clock and programmable timer for automatic switch ON/OFF, using M755.

SGS-THOMSON MICROELECTRONICS

M293

EPM 32 ELECTRONIC PROGRAM MEMORY FOR 32 STATIONS

- ONE CHIP INCLUDING CONTROL AND NV MEMORY
- SUPPLY VOLTAGE $V_{DD} = 5\ V \pm 5\ \%$ $V_{PP} = 25\ V \pm 1\ V$ (only for storage and reading)
- AUTOMATIC, SEMIAUTOMATIC AND MANUAL SEARCH MODES
- MANUAL SEARCH CONTROLLED BY ONLY TWO KEYS (up and down). THE SEARCH SPEED IS AUTOMATICALLY INCREASED SMOOTHLY WITH THE TIME
- 4 BAND OUTPUTS WITH STEP-BY-STEP SELECTION AND THE POSSIBILITY OF SKIPPING UNWANTED BANDS
- MEMORY ADDRESSING AND COPY CAPABILITY
- EXTERNALLY ADJUSTABLE SEARCH SPEED
- 445 TO 510 kHz CLOCK OSCILLATOR
- VOLTAGE SYNTHESIZER, 8192 STEP RESOLUTION
- FINE TUNING IN 8 STEPS, STORABLE FOR EACH PROGRAM SEPARATELY
- MINIMUM EXTERNAL COMPONENTS
- INTEGRATED DIGITAL POWER-ON RESET (1 second)
- TECHNICAL NOTE TN 153 AVAILABLE

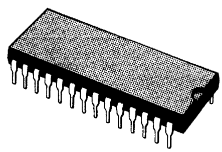
DESCRIPTION

The M293 is a monolithic integrated circuit constructed in N-channel silicon gate technology, designed to control a varicap tuner with a resolution of 8192 steps (13 bits) via a D/A converter, using the principle of voltage synthesis.

The device also includes a 544 bit NV Memory for storage of 32 stations. Each station is identified by a 17 bit word containing the information for tuning voltage (12 bits), band (2 bits) and fine tuning (3 bits). The circuit is able to operate in automatic, semiautomatic or manual modes. The search speed is controlled externally by an RC network and is adapted internally to the various bands and mode of operation. In the automatic mode the M293 works in conjunction with the TDA4433, which recognizes TV stations and converts the AFC-S-curve into a digital command. The stations are selected by applying a static bit binary word. A strobe input is also provide. A 7 segment decoder-driver (e.g. TDA4092) can be connected to the same lines for Program number display.

A serial information output is provided so that using the M191, the varicap voltage in the form of a linear bar and the selected band can be displayed on the screen.

The M293 is available in a 28 lead dual in-line plastic package.



DIP28

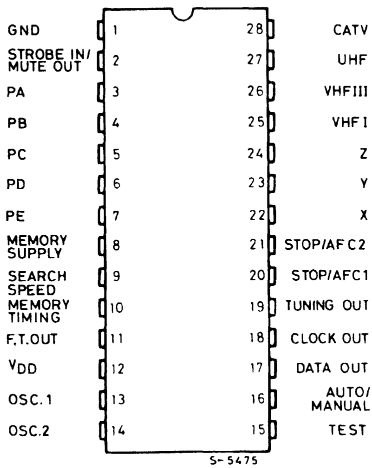
ORDER CODE : M293B1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 28	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O\,(off)}$	Off State Input Voltage (except pin 10) Pin 10	15 28	V V
I_{OL}	Output Current (except pins 11 – 19) Pins 11 – 19	5 7.5	mA mA
I_{OH}	Output Current (pin 2)	– 2	mA
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Teperature	– 25 to 125	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS

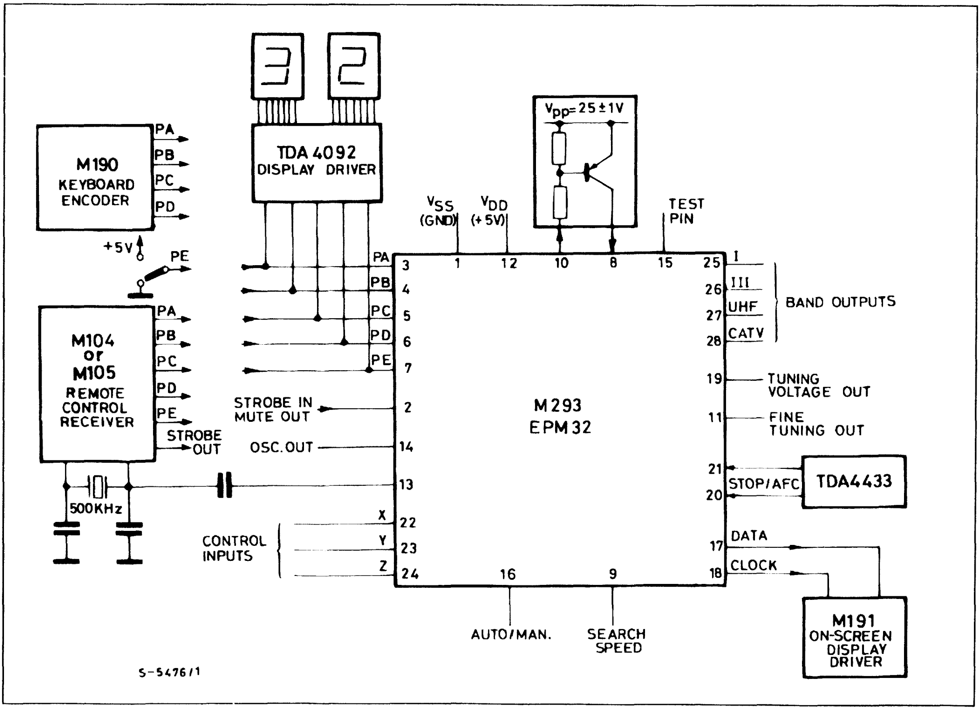


RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	4.75 to 5.25	V
V_{PP}	Memory Supply Voltage	24 to 26	V
V_I	Input Voltage	0 to 13.2	V
$V_{O\ (off)}$	Off State Input Voltage (except pin 10) Pin 10	Max. 13.2 Max. 26	V V
I_{OL}	Output Current (except pins 11 – 19) Pins 11 – 19	Max. 2.5 Max. 5	mA mA
I_{OH}	Output Current (pin 2)	Max. – 0.25	mA
t_{pd}	Delay between Memory Timing and Memory Supply Pulses	Max. 5	µs
f	Clock Frequency	500	kHz
T_{op}	Operating Temperature	0 to 70	°C
R9	Search Speed Resistance (pin 9)	18 to 330	KΩ
C9	Search Speed Capacitance (pin 9)	Max. 100	nF
t_d	Delay of V_{PP} from V_{DD} at Power-on	Max. 1	sec.
t_r	Rise Time of V_{PP} (during storage or reading)	2 to 10	µs
r_s	Serial Resistance of the Ceramic Resonator	Max. 20	Ω

BLOCK DIAGRAM

Figure 1.



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)
Typical Values are at 5 V and T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions	Value Min.	Value Typ.	Value Max.	Unit
V_{IL}	Input Low Voltage	2–3–4–5–6–7				0.8	V
		25–26–27–28				0.3	
		16–20–21–22 23–24				1.5	
V_{IH}	Input High Voltage	2–3–5–6–7				2	V
		25–26–27–28				3	
		16–20–21–22 23–24				3.5	
V_{OL}	Output Low Voltage	25–26–27–28	V_{DD} = 4.75 V I_{OL} = 1 mA			3	V
		11–19	V_{DD} = 4.75 V I_{OL} = 5 mA			1	
		2–7–18	V_{DD} = 4.75 V I_{OL} = 100 µA			0.4	
		10	V_{DD} = 4.75 V I_{OL} = 5 mA			8	
V_{OH}	Output High Voltage	2	V_{DD} = 4.75 V I_{OH} = – 0.25 mA			2.4	V
		17–18	V_{DD} = 4.75 V I_{OH} = – 0.15 mA			2.4	
$I_{O (off)}$	Output Leakage Current	25–26–27–28	V_{DD} = 5.25 V $V_{O (off)}$ = 13.2 V			100	µA
		11–19	V_{DD} = 5.25 V $V_{O (off)}$ = 13.2 V			50	
		10	V_{DD} = 4.75 V $V_{O (off)}$ = 26 V			100	
I_{IL}	Input Low Current	3–4–5–6–7 16–22–23–24	V_{DD} = 5.25 V V_{IL} = 0.8 V			– 0.4	mA
		20–21	V_{DD} = 5.25 V V_{IL} = 1.5 V			– 0.4	
		2	V_{DD} = 5.25 V V_{IL} = 0.4 V			– 1.6	
I_{DD}	Supply Current	12	V_{DD} = 5.25 V		20	50	mA
I_{PP}	Memory Supply Current	8	V_{PP} = 26 V Write Peak			40	mA
			Write Average			11	
			Erase Peak			7	
			Erase Average			4.5	
			Read Peak			6	
			Read Average			2	

DESCRIPTION (all timings are given with f_{ref} = 500 kHz)

The circuit description follows both pin sequence and pin function.

PIN 1. V_{SS}

The substrate of the integrated circuit is connected to this pin.

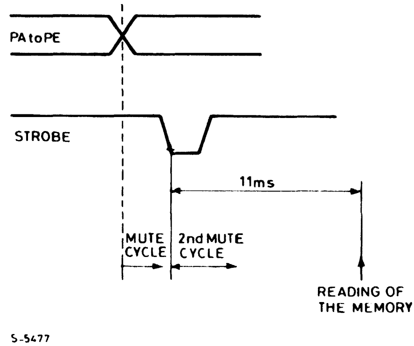
PIN 2. PROGRAM STROBE INPUT/MUTE INPUT

PROGRAM STROBE INPUT. Although the program change is internally detected and the M293 can also work with Remote Control receivers without any strobe output, the strobe function is useful, for example, to recall the stored tuning voltage after a search.

This input is active low and has an internal pull-up to 6 K (typ).

A second mute cycle restarts when the input goes low and the memory is read after 110 ms.

Figure 2.



MUTE OUTPUT. The output transistor is switched on when the Mute function is activated.

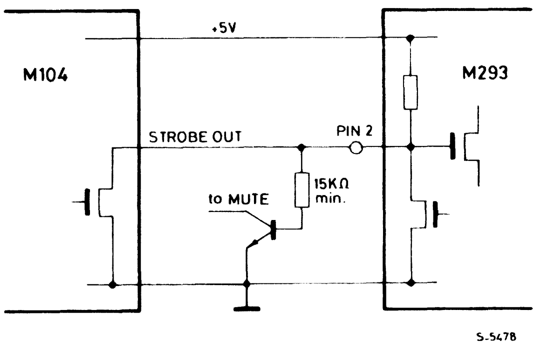
The Mute is present in the following cases :

- at band change } The mute is active 110 ms
- at program change } before the execution of the command and lasts 480 ms
- during automatic search

The Mute is active 110 ms before the start of the search

- when the supply voltage VDD is applied, for about 1 second
- when the supply voltage VDD is removed.

Figure 3.



PIN 3-4-5-6-7. PROGRAM SELECTION INPUTS

The programs are selected with a static 5 bit word according to the truth table given below. Input levels are TTL compatible. The inputs have an internal pull-up of 30 K (typ.). The memory is read with a delay of 110 ms, after the strobe command or the program change.

Program	PA	PB	PC	PD	PE	Program	PA	PB	PC	PD	PE
1	L	L	L	L	L	17	L	L	L	L	H
2	H	L	L	L	L	18	H	L	L	L	H
3	L	H	L	L	L	19	L	H	L	L	H
4	H	H	L	L	L	20	H	H	L	L	H
5	L	L	H	L	L	21	L	L	H	L	H
6	H	L	H	L	L	22	H	L	H	L	H
7	L	H	H	L	L	23	L	H	H	L	H
8	H	H	H	L	L	24	H	H	H	L	H
9	L	L	L	H	L	25	L	L	L	H	H
10	H	L	L	H	L	26	H	L	L	H	H
11	L	H	L	H	L	27	L	H	L	H	H
12	H	H	L	H	L	28	H	H	L	H	H
13	L	L	H	H	L	29	L	L	H	H	H
14	H	L	H	H	L	30	H	L	H	H	H
15	L	H	H	H	L	31	L	H	H	H	H
16	H	H	H	H	L	32	H	H	H	H	H

PIN 8. MEMORY SUPPLY VOLTAGE

A supply voltage of 25 ± 1 V has to be applied to this pin during the modify and read cycles.

MODIFY CYCLE

A modify cycle consists of three steps :

1. All "1"s are written in the bits of the selected word.
2. All bits of the selected word are erased (all "0"s).
3. The new content is written.

In this way a constant aging of all the bits of the word is obtained.

During both write and erase cycles the memory situation is checked continuously ; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

WRITE CYCLE. The peak of the current flowing through pin 8 during a write operation is shown in fig. 4, while fig. 5 shows the envelope of the same current.

The typical write time is 3-4 ms for the first cycles and increase to about 30 ms after 1000 cycles.

Figure 4.

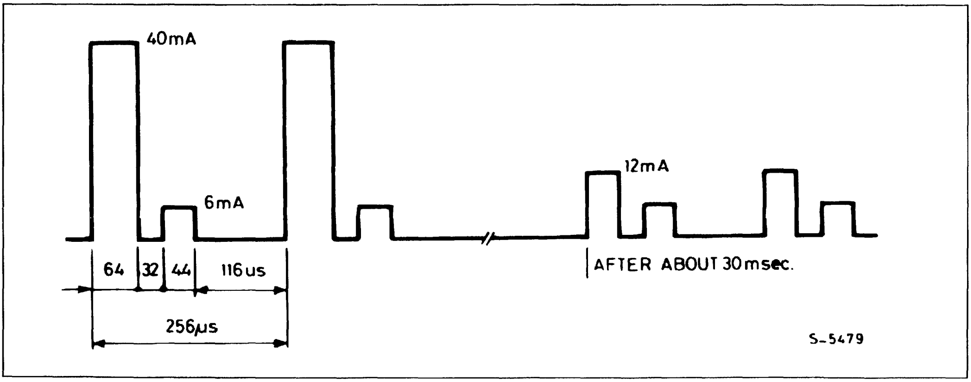
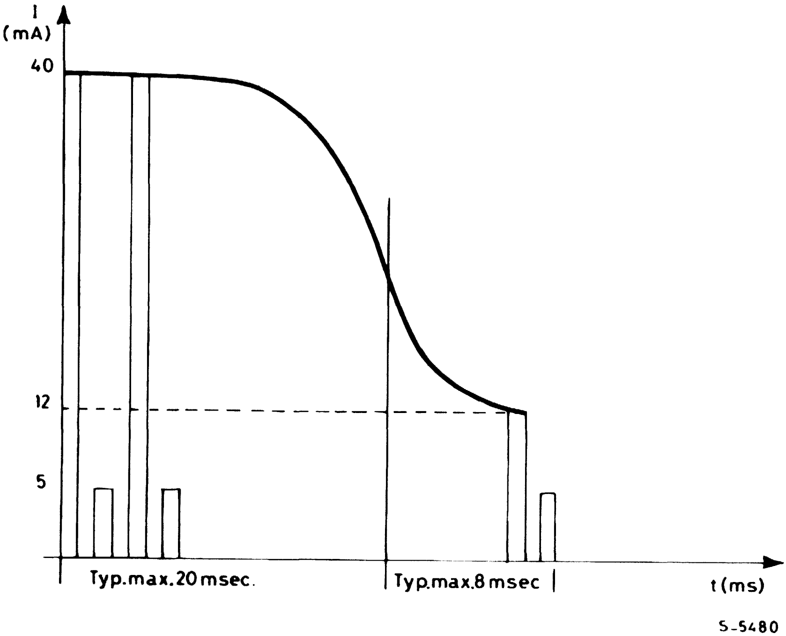


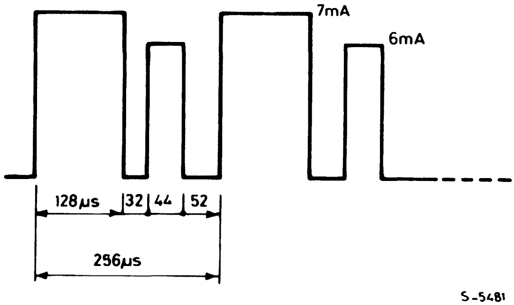
Figure 5.



ERASE CYCLE. Fig. 6 shows the timing and the waveform of the current flowing through pin 8 during the erase operation.

The peak current is 7 mA (max) during the erase cycle and 6 mA (max) during the read cycle. The typical erase time is 10 ms for a new device and it increases with the number of modify operations up to 200 ms after 1000 cycles.

Figure 6.

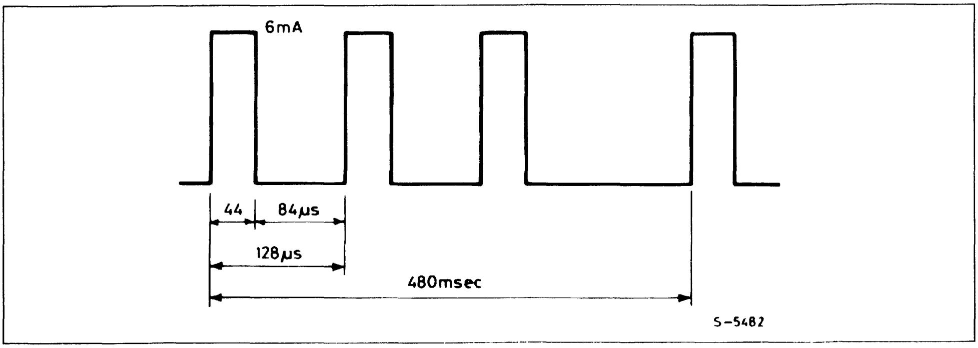


In order to protect the memory in case of failure of some bits the modify operation is stopped after 1 sec.

READ CYCLE

Fig. 7 shows the waveform of the current during a read operation.

Figure 7.



PIN 9. SEARCH SPEED

An external RC network is connected to this pin in order to set the frequency of the internal oscillator which, in turn, sets the scan speed during search.

The search speed ratios in the bands are explained in the description of pins 22, 23, 24 (UP/DOWN Manual) and of pins 20 and 21.

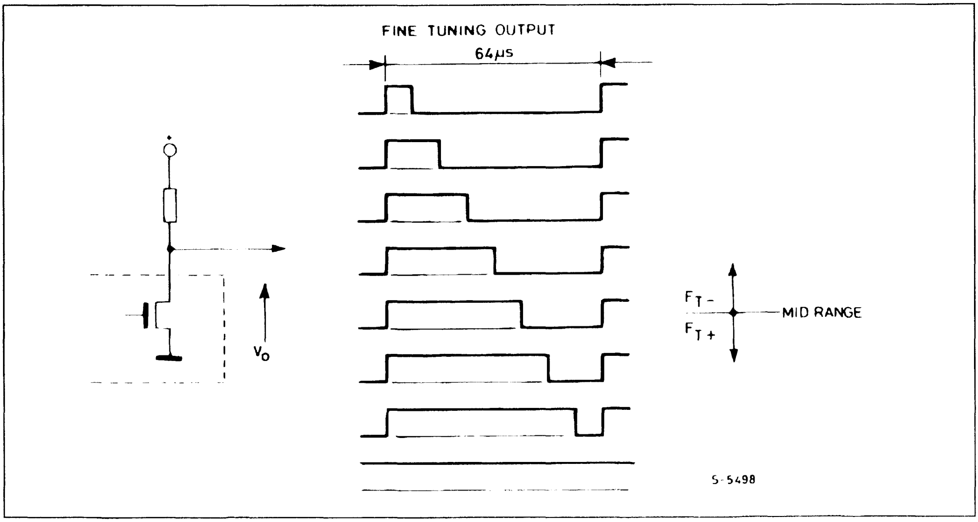
PIN 10. MEMORY TIMING OUTPUT

This output gives the timing for the pulses to be applied at pin 8 during the modify and read cycles. The output consists of an open drain transistor.

PIN 11. FINE TUNING OUT

Fine tuning information is available on this pin in the form of a square wave having a frequency of 15.625 Hz and duty cycle variable in 8 positions as indicated in fig. 8.

Figure 8.



The voltage generated after filtering is fed to the AFC loop and detunes the receiver by a small Δf while maintaining the action of the AFC.

The Fine tuning function operates as follows :

- At the start of the search (Auto or Manual) the output is set at mid range (see fig. 8).
- When the search has been completed it is possible to operate on the FINE TUNING ± commands.
  The STORE command memorizes this information together with the 12 tuning voltage and 2 bit band information.
- When a memorized channel is recalled it is possible to act on the FINE TUNING ± commands.

Any change is Fine tuning is memorized only by the STORE command. The output circuit consists of an open drain transistor.

PIN 12. V_{DD}

This pin has to be connected to a 5 V ± 0.25 V supply.

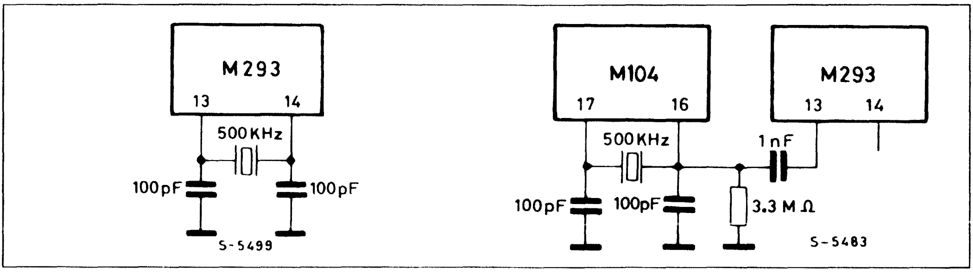
When the V_{DD} is applied to this pin an internal power on reset of 1 sec is generated : therefore, for a correct reading of the memory, the V_{PP} supply voltage must reach the value of 25 V within 1 sec after the presence of V_{DD}.

PIN 13-14. OSCILLATOR

The internal oscillator operates with a cheap 445 to 510 kHz ceramic resonator connected as shown in fig. 9.

If an external oscillator is used, the signal to be applied must be 0.5 V_{PP} min.

Figure 9.



PIN 16. AUTOMATIC/MANUAL SEARCH MODE SELECTION

This pin is used to change the search mode. When it is connected to V_{DD} the system works in Automatic mode ; when it is connected to V_{SS} the system works manually.

The change Auto-Manual or viceversa can be made at any time without affecting other circuit functions.

The input has an integrated pull-up of 30 KΩ (typ.).

PIN 17. DATA OUTPUT FOR EXTERNAL DISPLAY (M191)

A 16 bit burst is available on this pin. It contains the 8 MSB of the digitized tuning voltage, 2 bits for band information, 5 bits for program information and 1 bit which indicates that the system is in the search mode (both Automatic or Manual). The display is also enabled at the band change.

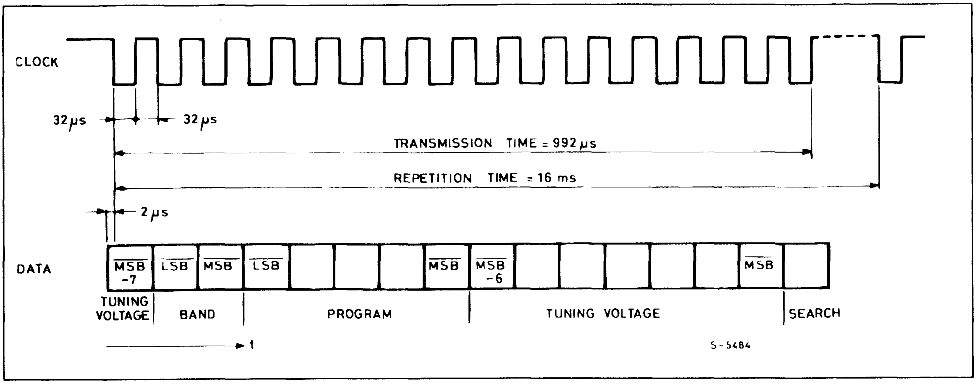
These outputs are active low and incorporate a 10 KΩ (typ) pull-up resistors.

PIN 18. CLOCK OUTPUT FOR EXTERNAL DISPLAY (M191)

A burst containing 16 clock pulses is available on this pin. This clock pulses are synchronized with Data Information as described in fig. 10.

A pull-up of 10 KΩ (typ) is integrated.

Figure 10.



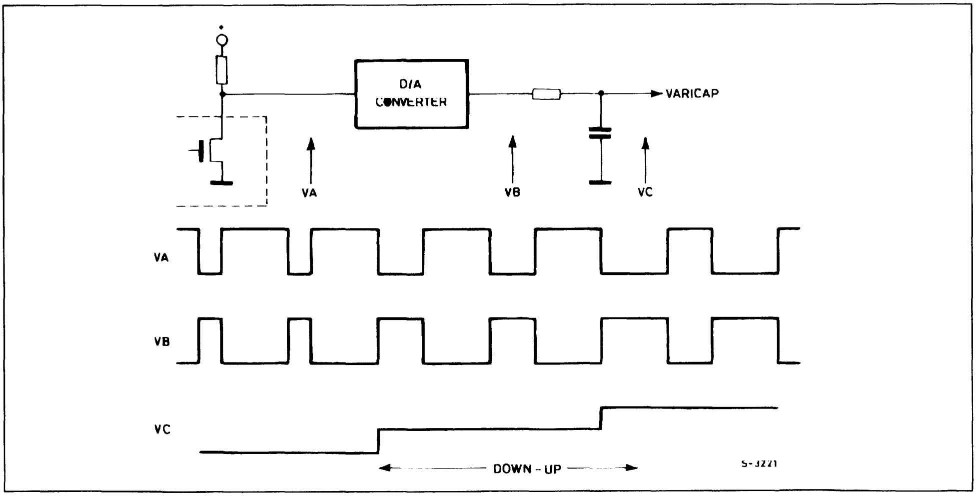
PIN 19. TUNING VOLTAGE OUT

A 2^{13} = 8192 step pulse modulated signal for the tuning voltage is available on this pin.

Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.

With a tuning voltage increasing from zero, the number of pulses increases continuously up to 2^8 = 256 ; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

Figure 11.



PIN 20-21. STOP/AFC

These pins are used only in automatic search mode.

When the M293 is in manual operation these pins are disabled internally.

The STOP/AFC inputs are also disabled internally during any program or band change for the duration of the Mute signal.

These pins work according to the truth table given below :

M293 Pin 20 TDA4433 Pin 2	M293 Pin 21 TDA4433 Pin 6	Function (referred to tuning voltage)
H	L	Up
L	H	Down
L	L	Middle
H	H	No Operation

These inputs have two different functions depending on whether the system is in the search or in normal operation (AFC control).

The inputs have internal pull-up resistors of 30 KΩ typ. (10 KΩ min).

A) **Search mode :** after depressing the Search start key, the levels of the signals coming from the TDA4433, applied to these pins, control the search function and determine when the search must stop, i.e. a TV station has been recognized. The circuit operates in the following sequence (see fig. 12 for reference and explanation of pins 22, 23, 24 for definition) :

1 - after pressing the search start key the search occurs in the FAST UP mode.

2 - eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.

If the system operates in VHF I and III the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station (for example if the search start command has been given just before an AFC control command).
After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).
A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).

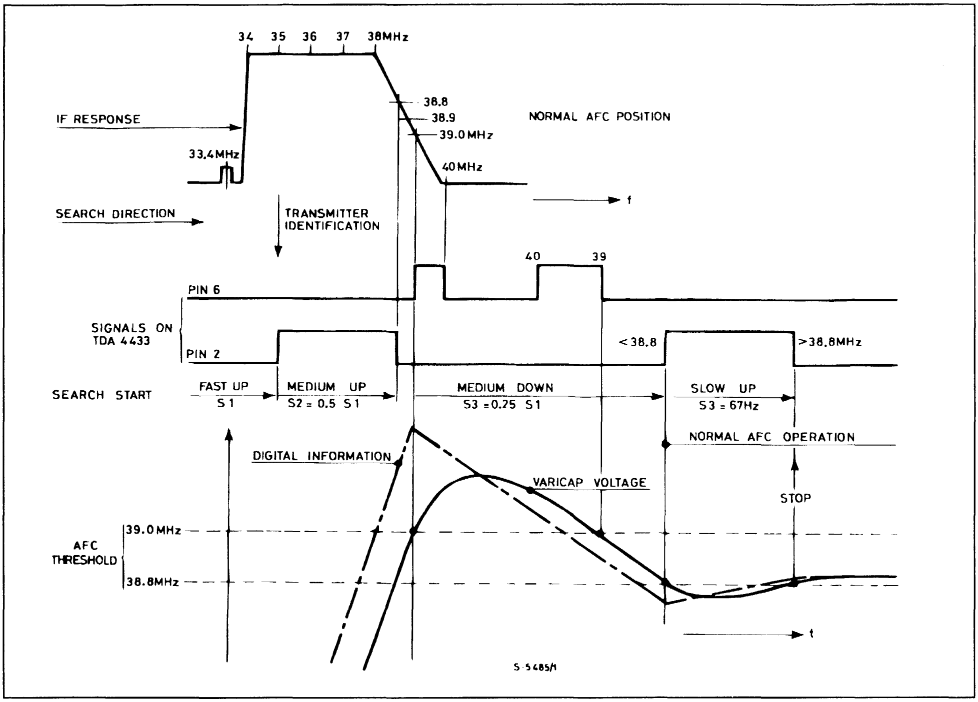
3 - the next UP signal will switch the search to SLOW UP speed (61 Hz).

At this point the system is in normal AFC operation.

B) **AFC operation :** when a station is perfectly tuned, the input signals coming from TDA4433 are at tuning condition.
If the tuning moves lower than the threshold below 38.9 MHz, the pin 20 is put H and pin 21 is put L ; the 13 bit internal counter is moved with SLOW UP speed to increase the varicap voltage.
When a detuning occurs in the opposite direction the input 20 goes low and 21 goes high and the tuning voltage is decreased with VERY SLOW DOWN speed (7.6 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.
Therefore during normal operation pins 20 and 21 act as the AFC control command.

C) **Recall from memory :** when the circuit is in automatic mode and a pre-memorized program is recalled from Memory, a fixed value of 8 steps (~ 31.2 mV) is subtracted from the tuning voltage. This corresponds to a detuning of 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFC operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.
This feature increases the AFC capture range and relaxes the stability requirements of the tuner, voltage references and the D/A converter.

Figure 12.



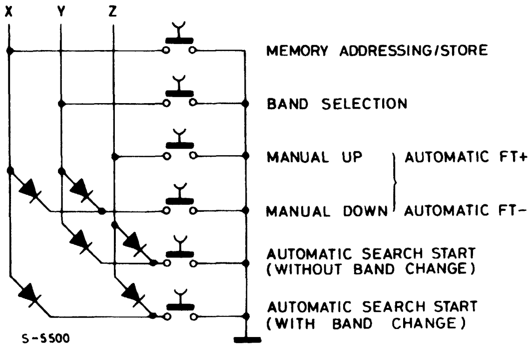
PINS 22-23-24 CONTROL INPUTS X - Y - Z

The M293 accepts binary coded commands as follows :

X	Y	Z	Function
H	H	H	--------
L	H	H	Memory Addressing/Store
H	L	H	Band Selection
H	H	L	Manual Mode (pin 16 L) { Up; Automatic Mode (pin 16 H) { FT+
L	L	H	Manual Mode (pin 16 L) { Down; Automatic Mode (pin 16 H) { FT–
H	L	L	Automatic Search Start (without band change)
L	H	L	Automatic Search Start (with band change)

The inputs have integrated pull-up resistors of 30 KΩ (typ). Commands are accepted after 30 ms of continuous presence. A new command is not accepted until the previous one has been released.

Figure 13.



MEMORY ADDRESSING/STORE. The normal sequence of program storage (program selection, search, store, new program selection and so on) can be changed in order to have the possibility to select the memory position (program number) after the search.

In this way the search is faster and continuous through the bands.

When the key is pressed it is possible to select the memory position. When the key is released the store function is activated (with 30 ms of acceptance time).

The proposed sequence of tuning and storage is as described below :

Step	Operation
1	Tune in station (manually or automatically)
2	Press "Memory addressing/Store" key and hold it pressed
3	Select the program where the tuning is to be stored
4	Release the "Memory addressing/ Store" key At this moment 12 bits of the digitizedt uning voltage, 2 bits for band 3 bits relative to Fine Tuning are stored

If this solution for memory addressing/store is not used, memorization will occur at the release of the key in the memory position previously selected.

This command is disabled during the Automatic search, During the store cycle any other operation is blocked. Only the program change command is stored internally and executed when the store cycle is over.

In order to protect the memory the store function is disabled internally after one store cycle. It is enabled after a program change or a tuning operation (it is not disabled by the AFC control).

BAND SELECTION. The bands can be step-by-step selected with the following sequence :

	Data Bus	
Band	MSB	LSB
VHF III	L	L
UHF	L	H
VHF I	H	L
CATV	H	H

Only one band change is performed at each accepted command.

Disabled bands are automatically skipped. A band can be disable by connecting the corresponding output to VSS.

MANUAL MODE UP/DOWN, AUTOMATIC MODE FT+/FT . The function of this pin depends on the search mode that is determine by pin 11.

Manual : when a command is accepted the search begins at low speed. One second later, the search speed is increased and it reaches the maximum value after 3 seconds.

Search	speed Time
÷ 8	Command accepted
÷ 4	After 1 second
÷ 2	After 2 seconds
÷ 1	After 3 seconds

The search is correlated to the selected band as follows :

Max search speeds :

Bands VHF I and VHF III : external rate divided by 3

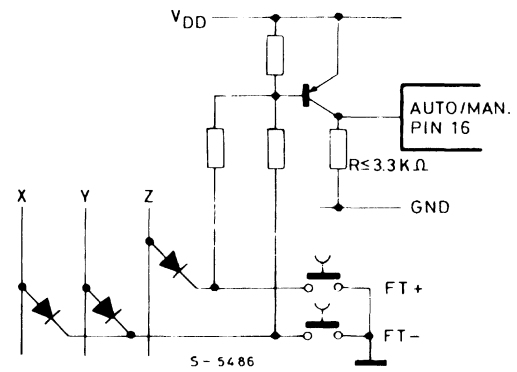
Bands UHF and CATV : external rate divided by 12

When the end of the band is reached the search restarts from the beginning of the same band after a delay of 480 ms.

Automatic fine tuning +/ : when the command is accepted, the PWM signal present at the fine tuning output (pin 11) is changed at the rate of one step every 480 ms.

Fine tuning is manual mode is possible switching temporarily the system to automatic modes as shown in fig. 14.

Figure 14.



AUTOMATIC SEARCH (without band change). When the command is accepted the search starts on the selected band. When the end of the band is reached the search restarts from the beginning of the same band after a delay of 480 ms.

If the key is held depressed another search can start only if the key is released and connected again to VSS.

During the search the tuning voltage is always changing from lower to higher voltage levels. The search is automatically stoppes when the first station is found.

The search is also stopped whenever a program selection command is given.

The search speed is determined by the RC network connected to pin 17 and is correlated to the band. UHF and CATV bands are scanned with the rate fixed externally divided by 4.

VHF bands are scanned with the rate fixed externally.

During the STOP sequence the search speed is automatically reduced as defined in the explanation of pins 20 and 21.

AUTOMATIC SEARCH (with band change). The search is effected starting from the tuning position.

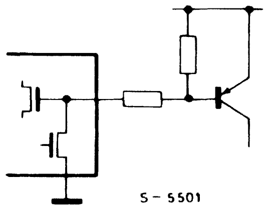
When the end of band is reached, the band is automatically changed in the sequence described at pins 22-23-24 (Band selection command). Disabled bands are automatically skipped.

PINS 25-26-27. BAND OUTPUTS/INPUTS

These outputs are provided to select up to 4 bands via external PNPs.

If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to V_{SS}.

Figure 15.

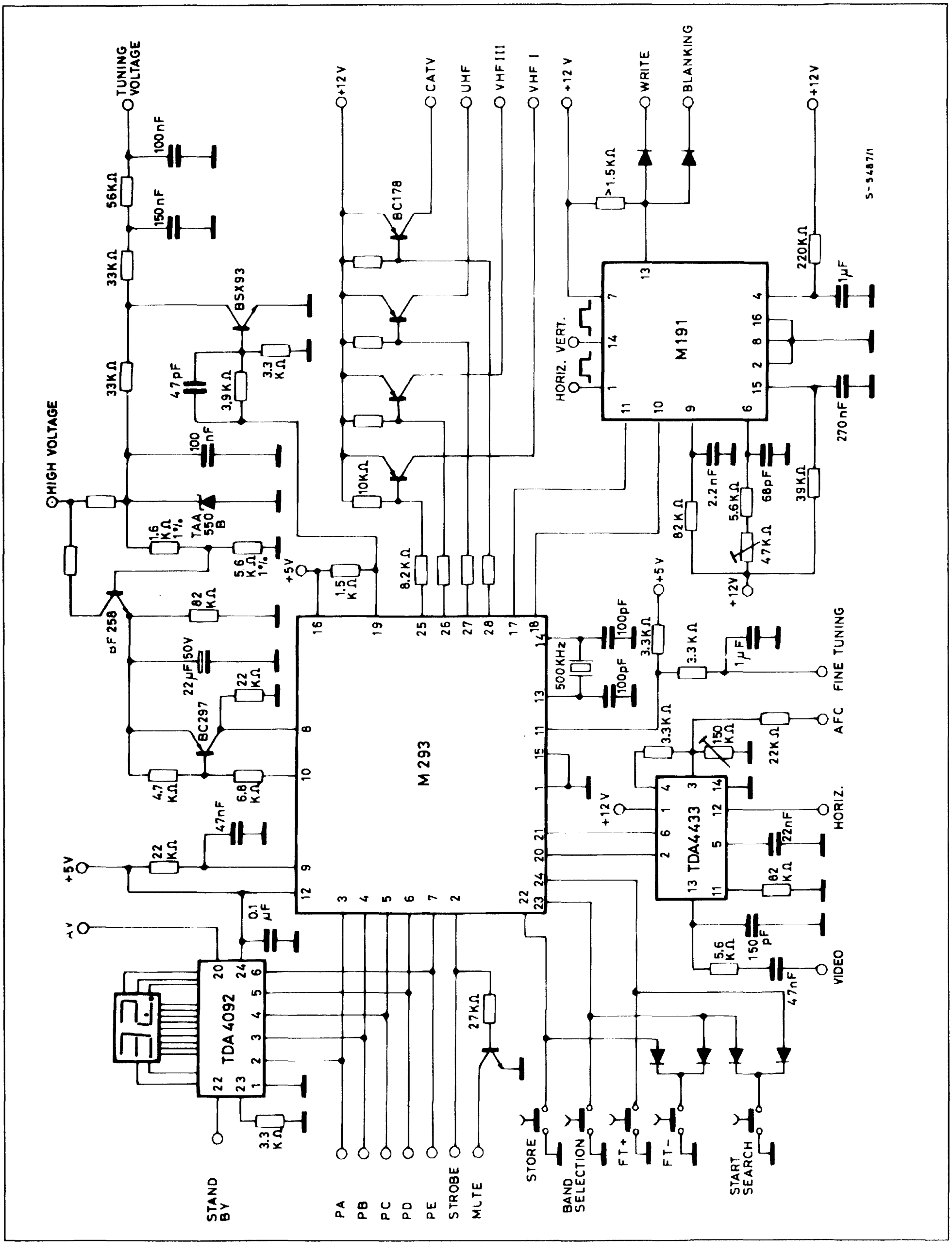


The relation between pins and bands are as follows :

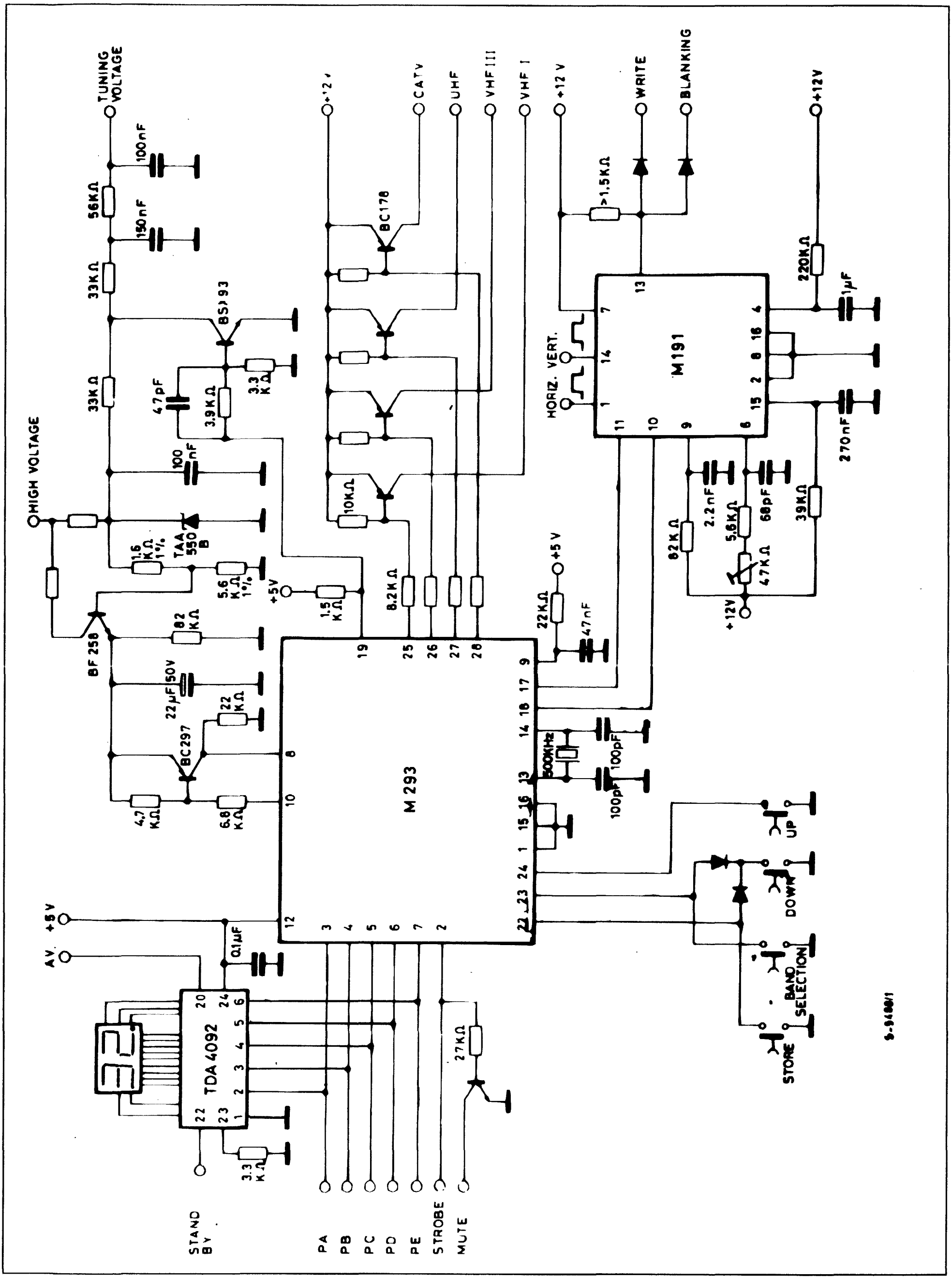
pin 25 = VHF I
pin 26 = VHF III
pin 27 = UHF
pin 28 = CATV

TYPICAL APPLICATIONS

Automatic Version.



Manual Version.



SGS-THOMSON MICROELECTRONICS

M490B
M491B

SINGLE CHIP VOLTAGE SYNTHESIS TUNING SYSTEMS WITH 1 ANALOG CONTROL

- M490B 16 STATION MEMORY - SINGLE DOT LED DISPLAY
- M491B 16 STATION MEMORY - 7 SEGMENT LED DISPLAY
- VOLTAGE SYNTHESIZER : 13 BITS
- 4 BAND PRESET CAPABILITY
- NON VOLATILE MEMORY : 304 BITS
  - 16 WORDS OF 19 BITS FOR TUNING VOLTAGE (13 bits) - BAND (2 bits) - FINE DETUNING (4 bits)
  - 10^4 MODIFY CYCLES PER WORD
  - MIN 10 YEARS DATA RETENTION
- PCM REMOTE CONTROL RECEIVER : DECODES SIGNAL TRANSMITTED BY M708
- VOLUME D/A : 6 BIT RESOLUTION/8 KHz
- MEMORY SKIP FUNCTION
- AUTOMATIC SEARCH WITH DIGITAL AFT CONTROL
- FINE DETUNING D/A ACTING ON AFT DISCRIMINATOR (16 steps) WITH SEPARATE STORAGE FOR EACH MEMORY POSITION. ALTERNATIVELY IT CAN BE USED TO CONTROL BRIGHTNESS OR COLOUR SATURATION
- MANUAL SEARCH WITH DIGITAL AFT CONTROL
- MANUAL SEARCH WITH LINEAR AFT
- SWEEP SEARCH DISPLAY OUTPUT
- SUPPLY VOLTAGES : V_{DD} = + 5 V
  V_{PP} = + 25 V FOR THE MEMORY
- CLOCK OSCILLATOR : 445 TO 510 KHz
- INTEGRATED DIGITAL POWER ON RESET (no external initialization circuitry required)

DESCRIPTION

The M490B and M491B are monolithic N-MOS LSI circuits including a Floating-gate Non-Volatile Memory for storage of up to 16 stations. Tuning of the station is performed with a 8192 step D/A converter, using the principle of voltage synthesis.

The M490B is designed to drive single dot LED displays (one LED is necessary for each used memory position). Direct and Up/Down memory selection is possible on the set or from remote control. Memory positions 11 to 16 can be skipped in case of Up/Down commands.

The M491B is designed for 7 segment LED displays. Direct memory selection is possible only from remote control while Up/Down memory scanning is possible on the set and also from remote control. An option input for 8 or 16 stations is available.

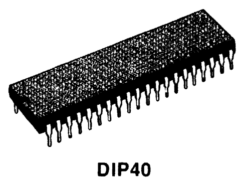
The circuits also include a PCM remote control receiver operating in conjunction with the transmitter M708. The highly reliable transmission code ensures error free signal detection even in presence of high noise conditions.

Search of the station is possible in automatic or manual modes. The circuits can operate with a Digital or Linear AFT control.

The Digital AFT mode is necessary for automatic search and requires an external circuit (TDA4433 or equivalent, e.g. dual comparator plus TV station detector) to convert the AFC-S-curve into a Up/Down command.

Fine tuning (detuning) is also possible with different modes of operation.

The circuits are assembled in 40 pin dual in-line plastic package.



DIP40

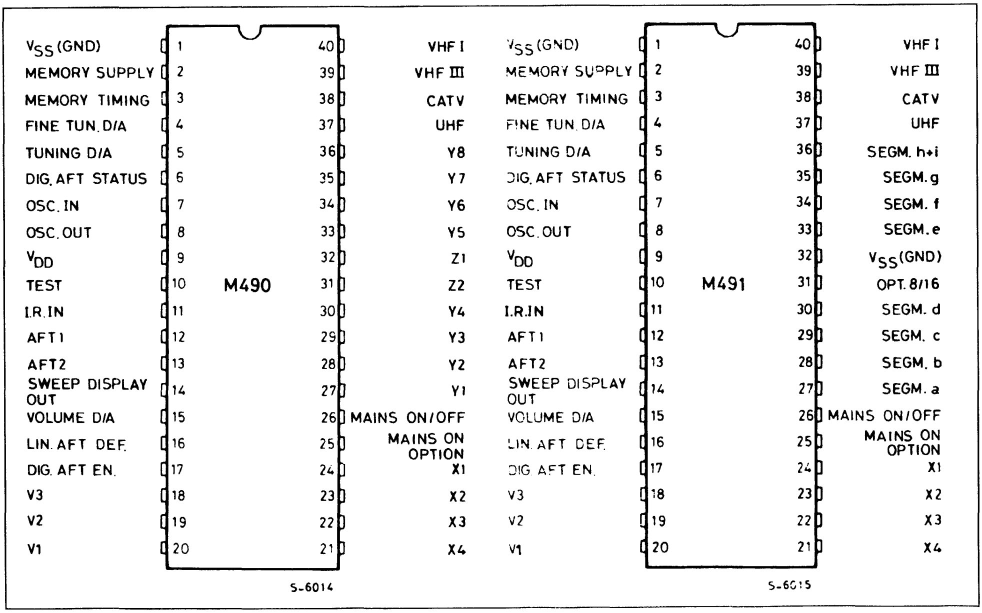
ORDER CODE : M490B B1
M491B B1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 28	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O\ (off)}$	Off State Input Voltage (except pin 3) Pin 3	15 28	V V
I_{OL}	Output Low Current Led Driver Outputs M490B Led Driver Outputs M491B Pins 6 – 14 Pins 4 – 5 All Other Outputs	 25 20 20 7.5 5	 mA mA mA mA mA
t_{pd}	Max. Delay between Memory Timing and Memory Supply Pulses	5	µs
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Teperature	– 25 to 125	°C
T_{op}	Operating Temperature	0 to 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM

Figure 1.

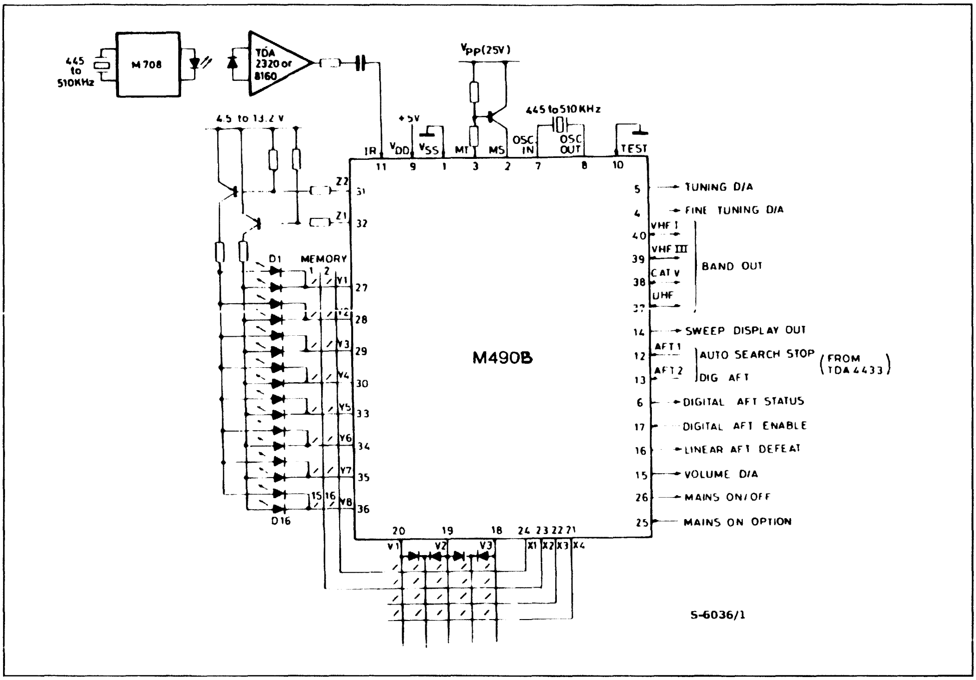
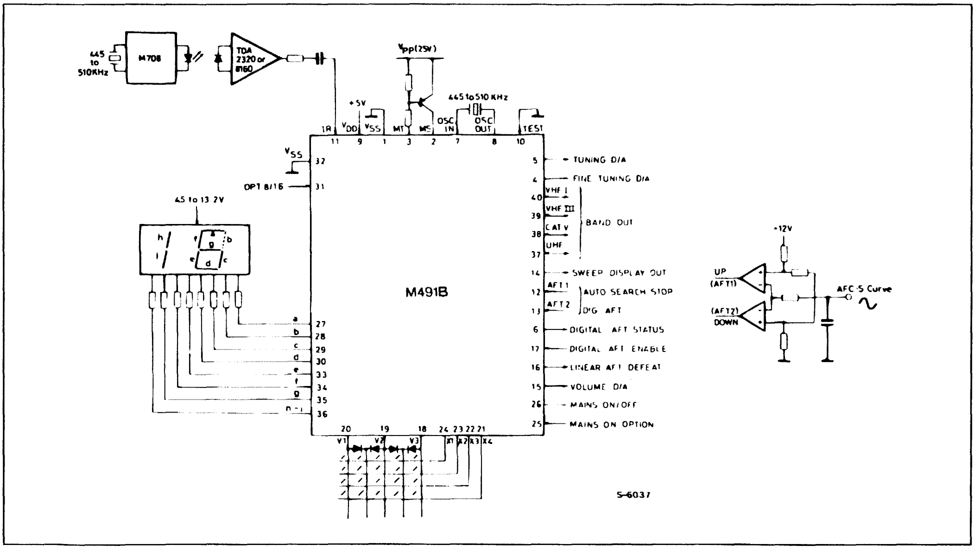


Figure 2.



M490B STATIC ELECTRICAL CHARACTERISTICS (t_{amb} = 0 to 70 °C, V_{DD} = 5 V unless otherwise specified)

Pins	Symbol	Parameter	Test Conditions		Value Min.	Value Typ.	Value Max.	Unit
2-Memory Supply	I_{PP}	Memory Supply Current	V_{PP} = 26 V					
			Write	Peak Average			42 12	mA mA
			Erase	Peak Average			9 5	mA mA
			Read	Peak Average			8 2.5	mA mA
	R	Pull Down Resistor					25	KΩ
3–Write Timing Out	V_{OL}	Output Low Voltage	V_{DD} = 4.75 V	I_{OL} = 2.5 mA			8	V
	$I_{O\ (off)}$	Output Leakage Current	V_{DD} = 4.75 V	V_{OUT} = 26 V			100	μA
4–Fine Tuning D/A 5–Tuning D/A	$I_{O\ (off)}$		V_{DD} = 5.25 V	$V_{O\ (off)}$ = 13.2 V			50	μA
	V_{OL}		V_{DD} = 4.75 V	I_{OL} = 5 mA			1	V
6–Digital AFT Out	V_{OL}		V_{DD} = 4.75 V	I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V	$V_{O\ (off)}$ = 13.2 V			100	μA
9–Power Supply	I_{DD}	Supply Current	V_{DD} = 5.25 V				100	mA
11–I.R. Input	V_{IPP}	Peak to Peak Voltage			0.5		13.2	V
12–AFT1 13–AFT2	V_{IL}	Input low Voltage	V_{DD} = 5.25 V				1.5	V
	V_{IH}	Input High Voltage	V_{DD} = 5.25 V		3.5			V
	I_{IL}	Input Low Current	V_{DD} = 5.25 V	V_{IL} = 1.5 V			– 0.4	mA
	R	Pull-up Resistor				30		KΩ
14—Display Out	V_{OL}		V_{DD} = 4.75 V	I_{OL} = 20 mA			1.5	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V	$V_{O\ (off)}$ = 13.2 V			100	μA
15–Volume D/A	V_{OL}		V_{DD} = 4.75 V	I_{OL} = 4 mA			1	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V	$V_{O\ (off)}$ = 13.2 V			50	μA
16–Linear AFT Out	V_{OL}		V_{DD} = 4.75 V	I_{OL} = 1 mA			0.4	V
	$I_{O\ (off)}$		V_{DD} = 5.25 V	$V_{O\ (off)}$ = 13.2 V			50	μA
17–Digital AFT Enable	V_{IL}						0.8	V
	V_{IH}				2.0			V
	I_{IL}		V_{DD} = 5.25 V	V_{IL} = 0.8 V			– 0.4	mA
	R	Pull-up Resistor				30		KΩ
18–19–20 V3, V2, V1 } Keyboard In	V_{IL}						1.5	V
	V_{IH}				3.5			V
	I_{IL}		V_{DD} = 5.25 V	V_{IL} = 0.8 V			– 0.4	mA
	R	Pull-up Resistor				30		KΩ

M490B STATIC ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Conditions	Values Min.	Values Typ.	Values Max.	Unit
21-22-23-24 X4, X3, X2, X1 Keyboard Out	V_{OL}		V_{DD} = 4.75 V I_{OL} = 1 mA			0.4	V
	$I_{O(off)}$		$V_{O(off)}$ = 5.5 V			25	µA
25–Mains On Enable	V_{IL}					0.8	V
	V_{IH}			2.4			V
	I_{IL}		V_{DD} = 5.25 V			–0.4	mA
	R	Pull-up Resistor	V_{IL} = 0.8 V		30		KΩ
26–Mains On/Off	V_{OL}		V_{DD} = 4.75 V I_{OL} = 100 µA			0.4	V
	I_O		V_{DD} = 4.75 V V_O = 0.7 V	–1.6			mA
27-28-29-30 33-34-35-36 Kyboard In and Display Out	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25 V V_{IL} = 0.8 V			–0.5	mA
	R	Pull-up Resistor			30		KΩ
	V_{OL}		V_{DD} = 4.75 V I_L = 20 mA			1.5	V
31–Z2, 32–Z1 MPX for Display Out	V_{OL}		V_{DD} = 4.75 V I_{OL} = 1 mA			0.4	V
	$I_{O(off)}$		V_{DD} = 5.25 V $V_{O(off)}$ = 13.2 V			50	µA
37–UHF, 38–CATV, 39–VHFIII, 40–VHFI BAND	V_{OL}		V_{DD} = 4.75 V I_{OL} = 1 mA			3	V
	V_{OH}		V_{DD} = 4.75 V I_{OH} = – 150 µA	2.4			V
	V_{IL}					0.3	V
	V_{IH}			3			V
	$I_{O(off)}$		V_{DD} = 5.25 V $V_{O(off)}$ = 13.2 V			50	µA

M491B : ALL PINS AS FOR M490B WITH EXCEPTION OF :

Pin	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
27-28-29-30 33-34-35 Display Out	V_{OL}		V_{DD} = 4.75 V I_{OL} = 20 mA			1.5	V
36–Display Out	V_{OL}		V_{DD} = 4.75 V I_{OL} = 30 mA			1.5	V
31–Memory 8/16	V_{IH}			2.0			V
	V_{IL}					0.8	V

DESCRIPTION (timings are with f_{clock} = 500 KHz)

PIN 1. V_{SS}

The substrate of the IC is connected to this pin. It is reference pin for all parameters of the IC.

PIN 2. MEMORY SUPPLY VOLTAGE

A supply voltage of 25 ± 1 V has to be applied to this pin during the modify and read cycles.

MODIFY CYCLE

A modify cycle consists of three steps :

1. All "1"s are written in the bits of the selected word.
2. All bits of the selected word are erased (all "0"s)
3. The new content is written.

In this way a constant aging of all the bits of the word is obtained.

During both write and erase cycles the memory situation is checked continuously ; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

WRITE CYCLE. The peak of the current flowing through pin 2 during a write operation is shown in fig. 3, while fig. 4 shows the envelope of the same current.

The typical write time is 3-4 ms for the first cycles and increases to about 30 ms after 1000 cycles.

Figure 3.

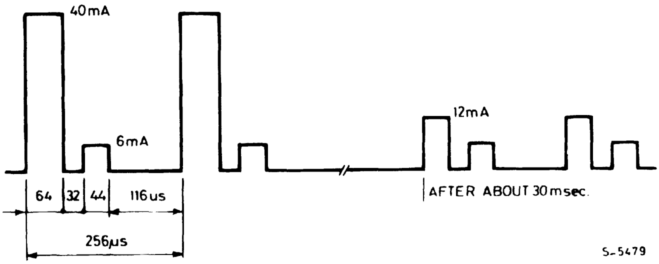
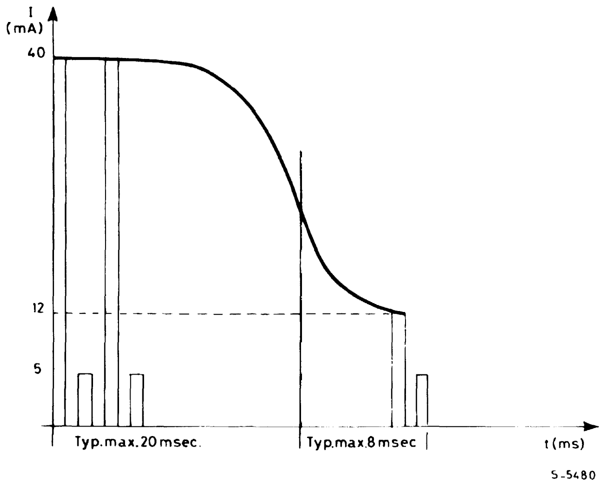
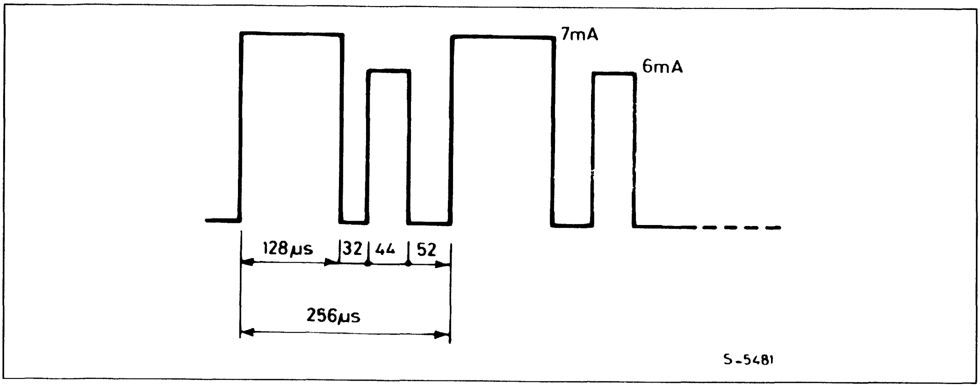


Figure 4.



ERASE CYCLE. Fig. 5 shows the timing and the waveform of the current flowing through pin 2 during the erase operation. The peak current is 7 mA (max) during the erase cycle and 6 mA (max) during the read cycle. The typical erase time is 10 ms for a new device and it increases with the number of modify operations up to 200 ms after 1000 cycles.

Figure 5.

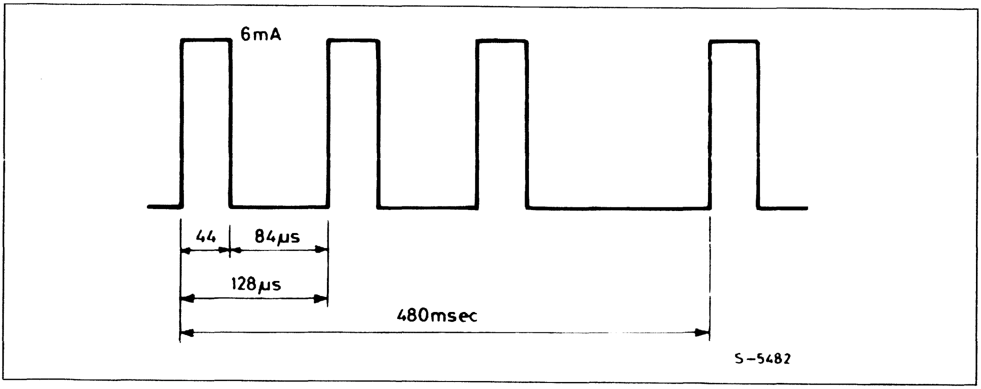


In order to protect the memory in case of failure of some bits the modify operation is stopped after 1 sec.

READ CYCLE

Fig. 6 shows the waveform of the current during a read operation.

Figure 6.



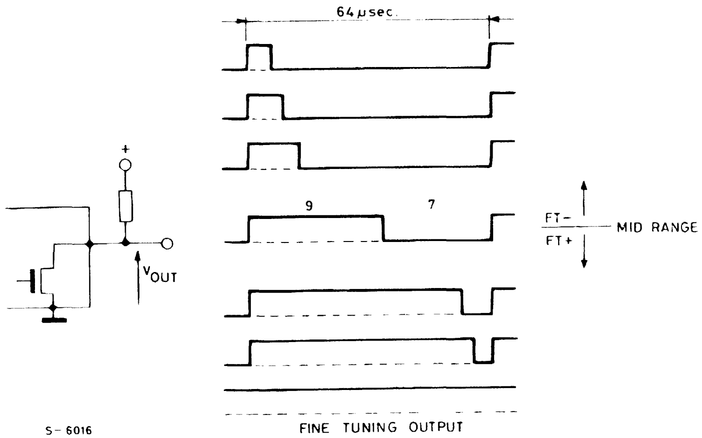
PIN 3. MEMORY TIMING OUTPUT

This output gives the timing for the pulses to be applied at pin 2 during the modify and read cycles. The output consists of an open drain transistor.

PIN 4. FINE TUNING D/A

A D/A converter with 16 step resolution and a frequency of 15 KHz can be used to generate a voltage which, if fed to a varicap diode in parallel to the AFC discriminator, will detune the receiver by a small Δf while maintaining the action of the Digital AFT. This output can be used in conjunction with both Linear and Digital AFT modes of operations.

Figure 7.



The Fine tuning function operates as follows :

- At the start of any automatic or manual search, the output is set at the mid range.
- When the search has been completed it is possible to operate on FT ± commands.
  The store command memorizes this information together with the 13 tuning voltage and 2 bit and information.
- Modification time of FT D/A is of 1 step every 200 ms if issued locally or every 2 received signals from Remote control transmitter.

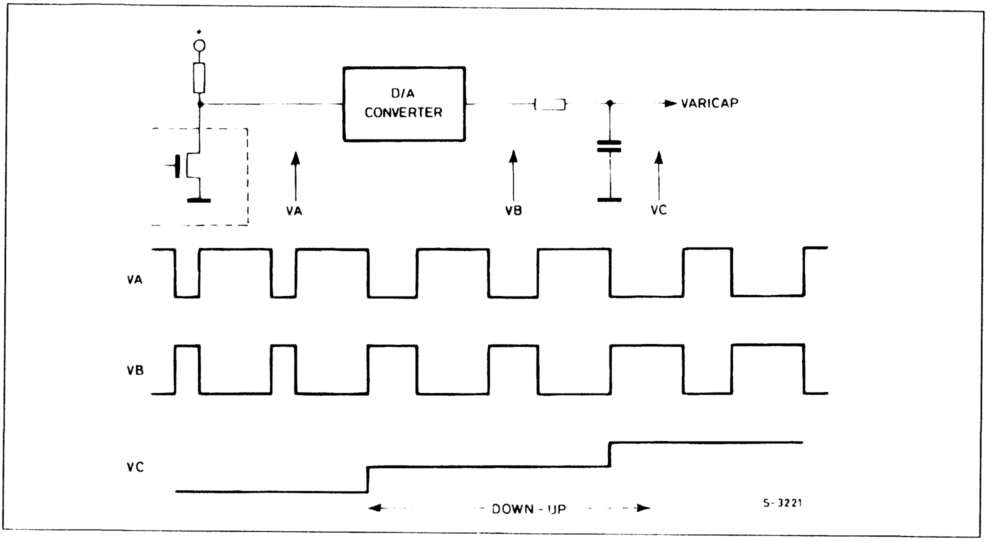
PIN 5. TUNING D/A

A 2^{13} = 8192 step pulse modulated signal for the tuning voltage is available on this pin.

Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.

With a tuning voltage increasing from zero, the number of pulses increases continuously up to 2^8 = 256 ; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

Figure 8.

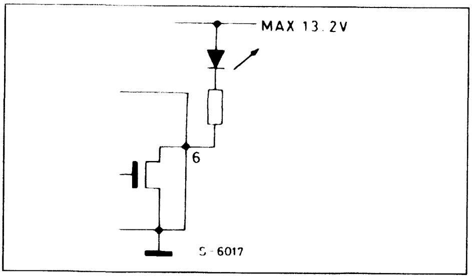


PIN 6. DIGITAL AFT STATUS OUTPUT

This output shows the status of the digital AFT. It is low when the digital AFT is enabled and it can directly drive a LED.

The output consists of an open drain transistor.

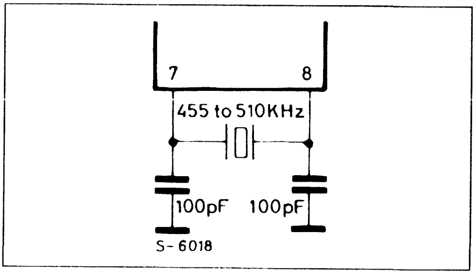
Figure 9.



PINS 7-8. OSCILLATOR INPUT/OUTPUT

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.

Figure 10.



PIN 9. V_{DD}

The supply voltage has to be comprised in the range 4.75 to 5.25 V. When it is applied an internal power on reset of 0.5 s is generated.

The memory position 1 is automatically read if the mains on option input (pin 25) is grounded.

PIN 10. TEST

This pin is used for testing and has to be connected to V_{SS}.

PIN 11. I.R. SIGNAL INPUT

The integrated receiver decodes signals transmitted by M708, address 9.

The minimum signal to be applied is 0.5 V peak to peak. (AC coupled).

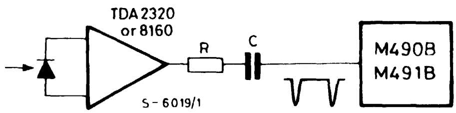
The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity :

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop-pulse
- check of noise level ; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored an decoded.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.

Figure 11.



Supply Voltage of TDA 2320	R	C
5	2.2 K	4.7 nF
12	10 K	4.7 nF

MA490B/M491B REMOTE CONTROL RECEIVER TRUTH TABLE. TRANSMITTER M708 ; ADDRESS CODE N°8

Command N°	I.R. Code						Function
	C1	C2	C3	C4	C5	C6	
0	0	0	0	0	0	0	End to Transmission
1	1	0	0	0	0	0	Power On/Off
2	1	1	0	0	0	0	Mute On/Off
3	0	0	1	0	0	0	Memory 1
4	1	0	1	0	0	0	Memory 2
5	0	1	1	0	0	0	Memory 3
6	1	1	1	0	0	0	Memory 4
7	1	0	0	0	1	0	Fine Detuning Up
8	1	1	0	0	1	0	Fine Detuning Down
9	0	0	1	0	1	0	Memory 5
10	1	0	1	0	1	0	Memory 6
11	0	1	1	0	1	0	Memory 7
12	1	1	1	0	1	0	Memory 8
13	1	0	0	0	0	1	Memory Up
14	1	1	0	0	0	1	Memory Down
15	0	0	1	0	0	1	Memory 9
16	1	0	1	0	0	1	Memory 10
17	0	1	1	0	0	1	Memory 11
18	1	1	1	0	0	1	Memory 12

MA490B/M491B REMOTE CONTROL RECEIVER TRUTH TABLE.
TRANSMITTER M708 ; ADDRESS CODE N°8

Command N°	I.R. Code						Function
	C1	C2	C3	C4	C5	C6	
19	1	0	0	0	1	1	Man. Search Up
20	1	1	0	0	1	1	Man. Search Down
21	0	0	1	0	1	1	Memory 13
22	1	0	1	0	1	1	Memory 14
23	0	1	1	0	1	1	Memory 15
24	1	1	1	0	1	1	Memory 16
25	1	0	0	1	1	1	Volume Up } Mute Off
26	1	1	0	1	1	1	Volume Down } Mute Off
27	0	0	1	1	1	1	Memory Addressing
28	1	0	1	1	1	1	Digital AFT On
29	0	1	1	1	1	1	Band Sequential
30	1	1	1	1	1	1	Automatic Search

PIN 12-13. AFT1-AFT2 (STOP/AFT INPUTS)

These pins are enabled during the automatic search and during normal operation, when the digital AFT is enabled (see description of pin 17).

The STOP/AFT inputs are also disabled internally during any program or band change for the duration of the Mute signal.

These pins work according to the truth table given below :

M49X Pin 12 TDA4433 Pin 2	M49X Pin 13 TDA4433 Pin 6	Function (referred to the tuning voltage)
H	L	Up
L	H	Down
L	L	Middle
H	H	No Operation

These inputs have two different functions depending on whether the system is in the search or in normal operation (AFT control).

The inputs have internal pull-up resistors of 30 KΩ typ.

A) **Search mode :** after depressing the Automatic search or preset keys, the levels of the signals coming from the TDA4433, applied to these pins, control the search function and determine when the search must stop, i.e. a TV station has been recognized.

The circuit operates in the following sequence (see fig. 12 for reference) :

1 - after pressing the search start key the search occurs in the FAST UP mode.

2 - eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.

If the system operates in VHF I and III the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station.

After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).

A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).

3 - the next UP signal will switch the search to SLOW UP speed (61 Hz).

At this point the systems is in normal AFT operation.

B) **Digital AFT operation :** when a station is perfectly tuned, the input signals coming from TDA4433 are at middle condition.

If the tuning moves lower than the threshold below 38.9 MHz, the pin 12 is put H and pin 13 is put L ; the 13 bit internal counter is moved SLOW UP speed to increase the varicap voltage.

When a detuning occurs in the opposite direction the input 12 goes Low and 13 goes High and the tuning voltage is decreased with VERY SLOW DOWN speed (7.6 Hz).

The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.

Therefore during normal operation pins 12 and 13 act as digital AFT control command.

C) **Recall from memory :** when the digital AFT is enabled and an information is recalled from Memory, a fixed value of 8 steps (~ 31.2 mV) is subtracted from the tuning voltage.

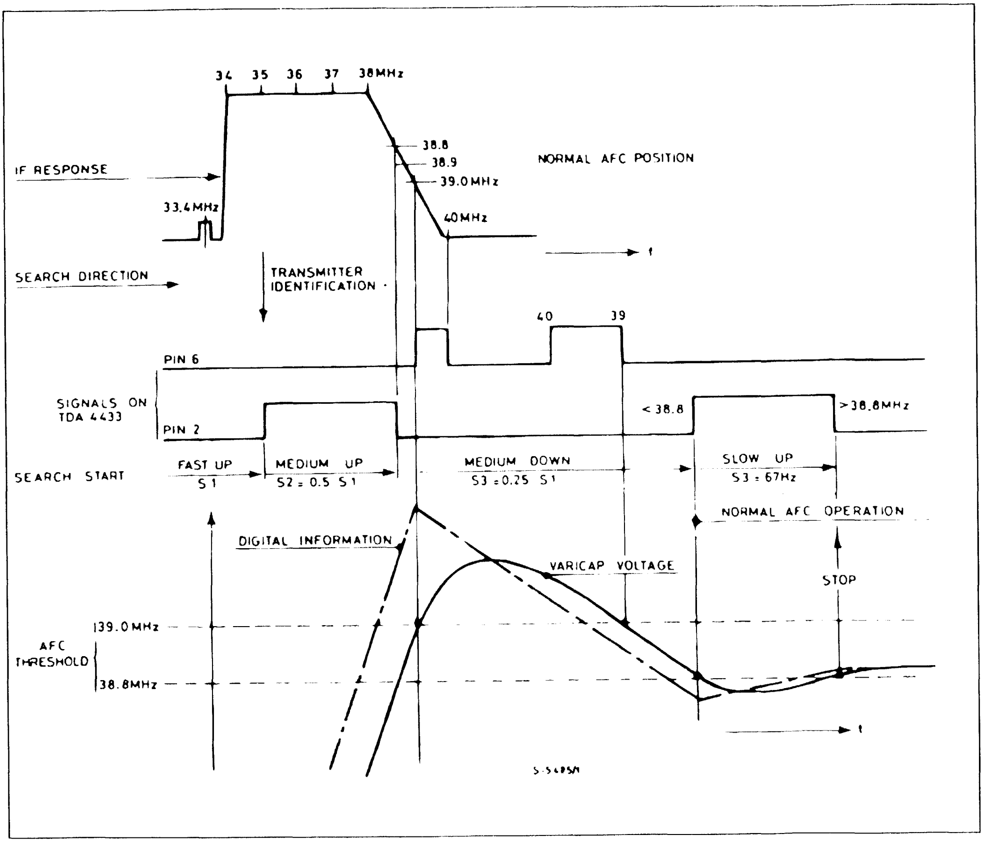
This corresponds to a detuning of 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.

At this point the AFT operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.

This feature increases the AFT capture range and relaxes the stability requirements of the tuner, voltage references and the D/A converter.

If the Digital AFT is disable (pin 17 at V_{SS}), the memory content is read without any change.

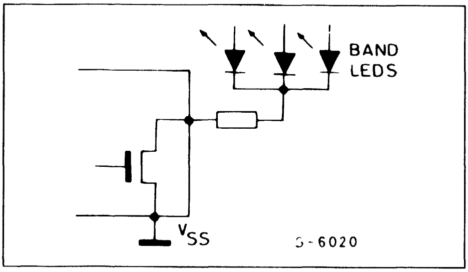
Figure 12.



PIN 14. SWEEP SEARCH DISPLAY OUTPUT

This output, which is normally Low, goes High during automatic search automatic preset et intervals of 160 ms for about 40 ms to blank the LED of band display.

Figure 13.



PIN 15. VOLUME D/A OUTPUT

This output delivers a square wave signal of 7.8 kHz and duty cycle variable in 63 steps. In case of a continuous command for varying the volume, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with f_{ref} = 500 kHz) or every 112 ms if issued locally.

Overflow and underflow protection are provided.

The volume output can be switched to V_{SS} and reset to the previous level by means of the mute on/off command. It is also reset by the volume Up/Down and the mains on/off commands.

The volume is muted at each mains on and off command for about 1 s during the power on reset time and program change (0.5 s).

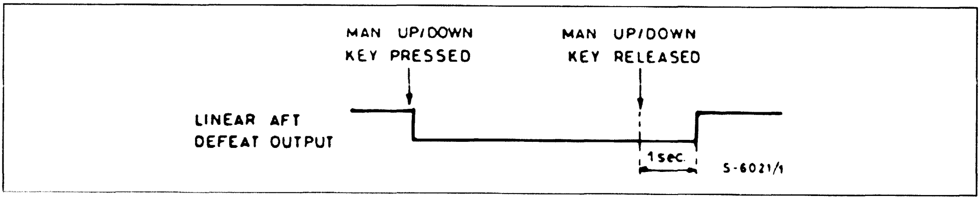
At the first power on reset of V_{DD1} the volume D/A is set at the level 21/64. The last level is preserved until V_{DD} is not removed.

PIN 16. LINEAR AFT DEFEAT OUTPUT

This output is normally High and goes Low when a Man Up/Down command is issued.

It returns High with a 1 second delay from the release of the key, in order to give the user the possibility of the tuning adjustment without the AFT intervention. It goes Low for 0.5 s during program change.

Figure 14.



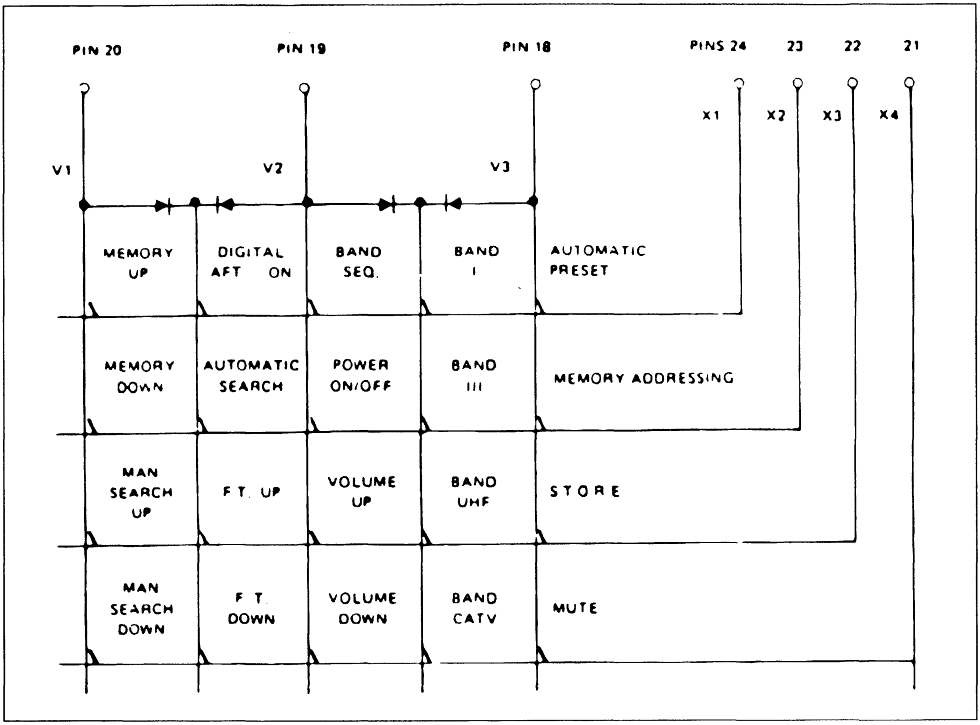
PIN 17. DIGITAL AFT ENABLE INPUT

If this input is connected to V_{SS} (GND), the digital AFT loop is always disabled. If pin 17 is left open or is connected to V_{DD}, the digital AFT is automatically enabled at power on. When a manual up/down search command is issued, the digital AFT loop is disabled and the digital AFT status output is switched off.

The digital AFT loop is restored by the commands : Digital AFT on/Automatic search/Automatic preset.

PINS 18-19-20-21-22-23-24. (keyboard matrix)

Figure 15.



A command is accepted if the corresponding contact has been closed for a minimum time of 30 ms.

Local input commands and I.R. commands have the same priority.

If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.

Viceversa an I.R. signal cannot be decoded until an issued local command has been executed.

MEMORY UP/DOWN

Depressing one of these two commands, the memory position is stepped in the UP or DOWN direction.

If the key is kept closed, the channels are stepped UP/DOWN every 0.5 second or every 5 commands from the transmitter.

In the M490B the locations from 11 to 16 can be skipped in groups of 2 connecting the relevant Y input to GND.

In the M491B the memory locations 9 to 16 are jumped if pin 31 is at GND.

BAND SELECTION

The bands can be directly selected or with a step-by-step command with the following sequence :

VHF I
CATV
VHF III
UHF
VHF I and so on

Only one band change is performed at each accepted command.

Disabled bands are automatically skipped. A band can be disabled connecting the corresponding output to V_{SS}.

SEARCH MODES

4 modes are available :

a) automatic search } (digital AFT)
b) automatic preset } (digital AFT)
c) man up/down (digital and linear AFT)
d) man up/down (linear AFT)

a) AUTOMATIC SEARCH. The search starts from the actual tuning and band position. During the search the tuning voltage is always changing from lower to higher voltage levels. When the end of the band is reached the search restarts from the beginning of the next band after a 480 ms interruption with the sequence of step by step band selection. Disable bands are automatically skipped.

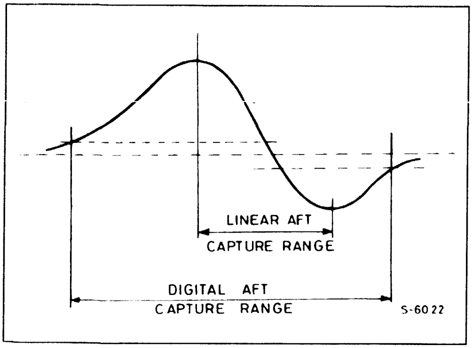
The search is stopped when the first station is found or if a channel selection command is given.

Stop of the automatic search is determined by the STOP/AFT inputs controlled by the TDA4433 which converts the AFC-S-curve into an up/down command.

At the end of the search the up/down command controls the correct tuning acting on the counter of the voltage synthesizer (Digital AFT).

It is important to call the attention to the Digital AFT capture range which is larger than the normal linear AFT as shown in fig. 16.

Figure 16.



Additionally the use of the Digital AFT allows storage of the tuning information corresponding to the zero point of the AFC-S-curve. This cannot be guaranteed using the Linear AFT method only. The latter is a cheaper system, because it does not require the use of the TDA4433 but it cannot guarantee what described above.

As a result of the use of the Digital AFT, the requirements for stability of the tuner, of the reference voltage source and of stability of the D/A converter are less critical.

Tuning speed in automatic search, if no station is found is :

VHF I	8 second
VHF III	8 second
UHF	32 second
CATV	32 second

The tuning and band information can be stored using the store/memory addressing command.

The search can be stopped by a memory selection command.

b) AUTOMATIC PRESET. The search starts from the lowest memory address, tuning voltage and VHF I band as described in automatic search mode.

When an active station is encountered, the corresponding tuning and band information is automatically stored in the Non-Volatile Memory.

Afterwards the system starts to search for the next station. The cycle is repeated until all bands have been swept or the tuning information have been stored into all address locations. After completing this cycle the system reads out the tuning information of the lowest address.

c) MAN UP/DOWN WITH DIGITAL AND LINEAR AFT (pin 17 at V_{DD}). Holding one of these commands pressed, the tuning voltage is increased or decreased.

During this operation, the Digital AFT is automatically defeated and can only be reconnected with the "AFT on" command or by an Automatic search or preset command.

The search speed is kept at minimum (there is no increment with the time)

Band	Sweep Time for the Complete Band	Number of Tuning Steps/Second
VHF I	128 seconds	64
VHF III	128 seconds	64
UHF	512 seconds	16
CATV	512 seconds	16

In case of command received from remote control, the counter is increased/decreased every two received commands.

No band switching is provided at the upper or lower tuning position.

The volume is automatically muted 3 second after the key pressure is immediately restored at the release of the key.

d) MANUAL UP/DOWN WITH LINEAR AFT (pin 17 at V_{SS}). When this control is used the Digital AFT is disabled.

The Linear AFT output goes low after an up or down command is issued and it remains Low 1 second after the release of the key.

The volume is automatically muted 3 second after the key pressure and is immediately restored at the release of the key.

Tuning speeds are as follows :

Band	Number of Tuning Steps are Second			
	Time 0	After 1 s	After 2 s	After 3 s
VHF I	64	128	256	512
VHF III	64	128	256	512
VHF	16	32	64	128
CATV	16	32	64	128

FINE TUNING UP/DOWN

See description of pin 4.

DIGITAL AFT ON

See description of pin 17.

VOLUME UP/DOWN

See description of pin 15.

MAINS ON/OFF

See description of pins 25 and 26.

STORE COMMANDS

2 modes of operations are available.

a) store

b) memory addressing

In order to protect the memory, the store function is internally disabled after one store cycle.

It is enabled after a program change or a tuning operation (it is not disabled by the Digital AFT control).

a) STORE. The tuning information (Tuning D/A, Fine tuning D/A and band) is stored in a previously selected memory address when this command is issued.

b) MEMORY ADDRESSING. The tuning information can also be stored with this command followed by the memory position selection.

When this command is accepted all the memory LEDs are blanked.

Selection of the memory position initiates the store operations and restores the display.

MUTE ON/OFF

See description of pin 15.

PIN 25. MAINS ON OPTION INPUT

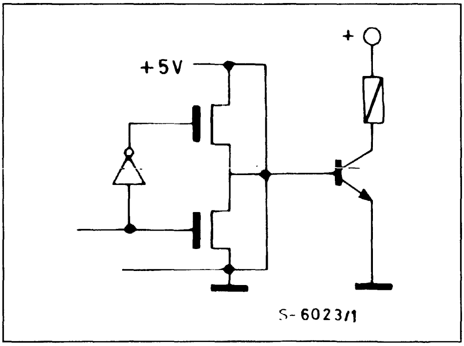
If connected to V_{SS} (GND) the Mains output is automatically switched on when V_{DD} is applied and memory 1 is read.

If it is connected to V_{DD} the circuit goes in stand by condition.

PIN 26. MAINS ON/OFF OUTPUT

Switch on of the set is controlled by the Mains on command issued for more than 0.3 s. The output transistor is set in the off condition to drive through an integrated pull-up resistor, an external NPN transistor.

Figure 17.



At each Mains on command a memory read out occurs. A V_{PP} (+ 25 V) is required for this operation, a 1 second delay starts when the mains output is switched off. For a correct reading of the memory the V_{PP} supply voltage must reach the value of 25 V within 1 second after a Mains on command.

In case of automatic switch on at power on caused by pin 25 at GND, the total delay is of 1.13 second (0.13s for V_{DD} power on reset plus 1 second for mains on).

The Mains on/off command, if repeated, will switch the output on (set off).

The last address information is preserved until V_{DD} is present.

Next Mains on command will switch the set at the previously selected memory address and a read operation will be performed.

PINS 27-28-29-30-33-34-35-36 - MEMORY ADDRESS INPUT/OUTPUT

M490B

Up to 16 Memory locations can be selected.

When V_{DD} is applied to the circuit the address is automatically preset to the first memory location.

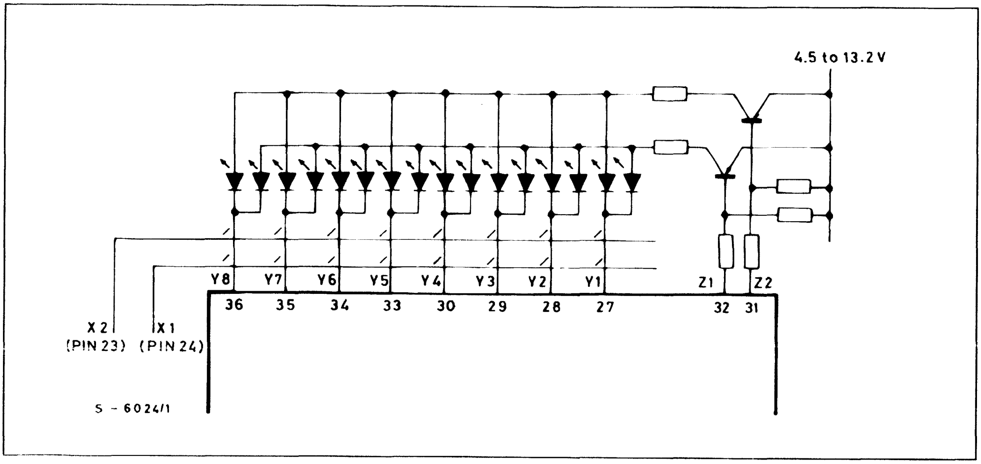
Selection of a memory location is provided connecting one address input line with an X scanning line for more than 30 ms ; this condition is internally latched and the corresponding output buffer is switched on to drive the LED.

Max drive capacity is of 20 mA with V_{OL} = 1.5 V

8 output are provided and 16 channel display is achieved multiplexing the LEDs with the control outputs "Z".

If pins 34, 35, 36 are connected to V_{SS}, the corresponding memory locations are skipped in case of up/down memory commands.

Figure 18.



M491B

These pins operate as output only for display of the selected memory location. Max drive capability is of 15 mA/1.2 V with the exception of pin 36 that is of 30 mA/1.5 V.

Direct memory selection is only possible by remote control. A local memory up/down command is available in case of emergency.

Pin 32 must be grounded.

If pin 31 is grounded, the memory position 9 to 16 are skipped in case of memory up/down commands.

For normal operation pin 31 can be left open or, better, connected to V_{DD}.

PINS 31-32

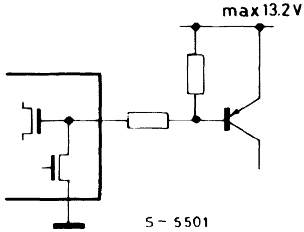
See description of pins 27 to 30 and 33 to 36.

PINS 37-38-39-40. BAND INPUT/OUTPUT

These outputs are provided to select up to 4 bands via external PNPs.

If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to V_{SS}.

Figure 19.

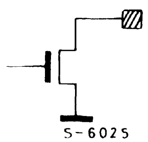


The relation between pins and bands are as follows :

pin 37 = UHF
pin 38 = CATV
pin 39 = VHF III
pin 40 = VHF I

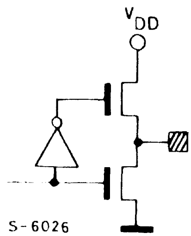
INPUT/OUTPUT CONFIGURATION

Output Open Drain.



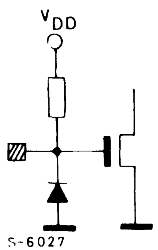
Pins 3, 4, 5, 6, 14, 15, 16, 31, 32 (M490B)
Pins 3, 4, 5, 6, 14, 15, 16, 27, 28, 29, 30, 33, 34, 35, 36 (M491B)

Output Push-pull.



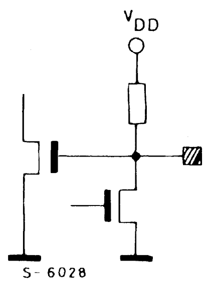
Pin 26.

Inputs with Pull-up Load.



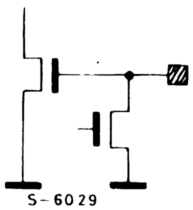
Pins 12, 13, 17, 18, 19, 20, 25 (M490B and M491B)
Pin 31 (M491 only)

Inputs/Output with Pull-up Resistor (M490B only).



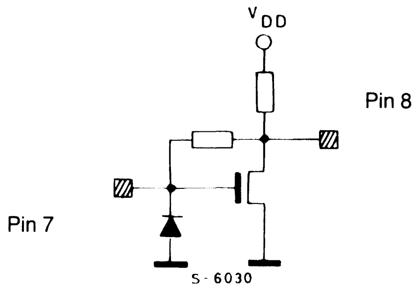
Pins 27, 28, 29, 30, 33, 34, 35, 36.

Inputs/Outputs (std).

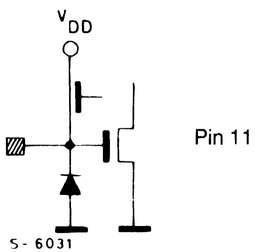


Pins 37, 38, 39, 40, 21, 22, 23, 24 (21, 22, 23, 24 are used only for testing purposes).

Oscillator.

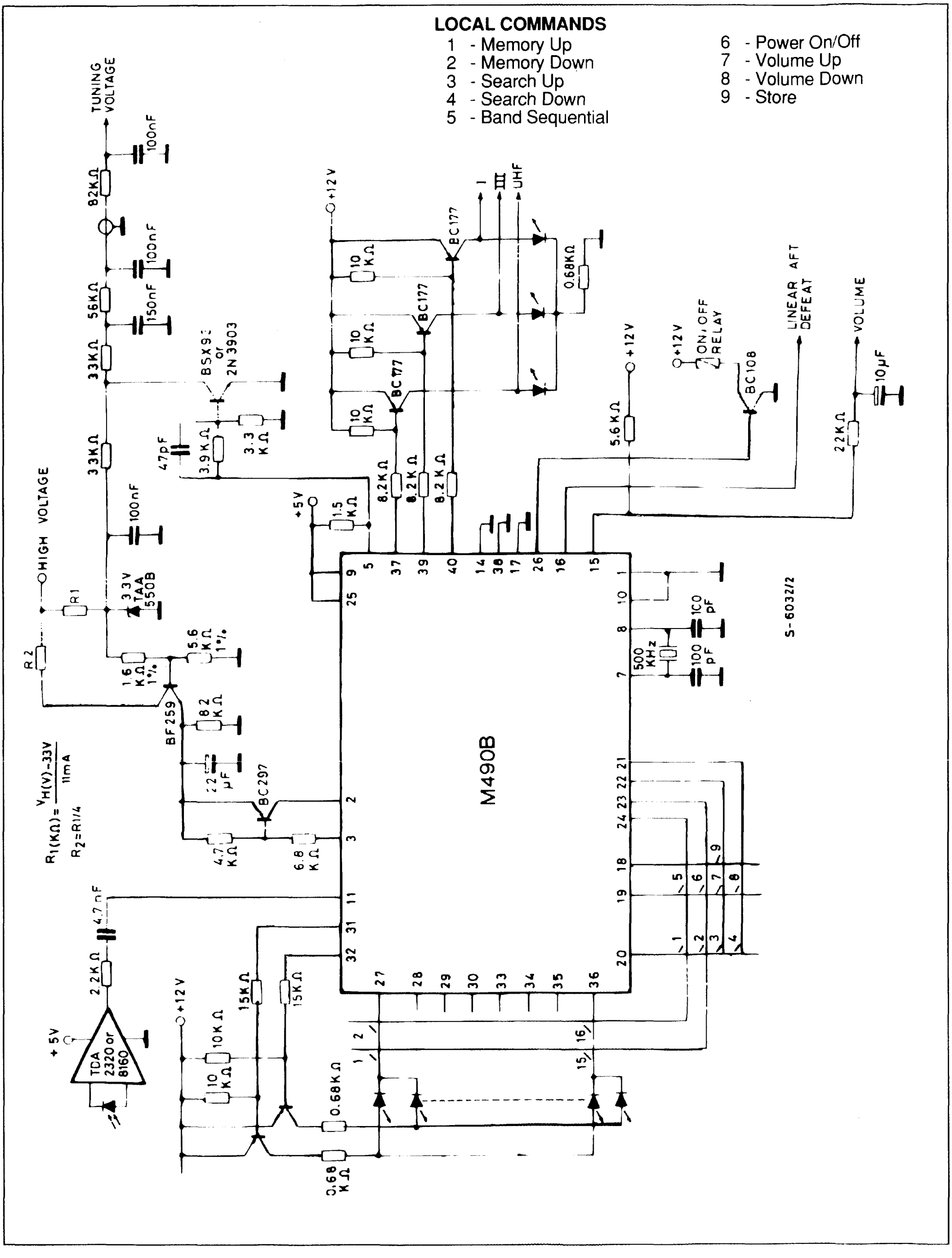


IR Input.



TYPICAL APPLICATIONS

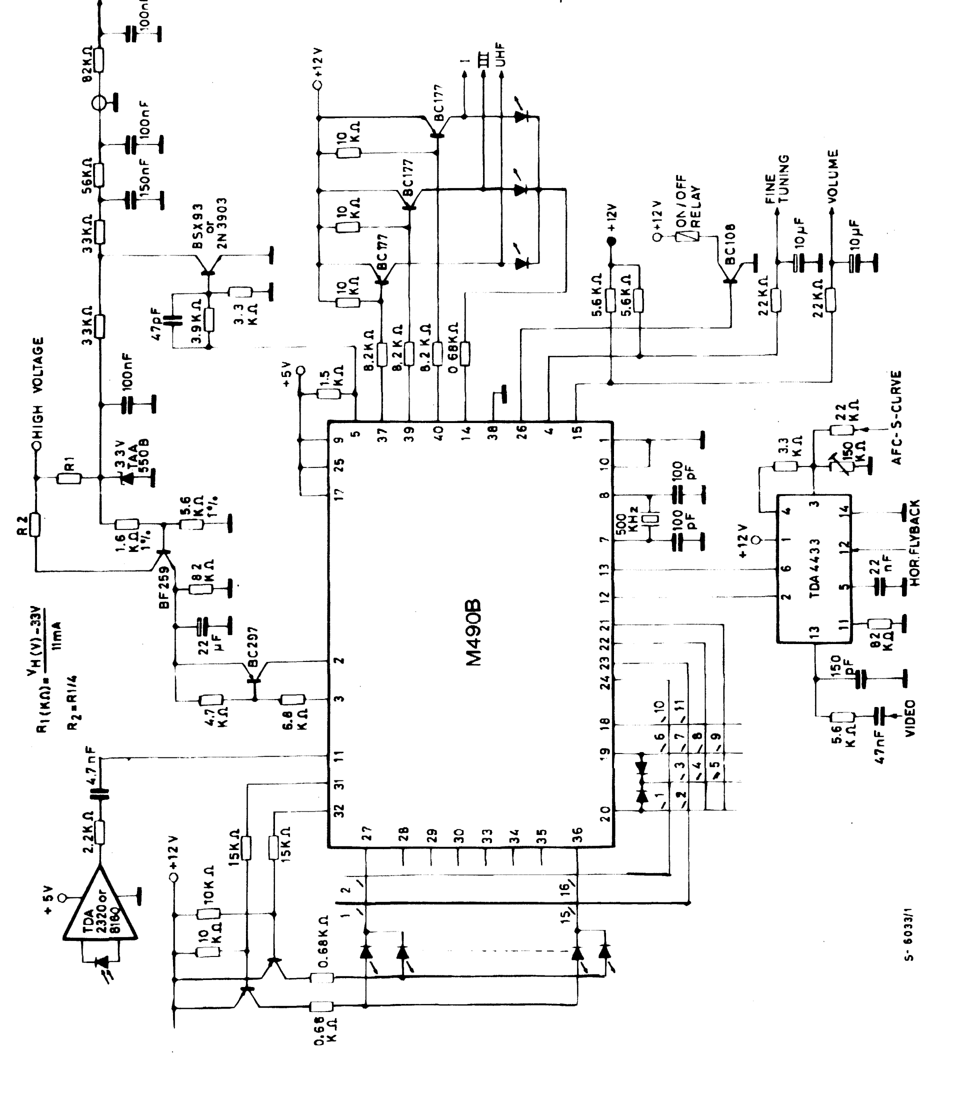
Manual Search with Linear AFT.



Automatic Search
Automatic Preset } Digital AFT
Fine Tuning with D/A

LOCAL COMMANDS

1 - Memory Up
2 - Memory Down
3 - Automatic Search
4 - Fine Tuning Up
5 - Fine Tuning Down
6 - Band Sequential
7 - Power on/off
8 - Volume Up
9 - Volume Down
10 - Automatic Preset
11 - Memory Addressing 1

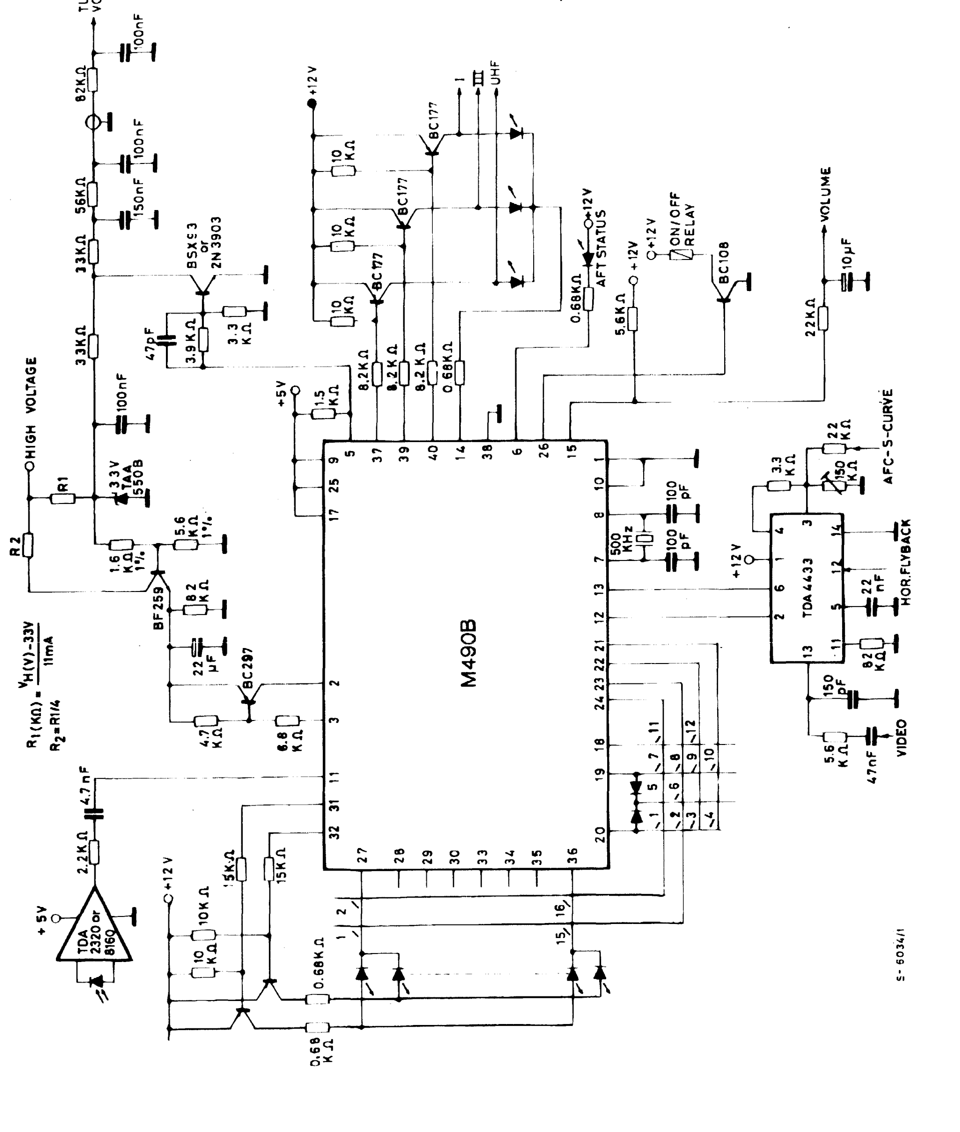


Automatic Search
Automatic Preset
Manual Up/Down

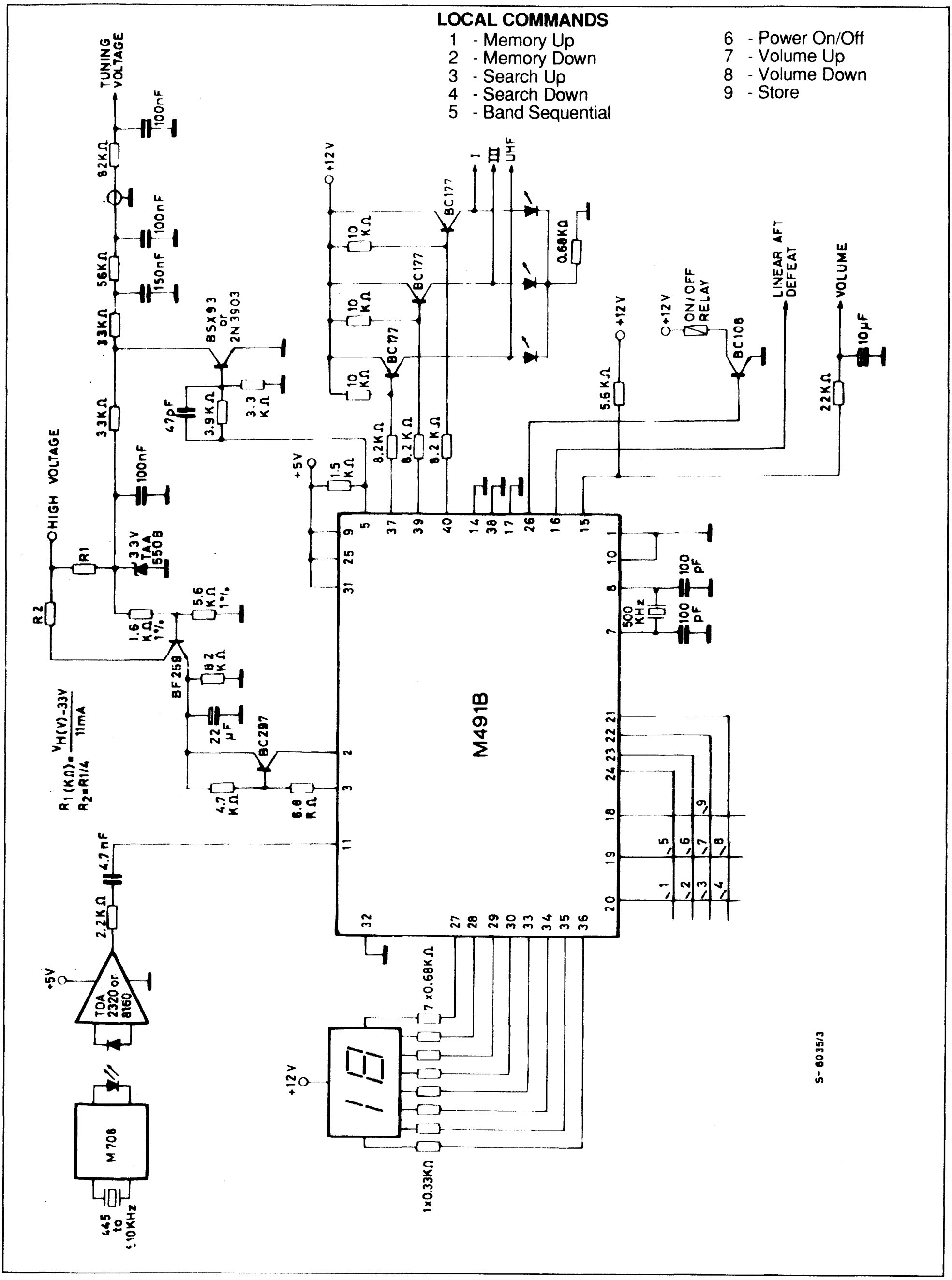
} Digital AFT

LOCAL COMMANDS

1/2 - Memory Up/Down
3/4 - Manual Search up/Down
5 - Digital AFT On
6 - Automatic Search
7 - Band Sequential
8 - Power On/Off
9/10 - Volume Up/Down
11 - Automatic Preset
12 - Store



M491. Manual Search with Linear AFT (16 memory option)

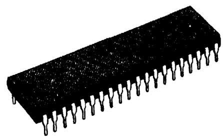


SGS-THOMSON MICROELECTRONICS

M494

SINGLE CHIP VOLTAGE TUNING SYSTEM WITH 4 ANALOG CONTROLS AND µP INTERFACE

- NV MEMORY FOR 20 PROGRAM WORDS (17 BIT x 20)
  - TUNING VOLTAGE 12 BITS
  - BAND 2 BITS
  - MULTI STANDARD 2 BITS
  - PROGRAM SKIP BIT 1 BIT
  - 10,000 MODIFY CYCLES PER WORD
  - MIN. 10 YEARS DATA RETENTION
- 13 BIT VOLTAGE SYNTHESIZER (BRM + PWM)
- NV MEMORY FOR 4 ANALOG CONTROLS (6 BIT x 4)
- 4 BAND SWITCH OUTPUTS (VHF I & III, UHF, CATV)
- 5 x 7 KEYBOARD
- 2 AUDIO VISUAL OUTPUTS (VCR & PC)
- 2 CODED MULTI STANDARD OUTPUTS (e.g. PAL, SECAM, NTSC etc.)
- DIRECT 1 1/2 DIGIT 7 SEGMENT COMMON ANODE LED DISPLAY DRIVING
- PCM REMOTE CONTROL RECEIVER (M708 transmitter)
- 5 BIT DATA INPUT + CONTROL LINE FOR P INTERFACE
- LINEAR AFC DEFEAT OUTPUT
- FLYBACK/SYNC. COINCIDENCE INPUT FOR SEMIAUTOMATIC SEARCH
- STANDBY OUTPUT
- OPTION SELECT :
- 16 OR 20 PROGRAMS
- POWER UP MODE
- PROGRAM SKIP DEFEAT
- AV OPTIONS
- 1 * OR DECADE MODE OPTION IN 20 PROGRAM OPTION
- TEMPORARY ANALOG UP/DOWN INDICATOR ON LED DISPLAY
- BAND SKIP OPTION
- 455 TO 510KHz CHEAP CERAMIC RESONATOR
- V_{DD} = 5V ± 5%. V_{PP} = 25V ± 1V



B
Plastic Package
Order Codes : M494 B1

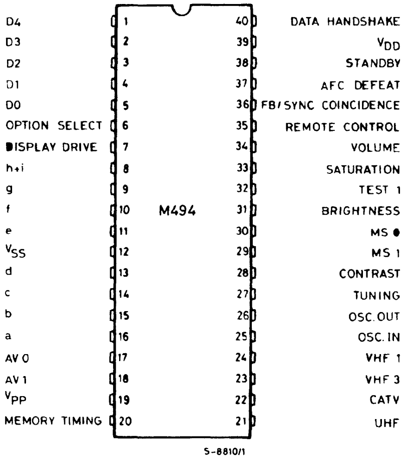
DESCRIPTION

The M494 is a monolithic LSI integrated circuit fabricated in SGS EPM 2 process ; an N-channel, Planox, double poly MOS process capable of including a floating gate NV memory cell (EEPROM).

The i.c. has been designed as a complete digital TV tuning system based on the voltage synthesis principle and as a replacement for all the conventional potentiometers and band switches particularly in low cost TV sets. It also provides some functions normally only associated with higher cost sets. NV memory is integrated on the chip together with all the necessary control circuitry to provide the program memory. Separate NV memory is also integrated to provide the memory for four analog controls. A seven segment LED display can be directly driven by the chip to display the program selected, and the direction of movement of the analog controls. Provision is made for a remote control receiver both on and off chip, the latter is interfaced via a data input and single control line. (This enables control by a microprocessor). A local keyboard can be used with the device in a variety of configurations. An option select pin provides for different program number options, power up options and skip associated functions. This device is another significant step towards the complete integration of TV control circuitry.

The device is packaged in a 40 pin DIL plastic package.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7	V
V_{PP}	Memory Supply Voltage	– 0.3 to 28	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Input Voltage	15	V
I_{OL}	Output Low Current LED Driver Outputs : pin a-g pin h + i All other Outputs	 20 35 5	 mA mA mA
t_{PD}	Max. Delay between Memory Timing & Memory Supply Pulses	5	µs
P_{tot}	Total Package Power Dissipation	1	W
T_{stg}	Storage Temperature	– 25 to + 125	°C
T_{op}	Operating Temperature	0 to + 70	°C
C_{os}	Capacitance on Option Select Pin	100	pF
R_{os}	Resistance on Option Select Pin	1	KΩ
C_{dk}	Capacitance on data outputs & keyboard inputs when lines are connected by a keyboard switch closure	150	pF
R_k	Series Resistance of Single Keyboard Switch	10	KΩ
C_{rts}	Capacitance on Data Handshake Pin	50	pF

Stresses above those under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DEFINITION OF TERMS

The M494 has four conditions or states that it can be in which are defined below. Logic LO 0V and logic HI ≡ 5V.

POWERED DOWN

V_{DD} = 0V. V_{PP} = 0V

ON

V_{DD} = 5V. V_{PP} = 25V. Device driving display normally. Data Handshake pin configured as RTS i/p. Standby o/p = HI. All other functions operating normally.

STANBDBY

V_{DD} = 5V. V_{PP} = 0V. Device driving display to show a single static bar (g segment). Data Handshake pin configured as RTS i/p. Standby o/p = LO. All keyboard commands are disabled except any program command On/Off. On/Standby. Memory sequence up or down, 1 * and ±10 (decade) commands. All RC and Data commands are disabled except any program command, On/Standby, Memory sequence up or down, 1 * and ±10 (decade) commands. Analog controls. Tuning, AV, MS and AFC defeat o/p's = LO. Band o/p's = HI (externally pulled up). See Standby section for more detail.

OFF

V_{DD} = 5V. V_{PP} = 0V. Device not driving display. Data Handshake pin configured as OFF o/p. Standby o/p = LO. Display disabled and Display drive o/p = HI (externally pulled up). All keyboard commands disabled except ON/OFF. Remote and data command sources disabled. Analog controls, Tuning, AV, MS and AFC defeat o/p's = HI (externally pulled up).

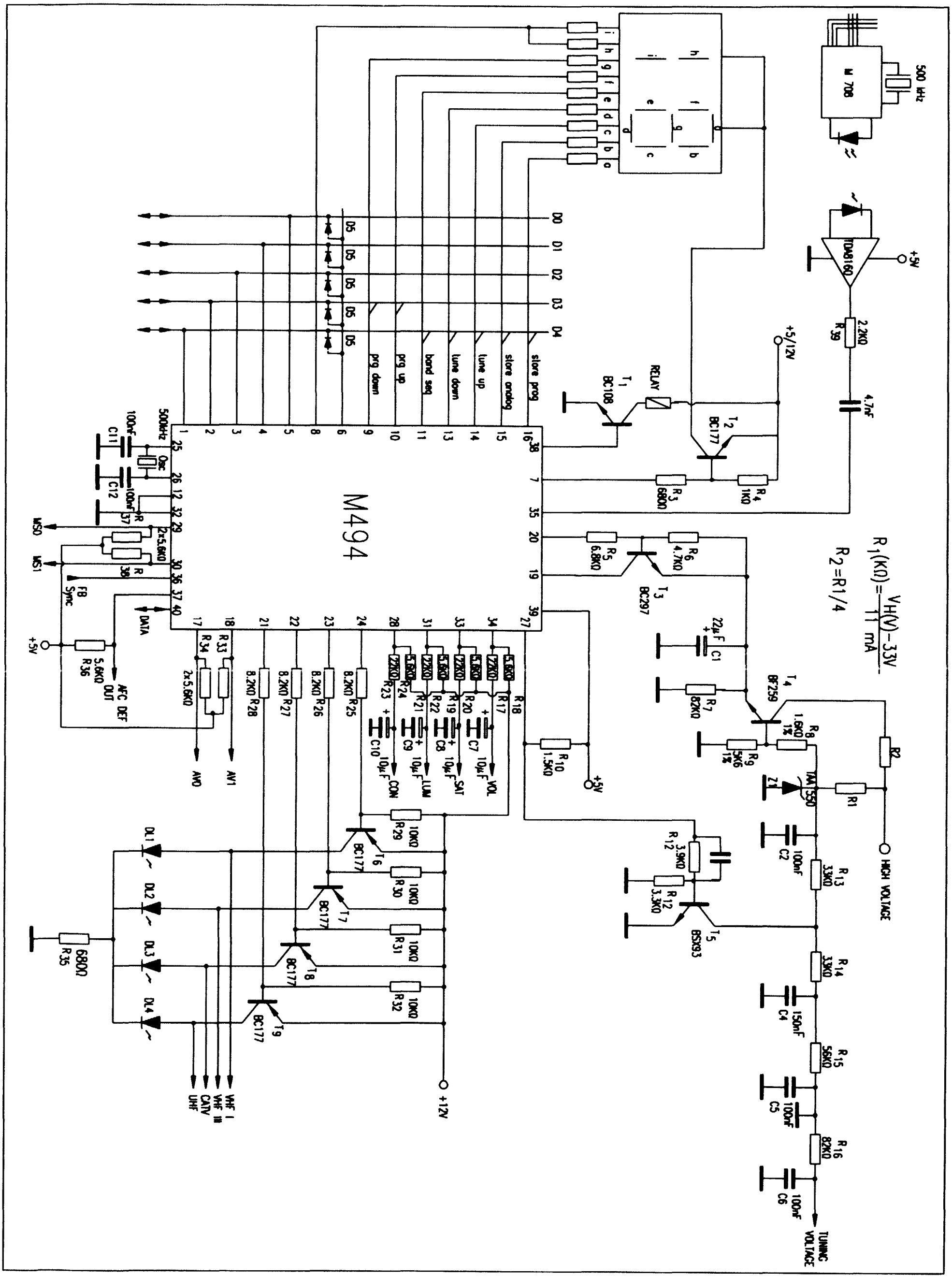
STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{DD} = 5V unless otherwise specified)

Pins	Symbol	Parameter	Test Conditions		Value			Unit
					Min.	Typ.	Max.	
Memory Supply	I_{PP}	Memory Supply Current	V_{PP} = 26V					
			Write	Pk.			35	mA
				Av.			10	mA
			Erase	Pk.			9	mA
				Av.			5	mA
			Read	Pk.			8	mA
				Av.			2.5	mA
	R	Pull Down					25	KΩ
Memory Timing	V_{OL}		V_{DD} = 4.75V	I_{OL} = 2.5mA			8	V
	$I_{O(off)}$	Leakage	V_{DD} = 4.75V	V_O = 26V			100	µA
Tuning	V_{OL}		V_{DD} = 4.75V	I_{OL} = 5mA			1	V
V_{DD}	I_{DD}	Supply Current	V_{DD} = 5.25V				100	mA
RC	V_I	pk to pk			0.5		13.2	V
FB/sync. Coin. Input	V_{IL}						0.8	V
	V_{IH}				2.0			V
	I_{IL}		V_{DD} = 5.25V	V_{IL} = 0.8V			– 0.4	mA
	R	Pull up				30		KΩ
Vol. Brigh. Sat. Contr. DACs	V_{OL}		V_{DD} = 4.75V	I_{OL} = 4mA			1	V
	$I_{O(off)}$		V_{DD} = 5.25V	V_O = 13.2V			50	µA
h + i	V_{IL}						1.5	V
	V_{IH}				3.5			V
	I_{IL}		V_{DD} = 5.25V	V_{IL} = 1.5V			– 50	µA
	R	Pull up				200		KΩ
	V_{OH}		V_{DD} = 4.75V	I_{OL} = 30mA			1.5	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Pins	Symbol	Parameter	Test Conditions	Value			Unit
				Min.	Typ.	Max.	
D0, D1 D2, D3 D4	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V V_{IL} = 1.5V			– 0.4	mA
	V_{OL}		V_{DD} = 4.75V I_{OL} = 1mA			0.4	V
	$I_{O(off)}$		$V_{O(off)}$ = 5.5V			25	µA
	R	Pull up			30		KΩ
MS0, MS1 AFC def. AV0, AV1	V_{OL}		V_{DD} = 4.75V I_{OL} = 1mA			0.4	V
	$I_{O(off)}$		V_{DD} = 5.25V V_O 13.2V			50	µA
Option Select	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V V_{IL} = 1.5V			– 0.4	mA
	R	Pull up			30		KΩ
Standby	V_{OL}		V_{DD} = 4.75V I_{OL} = 100µA			0.4	V
	I_O		V_{DD} = 4.75V V_O = 0.7V			1.6	mA
a, b, c, d, e, f, g	V_{IL}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V V_{IL} = 1.5V			– 50	µA
	R	Pull up			200		KΩ
	V_{OL}		V_{DD} = 4.75V I_{OL} = 15mA			1.5	V
Display Drive	V_{OL}		V_{DD} = 4.75V I_{OL} = 5mA			0.4	V
	$I_{O(off)}$		V_{DD} = 5.25V V_O = 13.2V			50	µA
UHF, III I, CATV	V_{OL}		V_{DD} = 4.75V I_{OL} = 1mA			3	V
	V_{OH}		V_{DD} = 4.75V I_{OH} = – 150µA	2.4			V
	V_{IL}					1.5	V
	V_{IH}			3.5			V
	$I_{O(off)}$		V_{DD} = 5.25V V_O = 13.2V			50	µA
Data Handshake	V_{OL}		V_{DD} = 4.75V I_{OL} = 1mA			3	V
	V_{OH}		V_{DD} = 4.75V I_{OH} = 150µA	2.4			V
	V_{IH}					1.5	V
	V_{IH}			3.5			V
	I_{IL}		V_{DD} = 5.25V V_{IL} = 1.5V			– 0.4	mA
	R	Pull up			30		KΩ
	$I_{O(off)}$		V_{DD} = 5.25V V_O = 13.2V			50	µA

SYSTEM CONFIGURATION



FUNCTIONAL DESCRIPTION

(clock frequency = 500kHz)

V_{DD} & V_{SS}

V_{DD} = + 5V ± 5%. When applied, an internal power on reset of 110ms is generated. The voltage threshold for the reset is in the range 3 to 3.5V but is in fact the point at which the internal clock phases start.

V_{SS} = 0V. This pin is connected to the substrate of the i.c. and is the reference for all parameters of the device.

OSCILLATOR I/O

The frequency of the oscillator should be between 445 and 510kHz using a cheap ceramic resonator. The reference frequency of the remote control transmitter must also be in the same range i.e. if the oscillator frequency is 455kHz then the transmitter frequency could be 510kHz or vice versa.

TEST

This pin is normally used for post fabrication testing purposes only and should be tied to V_{SS}. However this pin can be used by SGS-THOMSON Microelectronics or the OEM to enable external loading of the memory. Details of how to achieve this can be furnished by SGS-THOMSON.

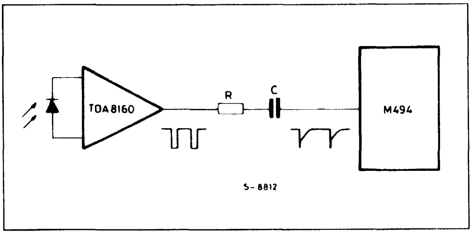
REMOTE CONTROL INPUT

The integrated RC receiver decodes signals transmitted by the M708 (address 10). The minimum signal amplitude should be 0.5V peak to peak at the input pin. The minimum pulse width should be 8s.

The signal from the preamplifier (TDA8160) is brought to the RC signal input via an AC coupling network (see fig. 1).

V_{DD} TDA8160	R	C
5V	2.2KΩ	4.7nF
12V	10KΩ	4.7nF

Figure 1.



The input is self biased to approx. 1.5V. When a large signal is applied to the input a level shift will take place predominantly due to the coupling network. However another time constant is also visible due to the coupling C and the internal resistor R_i. (see figs. 2 & 3).

Figure 2 .

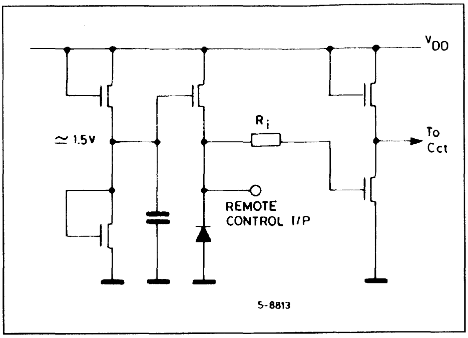
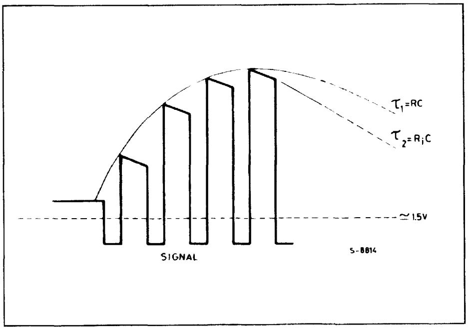


Figure 3 .



Several tests are performed on the signal :

a) Measurement of the pulse distance T (time base synchronization).

b) Check of the bit positions relative to the time base windows.

c) Check of the parity bit.

d) Check of the absence of pulses between parity and stop pulses.

e) Check of the noise level. The receiver checks the noise level for a time T after each pulse detected.

If all these tests are successful the received word is stored and decoded. If not it is rejected. The transmission is terminated on reception of the end of transmission (EOT) code or if the internal timer measures a transmission interruption of more than 550ms. For more detail concerning the operation of the RC receiver refer to SGS-THOMSON Technical Note No. 155 pp11-12.

The RC receiver and the local keyboard have the same command source priority i.e. a local command is not accepted until a previously accepted RC command has been completely executed and the EOT code transmitted. Similarly if a local command is under execution then an RC command will not be accepted. The RC truth table and commands are shown on the next page.

ANALOG CONTROL OUTPUTS

Four analog control outputs are implemented to provide for Volume, Brightness, Saturation and Contrast from four 6 bit D/A's. These D/A's use the Pulse Width Modulation technique to synthesize a pulse train of constant frequency but variable pulse width (PWM). Each output delivers a 7.8kHz square wave whose duty cycle is variable in 63 steps. External RC filtering and level shifting is required to realise a static DC voltage from the pulse train. If the analog outputs are continuously varied by command from the keyboard or data command sources the outputs will change approx. every 112ms (fck = 500kHz) or approx. every 102ms if the command is issued from the RC command source. One analog control is specifically designed as a volume control as mute circuitry is built in.

On start up reset the analog control outputs except volume are enabled after a period of approx. 1.1 seconds. In the Standby and Off states all the analog control outputs are pulled to logic LO.

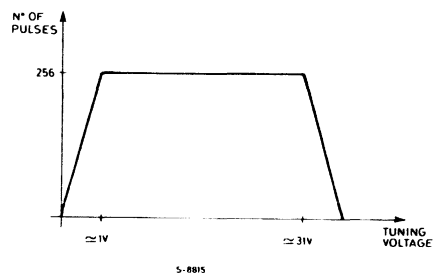
The normalise command reads the contents of each analog memory sequentially to its corresponding counter and D/A output.

TUNING OUTPUT

The tuning voltage is generated from a 13 bit counter. The program memory stores the 12 MSB's of the tuning word. The range of the AFC circuitry is at least 3 bits so the LSB of the tuning counter does not affect the resolution of tuning.

The contents of the counter are converted using a PWM and a Bit Rate Multiplier (BRM) technique. 13 bits gives 8192 steps which yields a resolution of approximately 3.9mV with a max. tuning voltage of 32V. This corresponds to a resolution of about 75kHz in the UHF band. The 5 MSB's of the tuning word are converted using PWM and the remaining 8 bits using BRM. Thus as the tuning word increases from all zeroes the number of pulses in one period increases to 256 with all the pulses being the same length (t_o = 2µs). For values larger then 256 PWM conversion takes place where the number of pulses in one period stays constant at 256 but the width changes. When the pulse width reaches $15t_o$ two successive pulses "link" together and the number of pulses decreases. (see fig. 4).

Figure 4 .



The pulse train is fed to an external low pass filter to realise a DC voltage. The temperature dependence of this system is predominantly the switching times of the output pulses and as there are only a maximum of 256 pulses in one period the temperature stability is very good.

In Standby and Off states the tuning output is pulled to logic LO.

M494 REMOTE CONTROL COMMANDS (address 10, code = 1001)

M708 Command Number	Function		Code					
	16 Programs	20 Programs	C1	C2	C3	C4	C5	C6
0	EOT	EOT	0	0	0	0	0	0
1	Standby	Standby	1	0	0	0	0	0
2	Mute (toggle)	Mute (toggle)	1	1	0	0	0	0
3	Program 1	Program 1	0	0	1	0	0	0
4	Program 2	Program 2	1	0	1	0	0	0
5	Program 3	Program 3	0	1	1	0	0	0
6	Program 4	Program 4	1	1	1	0	0	0
7	Contrast up	Contrast up	1	0	0	0	1	0
8	Contrast down	Contrast down	1	1	0	0	1	0
9	Program 5	Program 5	0	0	1	0	1	0
10	Program 6	Program 6	1	0	1	0	1	0
11	Program 7	Program 7	0	1	1	0	1	0
12	Program 8	Program 8	1	1	1	0	1	0
13	Memory Seq. up	Memory Seq. up	1	0	0	0	0	1
14	Memory Seq. down	Memory Seq. down	1	1	0	0	0	1
15	Program 9	Program 9	0	0	1	0	0	1
16	Program 10	Program 0	1	0	1	0	0	1
17	Program 11	– 10 (decade)	0	1	1	0	0	1
18	Program 12	+ 10 (decade)	1	1	1	0	0	1
19	Normalise	Normalise	1	0	0	0	1	1
20	On/stby (tog.)	On/stby (tog.)	1	1	0	0	1	1
21	Program 13	1*	0	0	1	0	1	1
22	Program 14	NOP	1	0	1	0	1	1
23	Program 15	NOP	0	1	1	0	1	1
24	Program 16	NOP	1	1	1	0	1	1
25	Volume up	Volume up	1	0	0	1	1	1
26	Volume down	Volume down	1	1	0	1	1	1
27	Brightness up	Brightness up	0	0	1	1	1	1
29	Brightness down	Brightness down	0	1	1	1	1	1
28	Saturation up	Saturation up	1	0	1	1	1	1
30	Saturation down	Saturation down	1	1	1	1	1	1

The above table showns the difference between the 16 and 20 program options with respect to the remote control commands. Commands 16, 17, 18 &21 change function between the two options. Commands 22, 23 & 24 should not be used in the 20 program option, as they have no function.
NOP = No operation

PROGRAM MEMORY

NV memory (EEPROM) is integrated on the chip to provide storage for up to 20 stations. Each memory location is 17 bits in length providing 12 bits for tuning voltage, 2 bits for band, 2 bits for two coded multi-standard outputs and 1 bit program skip flag. Individual program words can be read on command from the keyboard, remote or data command sources but can only be written on command from the keyboard. There are two methods for storing a program (writing the memory) : pre and post tuning selection of the program number. See Commands, section 7. Reading each memory location in sequence (up or down) can also be achieved from all the command sources.

All memory timing functions are provided on chip and only one external transistor is required to switch the external memory supply (25V). There are essentially two operations carried out on the memory : Write/Modify and Read. The Write/Modify cycle consists of 3 steps :

a) All "1s" are written to the bits of the addressed word.

b) All bits of the word are erased.

c) The new contents are written.

Using this method all the bits of the addressed word are aged the same. For more detail concerning the write, erase and read current waveforms at the Memory Supply pin see M490/1 datasheet.

MEMORY FOR ANALOG CONTROLS

The memory for the analog controls is electrically identical to the main program memory but is organised as four 6 bit words located in two sequentially addressed words at the memory. Each word
corresponds to the Volume, Brightness, Saturation and Contrast outputs. At power on reset and normalise command each memory word is read out to its corresponding counter and D/A in sequence.

DISPLAY, KEYBOARD AND DATA MULTIPLEXING

Logic is integrated on the chip to provide the multiplexing between the display, keyboard and data inputs. In the On state and with the Data Handshake pin at logic HI as an input the display and keyboard are muxed together. See fig. 5. Each column output goes to logic LO in sequence and the row inputs are scanned for a key closure. In chronological order across the total mux. period there is : initialisation, scan, decision and display periods.

The Data Handshake pin has a complex logical function. Is has two modes of operation : as a hand shake I/O line to a µP and as an output line to the P to signal that the M494 is in the Off state. In order to achieve this function careful signal timing is required both internally and externally to the chip. See fig. 6. When the device is in the OFF state the Data Handshake pin is used to signal this condition to the µP by being pulled LO.

Figure 5 .

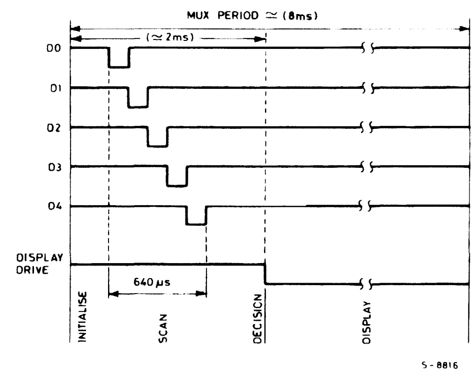
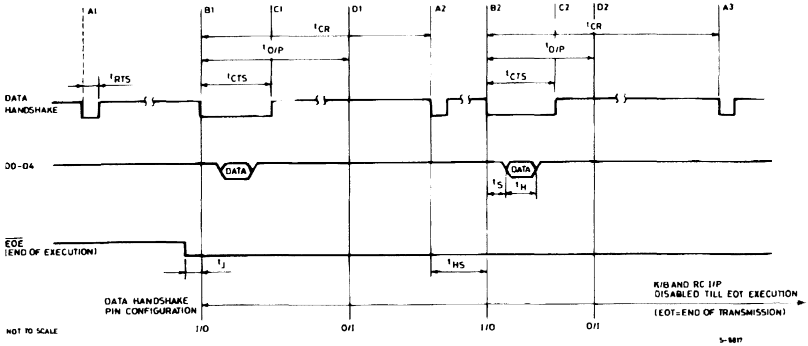


Figure 6 : Data-input-timing.



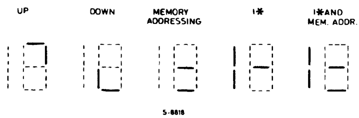
N°	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	t_{RTS}	Request to Send Pulse (RTS)	5		10	µs
2	t_{CTS}	Clear to Send (CTS)		512		µs
3	$t_{O/P}$	Pin Output Configuration		8		ms
4	t_{HS}	Handshake Time	12			µs
5	t_S	Data Set up Time	10		128	µs
6	t_H	Data Hold Time	128		256	µs
7	t_J	Synchronization Jitter			8	ms
8	t_{CR}	CTS to next RTS Pulse		98		ms

Note : Oscillator Clock = 500kHz.

DISPLAY

The M494 is capable of directly driving a 1 digit common anode LED display at the max. sink current of 15mA per segment. The h+i pin is capable of sinking a max. current of 30mA so that these two segments can be driven from the same pin and be the same brightness as the other segments.

On instruction from the internal command decoder the display shows programme number, direction of analog control movement, decade change or Memory Addressing function active. Analog controls in this context are defined as Tuning, Volume, Contrast, Saturation & Brightness. The formats of the display for analog control direction, decade change and Memory Addressing are shown below respectively :



For the analog controls the above condition is displayed with an "overrun" time of 300ms. i.e. the display will show the "arrows" for a period of 300ms after the release of any analog control up or down key. The Memory Addressing function display flashes at 5Hz after the Memory Addressing function is commanded and continues to flash until a programme is selected or any other command is given. In 1 * the g segment only flashes at 5Hz and continues to flash until a programme number is selected or any other command is given. If in Memory Addressing and 1 * is pressed then the display above is shown with segments g & d only flashing at 5Hz until a programme number is selected or any other commands is given. When Store or Set Skip Flag commands are executed the whole display is flashed at 5Hz for 1 second.

KEYBOARD

It is possible to implement a keyboard with a max. size of 35 keys as a 5 x 7 array. Fig. 8 shows the arrangement of the key matrix. Each key connects a row (a-g) with a column (D0-D4) with a max. resistance of 10KΩ. De-bounce logic is integrated on the chip that only allows acceptance of a command if the key is closed for longer than 40ms except for the On/Standby and On/Off commands where the relevant keys must be closed for approximately 100ms. This is equivalent to 2 received RC commands).

For the main keyboard matrix (a-g x D0-D4), if the logic detects two keys closed simultaneously the display is blanked to indicate this condition to the user and no command is executed. When the logic detects only one key pressed the display will re-illuminate and the command be executed.

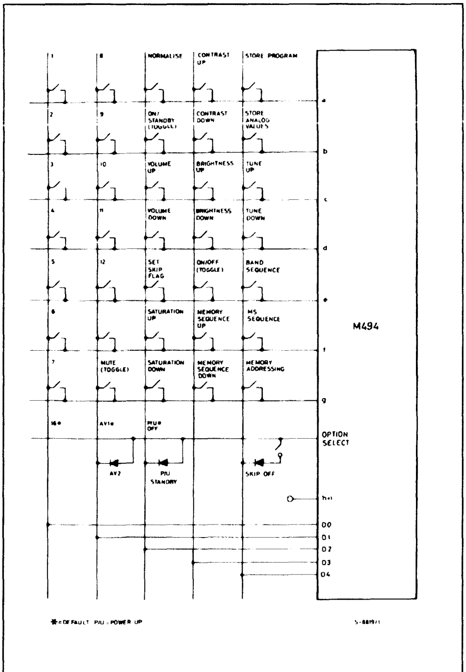
This avoids confusion as to which command should be executed and provides feed back to the user. For the Option select line all options/commands can be active simultaneously.

1 * mode or decade mode can be selected on the option select line by the presence of a diode or not respectively. These two modes are only active for the 20 program option and are described below :

In 1 * mode the display will toggle in & out of the condition shown in the Display Section. Access to programs in the first decade is made by simply pressing any 0-9 program key and access to programs in the second decade, whatever the current program is made by pressing 1 * followed by any 0-9 program key.

In decade mode on pressing either ±10 (decade) keys the display will light or extinguish the half digit respectively and simultaneously effect the tuning information. e.g. if the device is in program 3 pressing + 10 (decade) key will give program 13 and then pressing - 10 (decade) key will give program 3. Pressing - 10 (decade) again will have no effect.

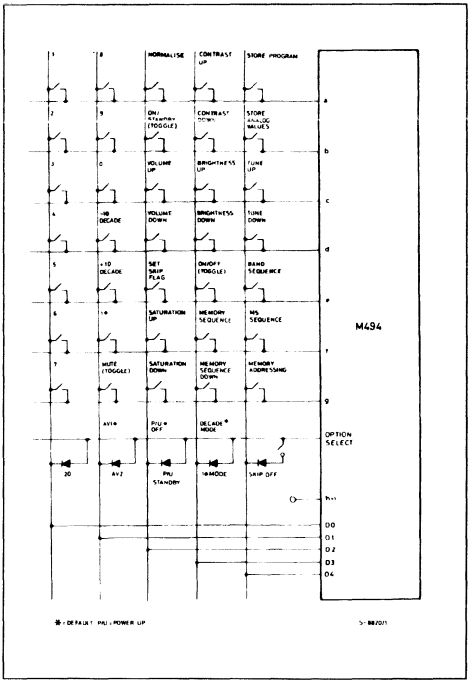
Figure 7 : Keyboard 16 Programs.



The 20 program option select acts like an enable for the 1 * or decade modes. i.e. the 1 * or decade modes are only selectable in the 20 program option. In 16 program option the function of the 1* key, program key 0, -10 (decade) & + 10 (decade) are changed to no function, programme 10, 11 & 12 respectively. i.e. The difference between fig. 7 & 8 for those keys that change function.

If the 1 * key is pressed followed by brightness up for example the device will increase the brightness only and reset the 1 * command **i.e. the last command from any command source will always be executed if it is a single keystroke command and the 1 * command will be reset by it.** It is possible to press the 1 * key on the keyboard and then a program 0-9 command from RC or Data command sources or vice versa. Thus there are 2 methods of selecting a program from the keyboard for the 16 program option : direct access (only up to 12 programs) or Memory sequence up/down. And there are 3 methods of selecting a program from the keyboard for the 20 program option : 1 * mode, decade mode and Memory sequence up/down.

Figure 8 : Keyboard 20 Programs.



DATA INPUT
Shown below are the codes for the commands :

M494 DATA COMMANDS

Command Number	Function		Code				
	16 Programs	20 Porgrams	D0	D1	D2	D3	D4
0	EOT	EOT	0	0	0	0	0
1	Program 1	Program 1	1	0	0	0	0
2	Program 2	Program 2	1	0	0	0	0
3	Program 3	Program 3	1	1	0	0	0
4	Program 4	Program 4	0	0	1	0	0
5	Program 5	Program 5	1	0	1	0	0
6	Program 6	Program 6	0	1	1	0	0
7	Program 7	Program 7	1	1	1	0	0
8	Program 8	Program 8	0	0	0	1	0
9	Program 9	Program 9	1	0	0	1	0
10	Program 10	Program 0	0	1	0	1	0
11	Program 11	– 10 (decade)	1	1	0	1	0
12	Program 12	+ 10 (decade)	0	0	1	1	0
13	Program 13	1*	1	0	1	1	0
14	Program 14	NOP	0	1	1	1	0
15	Program 15	NOP	1	1	1	1	0
16	Program 16	NOP	0	0	0	0	1
17	Normalise	Normalise	1	0	0	0	1
18	Volume up	Volume up	0	1	0	0	1
19	Volume down	Volume down	1	1	0	0	1
20	Contrast up	Contrast up	0	0	1	0	1
21	Contrast down	Contrast down	1	0	1	0	1
22	Brightness up	Brightness up	0	1	1	0	1
23	Brightness down	Brightness down	1	1	1	0	1
24	Saturation up	Saturation up	0	0	0	1	1
25	Saturation down	Saturation down	1	0	0	1	0
26	Memory Seq. up.	Memory Seq. up.	0	1	0	1	1
27	Memory Seq. down	Memory Seq. down	1	1	0	1	1
28	On/standby (toggle)	On/standby (toggle)	0	0	1	1	1
29	Standby	Standby	1	0	1	1	1
30	Mute (toggle)	Mute (toggle)	0	1	1	1	1
	NO TRANSMISSION (pulled up)		1	1	1	1	1

The above table shown the difference between the 16 and 20 program options with respect to the Data input commands. Commands 10, 11, 12 & 13 change function between the two options. Commands 14, 15 & 16 should not be used in the 20 program option, as they have no function.
NOP = No Operation

The Data input will accept signals whose timing is defined in fig. 6 and electrical characteristics defined in the table of static electrical characteristics. The EOT code must be transmitted after each command after a min. period of 112ms.

BAND OUTPUTS

Four band outputs are provided for selection of the signal band : VHF I & III, UHF and CATV. Band skip logic is implemented so that by tieing the relevant pin to V_{SS} a band can be skipped in regions of no transmission in that band. The bands can be selected only in a rolling sequence by the band sequence keyboard command. The sequence is as follows :

VHF III, UHF, VHF I, CATV

MULTI STANDARD OUTPUTS

Two coded multi standard outputs (or general purpose TV system flags) are provided so that the TV set can be designed for use in areas of more than one transmission standard. This function requires an external decoder to realise 4 different standards e.g. PAL 1, PAL 2, NTSC, SECAM etc. The multi standard sequence command available from the keyboard gives a simple binary count at the two outputs : 00, 01, 10, 11, 00 etc. In Standby and Off states the multistandard outputs are pulled to logic LO.

AUDIO VISUAL OUTPUTS

Two audio visual outputs are provided for automatic selection of a VCR and/or personal computer. The logic state of the pins depends on the AV option selected, the program option and the program number selected according to the truth tables below

AV Option 1		
16/20 Programs		
Program	AV0	AV1
16/0	1	0
15/19	0	1
Others	0	0

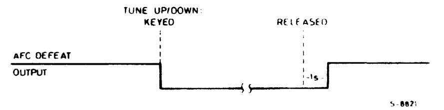
AV Option 2		
16/20 Programs		
Program	AV0	AV1
8/8	1	0
7/7	0	1
6/6	1	1
Others	0	0

External pull up resistors must be used to realise a logic HI as the outputs are open drain transistors. See I/O Configuration.

AFC DEFEAT OUTPUT

The AFC defeat output is a TTL compatible signal that is capable of switching the AFC circuitry in and out. The AFC defeat output is pulled LO on any program change including memory sequence up and down and is held LO for 500ms after execution of the command. When tune up or down are commanded the AFC defeat output is taken to logic LO. After the tuning operation the AFC defeat is held LO for 1 second after the key is released. See fig. 8. On power on & start up resets it is taken to logic LO for approx. 1.1 seconds.

Figure 9 .



STANDBY

The standby output is a push pull output capable of directly driving an NPN transistor for switching a relay. The states of this pin are defined in the definition of terms. When standby is commanded, available from all command sources as Standby or On/Standby commands, the standby output is enabled.

If the device goes into Standby from On then any program command will bring the device On with that program selected. On/Off command from keyboard only will execute the Off function. On/Standby, Memory sequence up or down, 1 * and ± 10 (decade) commands from any command source will bring the device On in the program selected before Standby with the display showing that program only, i.e. the device executes an On command only.

If the device goes into Standby from Powered down then the On/Off command from keyboard only and any program command, On/Standby, Memory sequence up or down, 1 * and ± 10 (decade) commands from any command source will bring the device On in program 1. i.e. the device executes an On command only.

OPTION SELECT

The Option select pin provides an extra line that performs a "hard wired keyboard function" in conjunction with the keyboard scanning lines D0-D4. This line has integrated logic associated with it that enables one or many of the functions to be active simultaneously. In contrast, the keyboard inputs a-g will allow one key active at any given time. See keyboard section.

Various options can be selected by the connection or not of a diode as shown in figs. 7 & 8. From left to right along the Option select line column 1 selects the number of programs. A diode connected here selects 20 programs (full complement) and no diode (default) selects 16 programs only that can be accessed. The 20 program option only enables selection of 1 * or decade modes in column 4. In column 2 the AV option defines the state of the AV outputs for two protocols. These are described in section Audio visual output. Column 3 defines the state the M494 powers up in. If no connection of a diode (default) is made here the device powers up in the Off state. If a diode is present then the device powers up in the Standby state. In column 4, activated by the 20 program option only, the presence of a diode places the device in 1 * mode and the absence of a diode selects decade mode. The diode and switch in column 5 defeats the skip condition and enables program memory words to be read with the skip flag set. This allows programming (or reprogramming) of previously skipped words.

SKIP FUNCTION

Program skip is implemented in the M494 by a single memory bit associated with each program word. The bit acts as a flag to the device to indicate that the program word should be skipped and the next program word read from the memory in ascending or descending order if the skip flag is set. Programs are skipped only when accessed using the memory sequence up/down commands. Direct access to a program from the keyboard, RC or data command sources will always override the skip function. e.g. if skip is set on prog. 7 and prog. 7 is commanded from RC then prog. 7 will be tuned even if there is nc prog. stored in that memory location.

In order to program the skip bit and to defeat its function when required two commands are available : set skip flag and skip defeat. The skip defeat switch is designed to be activated by a facia panel on the TV set under which are infrequently used controls.

On the set skip flag command the M494 stores the current contents of the tuning, band and MS counters and sets the skip bit. After the set skip flag operation the contents of the tuning, band and MS counters will not change and the device continues to output these values. The operation is transparent to the user in terms of function but is indicated on the display by the program number flashing at 5Hz for 1 second. In order to reset the skip bit for any program word the desired program should be selected with skip defeated. A station should then be tuned, if required, and then the store command issued. The store command automatically resets the skip flag.

The skip defeat command enables the reading and writing (plus resetting of skip flag) of memory words whose skip flag is set. If skip is defeated the device will only access the number of programs selected by the option select i.e. If 16 programs only are selected then skip defeat will NOT enable access to all 20 programs.

RESET

There are two conditions under which the M494 is reset : power on and start up (On command). Power on reset is triggered whenever V_{DD} falls below about 3V. The duration of this reset is 110ms after V_{DD} has been restored.

POWER ON RESET (Powered down to Off or Standby states)

After the reset period of 110ms :

a) The program counter is set to program 1.
b) The outputs are disabled as defined in the Off and Standby states. See Standby & Off definitions.
c) The option selection, keyboard, momentary on switch and, when in standby, the display, RC and data inputs become active. For the "activity level" of the keyboard in Off and standby states. See Standby & Off definitions.
d) An internal register is set to indicate that the device has powered up from the powered down state.

Start up reset (Standby or Off states to On state)

A start up reset is instigated by the reception of the commands given in the definition of terms or the Standby section. The following then occurs :

a) The internal register indicating that the device has powered up from the powered down state is read:
I) If the register is set than the memory word addres sed by the program counter is loaded into the tu ning counter and then the analog values are read rom the memory.
II) If the register is reset then the previously selec ted tuning and analog values are left unchanged.
b) The AFC is defeated and the volume muted for a period of approx 1.7 seconds or 0.6 seconds lon ger than the other analog outputs.

c) The tuning and analogue outputs, except volume, are enabled after approx. 1.1 seconds.

d) The volume output is enabled after 1.7 seconds

e) The standby output is pulled up internally to logic HI

f) The internal register is reset.

If the device has either of the power up options (power up in Off or standby states) selected then it will perform a power up reset but all the outputs and command sources will remain disabled, then on the On command, a start up reset will be performed. If the device is required to power up in the On state using the momentary mechanical switch connected to the h+i pin then it will perform an ordinary power on reset followed immediately by a start up reset. The outputs and command sources will be enabled after the periods defined above.

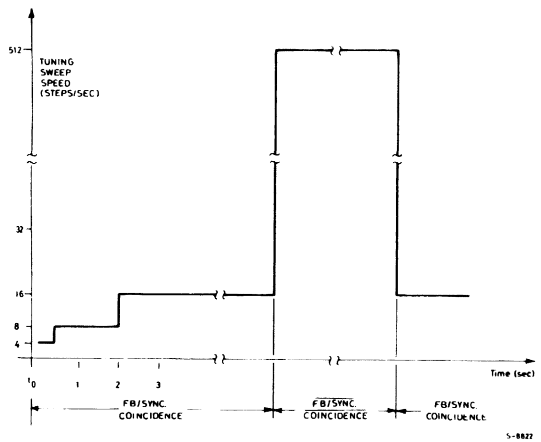
MANUAL TUNING

Manual tuning commands tune up or down, are available from keyboard only and are provided to allow both manual station search and tuning adjustments. If a continuous tuning up or down command is made from the keyboard the speed of movement of the tuning counter is as shown in fig. 10 for the UHF and CATV bands. Time t_o is the start time for the key being pressed. When the FB/sync. coincidence input is a logic HI the tuning speed is reduced to 16 steps/sec. If, at time t_o the FB/sync. coincidence input is at logic LO than the tuning.sweep speed jumps immediately to 512 steps/sec.

For VHF III & I all these levels are shifted up by a factor of 2 & 4 respectively giving slowest speeds of 8 steps/sec. and 16 steps/sec. and highest speeds of 1024 steps/sec and 2048 steps/sec. If the continuity of command is broken by releasing the keyboard for example then the tuning speed returns to its slowest speed when the FB/sync. coincidence input is at logic HI. If the upper or lower limit of a band is reached during manual tuning then tuning will continue in the same direction from the opposite limit after a 480ms delay to allow for the discharge of the external network.

The tuning counter is 13 bits in length giving a range of 8192 steps. The UHF band has a bandwidth of approx. 400MHz. Thus in the UHF band the slowest speed of 4 steps/sec. gives a tuning speed of about 200KHz/sec. The fastest speed of 512 step/sec. corresponds to a total band sweep time of 16 seconds.

Figure 10 : Tuning Sweep Speed (UHF & CATV BANDS).



PROGRAM MEMORY SEQUENCE

A continuous up/down program memory command from keyboard produces a program change every 500ms. From remote control and data command sources a continuous program memory sequence command produces a program change approx. every 500ms or every 5 received commands. A memory sequence up or down command issued from any source will bring the device out of standby to the program selected before standby was commanded. The memory sequence up or down will not then commence until the command is stopped and reissued from any source (until an EOT has been received or internally generated).

MUTE

The sound mute function is available as a toggle command from all command sources. There are other commands and functions during which the sound is muted :

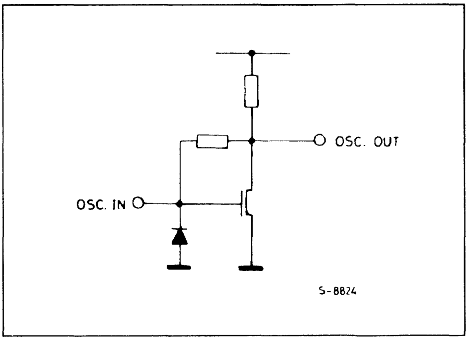
- FB/sync. coincidence - If there is no FB/sync. coincidence under any conditions the sound is muted.
- Start up reset - the sound is muted for approx. 1.7 seconds.
- Program change - the sound is muted for 0.6 seconds on any program change ; direct, 1 * + 0-9 program (only after the second keystroke), ±10 (decade) & Memory sequence up/down continuous or single keystrokes.
- Standby & Off states - the sound is muted.
- Band sequence - same as program change.
- The sound is demuted under the following conditions :
- When the mute command is received from any source.
- When the device is commanded On from standby of Off, i.e. if the device was muted when the standby command was issued then when On is commanded it will always start up with the sound demuted after the reset and settling period of approx. 17 seconds.
- Volume up - if volume up is commanded whilst the sound is muted then the volume will increase from zero.
- Volume down - if volume down is commanded whilst the sound is muted then there is no effect.
- Any program change - the sound is NOT demuted.

MOMENTARY ON SWITCH

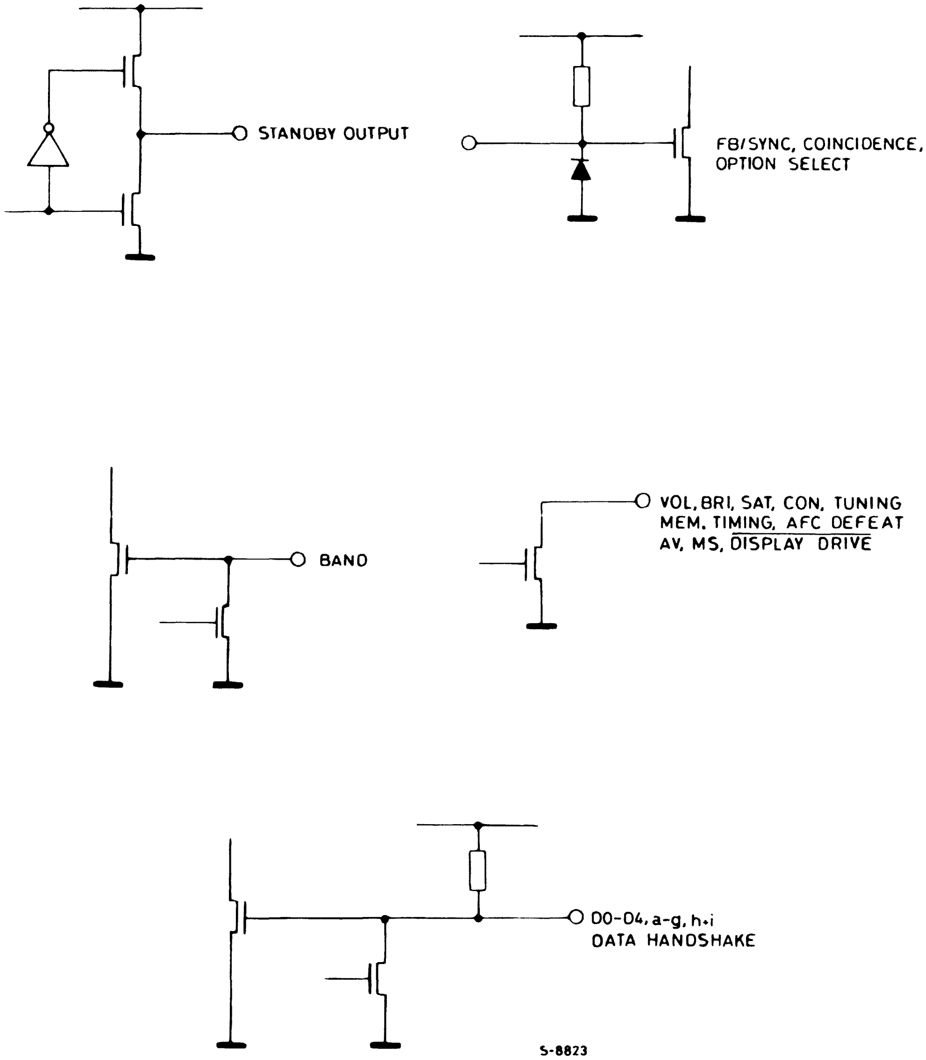
Provision is made for a momentary switch connected between the h+i pin and ground to force the M494 to make Power on and Start up resets automatically so that the device attains the On state immediately.

The condition of the h+i pin is latched after the reset period of 110ms. Therefore the period of switch contact closure should be a min. of 120ms.

INPUT/OUTPUT CONFIGURATION



INPUT/OUTPUT (continued)



COMMANDS

Command	Source	Function
Programs 1-12	KB, D,RC (16 opt.)	Reads the contents of the memory location : 2MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
Programs 0-9	KB, D, RC (20 opt.)	Reads the contents of the memory location : 2MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
Programs 13-16	D, RC (16 opt.)	Reads the contents of the memory location : 2 MSB's to the MS counter, next 2 MSB's to the band counter next 12 MSB's to the tuning counter and D/A and LSB to skip flag register. Initiates an on command only after standby.
– 10 (decade)	KB, D, RC (20 opt.)	Sustracts 10 from the current program (if possible). Initiates an on command only after standby.
+ 10 (decade)	KB, D, RC (20 opt.)	Adds 10 to the current program (if possible). Initiates an on command only after standby.
1*	KB, D, RC (20 opt.)	Commands the M494 to wait for a 0-9 program command or to reset on any other command. Display shows static half digit and g segment flashing at 5Hz. Initiates an on command only after standby.
Vol. up/down Bri. up/down Sat. up/down Con. up/down	KB, D, RC	Increments up or down the relevant analog control counter every keystroke or continuously every 112ms from KB and every 102ms from the RC and data inputs. The display shows an up/down arrow for 300ms min.
Tune up/down	KB	Increments up or down the tuning counter. The speed or increment/decrement is defined by Fig. 10. The display shows an up/down arrow for 300ms min.
Mem. up/down	KB, D, RC	The program number (memory location) is incremented/decremented.
Mute (toggle)	KB, D, RC	Volume Mute. See mute section.
Standby	D, RC	Commands the standby state.
On/standby (toggle)	KB, D, RC	Commands the standby state from the on state and the on state from the standby state.
ON/OFF	KB	Commands the on state when in the off state and commands the off state when in the on state. See standby section.
Store Program	KB	The currently addressed memory location is written from the tuning, band and MS counters and the skip flag is reset. See fig. 11. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Store analog Controls	KB	The analog control memories are written in sequence from the analog control counters. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Band Sequence	KB	Command the next band in the sequence as defined in bands outputs section. One step for each key stroke.
MS Sequence	KB	Increments the MS counter by binary one. One step for each key stroke.
Normalise Analog	KB, D, RC	Reads the analog memories in sequence to their corresponding D/A's. The analog control outputs are disabled during the read sequence.
Memory addressing	KB	Strokes the program selected immediately after the memory addressing command (post tuning program selection). See fig. 12.
Set Skip Flag	KB	Sets the skip flag on the currently selected program. Execution of this command is indicated by the display flashing at 5Hz for 1 second.
Skip Defeat	OS	Defeats the function of the skip bit to allow reading and writing of the currently selected program.

KB = Keyboard; D = Data; RC = Remove Control; OS = Option Select.

Figs. 11 & 12 respectively show in flow diagram form the two methods for storing a station : pretuning program selection and post tuning program selection. Figs. 13, 14 & 15 show the select programme subroutine for figs. 11 & 12 for either 16 program option or 20 program option with 1 * or ±10 (decade modes).

Figure 11 : Normal Methods for Storing a Station (preselection of program number).

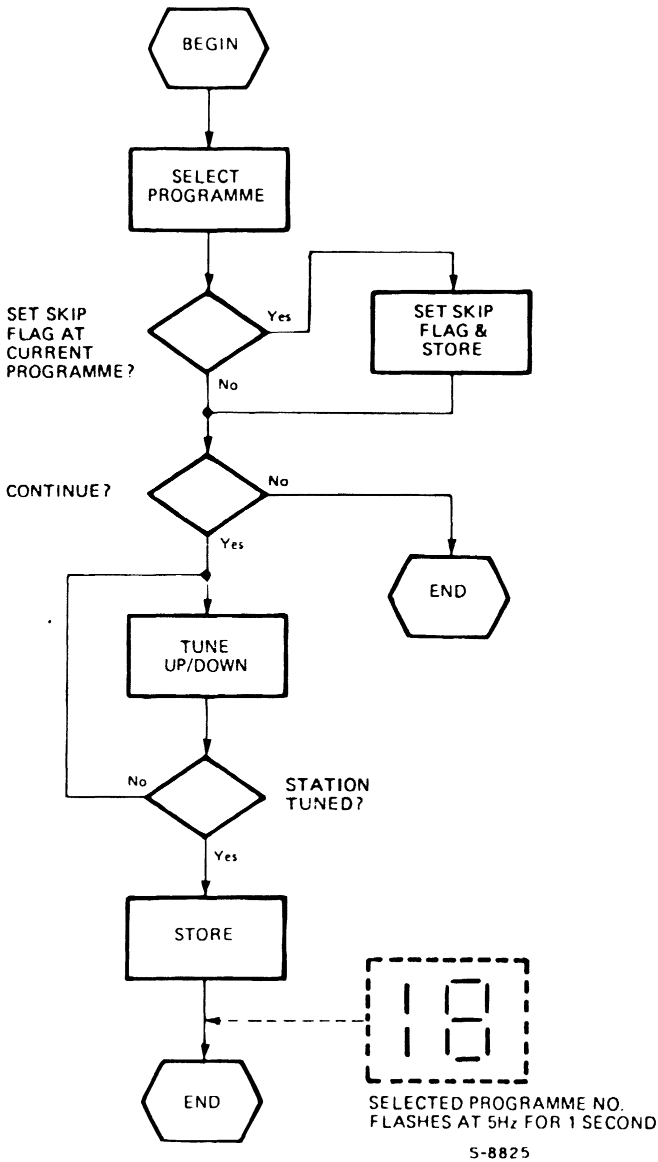


Figure 12 : Secondary Method for Storing a Station (postselection of program number).

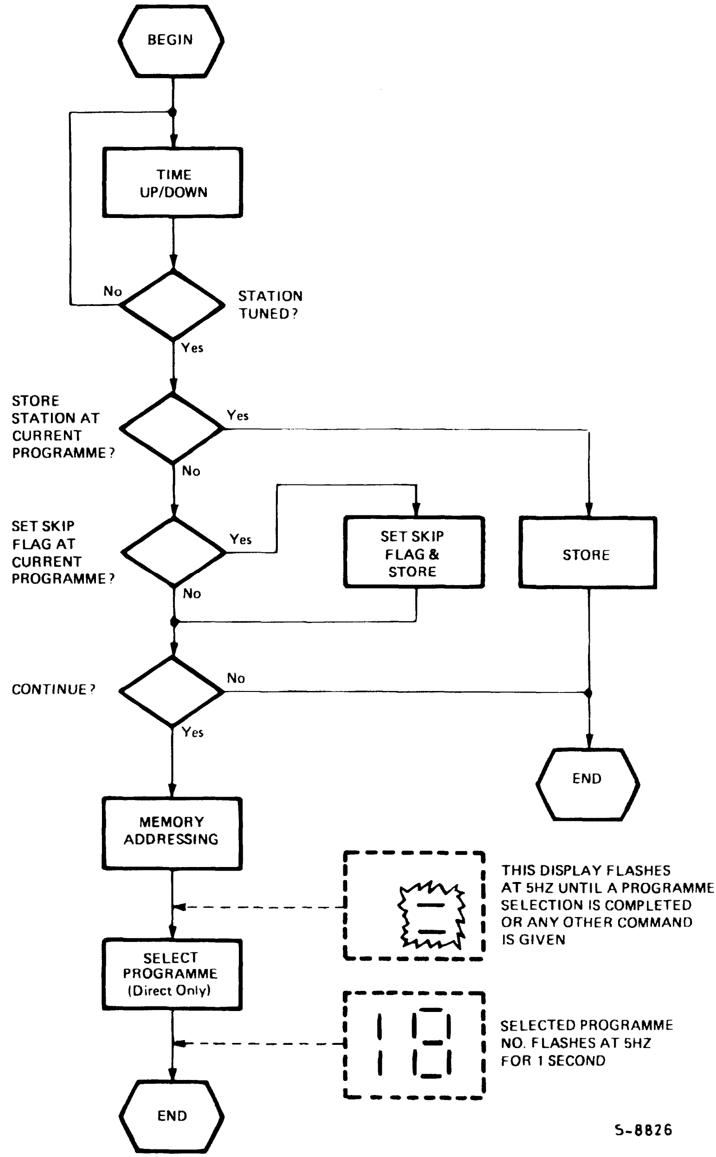


Figure 13 : Program Selection Routine (16 program).

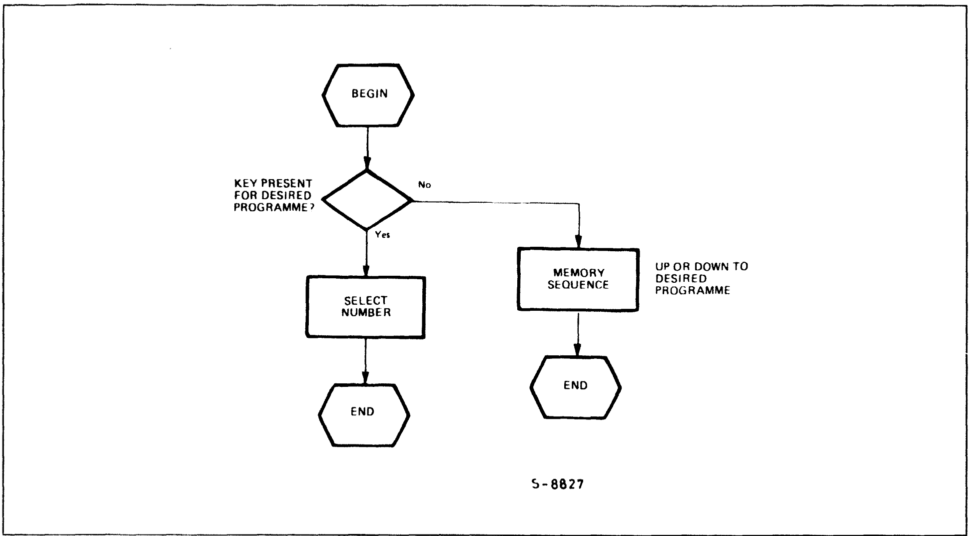


Figure 14 : Program Selection Routine (20 program, 1 * mode).

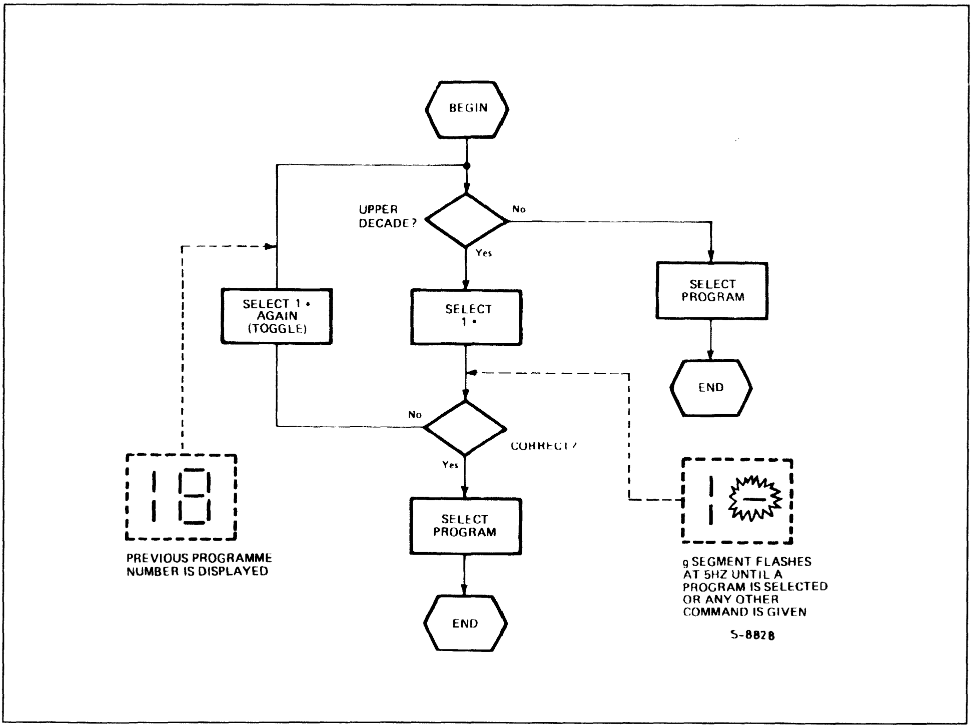
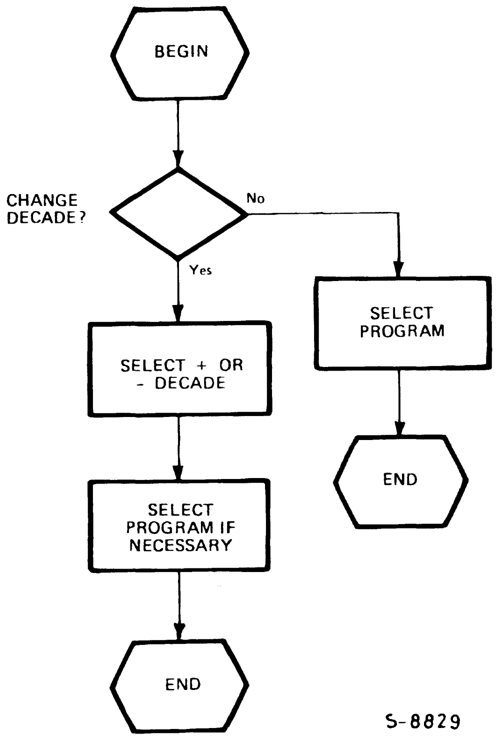
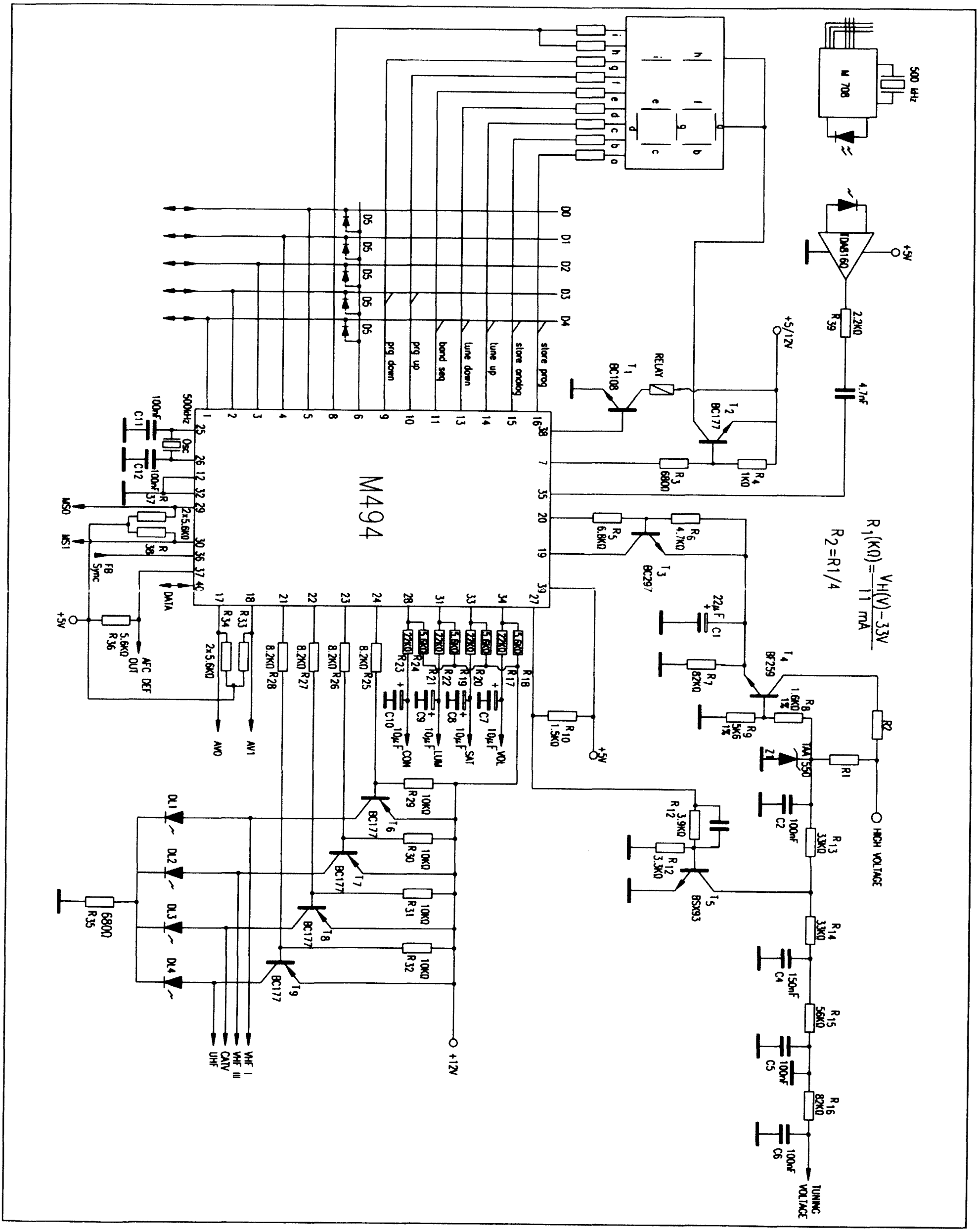


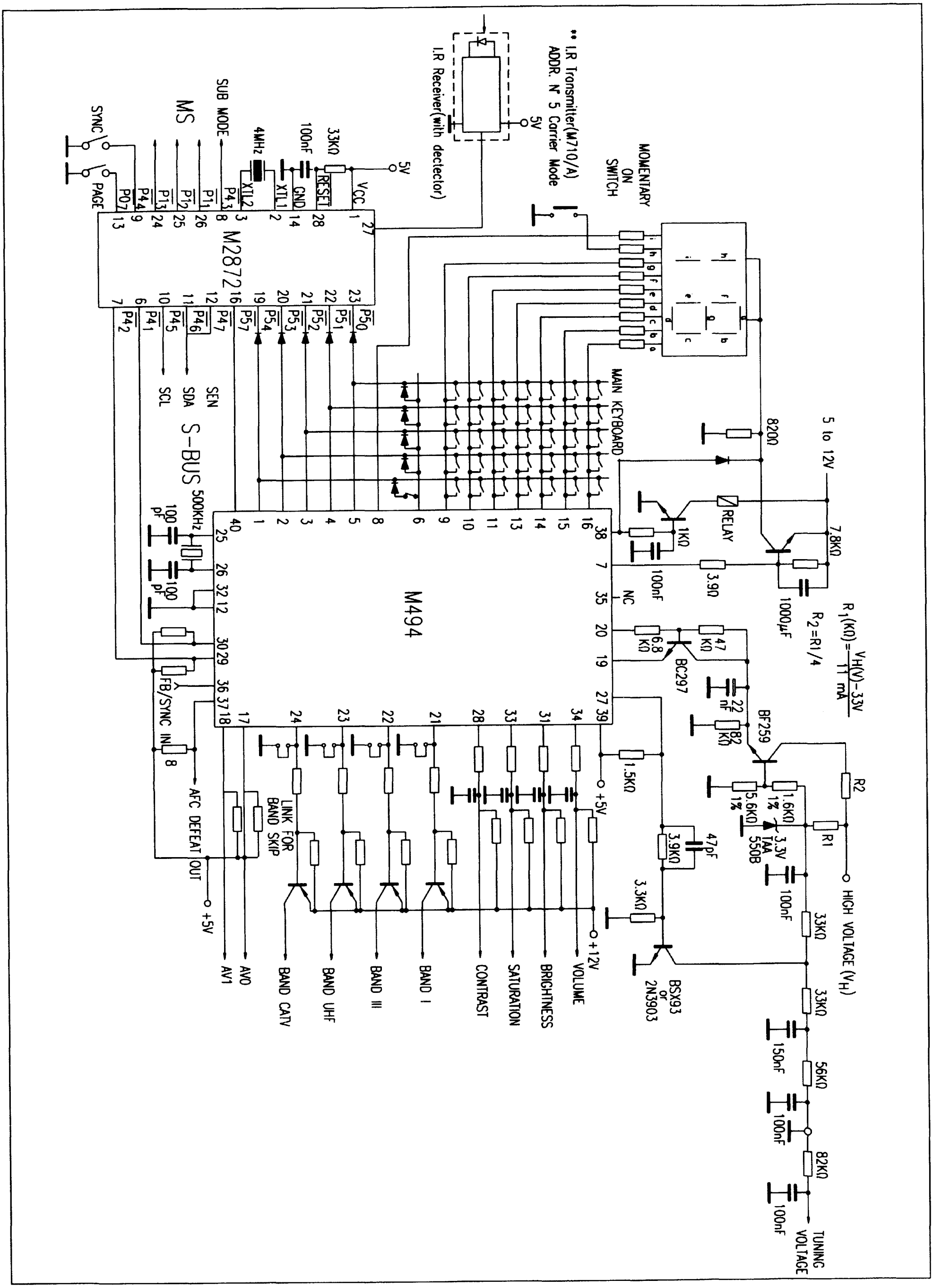
Figure 15 : Program Selection Routine (20 program, decade mode).



TYPICAL APPLICATIONS

Below are shown the circuit diagram for various system configurations. The configurations shown include the remote control feature and the application for the teletext in conjunction with the M2872 microprocessor. Also system configuration without remote control can be implemented for low cost application.




M2872
M494
S-BUS
MAIN KEYBOARD
MOMENTARY ON SWITCH
I.R Receiver(with dectector)
** I.R Transmitter(M710/A) ADDR. N° 5 Carrier Mode
SUB MODE
MS
SYNC
PAGE
SEN
SDA
SCL
4MHz
500KHz
RELAY
5 to 12V
HIGH VOLTAGE (VH)
TUNING VOLTAGE
VOLUME
BRIGHTNESS
SATURATION
CONTRAST
BAND I
BAND III
BAND UHF
BAND CATV
AV0
AV1
AFC DEFEAT OUT
FB/SYNC IN
LINK FOR BAND SKIP
BC297
BF259
BSX93 or 2N3903
TAA 550B
R2=R1/4

PCM REMOTE CONTROL TRANSMITTER

ADVANCED DATA

- 30 CHANNELS/4 ADDRESSES
- SELECTABLE FLASH/CARRIER TRANSMISSION MODE
- END OF TRANSMISSION CODE
- VERY LOW POWER DISSIPATION DURING TRANSMISSION : DUTY CYCLE 0.15 % (flash mode), 0.7 % (carrier mode)
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M708 4.5 to 10.5 V)/(M708A 3 to 10.5 V)
- WIDE REFERENCE FREQUENCY RANGE (445 to 510 kHz ceramic resonator)
- 20 PIN PLASTIC PACKAGE
- TO BE USED IN CONJUNCTION WITH M490/M491 SINGLE CHIP STATION MEMORY AND R.C. RECEIVER (flash mode) OR WITH MICROPROCESSOR CONTROLLED SYSTEM (carrier mode)

When the M708 works in conjunction with M490/M491 single chip Station Memory and R.C. receiver the oscillator frequency can be in the range 445 to 510 kHz and no synchronization is required with the receiver clock.

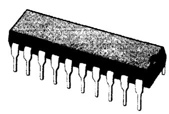
The M708 is produced with CMOS Si-gate technology and is available in a 20 pin dual in-line plastic package.

DESCRIPTION

This IC has been developed for remote control in consumer applications. It uses a highly reliable transmission code which has the capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command. However only 2 addresses and 30 commands are available in this IC. An additional command (000000) is used to transmit the "end of transmission code" when the key is released.

Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides simultaneous applications without interference among each system.

The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. Four addresses are available for this purpose. The reference oscillator is controlled by a cheap ceramic resonator.

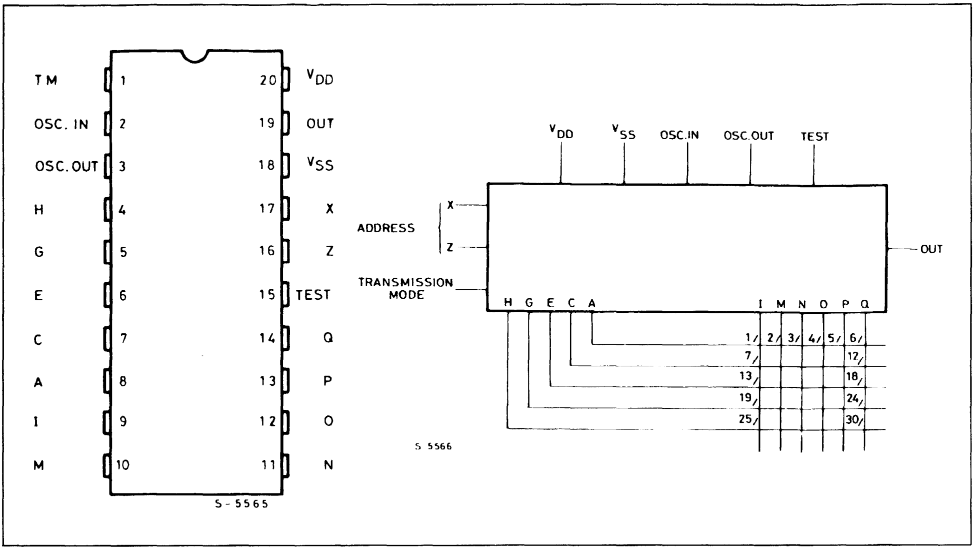


DIP20

ORDER CODES : M708 B1
M708A B1

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS



Note : The test pin must be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

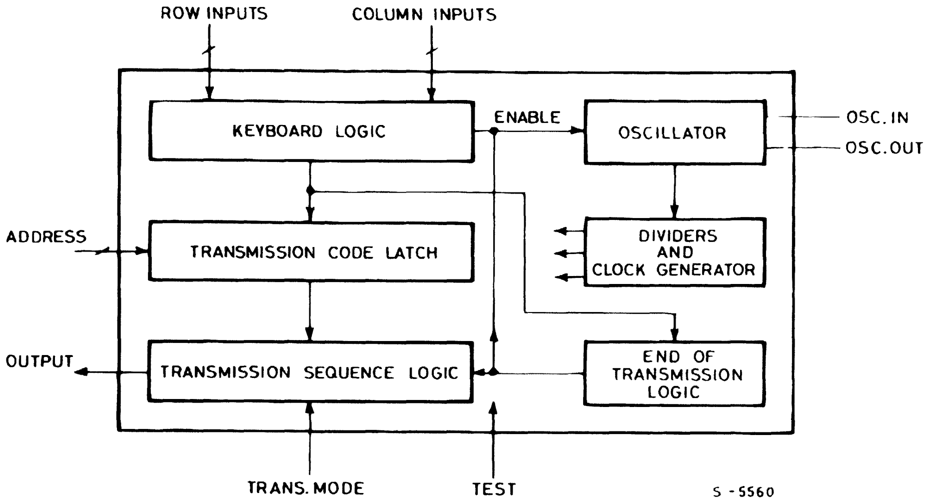
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 12	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.3	V
$\lvert I_O \rvert$	IR Output Current (t < 50 µs)	10	mA
T_{op}	Operating Temperature	0 to 70	°C
P_{tot}	Total Package Power Dissipation	200	mW
T_{stg}	Storage Temperature	– 55 to 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : M708 M708A	4.5 to 10.5 3 to 10.5	V V
V_I	Input Voltage	0 to V_{DD}	
$\lvert I_O \rvert$	IR Output Current (t < 50 µs)	max. 2.5	mA
f_{ref}	Reference Frequency	445 to 510	kHz
T_{op}	Operating Temperature	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max. 2.5	KΩ
r_p	Parallel Resistance of Open Key Contact	min. 2.2	MΩ
R_s	Serial Resistance of the Ceramic Resonator	max. 20	Ω

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 9 V and T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions		Value Min.	Value Typ.	Value Max.	Unit
I_{DD}	Supply Voltage		V_{DD} = 9 V IR Output Open	Stand–by		5	15	µA
				Operating (one key closed)		4	7	mA
I_{OH}	H State IR Output Current		V_{DD} = 9 V	V_{OH} = 8 V	– 1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OH} = 3.5 V	– 0.3	– 0.5		
I_{OL}	L State IR Output Current		V_{DD} = 9 V	V_{OL} = 1 V	1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OL} = 1 V	0.3	0.5		
V_{TH}	Input Threshold High	Selection Inputs A to H	V_{DD} = 9 V				6	V
			V_{DD} = 4.5 V				3	
V_{TL}	Input Threshold Low	Selection Inputs K to Q	V_{DD} = 9 V		3			V
			V_{DD} = 4.5 V		1.5			
I_{IL}	Input Low Current	Pull–up Inputs A to H	V_{DD} = 9 V, V_{IL} = 4.5 V		– 60		– 300	µA
I_{IH}	Input High Current	Pull–down Inputs K to Q	V_{DD} = 9 V, V_{IH} = 4.5 V		60		300	µA
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 9 V, V_{IL} = 8.25 V (oscillator running)				150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 9 V, V_{IN} = 0 to 9 V				1	µA
I_{OS}	Output Current	Osc. Out.	V_{DD} = 9 V, Osc. In. = V_{SS}		– 2		– 8	µA

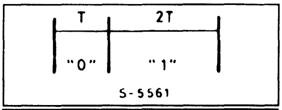
TRUTH TABLE

Command N°	Input Code											Command Bits					
	A	C	E	G	H	I	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	END OF TRANSMISSION											0	0	0	0	0	0
1	X					X						1	0	0	0	0	0
2	X						X					1	1	0	0	0	0
3	X							X				0	0	1	0	0	0
4	X								X			1	0	1	0	0	0
5	X									X		0	1	1	0	0	0
6	X										X	1	1	1	0	0	0
7		X				X						1	0	0	0	1	0
8		X					X					1	1	0	0	1	0
9		X						X				0	0	1	0	1	0
10		X							X			1	0	1	0	1	0
11		X								X		0	1	1	0	1	0
12		X									X	1	1	1	0	1	0
13			X			X						1	0	0	0	0	1
14			X				X					1	1	0	0	0	1
15			X					X				0	0	1	0	0	1
16			X						X			1	0	1	0	0	1
17			X							X		0	1	1	0	0	1
18			X								X	1	1	1	0	0	1
19				X		X						1	0	0	0	1	1
20				X			X					1	1	0	0	1	1
21				X				X				0	0	1	0	1	1
22				X					X			1	0	1	0	1	1
23				X						X		0	1	1	0	1	1
24				X							X	1	1	1	0	1	1
25					X	X						1	0	0	1	1	1
26					X		X					1	1	0	1	1	1
27					X			X				0	0	1	1	1	1
28					X				X			1	0	1	1	1	1
29					X					X		0	1	1	1	1	1
30					X						X	1	1	1	1	1	1

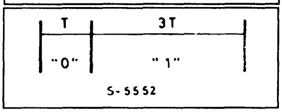
DESCRIPTION

The signals are transmitted with infrared light using a Pulse Code Modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses. If "T" is the time base, the bits are coded as follows :

Odd bits (1, 3, etc)
0 = T
1 = 2T

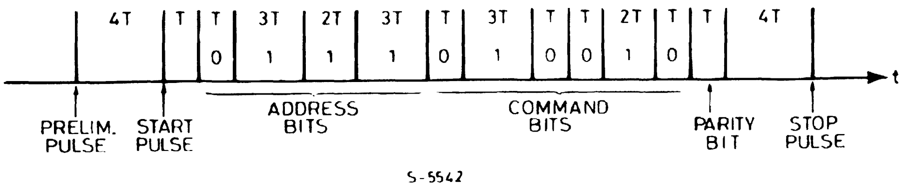


Even bits (2, 4, etc.)
0 = T
1 = 3T



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected. A Parity bit is also added in order to further increase the reliability of the transmission. This bit is "1" if the number of transmitted "1" is even while it is "0" if the number of transmitted "1" is odd. In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after a 4T interval by a stop pulse. Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T. A word containing ten "1s" has a duration of 36T.

Example :



SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER

The transmitter and the receiver can operate with different reference frequencies. Typical values suitable for correct operation of the system should be comprised between 445 and 510 kHz, using a cheap ceramic resonator.

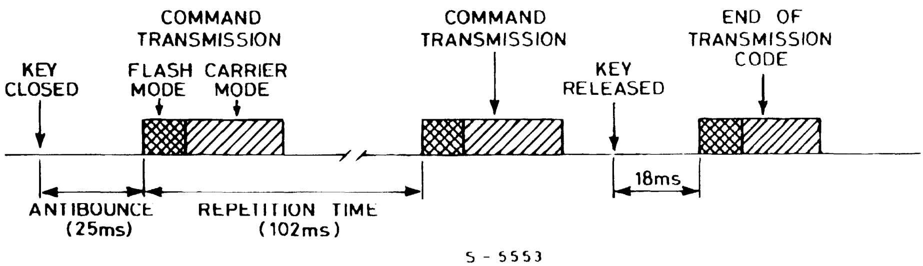
Synchronization between the transmitter and the receiver, necessary to obtain the above described wide range of frequency tolerance is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD/CODE REPETITION

One column, input (pins IMNOPQ) has to be connected to one row (pins ACEGH) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.

Double and multiple contact operations are not accepted. The command information is repeatedly transmitted at intervals of 102 ms (f_{ref} = 500 kHz) as long as the push button remains operated. When the contact is interrupted the circuit transmits, after a pause of 18 ms, the "end of transmission code" and returns to stand-by mode. If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

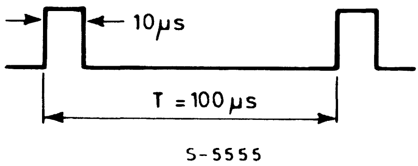
No command is accepted until the "end of transmission code" is over.



TRANSMISSION MODE (pin T)

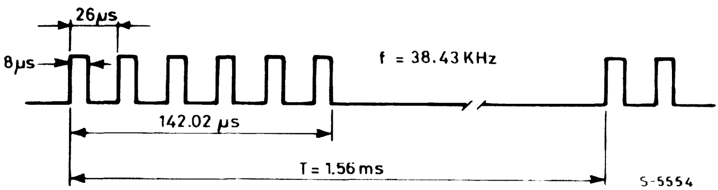
The M708 can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes. Using a reference frequency of 500 kHz the output signal has these formats respectively :

Flash Mode



Transmission time
min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15 %

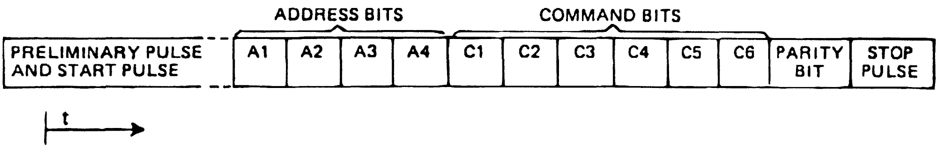
Carrier Mode



Transmission time
min. = 32.76 ms
max = 56.16 ms
duty cycle = 0.7 %

ADDRESS (pins X, Z)

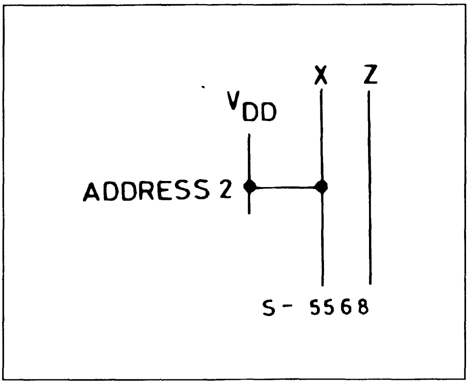
The address information is coded and transmitted as follows.



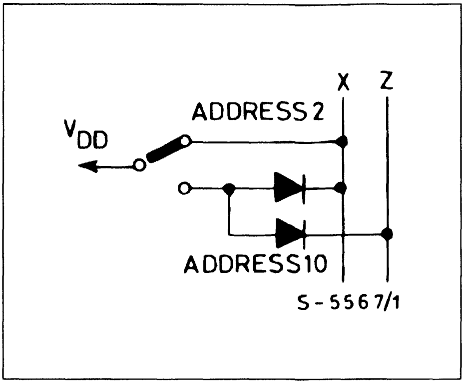
Address Number	Transmitted Code				Address Input Code	
	A1	A2	A3	A4	X	Z
1	0	0	0	0	L	L
2	1	0	0	0	H	L
9	0	0	0	1	L	H
10	1	0	0	1	H	H

The Address inputs have internal pull-downs which are disabled during stand-by.

Single address selection



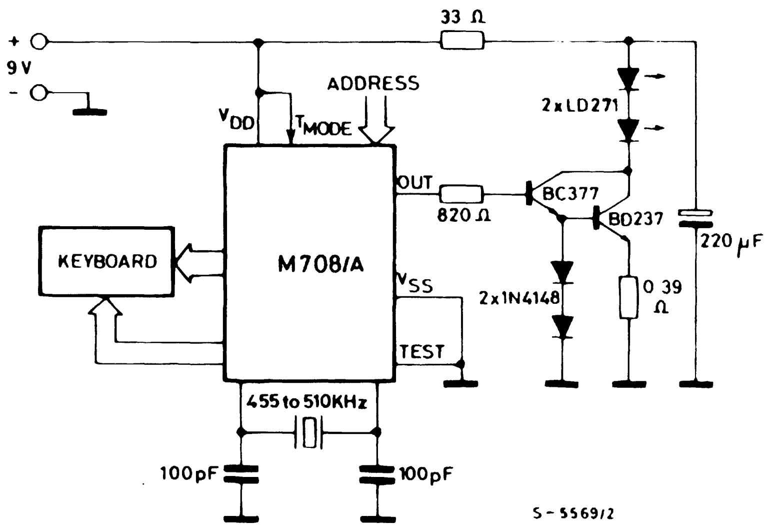
Multiple address selection



Note : Unused inputs can be left open or connected to V_{SS}.

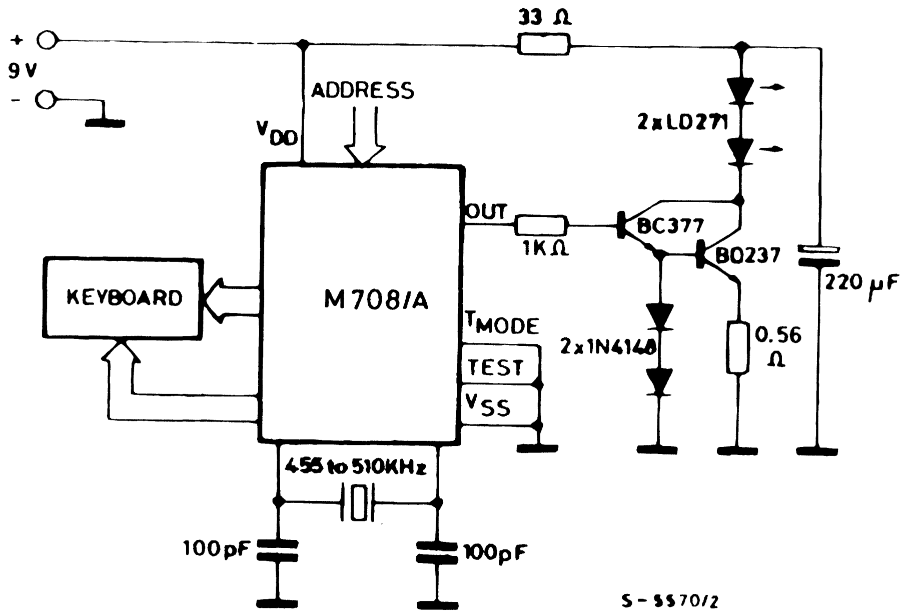
TYPICAL APPLICATIONS

FLASH MODE



INFRARED DIODE PEAK CURRENT = 1.8 A
TOTAL AVERAGE CONSUMPTION = 6.5 mA

CARRIER MODE



INFRARED DIODE PEAK CURRENT = 1.25 A
TOTAL AVERAGE CONSUMPTION = 13 mA

PCM REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

- 2.2 TO 5 V OPERATING SYPPLY VOLTAGE RANGE
- 30 CHANNELS/4 ADDRESSES
- SELECTABLE FLASH/CARRIER TRANSMISSION MODE
- END OF TRANSMISSIONE CODE
- VERY LOW POWER DISSIPATION DURING TRANSMISSION. DUTY CYCLE : 0.15 % (flash mode), 0.7 % (carrier mode)
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE REFERENCE FREQUENCY RANGE (455 to 510 KHz ceramic or LC resonator)
- 20 PIN PLASTIC PACKAGE
- TO BE USED IN CONJUNCTION WITH M490/M491 SINGLE CHIP STATION MEMORY AND R.C. RECEIVER (flash mode)

DESCRIPTION

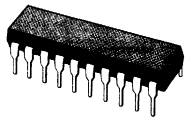
This IC has been developed for remote control in consumer applications. It uses a highly reliable transmission code wich has the capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command. However only 2 addresses and 30 commands are available in this IC. An additional command (000000) is used to transmit the "end of transmission code" when the key is released.

Additional bits are transmitted for synchronization of transmitter and receiver clock and for security checks. The address organization provides simultaneous applications without interference among each system.

The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. Two address are available for this purpose. The reference oscillator is controlled by a cheap ceramic resonator.

When the M708L works in conjunction with M490/M491 single chip Station Memory and R.C. receiver the oscillator frequency can be in the range 445 to 510 KHz and no synchronization is required with the receiver clock.

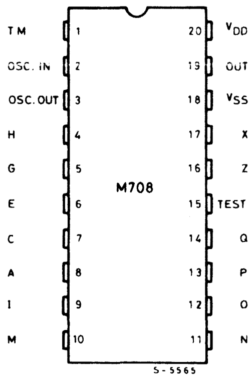
The M708L is produced with CMOS Si-gate technology and is available in a 20 pin dual in-line plastic package.

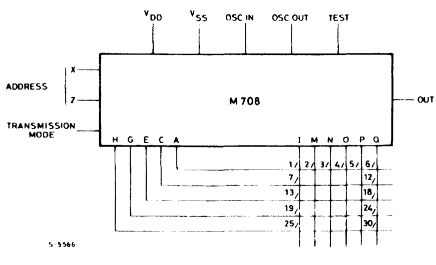


B
Plastic Package

ORDER CODE : M708LB1

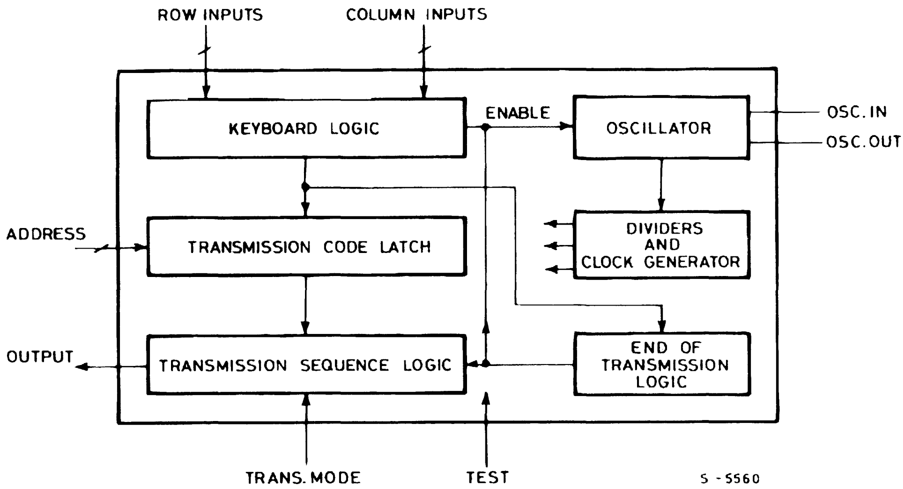
PIN CONNECTIONS (top view)





Note : The test pin must be connected to V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 5.5	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.3	V
$\|I_O\|$	IR Output Current (t < 50 µs)	10	mA
T_{op}	Operating Temperature	0 to 70	°C
P_{tot}	Total Package Power Dissipation	200	mW
T_{stg}	Storage Temperature	– 55 to 125	°C

Stresses above those listed under " Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	2.2 to 5	V
V_I	Input Voltage	0 to V_{DD}	
$\|I_O\|$	IR Output Current (t < 50 µs)	max 2.5	mA
f_{ref}	Reference Frequency	445 to 510	kHz
T_{op}	Operating Temperature	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max 2.5	kΩ
r_p	Parallel Resistance of Open Key Contact	min 2.2	MΩ
R_s	Serial Resistance of the Ceramic Resonator	max 20	Ω

TRUTH TABLE

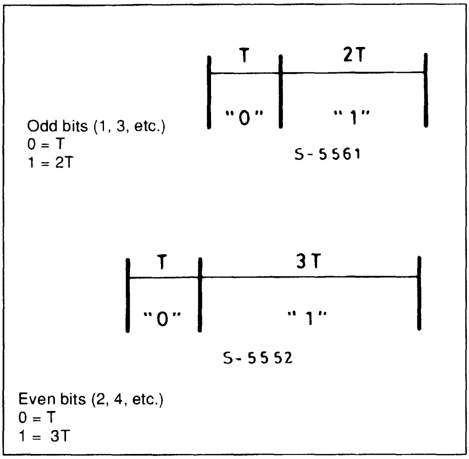
Command N°	Input Code											Command Bits					
	A	C	E	G	H	I	M	N	O	P	Q	C 1	C 2	C 3	C 4	C 5	C 6
0	End of Transmission											0	0	0	0	0	0
1	X					X						1	0	0	0	0	0
2	X						X					1	1	0	0	0	0
3	X							X				0	0	1	0	0	0
4	X								X			1	0	1	0	0	0
5	X									X		0	1	1	0	0	0
6	X										X	1	1	1	0	0	0
7		X				X						1	0	0	0	1	0
8		X					X					1	1	0	0	1	0
9		X						X				0	0	1	0	1	0
10		X							X			1	0	1	0	1	0
11		X								X		0	1	1	0	1	0
12		X									X	1	1	1	0	1	0
13			X			X						1	0	0	0	0	1
14			X				X					1	1	0	0	0	1
15			X					X				0	0	1	0	0	1
16			X						X			1	0	1	0	0	1
17			X							X		0	1	1	0	0	1
18			X								X	1	1	1	0	0	1
19				X		X						1	0	0	0	1	1
20				X			X					1	1	0	0	1	1
21				X				X				0	0	1	0	1	1
22				X					X			1	0	1	0	1	1
23				X						X		0	1	1	0	1	1
24				X							X	1	1	1	0	1	1
25					X	X						1	0	0	1	1	1
26					X		X					1	1	0	1	1	1
27					X			X				0	0	1	1	1	1
28					X				X			1	0	1	1	1	1
29					X					X		0	1	1	1	1	1
30					X						X	1	1	1	1	1	1

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Pins	Test Conditions		Value			Unit
					Min.	Typ.	Max.	
I_{DD}	Supply Voltage		V_{DD} = 5 V IR Output Open	Stand-by		3	10	µA
				Operating (one key closed)		4	7	mA
I_{OH}	H State IR Output Current		V_{DD} = 3 V	V_{OH} = 2 V	– 1	– 2		mA
			V_{DD} = 2.2 V	V_{OH} = 1 V	– 0.3	– 0.5		
I_{OL}	L State IR Output Current		V_{DD} = 3 V	V_{OL} = 1 V	1	2		mA
			V_{DD} = 2.2 V	V_{OL} = 1 V	0.3	0.5		
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 3 V, V_{IL} = 3 V (oscillator running)				150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 3 V, V_{IN} = 0 to 3 V				1	µA

DESCRIPTION

The signals are transmitted with infrared light using a Pulse Code Modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses. If "T" is the time base, the bits are coded as follows :



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected. A Parity bit is also added in order to further increase the reliability of the transmission. This bit is "1" if the number of transmitted "1" is even while it is "0" if the number of transmitted "1" is odd. In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after a 4T interval by a stop pulse. Consequently, a word in which the ninary digit 0 occurs ten times has a total duration of 21T. A word containing ten "1s" has a duration of 36T.(see Example)

SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER.

The transmitter and the receiver can operate with different reference frequencies. Typical values suitable for correct operation of the system should be comprised between 445 and 510 KHz, using a cheap ceramic resonator.

Synchronization between the transmitter and the receiver necessary to obtain the above described wide range of frequency tolerance is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD/CODE RECEPTION.

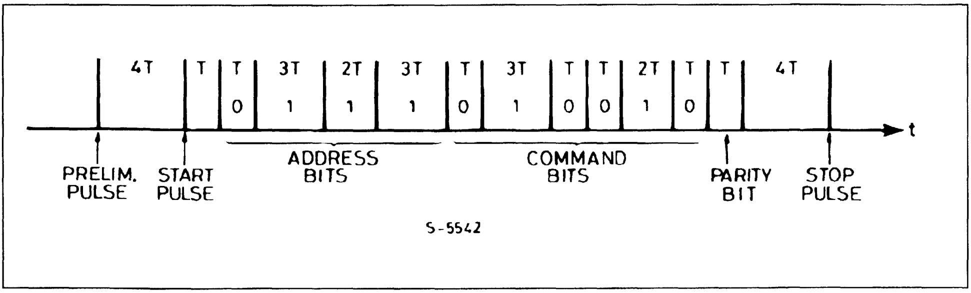
One column input (pins IMNOPQ) has to be connected to one row (pins ACEGH) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.

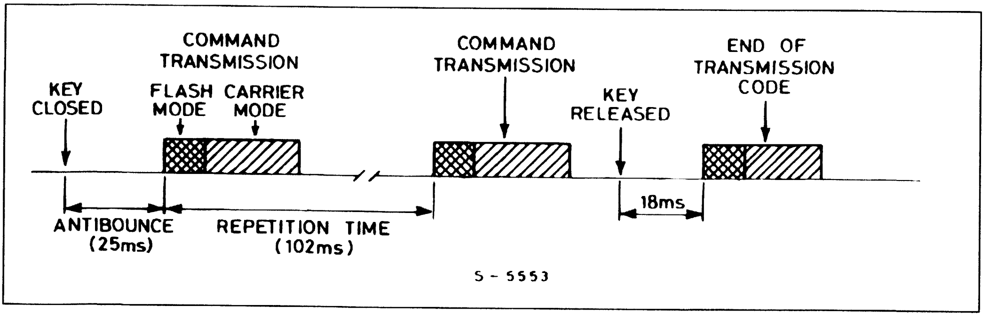
Double and multiple contact operations are not accepted. The command information is repatedly transmitted at intervals of 102 ms (f_{ref} = 500 KHz) as long as the push button remains operated.

When the contact is interrupted the circuit transmits, after a pause of 18 ms, the "end of transmission code" and returns to stand-by mode. If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

No command is accepted until the "end of transmission code" is over.

Example

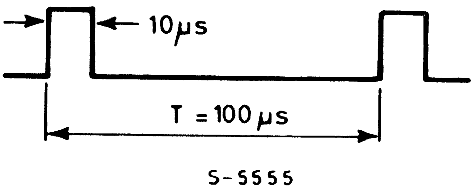




TRANSMISSION MODE (Pin T).

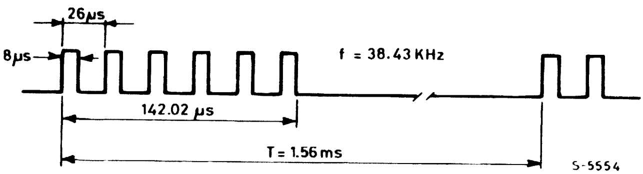
The M708 can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes. Using a reference frequency of 500 KHz the output signal has these formats respectively :

Flash mode



Transmission time
min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15%

Carrier mode



Transmission time
min. = 32.76 ms
max. = 56.16 ms
duty cycle = 0.7%

ADDRESS (Pin X, Z).

The address information is coded and transmitted as follows :

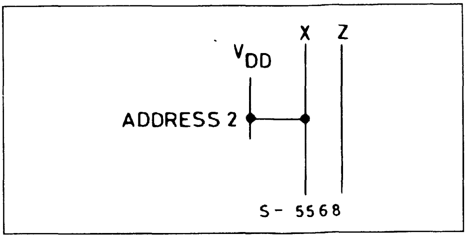
	ADDRESS BITS				COMMAND BITS							
PRELIMINARY PULSE AND START PULSE	A1	A2	A3	A4	C1	C2	C3	C4	C5	C6	PARITY BIT	STOP PULSE

t →

Address Number	Transmitted Code				Address Input Code	
	A1	A2	A3	A4	X	Z
1	0	0	0	0	L	L
2	1	0	0	0	H	L
9	0	0	0	1	L	H
10	1	0	0	1	H	H

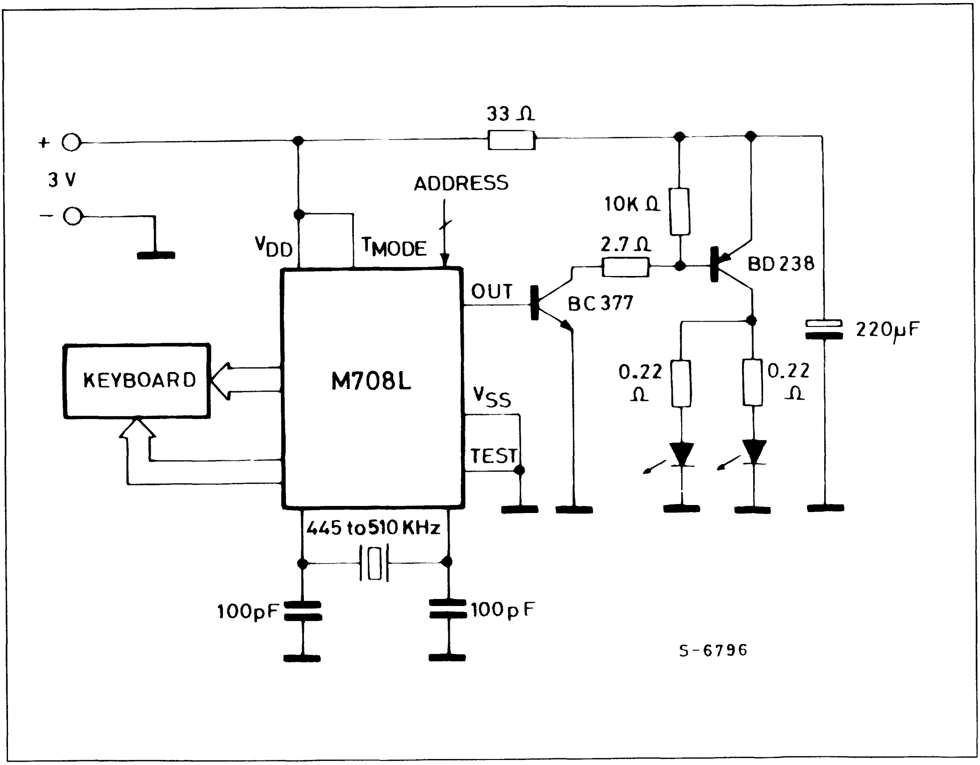
The Address inputs have internal pull-downs which are disabled during stand-by.

Note : Unused inputs can be left open or connected to V_{SS}.

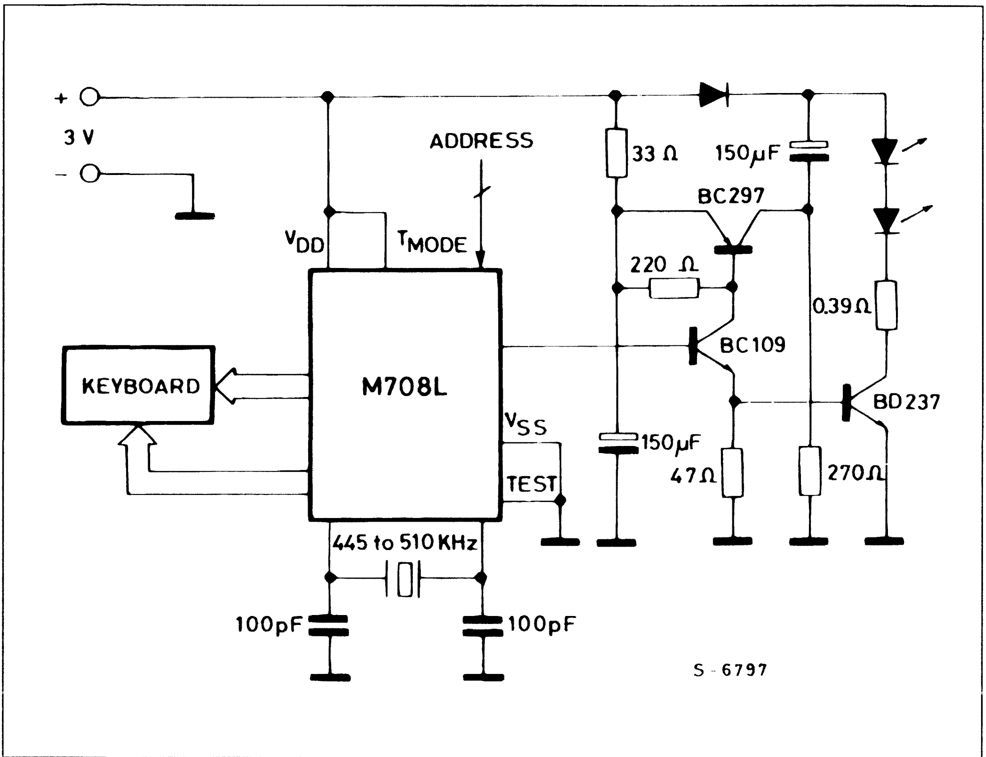


TYPICAL APPLICATION (flash mode)

STANDARD



VOLTAGE DUPLICATOR



SGS-THOMSON MICROELECTRONICS

M709/A M710/A

PCM REMOTE CONTROL TRANSMITTERS

- M 709 : 40 COMMANDS x 16 ADDRESSES
- M 710 : 64 COMMANDS x 16 ADDRESSES
- ADDRESS ORGANIZATION PROVIDES WIDE RANGE OF SIMULTANEOUS APPLICATIONS WITHOUT INTERFERENCE BETWEEN SYSTEMS
- IMPROVED PCM TRANSMISSION CODE PROVIDES EASY RECOGNITION OF FALSE SIGNALS
- "FLASH" OR "CARRIER" PIN SELECTABLE TRANSMISSION MODES
- END OF TRANSMISSION CODE
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M709/M710 4.5 to 10.5 V) / (M709A 3 to 10.5 V)
- WIDE REFERENCE FREQUENCY RANGE (445 to 510 kHz ceramic resonator)
- VERY LOW POWER CONSUMPTION DURING TRANSMISSION. OUTPUT DUTY CYCLE 0.15 % (flash mode). 0.7 % (carrier mode)
- TO BE USED IN CONJUNCTION WITH M104 OR M105 R.C. RECEIVERS (flash mode). THE CARRIER MODE IS FOR μP DECODING (e.g. PLL frequency synthesizer with M3870/M3872 and M206)

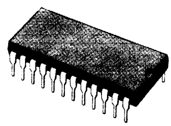
DESCRIPTION

These ICs have been developed for remote control in consumer applications (TV, radio, videorecorders) or in the industrial field and use a highly reliable transmission code which has a capacity of 1024 channels. Each transmitted word is structed into 4 bits which constitute the address and 6 bits which constitute the command (64 commands available). One command (1 st = 000000) is used to transmit the "end of transmission code " when the key is released. Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides a wide range of simultaneous applications without interference between systems. The receiver accents the decoded command only if the transmitted address matches the address selected at the receiver. 16 addresses are available for this purpose.

The reference oscillator is controlled by a cheap ceramic or LC resonator and when the M709/M710 work in conjunction with the M104 or M105 R.C. receives the oscillator frequency can be in the range 445 to 510 kHz and no synchronization is required with the receiver clock. Two types of transmission mode are available : "Flash" or "Carrier" mode.

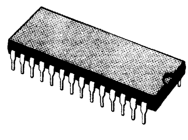
The M709 is a simplified version of the M710 which can only transmit 40 commands with 16 possible addresses. The M710 on the other hand has the full system capacity : it can transmit 64 commands with 16 addresses.

The M709 and M710 are produced with CMOS Si-gate technology and are available in 24 and 28-pin dual in-line plastic packages respectively.



M709/A

DIP-24

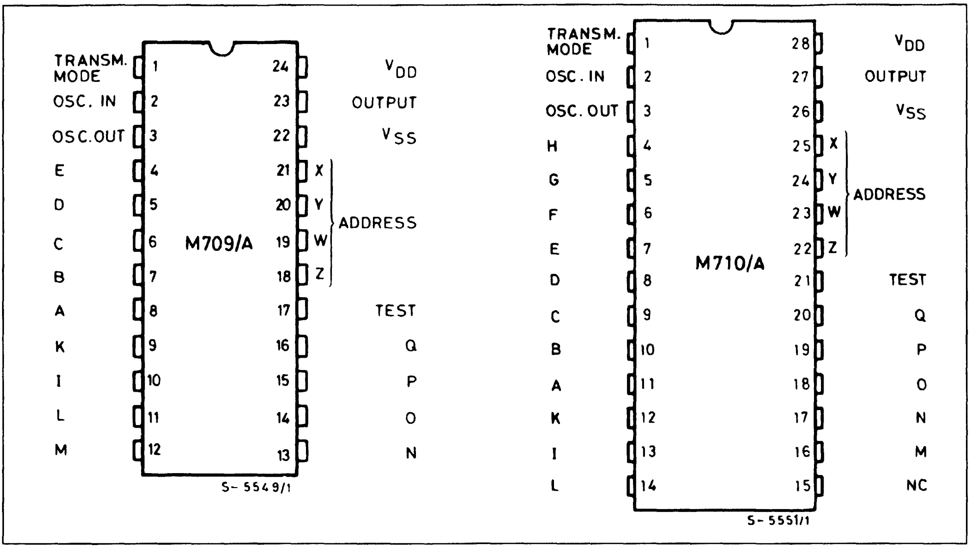


M710/A

DIP-28

ORDER CODE : M709 B1
M710 B1
M709A B1
M710A B1

PIN CONNECTIONS



Note : The test pin must be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

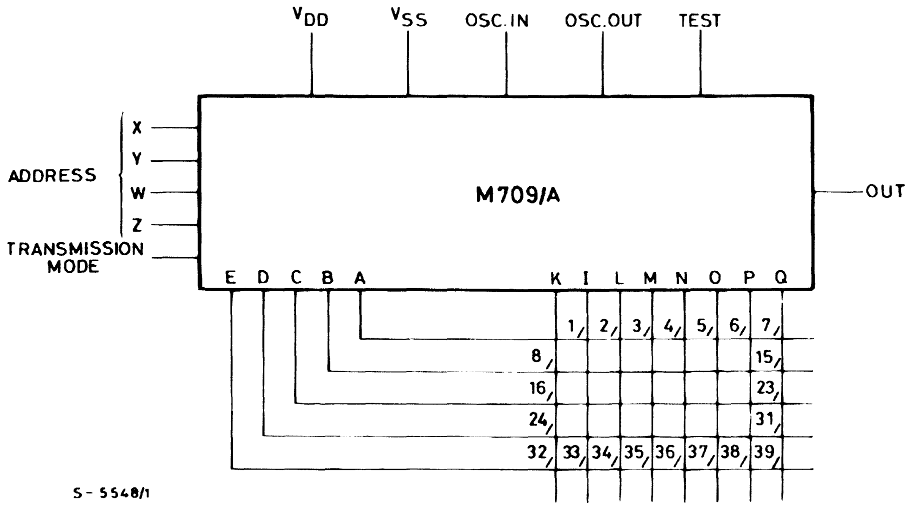
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 12	V
V_I	Input Voltage	– 0.3 to V_{DD} + 0.3	V
$\|I_O\|$	IR Output Current (t < 50 µs)	10	mA
P_{tot}	Total Package Power Dissipation	200	mW
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to + 125	°C

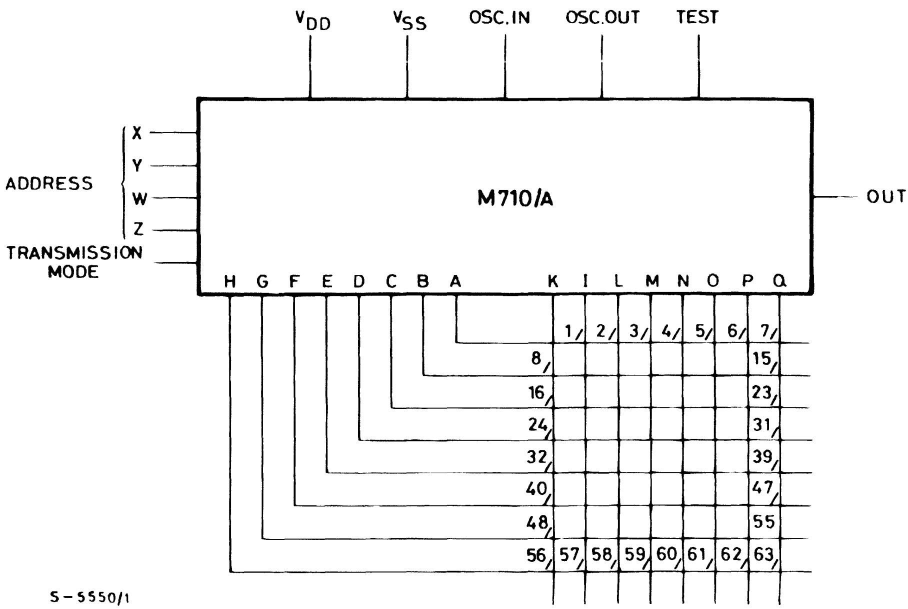
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

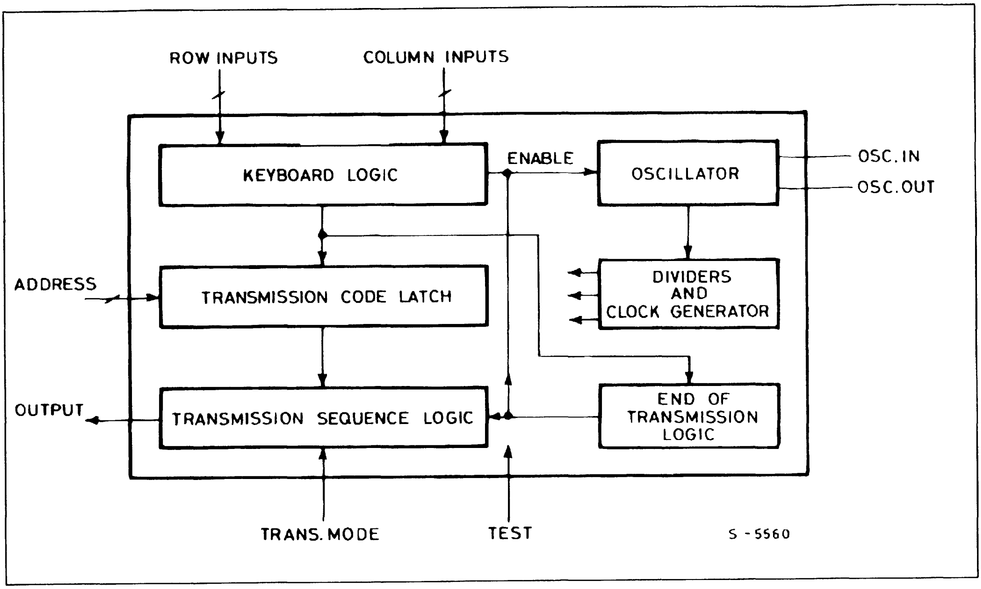
Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : M709/M710 M709A/M710A	4.5 to 10.5 3 to 10.5	V V
V_I	Input Voltage	0 to V_{DD}	
$\|I_O\|$	IR Output Current (t < 50 µs)	max. 2.5	mA
f_{ref}	Reference Frequency	445 to 510	kHz
T_{op}	Operating Temperature	0 to 70	°C
r_s	Serial Resistance of a Closed Key Contact	max. 2.5	KΩ
r_p	Parallel Resistance of Open Key Contact	min. 2.2	MΩ
R_s	Serial Resistance of the Ceramic Resonator	max. 20	Ω

FUNCTIONAL DESCRIPTION





BLOCK DIAGRAM



TRUTH TABLE

Command	Input Code																Command Bits					
N°	A	B	C	D	E	F	G	H	K	I	L	M	N	O	P	Q	C1	C2	C3	C4	C5	C6
0	End of Transmission																0	0	0	0	0	0
1	X									X							1	0	0	0	0	0
2	X										X						0	1	0	0	0	0
3	X											X					1	1	0	0	0	0
4	X												X				0	0	1	0	0	0
5	X													X			1	0	1	0	0	0
6	X														X		0	1	1	0	0	0
7	X															X	1	1	1	0	0	0
8		X							X								0	0	0	1	0	0
9		X								X							1	0	0	1	0	0
10		X									X						0	1	0	1	0	0
11		X										X					1	1	0	1	0	0
12		X											X				0	0	1	1	0	0
13		X												X			1	0	1	1	0	0
14		X													X		0	1	1	1	0	0
15		X														X	1	1	1	1	0	0
16			X						X								0	0	0	0	1	0
17			X							X							1	0	0	0	1	0
18			X								X						0	1	0	0	1	0
19			X									X					1	1	0	0	1	0
20			X										X				0	0	1	0	1	0
21			X											X			1	0	1	0	1	0
22			X												X		0	1	1	0	1	0
23			X													X	1	1	1	0	1	0
24				X					X								0	0	0	1	1	0
25				X						X							1	0	0	1	1	0
26				X							X						0	1	0	1	1	0
27				X								X					1	1	0	1	1	0
28				X									X				0	0	1	1	1	0
29				X										X			1	0	1	1	1	0
30				X											X		0	1	1	1	1	0
31				X												X	1	1	1	1	1	0
32					X				X								0	0	0	0	0	1
33					X					X							1	0	0	0	0	1
34					X						X						0	1	0	0	0	1
35					X							X					1	1	0	0	0	1
36					X								X				0	0	1	0	0	1
37					X									X			1	0	1	0	0	1
38					X										X		0	1	1	0	0	1
39					X											X	1	1	1	0	0	1
40						X			X								0	0	0	1	0	1
41						X				X							1	0	0	1	0	1
42						X					X						0	1	0	1	0	1
43						X						X					1	1	0	1	0	1
44						X							X				0	0	1	1	0	1
45						X								X			1	0	1	1	0	1
46						X									X		0	1	1	1	0	1
47						X										X	1	1	1	1	0	1
48							X		X								0	0	0	0	1	1
49							X			X							1	0	0	0	1	1
50							X				X						0	1	0	0	1	1
51							X					X					1	1	0	0	1	1
52							X						X				0	0	1	0	1	1
53							X							X			1	0	1	0	1	1
54							X								X		0	1	1	0	1	1
55							X									X	1	1	1	0	1	1
56								X	X								0	0	0	1	1	1
57								X		X							1	0	0	1	1	1
58								X			X						0	1	0	1	1	1
59								X				X					1	1	0	1	1	1
60								X					X				0	0	1	1	1	1
61								X						X			1	0	1	1	1	1
62								X							X		0	1	1	1	1	1
63								X								X	1	1	1	1	1	1

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 9 V and T_{amb} = 25 °C

Symbol	Parameter	Pins	Test Conditions		Value Min.	Value Typ.	Value Max.	Unit
I_{DD}	Supply Voltage	M709 Pin 24 M710 Pin 28	V_{DD} = 9 V IR Output Open	Stand–by		5	15	µA
				Operating (one key closed)		4	7	mA
I_{OH}	H State IR Output Current	M709 Pin 23 M710 Pin 27	V_{DD} = 9 V	V_{OH} = 8 V	– 1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OH} = 3.5 V	– 0.3	– 0.5		
I_{OL}	L State IR Output Current	M709 Pin 23 M710 Pin 27	V_{DD} = 9 V	V_{OL} = 1 V	1.5	– 2.5		mA
			V_{DD} = 4.5 V	V_{OL} = 1 V	0.3	0.5		
V_{TH}	Input Threshold High	Selection Inputs A to H	V_{DD} = 9 V				6	V
			V_{DD} = 4.5 V				3	
V_{TL}	Input Threshold Low	Selection Inputs K to Q	V_{DD} = 9 V		3			V
			V_{DD} = 4.5 V		1.5			
I_{IL}	Input Low Current	Pull–up Inputs A to H	V_{DD} = 9 V V_{IL} = 4.5 V		– 60		– 300	µA
I_{IH}	Input High Current	Pull–down Inputs K to Q	V_{DD} = 9 V V_{IH} = 4.5 V		60		300	µA
I_{IH}	Input High Current	Address Selection Inputs	V_{DD} = 9 V V_{IL} = 8.25 V (oscillator running)				150	µA
I_L	Input Leakage Current	Trans. Mode Test Pin	V_{DD} = 9 V V_{IN} = 0 to 9 V				1	µA
I_{OS}	Output Current	Osc. Out.	V_{DD} = 9 V Osc. In. = V_{SS}		– 2		– 8	µA

DESCRIPTION

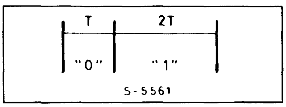
The signals are transmitted with infrared light using pulse code modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses.

If "T" is the time base, the bits are coded as follows :

Odd bits (1, 3, etc)

0 = T

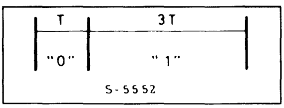
1 = 2T



Even bits (2, 4, etc)

0 = T

1 = 3T



The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected.

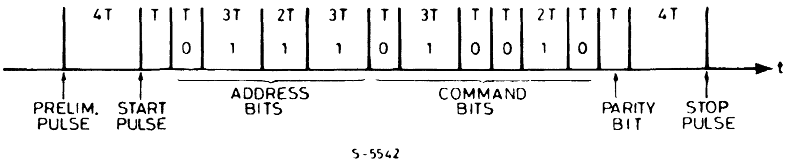
A parity bit is also added in order to further increase the reliability of the transmission. This bits is "1" if the number of transmitted "1s" is even while it is "0" if the number of transmitted "1s" is odd.

In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after 4T interval by a stop pulse.

Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T.

A word containing ten "1s" has a duration of 36T.

Example :



SYNCHRONIZATION BETWEEN TRANSMITTER AND RECEIVER

The transmitter and the receiver can operate with different reference frequencies.

Typical values suitable for correct operation of the system should be between 445 and 510 kHz, using a cheap ceramic resonator.

Synchronization between the transmitter and the receiver, necessary to obtain the wide range of frequency tolerance described above is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

KEYBOARD (pins A to Q) / CODE REPETITION

One column input (K to Q) has to be connected to one row (A to H) input to activate the transmitter.

The contact must be continuously closed for a minimum of 25 ms.

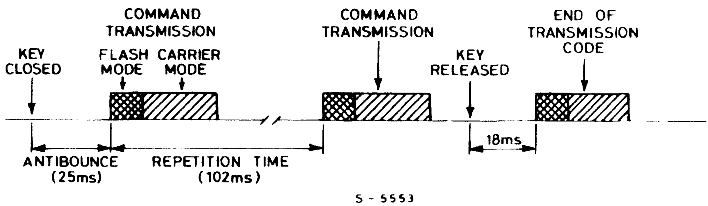
Double and multiple contact operations are not accepted.

The command information is repeatedly transmitted at intervals of 102 ms (f_{ref} = 500 kHz) as long as the push button remains operated.

When the contact is interrupted the circuit transmits, after a pause of about 18 ms, the "end of transmissioncode" and returns ,to stand-by mode.

If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.

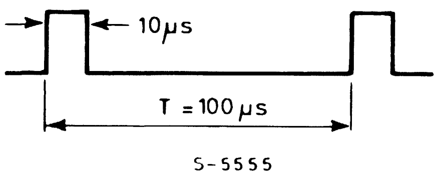
No command is accepted until the "end of transmission code" is over.



TRANSMITION MODE (pin 7)

The M709/M710 can operate in Flash (pin T = V_{DD}) or Carrier (pin T = V_{SS}) transmission modes. Using a reference frequency of 500 kHz the output signal has these formats :

Flash mode



Transmission time

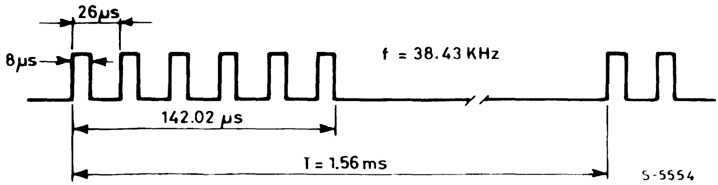
min. = 2.1 ms

max. = 3.6 ms

duty cycle = 0.15 %

Carrier mode

T



ransmission time

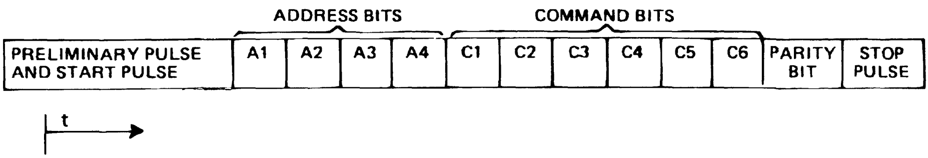
min. = 32.76 ms

max. = 56.16 ms

duty cycle = 0.7 %

ADDRESS (pins X, Y, W, Z)

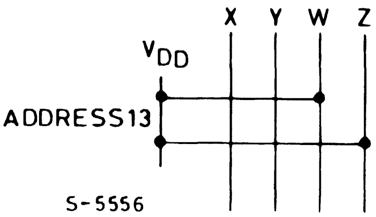
The Address information is coded and transmitted as follows :



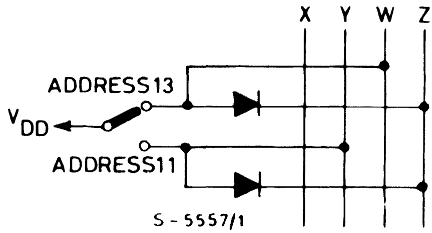
Address Number	Transmitted Code				Address Input Code			
	A1	A2	A3	A4	X	Y	W	Z
1	0	0	0	0	L	L	L	L
2	1	0	0	0	H	L	L	L
3	0	1	0	0	L	H	L	L
4	1	1	0	0	H	H	L	L
5	0	0	1	0	L	L	H	L
6	1	0	1	0	H	L	H	L
7	0	1	1	0	L	H	H	L
8	1	1	1	0	H	H	H	L
9	0	0	0	1	L	L	L	H
10	1	0	0	1	H	L	L	H
11	0	1	0	1	L	H	L	H
12	1	1	0	1	H	H	L	H
13	0	0	1	1	L	L	H	H
14	1	0	1	1	H	L	H	H
15	0	1	1	1	L	H	H	H
16	1	1	1	1	H	H	H	H

The address inputs have internal pull-downs which are disabled during stand-by

Single address selection



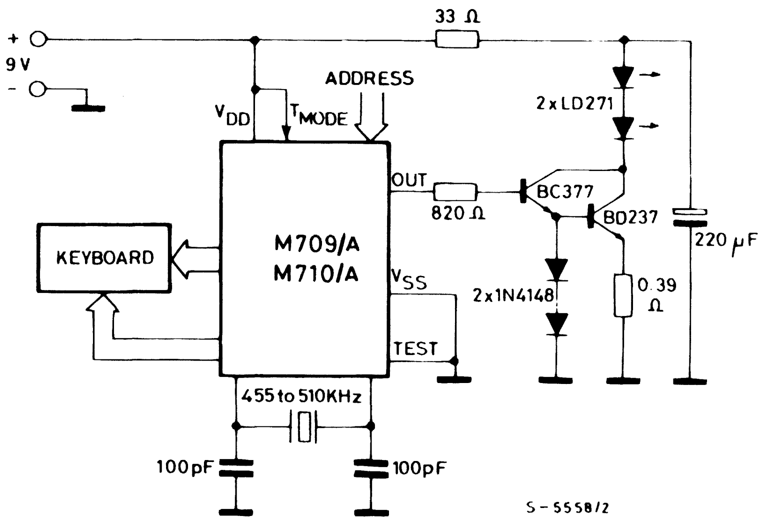
Multiple address selection



Note : unused inputs can be left open or connected to V_{SS}

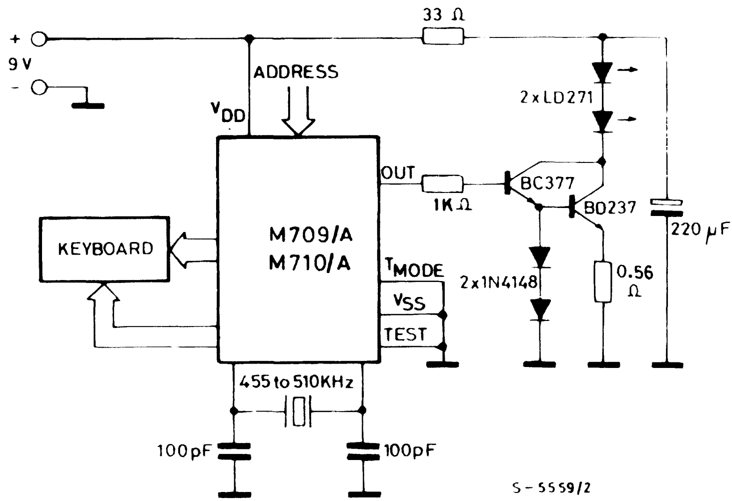
TYPICAL APPLICATIONS

FLASH MODE



INFRARED DIODE PEAK CURRENT = 1.8 A
TOTAL AVERAGE CONSUMPTION = 6.5 mA

CARRIER MODE



INFRARED DIODE PEAK CURRENT = 1.25 A
TOTAL AVERAGE CONSUMPTION = 13 mA

REMOTE CONTROL TRANSMITTER

ADVANCE DATA

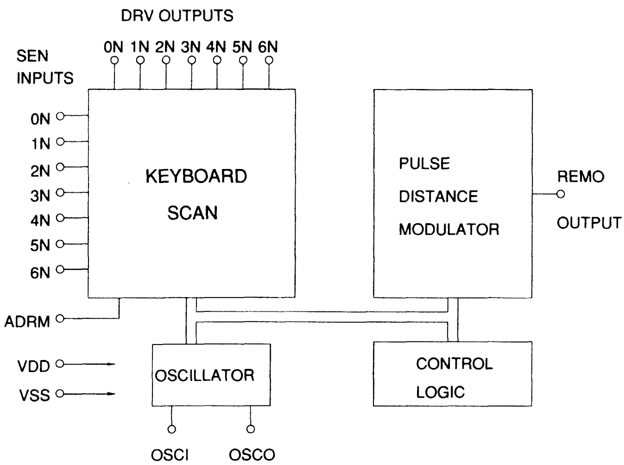
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT VDD = 6V (– IOH = 120mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 12V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 20-LEAD PLASTIC DIL

DESCRIPTION

The M3004AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004AB1 the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmision.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple keystroke sequence.

Table 1: Pulse train Timing.

Mode	T_O ms	t_P µs	t_M µs	t_{ML} µs	t_{MH} µs	t_W ms
Flashed	2.53	8.8	–	–	–	121
Modulated	2.53	–	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	5529 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	$2 \times T_o$
Logic "1"	$3 \times T_o$
Toggle Bit Time	$2 \times T_o$ or $3 \times T_o$
Reference Time	$3 \times T_o$

Table 3 : Transmission mode and sub-system address selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub-system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
M											
O	0	1	1	1							O
D	1	0	0	0	O						O
U	2	0	0	1	X	O					O
L	3	0	1	0	X	X	O				O
A	4	0	1	1	X	X	X	O			O
T	5	1	0	0	X	X	X	X	O		O
E	6	1	0	1	X	X	X	X	X	O	O
D											

O = connected to ADRM
blank = not connected to ADRM
X = don't care.

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
VSS	SEN0N	0	0	0	1	1	1	7
VSS	SEN1N	0	0	1	1	1	1	8 to 15
VSS	SEN2N	0	1	0	1	1	1	16 to 23
VSS	SEN3N	0	1	1	1	1	1	24 to 31
VSS	SEN4N	1	0	0	1	1	1	32 to 39
VSS	SEN5N	1	0	1	1	1	1	40 to 47
VSS	SEN6N	1	1	0	1	1	1	48 to 55
VSS	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDD	Supply Voltage Range	– 0.3 to + 13	V
V_I	Input Voltage Range	– 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	– 0.3 to (V_{DD} + 0.3)	V
± I	D. C. Current into Any Input or Output	Max. 10	mA
– I(REMO)M	Peak REMO Output Current during 10µs ; Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_{amb} = – 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
T_{amb}	Operating Ambient Temperature Range	– 20 to + 70	°C

ELECTRICAL CHARACTERISTICS V_{SS} = 0V ; T_{amb} = 25°C ; unless otherwise specified

Symbol	VDD (V)	Parameter	Min.	Typ.	Max.	Unit
V_{DD} (1)		Supply Voltage T_{amb} = 0 to + 70°C	4		12	V
		Supply Current ;				
I_{DD}	6	Act. f_{OSC} = 455kHz ;		0.4	1	mA
I_{DD}	9	REM0 Outp. Unload.		0.8	2	mA
		Supply Current ;				
IDD	6	Inactive (stand-by mode)			2	µA
IDD	9	T_{amb} = 25°C			2	µA
f_{osc}	4 to 11	Oscill. Frequency (cer. resonator)	350		600	kHz
		Keyboard Matrix				
		Inputs SEN0N to SEN6N				
V_{IL}	4 to 11	Input Voltage LOW			0.2 x VDD	V
V_{IH}	4 to 11	Input Voltage HIGH	0.8 x VDD			V
$-I_I$	4	Input Current	25		250	µA
$-I_I$	11	V_I = 0V	75		750	µA
I_I	11	Input Leakage Current			1	µA
		V_I = VDD				
		Outputs DRV0N to DRV6N				
		Output Volt. "ON"				
V_{OL}	4	I_O = 0.1mA			0.3	V
V_{OL}	11	I_O = 1.0mA			0.5	V
		Outp. Current "OFF"				
I_O	11	V_O = 11V			10	µA
		Control Input ADRM				
V_{IL}		Input Voltage LOW			0.2 x V_{DD}	V
V_{IH}		Input Volt. HIGH	0.8 x V_{DD}			
		Input Current (switched P-and N-channel				V
		pull-up/pull-down)				
I_{IL}	4	Pull-up Act., Oper. Condition ;	25		250	µA
I_{IL}	11	V_{IN} = VSS	75		750	µA
I_{IH}	4	Pull-down Active Standby Cond. ;	25		250	µA
I_{IH}	11	V_{IN} = VDD	75		750	µA
		Data Output REMO				
V_{OH}	6	Output Volt. HIGH	3			V
V_{OH}	9	$-I_{OH}$ = 100mA	6			V
V_{OL}	6	Output Volt. LOW			0.2	V
V_{OL}	9	I_{OL} = 6mA			0.1	V
t_{OH}	6	Pulse Length, Oscill. Stopped			1	msec
		Oscillator				
		Input Current				
I_I	6	OSC1 at V_{DD}	0.8		2.7	µA
		Output Volt. HIGH				
V_{OH}	6	$-I_{OL}$ = 0.1mA			VDD – 0.6	V
		Output Volt. LOW				
V_{OL}	6	I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

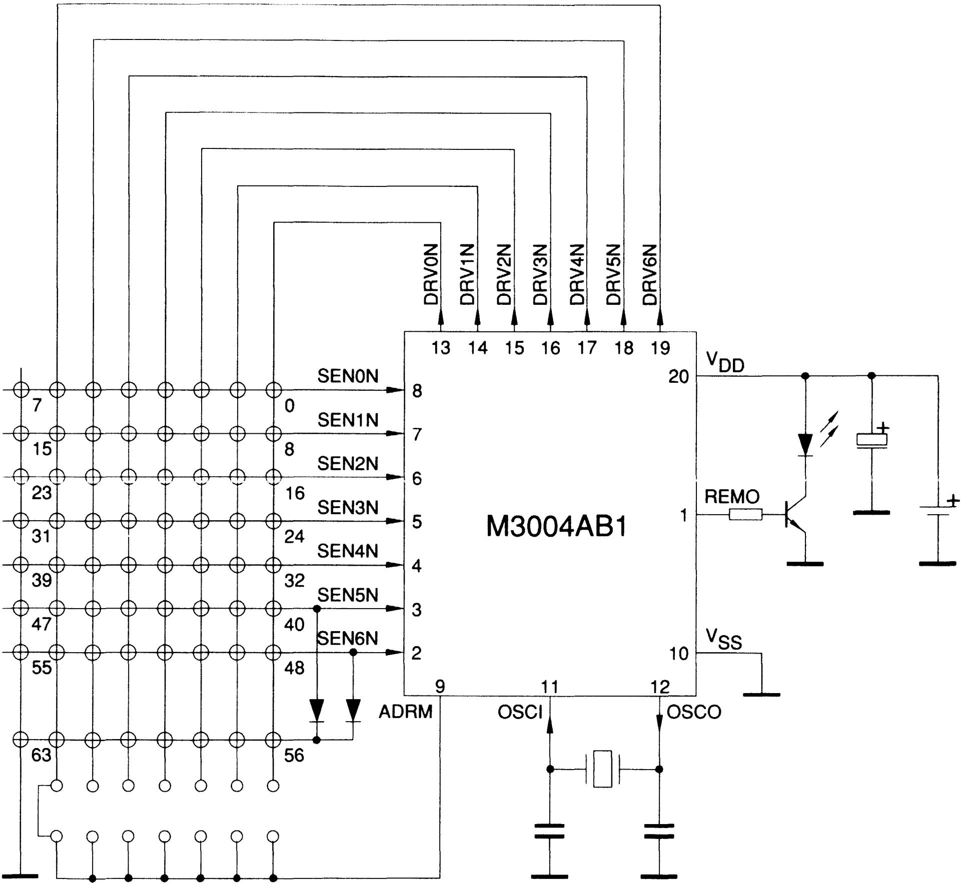


Figure 2 : Data Format of REMO Output ; REF = Reference Time ; T0 and T1 = Toggle bits ; S0, S1 and S2 = system Address ; A, B, C, D, E and F = command bits.

(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed).

(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

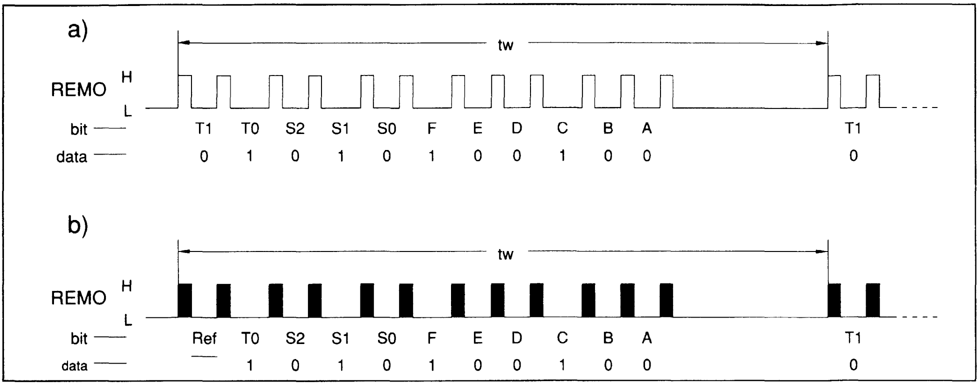


Figure 3 : REMO Output Waveform.

(a) flashed pulse.

(b) modulated pulse $\{t_{PW} = (5 \times t_M) + t_{MH})\}$.

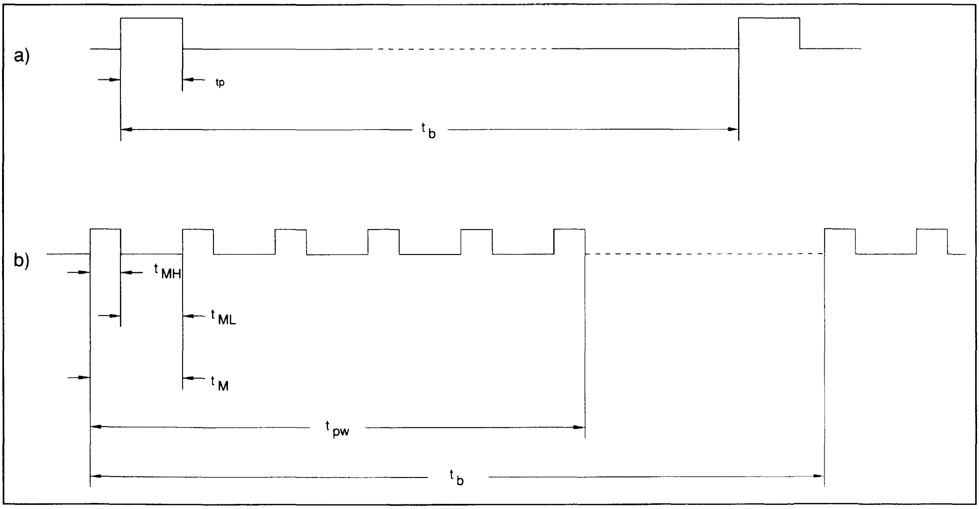


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

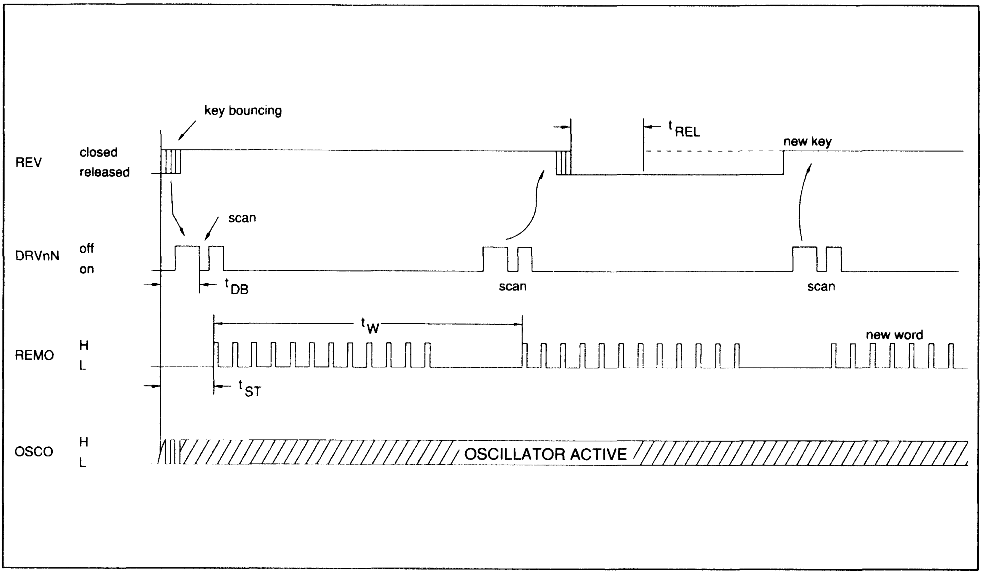
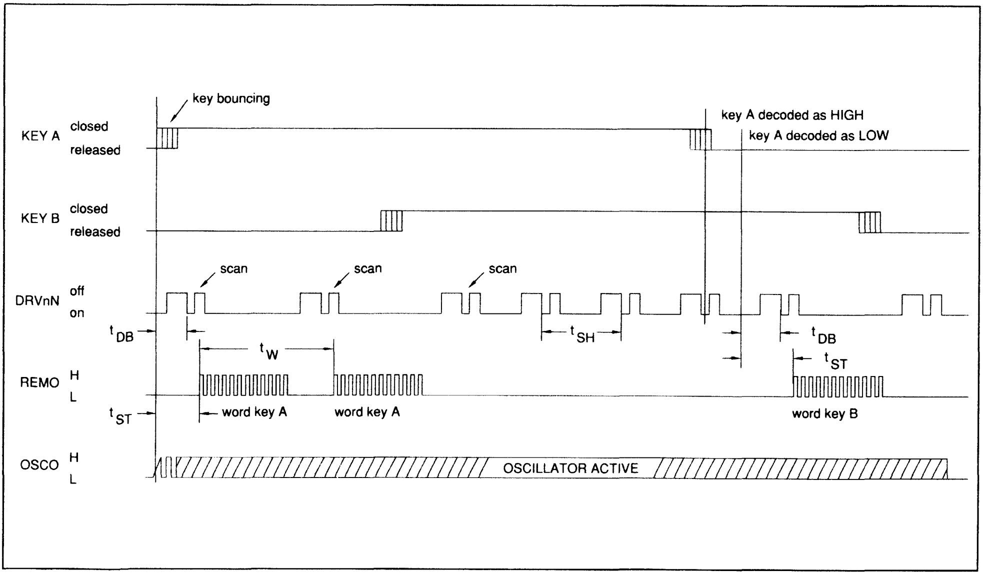


Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O



REMOTE CONTROL TRANSMITTER

ADVANCE DATA

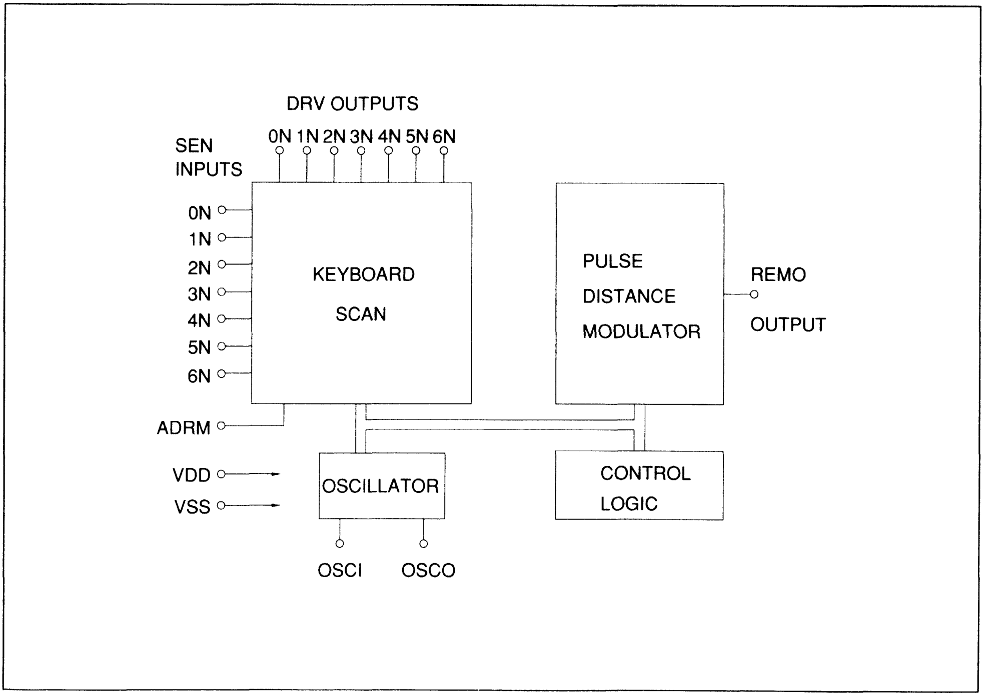
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT V_{DD} = 6V ($-I_{OH}$ = 120mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 20-LEAD PLASTIC DIL

DESCRIPTION

The M3004 LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3004 LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode, only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance t_b between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to V_{SS}). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple key-strokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1: Pulse train Timing.

Mode	T_O ms	t_P µs	t_M µs	t_{ML} µs	t_{MH} µs	t_W ms
Flashed	2.53	8.8	–	–	–	121
Modulated	2.53	–	26.4	17.6	8.8	121

f_{OSC}	455kHz	t_{OSC} = 2.2µs
t_P	4 x t_{OSC}	Flashed Pulse Width
t_M	12 x t_{OSC}	Modulation Period
t_{ML}	8 x t_{OSC}	Modulation Period LOW
t_{MH}	4 x t_{OSC}	Modulation Period HIGH
T_O	1152 x t_{OSC}	Basic Unit of Pulse Distance
t_W	5529 x t_{OSC}	Word Distance

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	$2 \times T_o$
Logic "1"	$3 \times T_o$
Toggle Bit Time	$2 \times T_o$ or $3 \times T_o$
Reference Time	$3 \times T_o$

Table 3 : Transmission mode and sub-system address selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub–system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

O = connected to ADRM
blank = not connected to ADRM
X = don't care.

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
VSS	SEN0N	0	0	0	1	1	1	7
VSS	SEN1N	0	0	1	1	1	1	8 to 15
VSS	SEN2N	0	1	0	1	1	1	16 to 23
VSS	SEN3N	0	1	1	1	1	1	24 to 31
VSS	SEN4N	1	0	0	1	1	1	32 to 39
VSS	SEN5N	1	0	1	1	1	1	40 to 47
VSS	SEN6N	1	1	0	1	1	1	48 to 55
VSS	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage Range	– 0.3 to + 7	V
V_I	Input Voltage Range	– 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range	– 0.3 to (V_{DD} + 0.3)	V
+ I	D. C. Current into Any Input or Output	Max. 10	mA
– I(REMO)M	Peak REMO Output Current during 10µs ; Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_{amb} = – 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	– 55 to + 125	°C
T_{amb}	Operating Ambient Temperature Range	– 20 to + 70	°C

ELECTRICAL CHARACTERISTICS V_{SS} = 0V ; T_{amb} = 25°C ; unless otherwise specified

Symbol	V_{DD}(V)	Parameter	Min.	Typ.	Max.	Unit
V_{DD}		Supply Voltage T_{amb} = 0 to + 70°C	2		6.5	V
I_{DD}	3	Supply Current ; Act. f_{OSC} = 455kHz ; REMO		0.25		mA
I_{DD}	6	Outp. Unload.		1.0		mA
I_{DD}	6	Supply Current ; Inactive (stand-by mode) T_{amb} = 25°C			4	µA
fosc	2 to 6.5	Oscill. Frequency (cer. resonator)	350		600	kHz
		<u>Keyboard Matrix</u>				
		Inputs SEN0N to SEN6N				
V_{IL}	2 to 6.5	Input Voltage LOW			0.3 x V_{DD}	V
V_{IH}	4 to 11	Input Voltage HIGH	0.7 x V_{DD}			V
$-I_I$	2	Input Current	10		100	µA
$-I_I$	6.5	V_I = 0V	100		600	µA
I_I	6.5	Input Leakage Current			1	µA
		V_I = V_{DD}				
		<u>Outputs DRV0N to DRV6N</u>				
		Output Volt. "ON"				
V_{OL}	2	I_O = 0.1mA			0.3	V
V_{OL}	6.5	I_O = 1.0mA			0.6	V
		Outp. Current "OFF"				
I_O	6.5	V_O = 11V			10	µA
		<u>Control Input ADRM</u>				
V_{IL}		Input Voltage LOW			0.3 x V_{DD}	V
V_{IH}		Input Volt. HIGH	0.7 x V_{DD}			
		Input Current (switched P-and N-channel				V
		pull-up/pull-down)				
I_{IL}	2	Pull-up Act., Oper. Condition ;	10		100	µA
I_{IL}	6.5	V_{IN} = V_{SS}	100		600	µA
I_{IH}	2	Pull-down Active Standby Cond. ;	10		100	µA
I_{IH}	6.5	V_{IN} = V_{DD}	100		600	µA
		<u>Data Output REMO</u>				
V_{OH}	2	Output Volt. HIGH	0.8			
V_{OH}	6.5	$-I_{OH}$ = 40mA	5.0			V
V_{OL}	2	Output Volt. LOW			0.4	V
V_{OL}	6.5	I_{OL} = 0.3mA			0.4	V
t_{OH}	6.5	Pulse Length, Oscill. Stopped			1	ms
		<u>Oscillator</u>				
I_I	2	Input Current			5.0	µA
I_I	6.5	OSC1 at V_{DD}	5.0		7.0	µA
		Output Volt. HIGH				
V_{OH}	6.5	$-I_{OL}$ = 0.1mA	V_{DD} – 0.8			V
		Output Volt. LOW				
V_{OL}	6.5	I_{OH} = 0.1mA			0.7	V

Figure 1 : Typical Application.

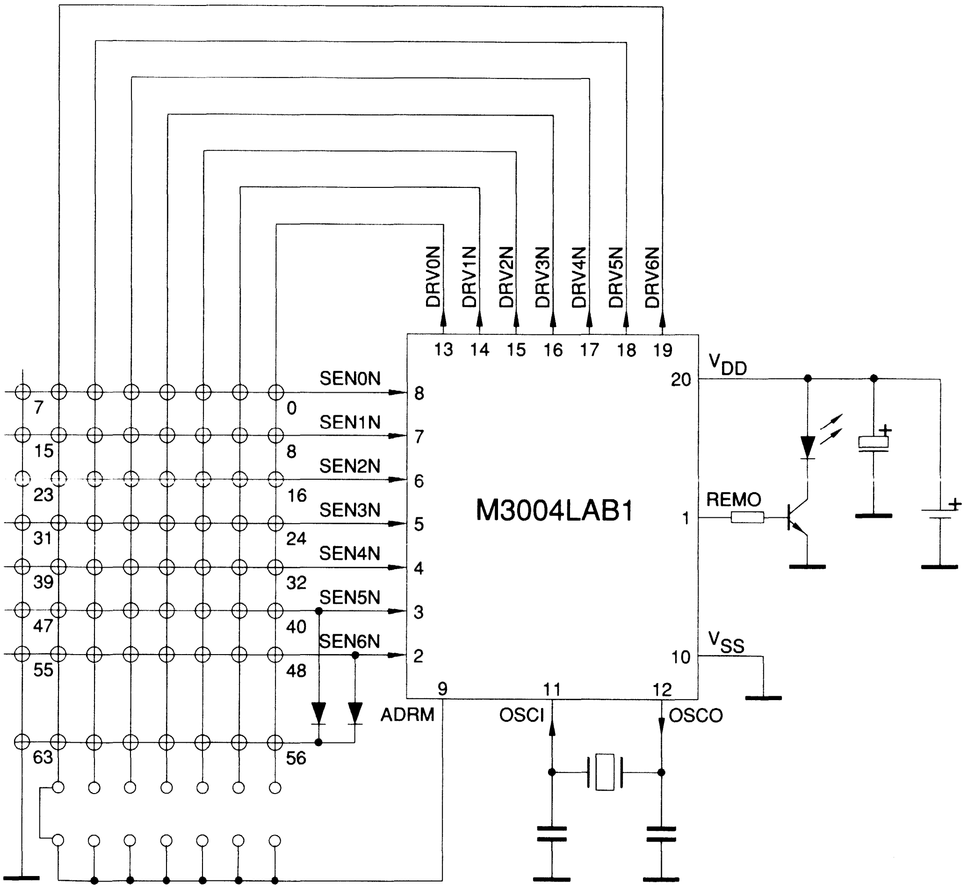


Figure 2 : Data Format of REMO Output ; REF = Reference Time ; T0 and T1 = Toggle bits ; S0, S1 and S2 = system Address ; A, B, C, D, E and F = command bits.

(a) flashed mode : transmission with 2 toggle bits and 3 address bits, followed by 6 command bits (pulses are flashed)

(b) modulated mode : transmission with reference time, 1 toggle bit and 3 address bits, followed by 6 command bits (pulses are modulated).

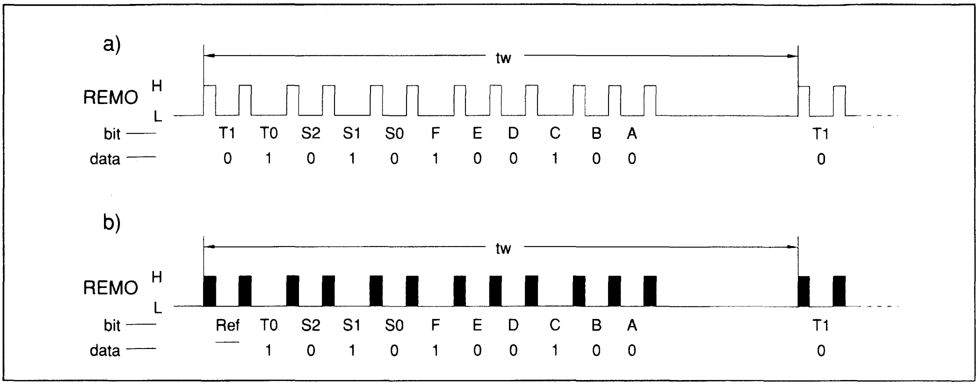


Figure 3 : REMO Output Waveform.

(a) flashed pulse.

(b) modulated pulse $\{t_{PW} = (5 \times t_M) + t_{MH})\}$

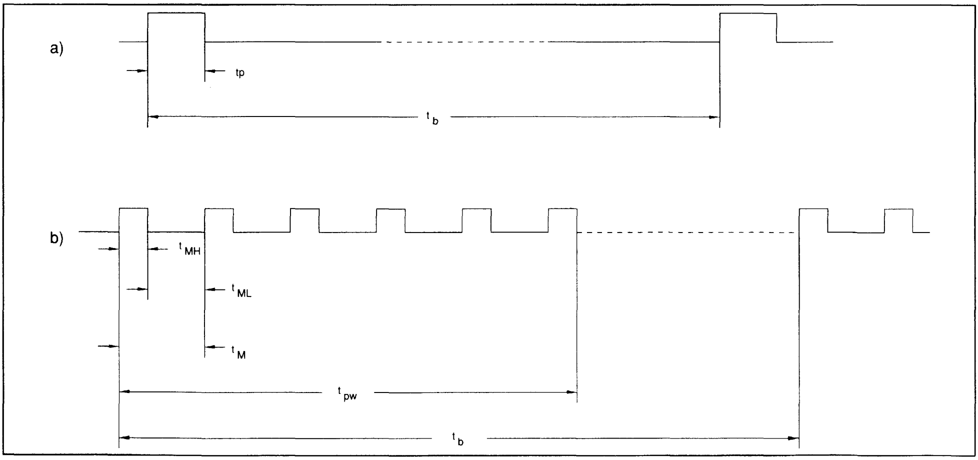


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

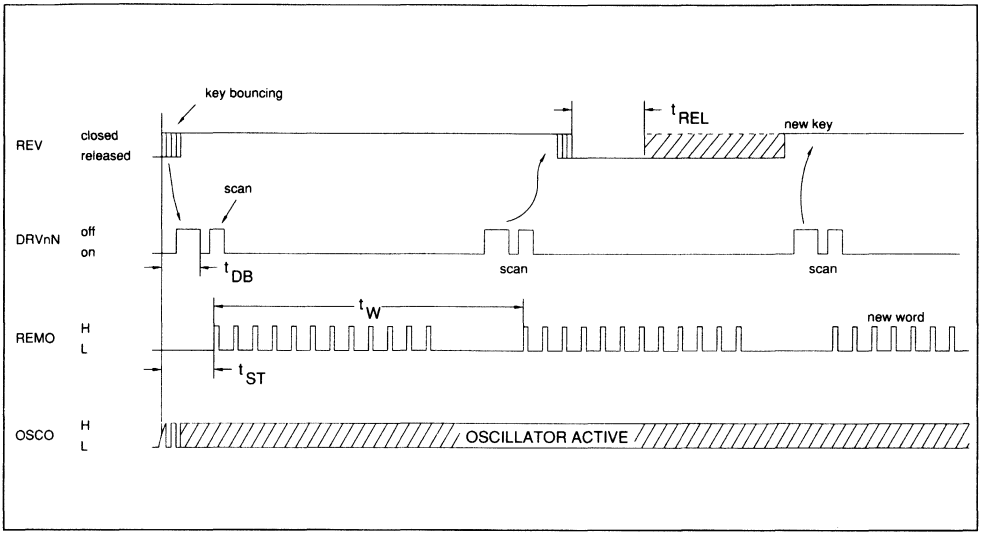
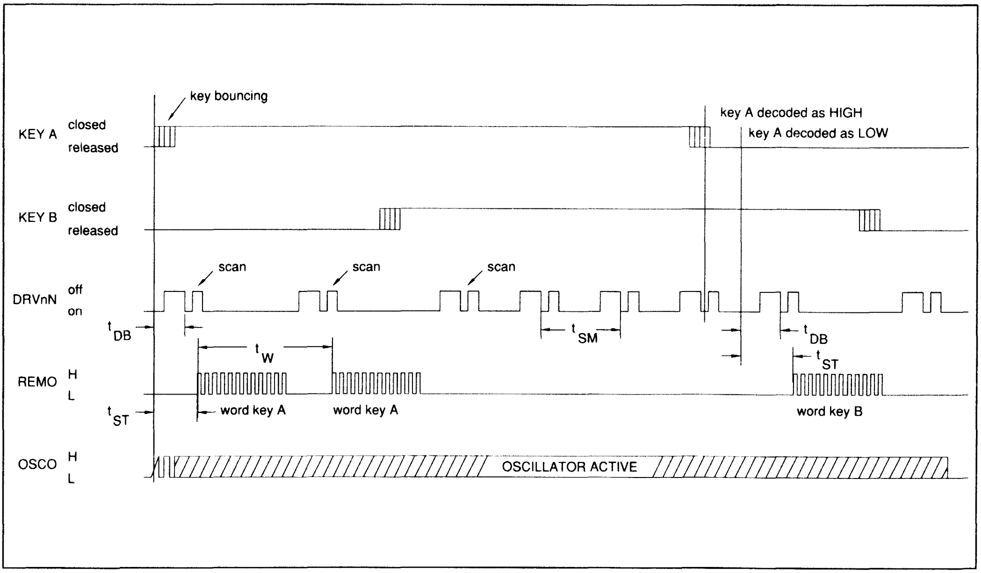


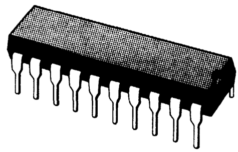
Figure 5 : Multiple Key-Stroke Sequence.
Scan rate multiple key-stroke : t_{SM} = 8 to 10 x T_O.



REMOTE CONTROL TRANSMITTER

ADVANCE DATA

- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT VDD = 6V ($-I_{OH}$ = 100mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 4 TO 12V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 20-LEAD PLASTIC DIL



DIP20
(Plastic Package)

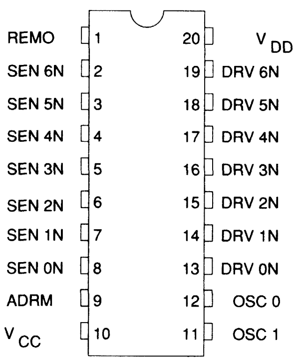
ORDER CODE : M3005AB1

DESCRIPTION

The M3005 AB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

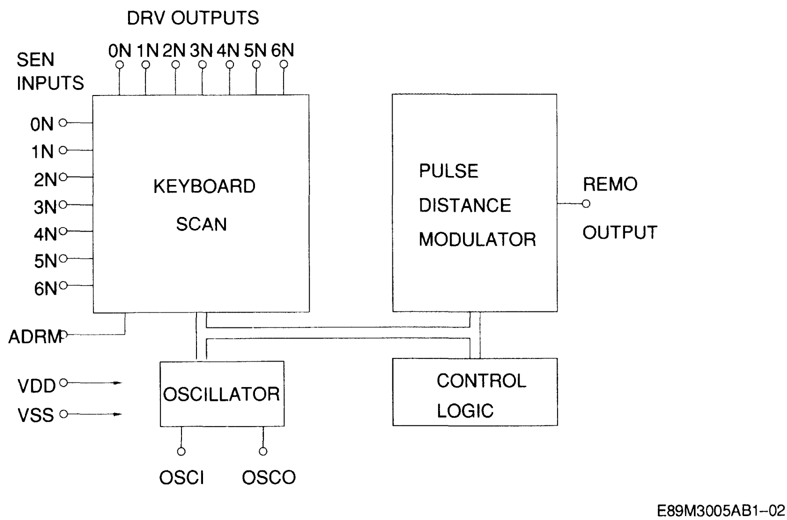
The M3005 AB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

PIN CONNECTIONS



E89M3005AB1-01

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRVON to DRV6N and SENON to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRVON to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SENON to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRVON to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance tb between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO-output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

Keyboard operation.

In the stand-by mode all drivers (DRVON to DRV6N) are on (low impedance to VSS). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time tDB (see fig. 4) the output drivers (DRVON to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time tREL (see fig. 4). The toggle bits remain unchanged within a multiple key-stroke sequence.

Table 1: Pulse Train Timing.

Mode	T_O ms	t_P µs	t_M µs	t_W ms
Flashed	2.53	8.8	–	121
Modulated	2.53	–	t_{OSC}	121

	Flash Mode	Carrier Mode	
t_{OSC}	455kHz	600kHz	
t_P	4 x t_{OSC}	–	Flashed Pulse Width
t_M	–	t_{OSC}	Modulation Period
N	–	8*	Number od Modulation Pulses
T_O	1152 x t_{OSC}	1536 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	73728 x t_{OSC}	Word Distance

The following number of pulses may be selected by Metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_o and t_w between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of a 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_o and t_W. For first samples, the correct divider ratio is obtained by a metal mask option. For final parts, this is automatically done together with the selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_o
Logic "1"	3 x T_o
Toggle Bit Time	2 x T_o or 3 x T_o

Table 3 : Transmission mode and sub-system address selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRVON to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub–system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
FLASHED	0	1	1	1							
	1	0	0	0	O						
	2	0	0	1	X	O					
	3	0	1	0	X	X	O				
	4	0	1	1	X	X	X	O			
	5	1	0	0	X	X	X	X	O		
	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

0 = connected to ADRM
blank. = not connected to ADRM
X = don't care.

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
VSS	SEN0N	0	0	0	1	1	1	7
VSS	SEN1N	0	0	1	1	1	1	8 to 15
VSS	SEN2N	0	1	0	1	1	1	16 to 23
VSS	SEN3N	0	1	1	1	1	1	24 to 31
VSS	SEN4N	1	0	0	1	1	1	32 to 39
VSS	SEN5N	1	0	1	1	1	1	40 to 47
VSS	SEN6N	1	1	0	1	1	1	48 to 55
VSS	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VDD	Supply Voltage Range	– 0.3 to + 13	V
V_I	Input Voltage Range	– 0.3 to VDD + 0.3	V
V_O	Output Voltage Range	– 0.3 to VDD + 0.3	V
± I	D. C. Current into Any Input or Output	Max. 10	mA
– I(REMO)M	Peak REMO Output Current during 10µs ; Duty Factor = 1%	Max. 300	mA
P_{tot}	Power Dissipation per Package for T_{amb} = – 20 to + 70°C	Max. 200	mW
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
T_{amb}	Operating Ambient Temperature Range	– 20 to + 70	°C

ELECTRICAL CHARACTERISTICS VSS = 0V ; T_{amb} = 25°C ; unless otherwise specified

Symbol	VDD(V)	Parameter	Min.	Typ.	Max.	Unit
VDD		Supply Voltage T_{amb} = 0 to + 70°C	4		12	V
IDD IDD	6 9	Supply Current ; Act. f_{OSC} = 455kHz ; REM0 Outp. Unload.		0.4 0.8	1 2	mA mA
IDD IDD	6 9	Supply Current ; Inactive (stand-by mode) T_{amb} = 25°C			2 2	µA µA
fosc	4 to 11	Oscill. Frequency (cer. resonator)	350		600	kHz
		Keyboard Matrix Inputs SENON to SEN6N				
V_{IL}	4 to 11	Input Voltage LOW			0.2 x VDD	V
V_{IH}	4 to 11	Input Voltage HIGH	0.8 x VDD			V
$-I_I$	4	Input Current	25		250	µA
$-I_I$	11	V_I = 0V	75		750	µA
I_I	11	Input Leakage Current V_I = VDD			1	µA
		Outputs DRVON to DRV6N Output Volt. "ON"				
V_{OL}	4	I_O = 0.25mA			0.3	V
V_{OL}	11	I_O = 22.5mA			0.5	V
I_O	11	Outp. Current "OFF" V_O = 11V			10	µA
		Control Input ADRM				
V_{IL}		Input Voltage LOW			0.2 x VDD	V
V_{IH}		Input Volt. HIGH	0.8 x VDD			V
		Input Current (switched P-and N-channel pull-up/pull-down)				
I_{IL}	4	Pull-up Act., Oper. Condition ;	25		250	µA
I_{IL}	11	V_{IN} = VSS	75		750	µA
I_{IH}	4	Pull-down Active Standby Cond. ;	25		250	µA
I_{IH}	11	V_{IN} = VDD	75		750	µA
		Data Output REMO				
V_{OH}	6	Output Volt. HIGH	3			V
V_{OH}	9	$-I_OH$ = 100mA	6			V
V_{OL}	6	Output Volt. LOW			0.2	V
V_{OL}	9	I_{OL} = 0.6 mA			0.1	V
t_{MH}/t_{OSC}	6	Pulse Duty Cycle During Carrier Mode	0.4	0.5	0.6	
t_{OH}	6	Pulse Length, Oscill. Stopped			1	ms
		Oscillator				
I_I	6	Input Current OSC1 at VDD	0.8		2.7	µA
V_{OH}	6	Output Volt. HIGH $-I_{OL}$ = 0.1mA			VDD – 0.6	V
V_{OL}	6	Output Volt. LOW I_{OH} = 0.1mA			0.6	V

Figure 1 : Typical Application.

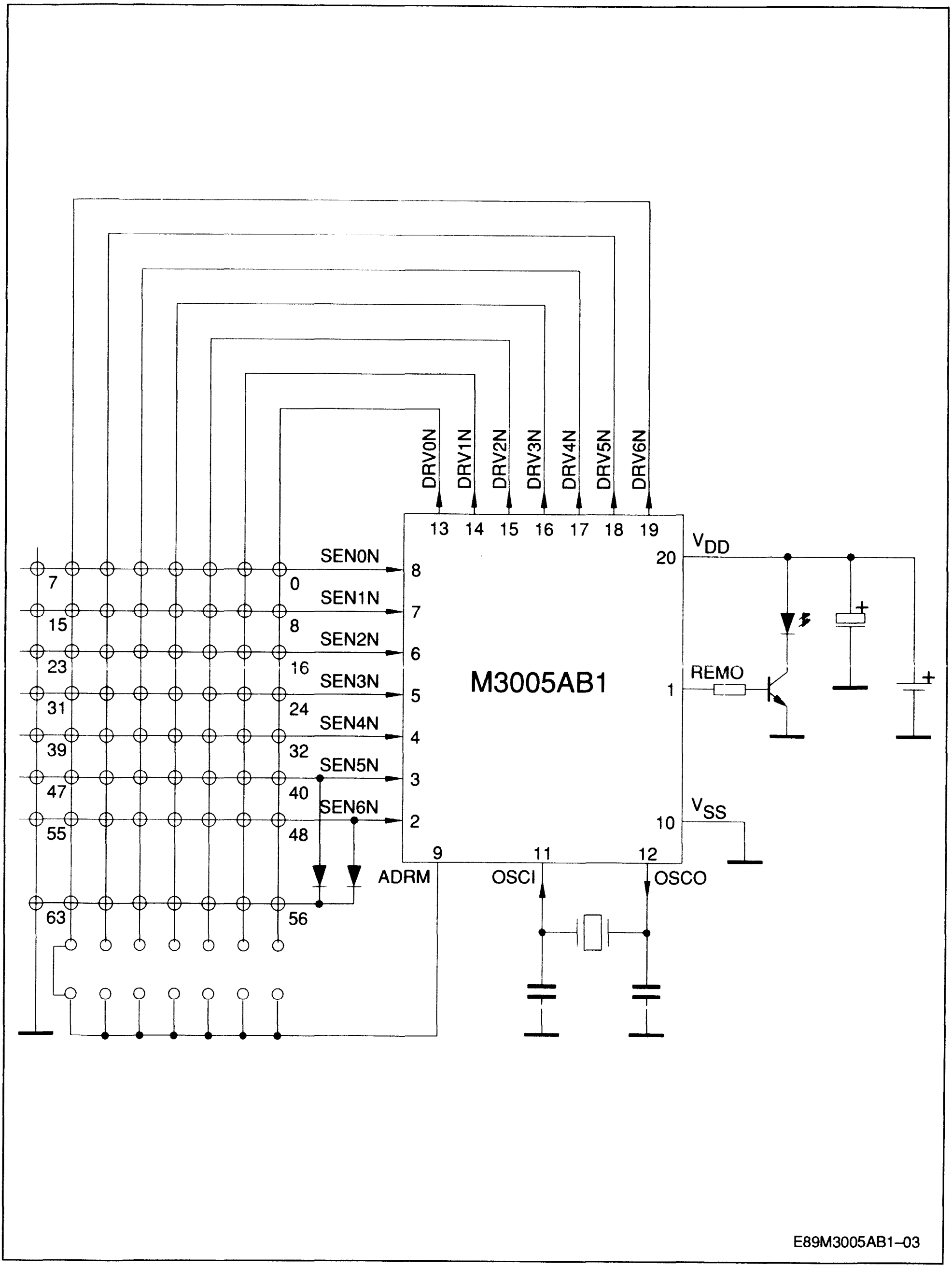


Figure 2 : Data Format of REMO Output.

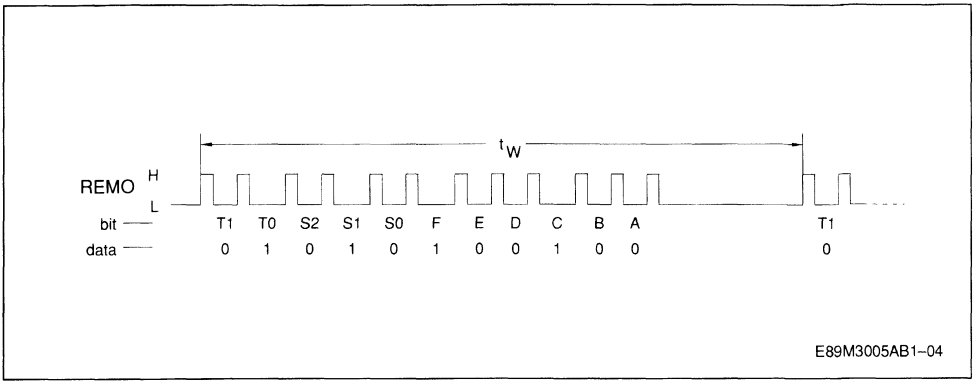


Figure 3 : REMO Output Waveform.
(a) flashed pulse.
(b) modulated pulse

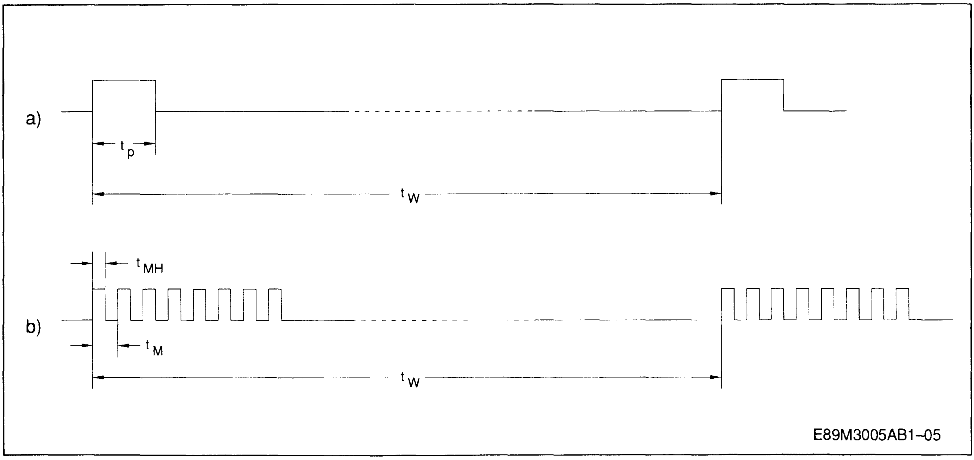


Figure 4 : Single Key - Stroke Sequence.
Debounce time : t_{DB} = 4 to 9 x T_O
Start time : t_{ST} = 5 to 10 x T_O
Minimum release time : t_{REL} = T_O.

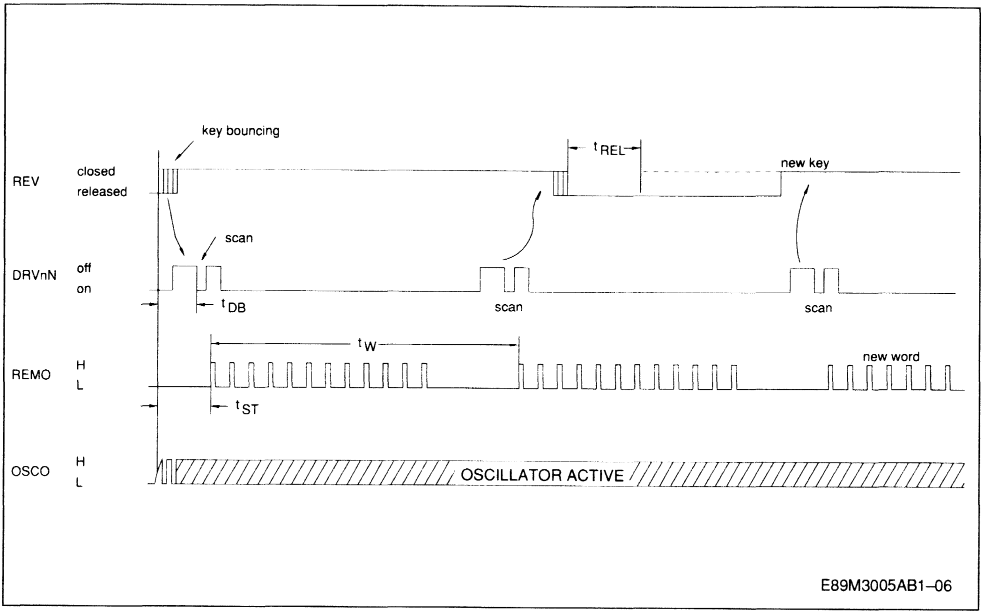
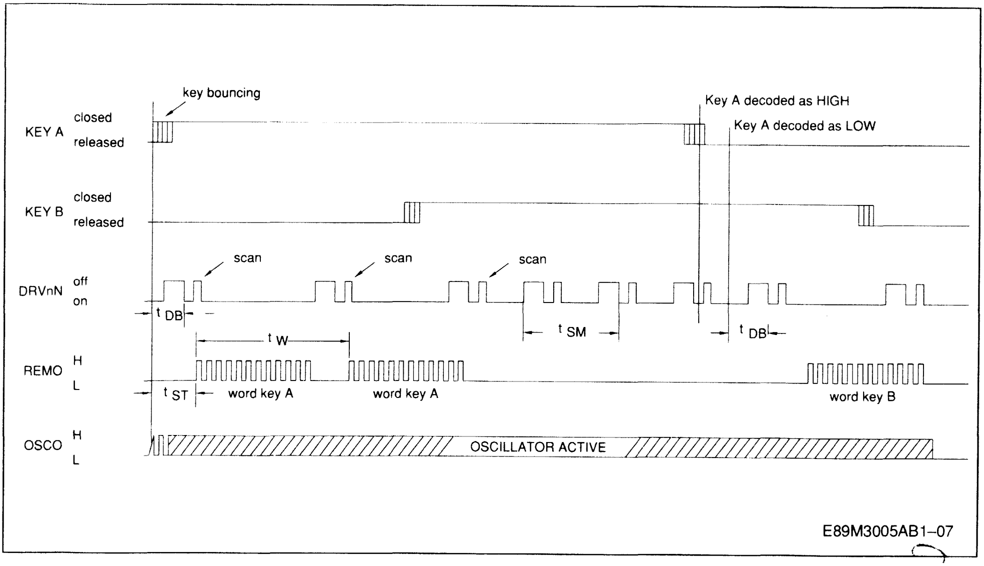
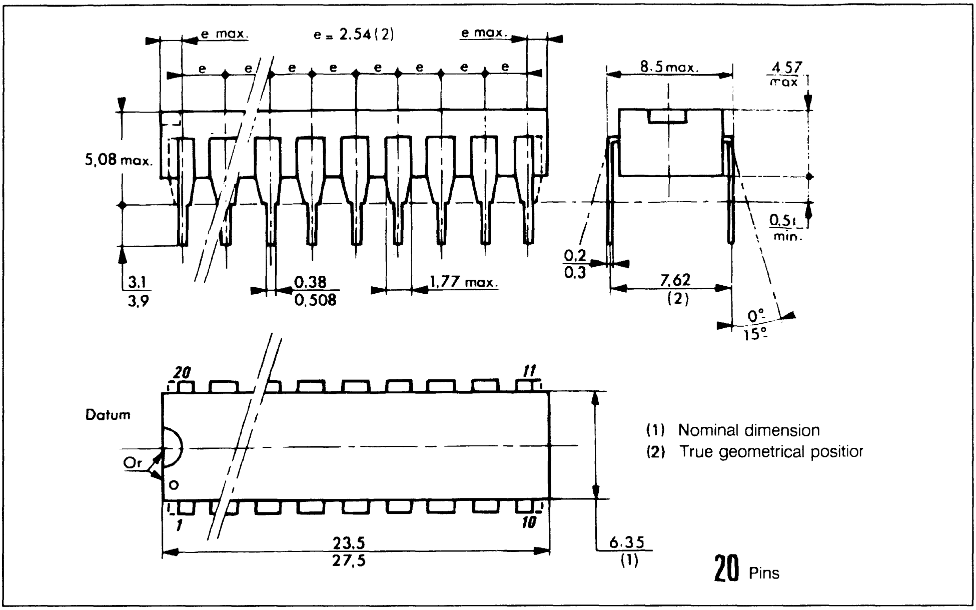


Figure 5 : Key - Stroke Sequence
Multiple Key-stroke : t_{SM} = 8 to 10 x T_O.



PACKAGE MECHANICAL DATA

20 PINS – PLASTIC DIP



MONOLITHIC MICROSYSTEMS DIVISION

ADVANCE DATA

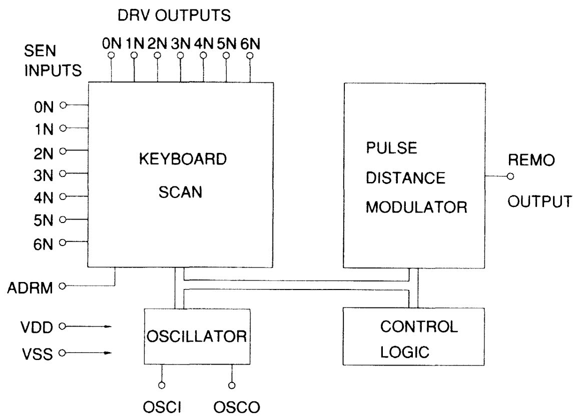
- FLASHED OR MODULATED TRANSMISSION
- 7 SUB-SYSTEM ADDRESSES
- UP TO 64 COMMANDS PER SUB-SYSTEM ADDRESS
- HIGH-CURRENT REMOTE OUTPUT AT VDD = 6V ($-I_{OH}$ = 40mA)
- LOW NUMBER OF ADDITIONAL COMPONENTS
- KEY RELEASE DETECTION BY TOGGLE BITS
- VERY LOW STAND-BY CURRENT (< 2μA)
- OPERATIONAL CURRENT < 1mA AT 6V SUPPLY
- SUPPLY VOLTAGE RANGE 2 TO 6.5V
- CERAMIC RESONATOR CONTROLLED FREQUENCY (typ. 450kHz)
- ENCAPSULATION : 20-LEAD PLASTIC DIL

REMOTE CONTROL TRANSMITTER

The M3005LAB1 transmitter IC is designed for infrared remote control systems. It has a total of 448 commands which are divided into 7 sub-system groups with 64 commands each. The sub-system code may be selected by a press button, a slider switch or hard wired.

The M3005LAB1 generates the pattern for driving the output stage. These patterns are pulse distance coded. The pulses are infrared flashes or modulated. The transmission mode is defined in conjunction with the sub-system address. Modulated pulses allow receivers with narrow-band preamplifiers for improved noise rejection to be used. Flashed pulses require a wide-band preamplifier within the receiver.

BLOCK DIAGRAM



INPUTS AND OUTPUTS

Key matrix inputs and outputs (DRV0N to DRV6N and SEN0N to SEN6N).

The transmitter keyboard is arranged as a scanned matrix. The matrix consists of 7 driver outputs and 7 sense inputs as shown in fig. 1. The driver outputs DRV0N to DRV6N are open drain N-channel transistors and they are conductive in the stand-by mode. The 7 sense inputs (SEN0N to SEN6N) enable the generation of 56 command codes. With 2 external diodes all 64 commands are addressable. The sense inputs have P-channel pull-up transistors so that they are HIGH until they are pulled LOW by connecting them to an output via a key depression to initiate a code transmission.

ADDRESS MODE INPUT (ADRM)

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes. This allows the definition of seven sub-system addresses as shown in table 3. If driver DRV6N is connected to ADRM, the data output format of REMO is modulated or if not connected, flashed.

The ADRM input has switched pull-up and pull-down loads. In the stand-by mode only the pull-down device is active. Whether ADRM is open (sub-system address 0, flashed mode) or connected to the driver outputs, this input is LOW and will not cause unwanted dissipation. When the transmitter becomes active by pressing a key, the pull-down device is switched off and the pull-up device is switched on, so that the applied driver signals are sensed for the decoding of the sub-system address and the mode of transmission.

The arrangement of the sub-system address coding is such that only the driver DRVnM with the highest number (n) defines the sub-system address, e.g. if drivers DRV2N and DRV4N are connected to ADRM, only DRV4N will define the sub-system address. This option can be used in systems requiring more than one sub-system address. The transmitter may be hard-wired for sub-system address 2 by connecting DRV1N to ADRM. If now DRV3N is added to ADRM by a key or a switch, the transmitted sub-system address changes to 4. A change of the sub-system address will not start a transmission.

REMOTE CONTROL SIGNAL OUTPUT (REMO)

The REMO signal output stage is a push-pull type. In the HIGH state, a bipolar emitter-follower allows a high output current. The timing of the data output format is listed in tables 1 and 2. The information is defined by the distance tb between the leading edges of the flashed pulses or the first edge of the modulated pulses (see fig. 3). The format of the output data is given in fig. 2 and 3. The data word starts with two toggle bits T1 and T0, followed by three bits for defining the sub-system address S2, S1 and S0, and six bits F, E, D, C, B and A which are defined by the selected key.

In the modulated transmission mode the first toggle bit is replaced by a constant reference time bit (REF). This can be used as a reference time for the decoding sequence. The toggle bits function as an indication for the decoder that the next instruction has to be considered as a new command. The codes for the sub-system address and the selected key are given in tables 3 and 4.

The REMO-output is protected against "Lock-up", i.e. the length of an output pulse is limited to < 1msec, even if the oscillator stops during an output pulse. This avoids the rapid discharge of the battery that would otherwise be caused by the continuous activation of the LED.

OSCILLATOR INPUT/OUTPUT (osci and osco)

The external components must be connected to these pins when using an oscillator with a ceramic resonator. The oscillator frequency may vary between 350kHz and 600kHz as defined by the resonator.

FUNCTIONAL DESCRIPTION

KEYBOARD OPERATION

In the stand-by mode all drivers (DRV0N to DRV6N) are on (low impedance to VSS). Whenever a key is pressed, one or more of the sense inputs (SENnN) are tied to ground. This will start the power-up sequence. First the oscillator is activated and after the debounce time t_{DB} (see fig. 4) the output drivers (DRV0N to DRV6N) become active successively).

Within the first scan cycle the transmission mode, the applied sub-system address and the selected command code are sensed and loaded into an internal data latch.

In contrast to the command code, the sub-system is sensed only within the first scan cycle. If the applied sub-system address is changed while the command key is pressed, the transmitted sub-system address is not altered.

In a multiple key stroke sequence (see fig. 5) the command code is always altered in accordance with the sensed key.

MULTIPLE KEY-STROKE PROTECTION

The keyboard is protected against multiple keystrokes. If more than one key is pressed at the same time, the circuit will not generate a new output at REMO (see fig. 5). In case of a multiple key-stroke, the scan repetition rate is increased to detect the release of a key as soon as possible.

There are two restrictions caused by the special structure of the keyboard matrix :

- The keys switching to ground (code numbers 7, 15, 23, 31, 39, 47, 55 and 63) and the keys connected to SEN5N and SEN6N are not covered completely by the multiple key protection. If one sense input is switched to ground, further keys on the same sense line are ignored, i.e. the command code corresponding to "key to ground" is transmitted.
- SEN5N and SEN6N are not protected against multiple keystroke on the same driver line, because this condition has been used for the definition of additional codes (code number 56 to 63).

OUTPUT SEQUENCE (data format)

The output operation will start when the selected code is found. A burst of pulses, including the latched address and command codes, is generated at the output REMO as long as a key is pressed. The format of the output pulse train is given in fig. 2 and 3. The operation is terminated by releasing the key or if more than one key is pressed at the same time. Once a sequence is started, the transmitted data words will always be completed after the key is released.

The toggle bits T0 and T1 are incremented if the key is released for a minimum time t_{REL} (see fig. 4). The toggle bits remain unchanged within a multiple keystroke sequence.

Table 1: Pulse Train Timing.

Mode	T_O ms	t_P µs	t_M µs	t_W ms
Flashed	2.53	8.8	–	121
Modulated	2.53	–	tosc	121

	Flash Mode	Carrier Mode	
t_{OSC}	455kHz	600kHz	
t_P	4 x t_{OSC}	–	Flashed Pulse Width
t_M	–	t_{OSC}	Modulation Period
N	–	8*	Number od Modulation Pulses
To	1152 x t_{OSC}	1536 x t_{OSC}	Basic Unit of Pulse Distance
t_W	55296 x t_{OSC}	73728 x t_{OSC}	Word Distance

* The following number of pulses may be selected by metal option : N = 8, 12, 16.

Note : The different dividing ratio for T_O and t_W between flash mode and carrier mode is obtained by changing the modulo of a particular divider from divide by 3 during flash mode to divide by 4 during carrier mode. This allows the use of 600kHz ceramic resonator during carrier mode to obtain a better noise immunity for the receiver without a significant change in T_O and t_W. For first samples, the correct divider ratio is obtained by a metal mask option. For final parts, this is automatically done together with selection of flash-/carrier mode.

Table 2 : Pulse Train Separation (t_b).

Code	t_b
Logic "0"	2 x T_o
Logic "1"	3 x T_o
Toggle Bit Time	2 x T_o or 3 x T_o

Table 3 : Transmission Mode and Sub-system Address Selection.

The sub-system address and the transmission mode are defined by connecting the ADRM input to one or more driver outputs (DRV0N to DRV6N) of the key matrix. If more than one driver is connected to ADRM, they must be decoupled by diodes.

Mode	Sub–system Address				Driver DRVnN for n =						
	#	S2	S1	S0	0	1	2	3	4	5	6
F	0	1	1	1							
L	1	0	0	0	O						
A	2	0	0	1	X	O					
S	3	0	1	0	X	X	O				
H	4	0	1	1	X	X	X	O			
E	5	1	0	0	X	X	X	X	O		
D	6	1	0	1	X	X	X	X	X	O	
MODULATED	0	1	1	1							O
	1	0	0	0	O						O
	2	0	0	1	X	O					O
	3	0	1	0	X	X	O				O
	4	0	1	1	X	X	X	O			O
	5	1	0	0	X	X	X	X	O		O
	6	1	0	1	X	X	X	X	X	O	O

O = connected to ADRM.
blank = not connected to ADRM.
X = don't care.

Table 4 : Key Codes.

Matrix Drive	Matrix Sense	Code						Matrix Position
		F	E	D	C	B	A	
DRV0N	SEN0N	0	0	0	0	0	0	0
DRV1N	SEN0N	0	0	0	0	0	1	1
DRV2N	SEN0N	0	0	0	0	1	0	2
DRV3N	SEN0N	0	0	0	0	1	1	3
DRV4N	SEN0N	0	0	0	1	0	0	4
DRV5N	SEN0N	0	0	0	1	0	1	5
DRV6N	SEN0N	0	0	0	1	1	0	6
VSS	SEN0N	0	0	0	1	1	1	7
VSS	SEN1N	0	0	1	1	1	1	8 to 15
VSS	SEN2N	0	1	0	1	1	1	16 to 23
VSS	SEN3N	0	1	1	1	1	1	24 to 31
VSS	SEN4N	1	0	0	1	1	1	32 to 39
VSS	SEN5N	1	0	1	1	1	1	40 to 47
VSS	SEN6N	1	1	0	1	1	1	48 to 55
VSS	SEN5N and SEN6N	1	1	1	1	1	1	56 to 63

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the absolute maximum system (IEC 134).

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage Range		– 0.3 to + 7	V
V_I	Input Voltage Range		– 0.3 to (V_{DD} + 0.3)	V
V_O	Output Voltage Range		– 0.3 to (V_{DD} + 0.3)	V
± I	D.C. Current into Any Input or Output	Max.	10	mA
– I(REMO)M	Peak REMO Output Current during 10µs ; Duty Factor = 1%	Max.	300	mA
P_{tot}	Power Dissipation per Package for T_{amb} = – 20 to + 70°C	Max.	200	mW
T_{stg}	Storage Temperature Range		– 55 to + 125	°C
T_{amb}	Operating Ambient Temperature Range		– 20 to + 70	°C

ELECTRICAL CHARACTERISTICS V_{SS} = 0V ; T_{amb} = 25°C ; unless otherwise specified

Symbol	V_{DD}(V)	Parameter	Min.	Typ.	Max.	Unit
V_{DD}		Supply Voltage T_{amb} = 0 to + 70°C	2		6.5	V
		Supply Current ;				
I_{DD}	3	Act. f_{OSC} = 455kHz ;		0.25		mA
I_{DD}	6	REMO Outp. Unload.		1.0		mA
		Supply Current ; Inactive (stand-by mode)				
I_{DD}	6	T_{amb} = 25°C			4	µA
f_{osc}	2 to 6.5	Oscill. Frequency (cer. resonator)	350		600	kHz
		Keyboard Matrix				
		Inputs SEN0N to SEN6N				
V_{IL}	2 to 6.5	Input Voltage LOW			0.3 x V_{DD}	V
V_{IH}	2 to 6.5	Input Voltage HIGH	0.7 x V_{DD}			V
$-I_I$	2	Input Current	10		100	µA
$-I_I$	6.5	V_I = 0V	100		600	µA
I_I	6.5	Input Leakage Current			1	µA
		V_I = V_{DD}				
		Outputs DRV0N to DRV6N				
		Output Volt. "ON"				
V_{OL}	2	I_O = 0.25mA			0.3	V
V_{OL}	6.5	I_O = 2.5mA			0.6	V
		Outp. Current "OFF"				
I_O	6.5	V_O = 11V			10	µA
		Control Input ADRM				
V_{IL}		Input Voltage LOW			0.3 x V_{DD}	V
V_{IH}		Input Volt. HIGH	0.7 x V_{DD}			V
		Input Current (switched P-and N-channel pull-up/pull-down)				
I_{IL}	2	Pull-up Act., Oper. Condition ;	10		100	µA
I_{IL}	6.5	V_{IN} = V_{SS}	100		600	µA
I_{IH}	2	Pull-down Active Standby Cond. ;	10		100	µA
I_{IH}	6.5	V_{IN} = V_{DD}	100		600	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	V_{DD}(V)	Parameter	Min.	Typ.	Max.	Unit
		Data Output REMO				
V_{OH}	2	Output Volt. HIGH	0.8			V
V_{OH}	6.5	$- I_{OH} = 40mA$	5.0			V
V_{OL}	2	Output Volt. LOW			0.4	V
V_{OL}	6.5	$I_{OL} = 0.5$ mA			0.4	V
t_{MH}/t_{OSC}	6	Pulse Duty Cycle During Carrier Mode	0.4	0.5	0.6	
t_{OH}	6.5	Pulse Length, Oscill. Stopped			1	msec
		Oscillator				
I_I	2	Input Current			5.0	µA
I_I	6.5	OSC1 at V_{DD}	5.0		70	µA
		Output Volt. HIGH				
V_{OH}	6.5	$- I_{OL} = 0.1mA$	$V_{DD} - 0.8$			V
		Output Volt. LOW				
V_{OL}	6.5	$I_{OH} = 0.1mA$			0.7	V

Figure 1 : Typical Application.

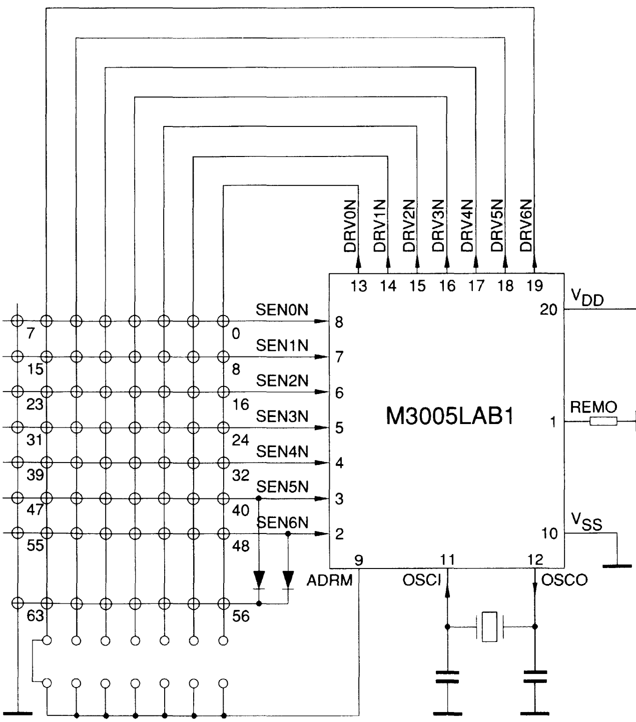


Figure 2 : Data Format of REMO Output.

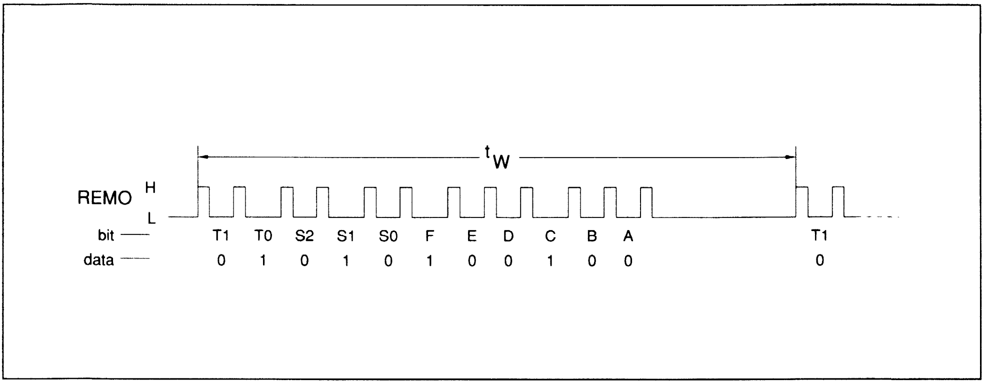


Figure 3 : REMO Output Waveform : (a) flashed pulse.
(b) modulated pulse.

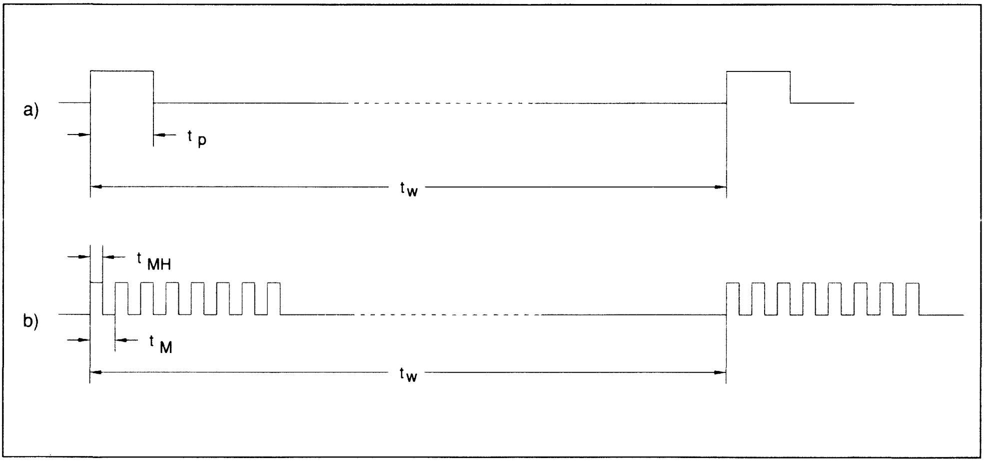


Figure 4 : Single Key - Stroke Sequence.
Debounce Time : t_{DB} = 4 to 9 x T_O
Start Time : t_{ST} = 5 to 10 x T_O
Minimum Release Time : t_{REL} = T_O.

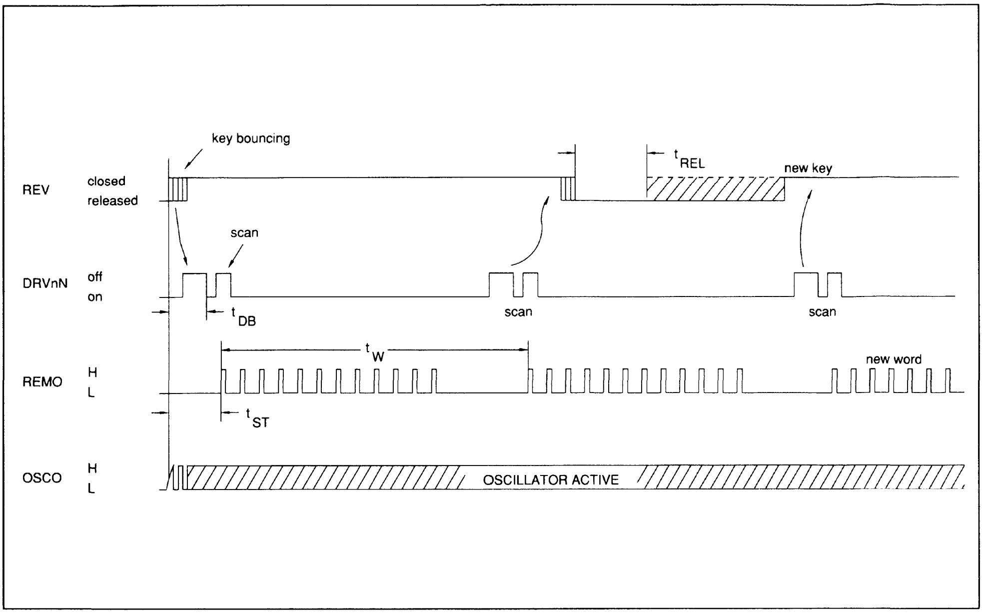
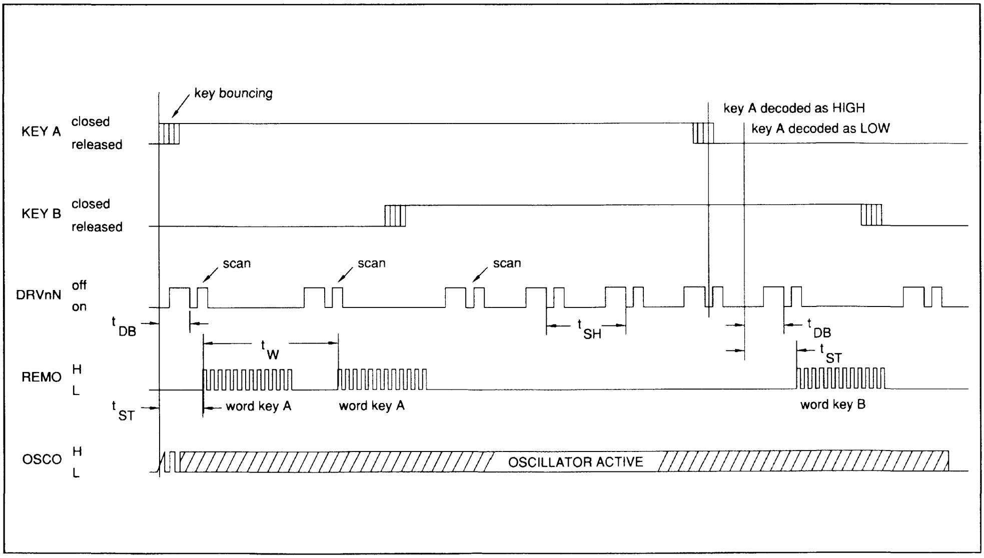


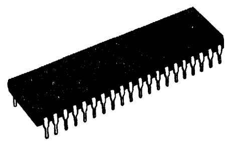
Figure 5 : Multiple Key - Stroke Sequence.
Scan Rate Multiple Key-stroke : t_{SM} = 8 to 10 x T_O.



LED DISPLAY DRIVERS

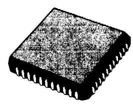
- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples :
- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS



DIP-40

ORDER CODES : M5450B7
M5451B7



PLCC44

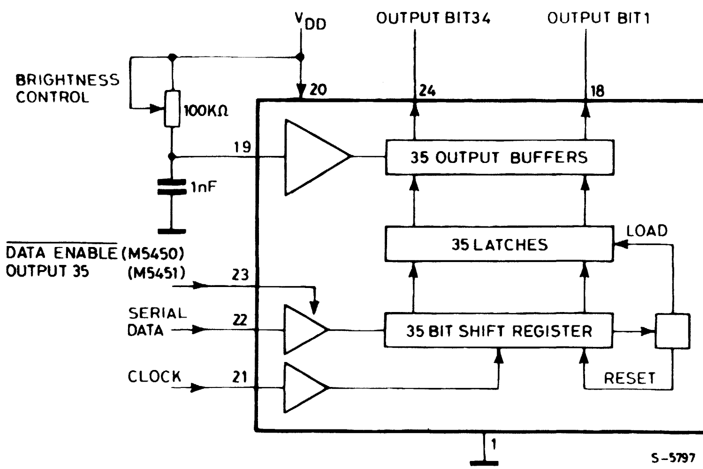
ORDER CODES : M5450C7
M5451C7

DESCRIPTION

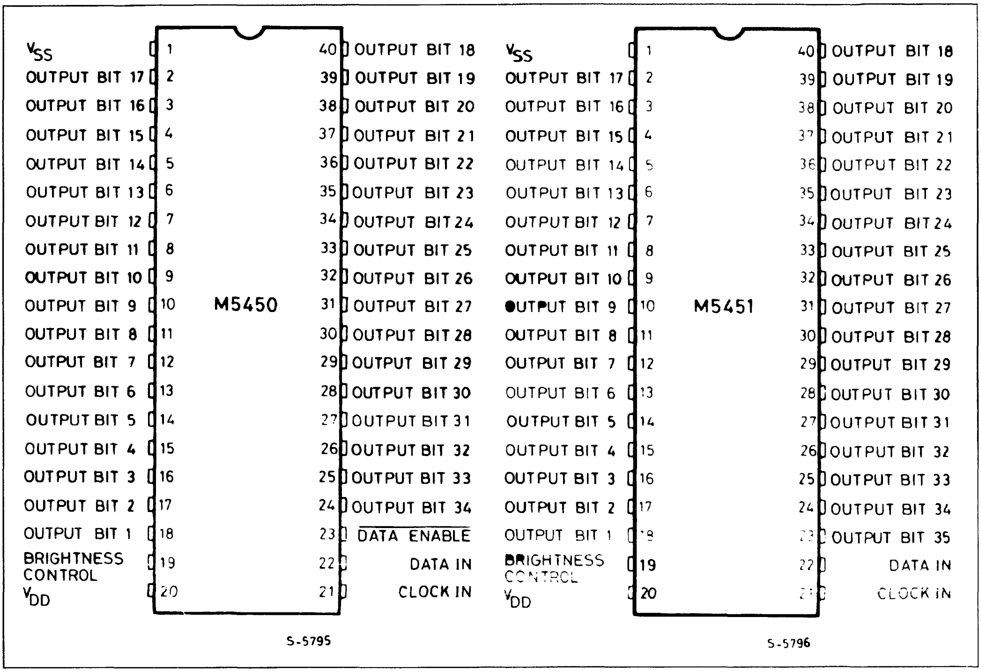
The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

Figure 1 : Block Diagram.



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 15	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Output Voltage	15	V
I_O	Output Sink Current	40	mA
P_{tot}	Total Package Power Dissipation at 25°C at 85°C	1 560	W mW
T_j	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	– 25 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specially designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current LED displays.

A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in figure 1. For the M5450 a DATA ENABLE is used instead of the 35th output. The DATA ENABLE input is a metal option for the M5450.

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationship between Data, Clock and DATA ENABLE.

A max clock frequency of 0.5MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

$$T_j = [(V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7mA)]\ (124°C/W) + T_{amb}$$

where :

T_j = junction temperature (150°C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2V			7	mA
V_I	Input Voltage Logical "0" Level Logical "1" Level	± 10µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	– 0.3 2.2 V_{DD}–2		0.8 V_{DD} V_{DD}	V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input Current = 750µA	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3) Segment OFF Segment ON	 V_O = 3V V_O = 1V (note 4) Brightness In. = 0µA Brightness In. = 100µA Brightness In. = 750µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40mA.
4. The V_O voltage should be regulated by the user. See figures 5 and 6 for allowable V_O versus I_O operation.

Figure 2 : Input Data Format.

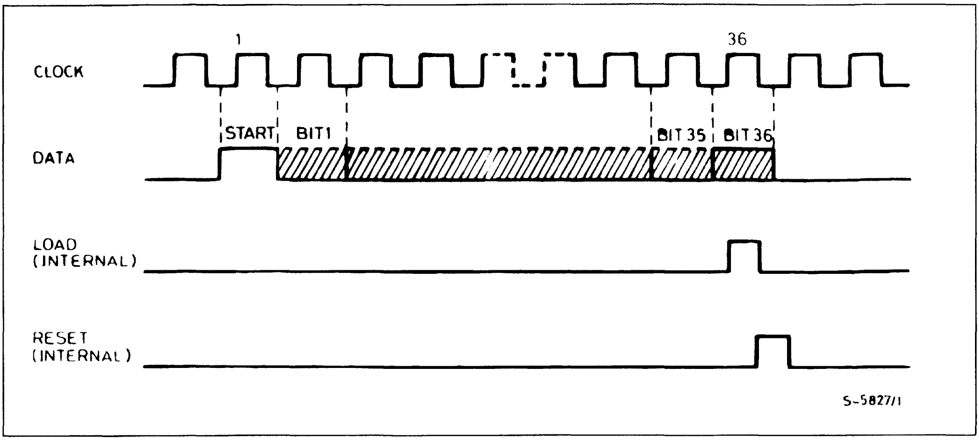


Figure 3.

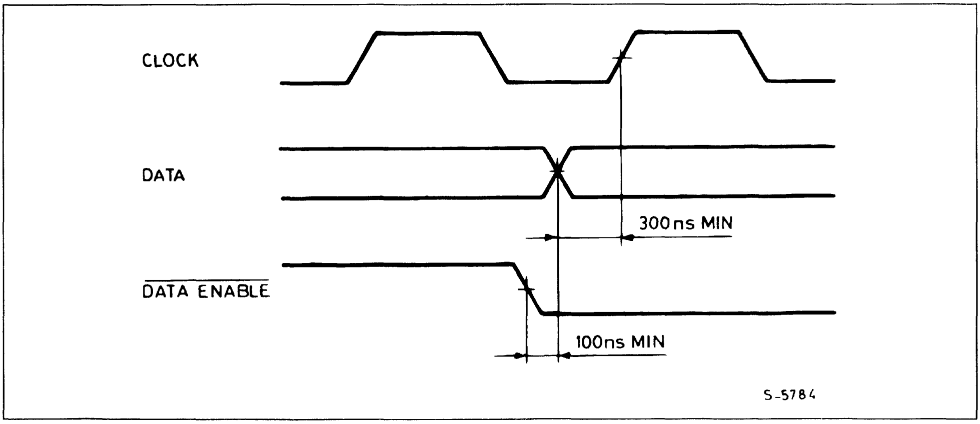


Figure 4.

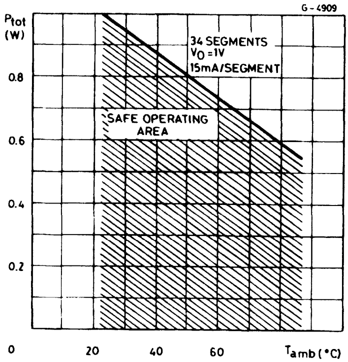


Figure 5.

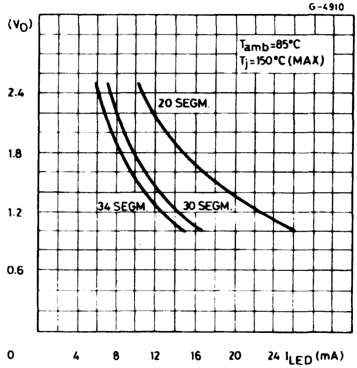
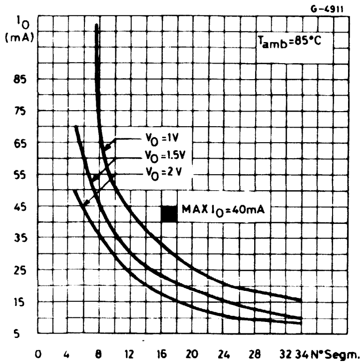
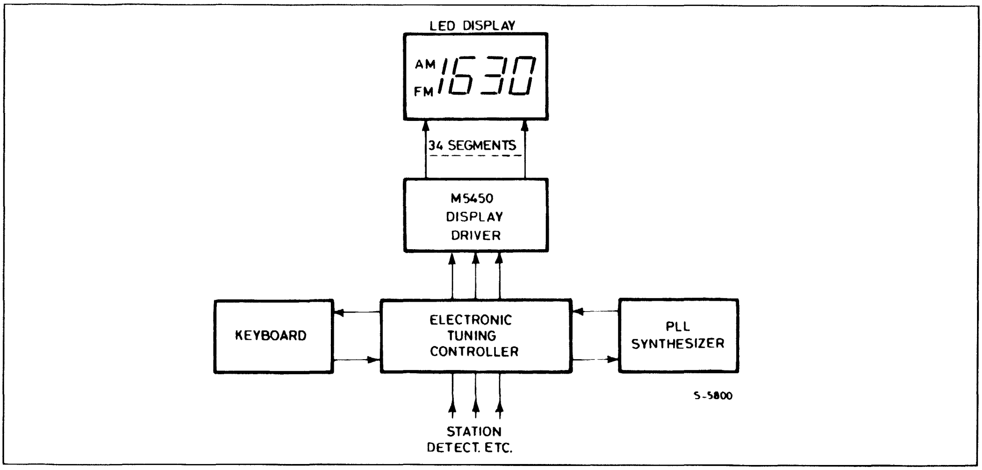


Figure 6.

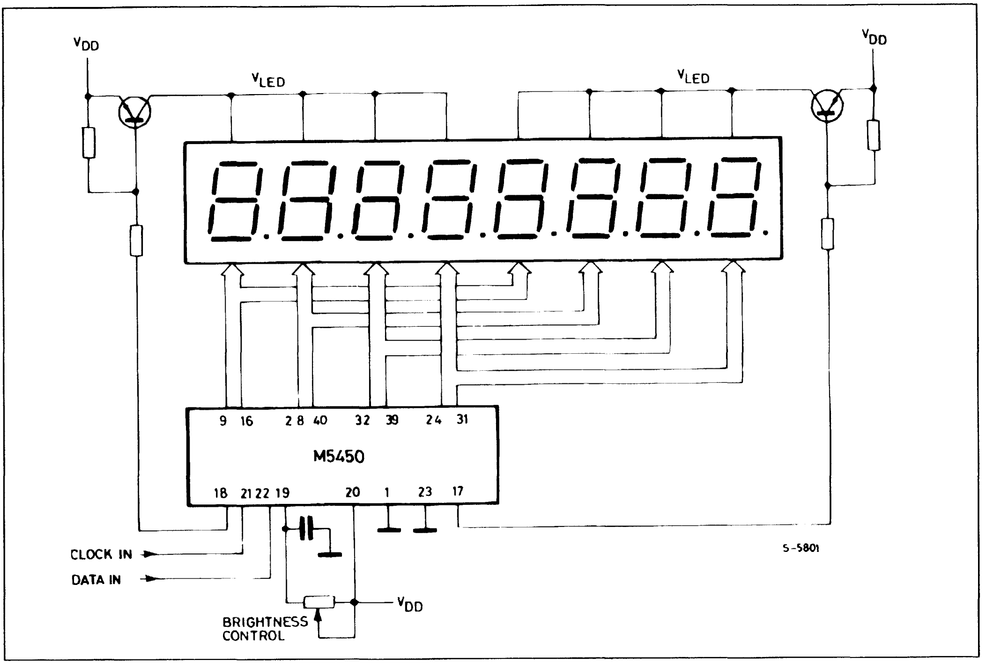


TYPICAL APPLICATIONS

BASIC ELECTRONICALLY TUNED RADIO OR TV SYSTEM.



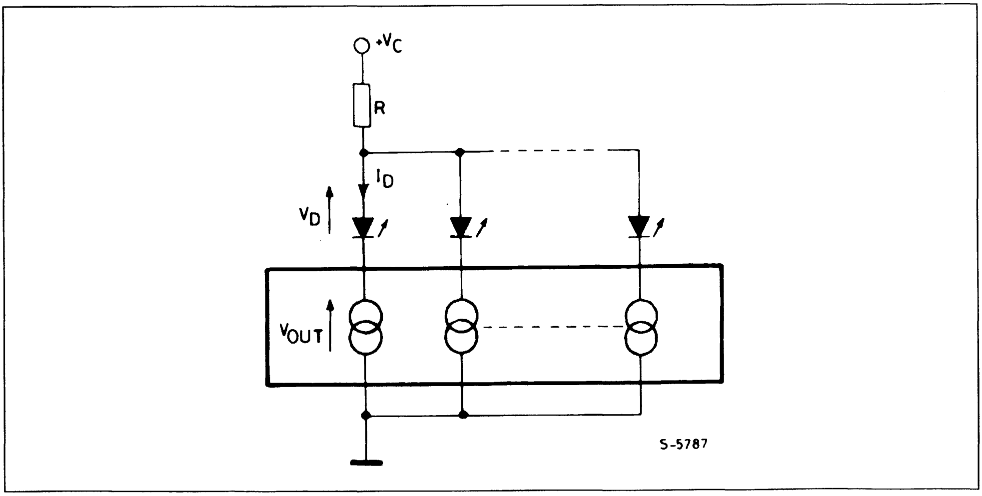
DUPLEXING 8 DIGITS WITH ONE M5450.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a) In the application R must be chosen taking into account the worst operating conditions.



R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

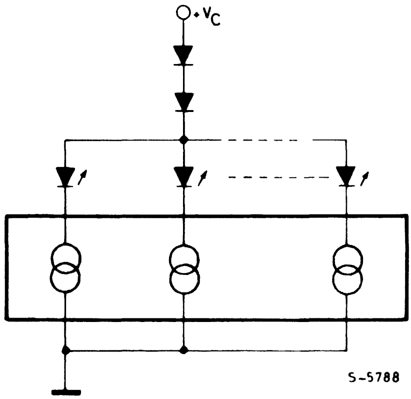
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

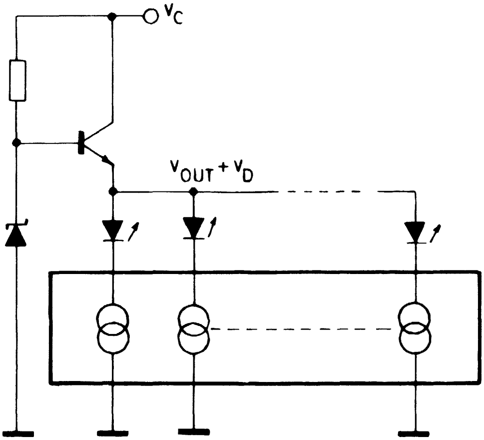
In this case the current variation in the single resistor is reduced and P_{tot} limited.

b) In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.



c) In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.



LED DISPLAY DRIVER

- 3 1/2 DIGIT LED DRIVER (23 segments)
- CURRENT GENERATOR OUTPUTS (no resistors required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

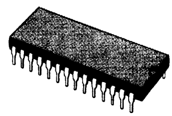
Applications examples :

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION

The M5480 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3 1/2 digit dispaly. A single pin controls the LED dispaly brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

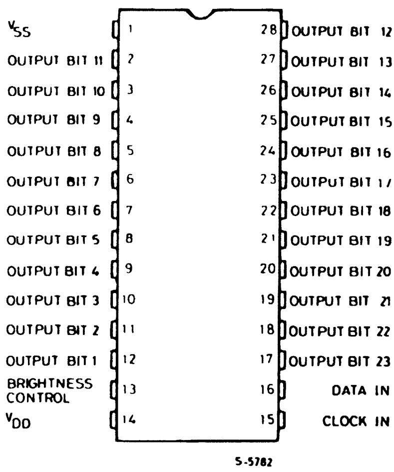
The M5480 is a pin-to-pin replacement of the NS MM 5480.



DIP-28
(Plastic)

ORDER CODE : M5480 B7

CONNECTION DIAGRAM



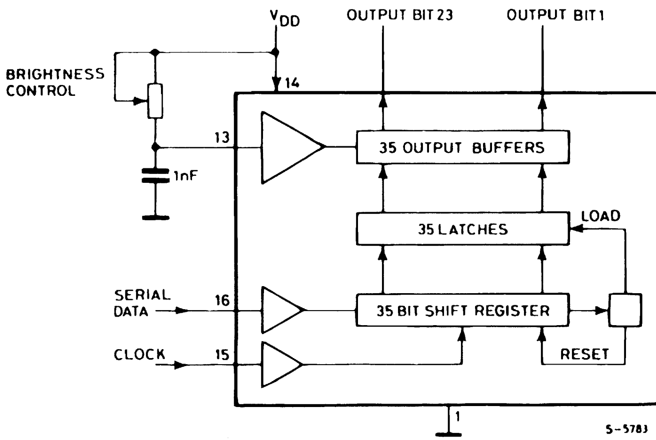
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 to 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	940 490	mW mW
T_j	Junction Temperature		150	°C
T_{op}	Operating Temperature Range		– 25 to 85	°C
T_{stg}	Storage Temperature Range		– 65 to 150	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

Figure 1.



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD} = 4.75 V to 13.2 V, V_{SS} = 0 V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	 ± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 – 0.3 2.2 V_{DD} – 2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 13)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage			13.2	18	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1.Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2.With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3.Absolute maximum for each output should be limited to 40 mA.
4.The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate 3 1/2 digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.

There is an internal limiting resistor of 400 Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

FUNCTIONAL DESCRIPTION

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

T_j = [(V_{OUT}) (I_{LED}) (No.of segments) + V_{DD} . 7 mA] (132 °C/W) + T_{amb}

where:

T_j = junction temperature (150 °C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

132 °C/W = thermal coefficient of the package

T_{amb} = ambient temperature

Figure 2 : Input Data Format.

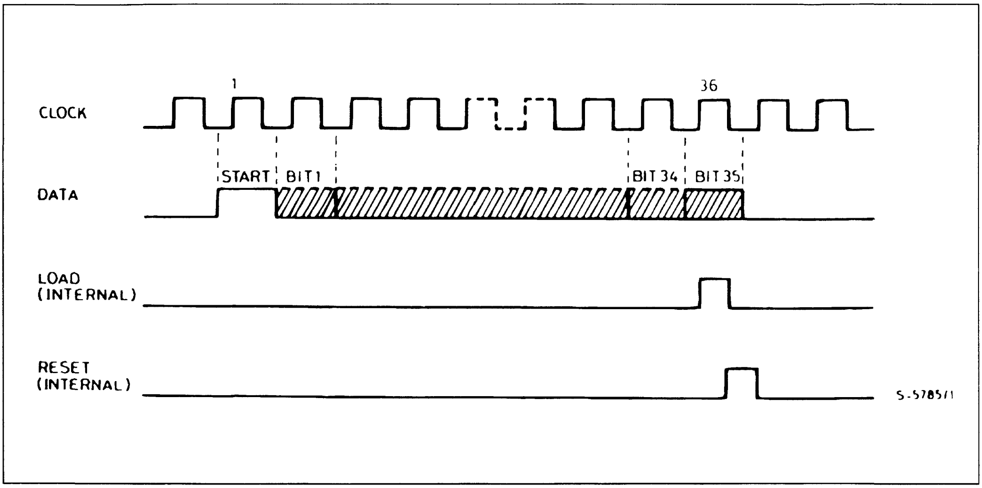


Figure 3 .

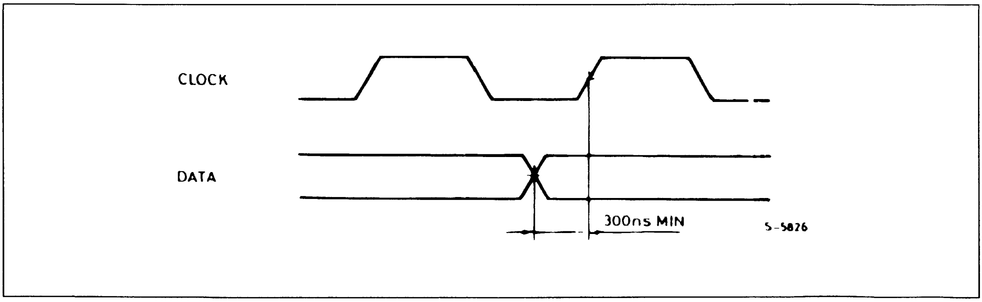


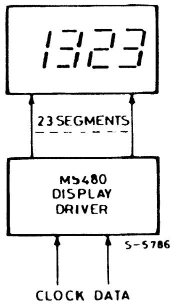
Figure 4 : Serial Data Bus / Outputs Correspondence.

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	START
5480	X	23	22	21	20	19	X	X	18	X	17	16	15	14	13	12	X	START

5451	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5480	X	X	X	11	10	9	8	X	X	X	7	6	5	4	3	2	1	X	START

TYPICAL APPLICATION

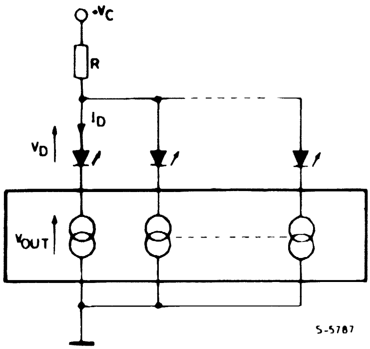
BASIC 3 1/2 Digit Interface.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{OUT\,MIN}}{N_{MAX} \cdot I_D}$$

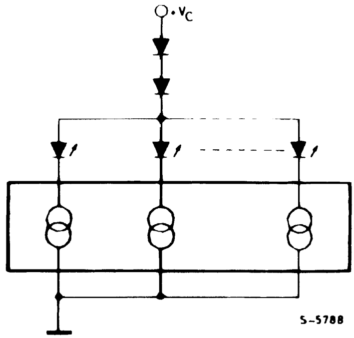
The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.

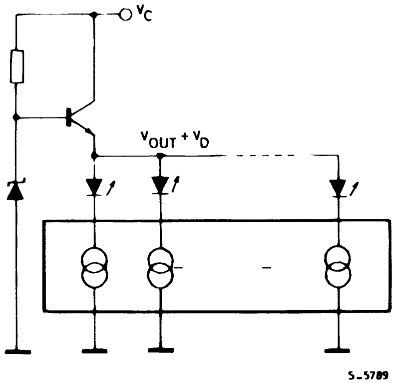
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (14 segments)
- CURRENT GENERATOR OUTPUTS (no resistor required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

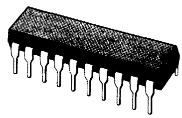
Application examples

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

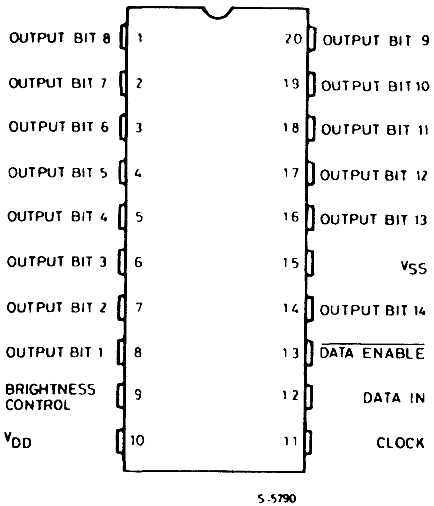
The M5481 is a pin-to-pin replacement of the NS MM 5481.



DIP-20
(Plastic 0.25)

ORDER CODE : M5481 B7

CONNECTION DIAGRAM



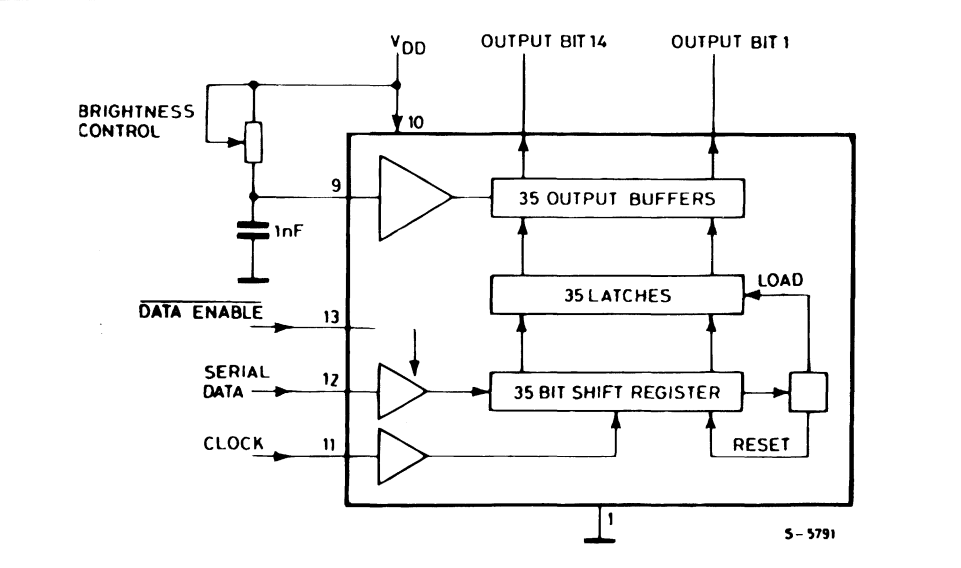
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 tò 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	1.5 800	W mW
T_j	Junction Temperature		150	°C
T_{op}	Operating Temperature Range		– 25 to 85	°C
T_{stg}	Storage Temperature Range		– 65 to 150	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

Figure 1.



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD} = 4.75 V to 13.2 V, V_{SS} = 0 V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	 ± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 – 0.3 2.2 V_{DD} – 2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

These is an internal limiting resistor of 400 Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and DATA ENABLE.

A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

$T_j \equiv [(V_{OUT})(I_{LED})(\text{No. of segments}) + V_{DD} . 7 \text{ mA}] (80\ °C/W) + T_{amb}$

where: T_j = junction temperature (150 °C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

80 °C/W = thermal coefficient of the package

T_{amb} = ambient temperature

Figure 2 : Input Data Format.

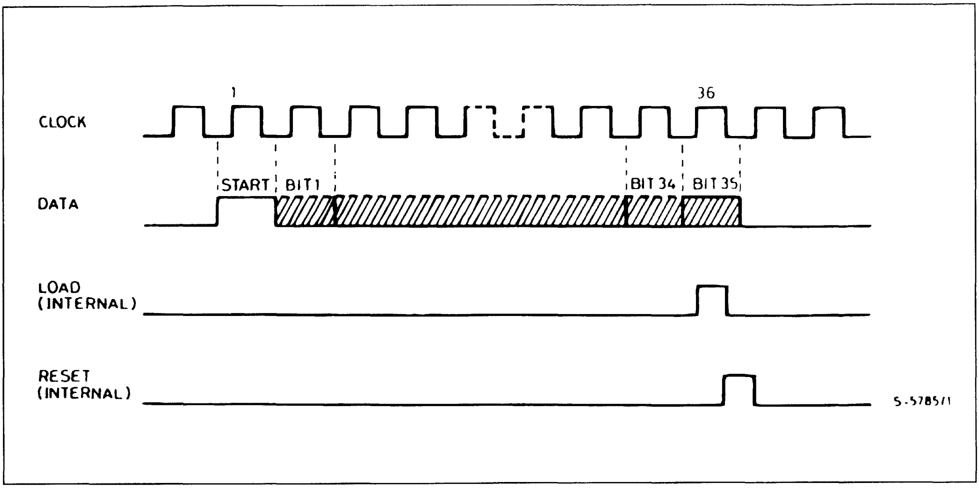


Figure 3 .

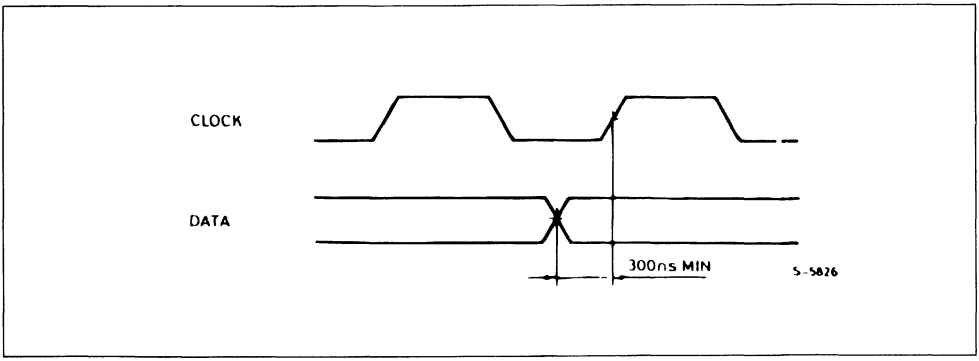


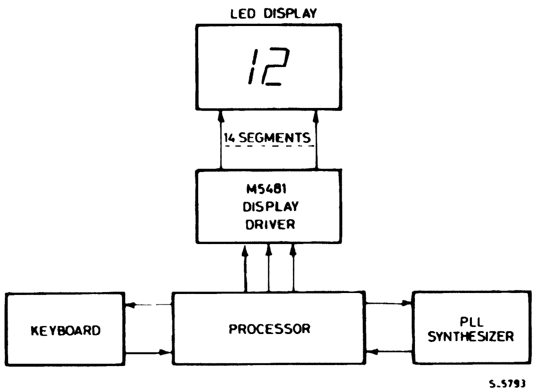
Figure 4 : Serial Data Bus / Outputs Correspondence.

5450	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	START
5481	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	START

5450	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

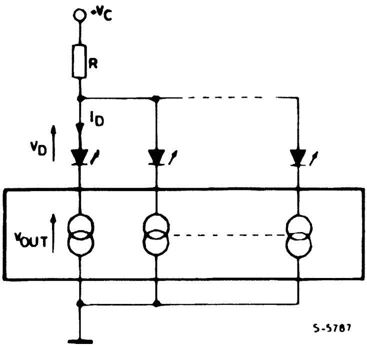
BASIC electronically tuned TV system.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

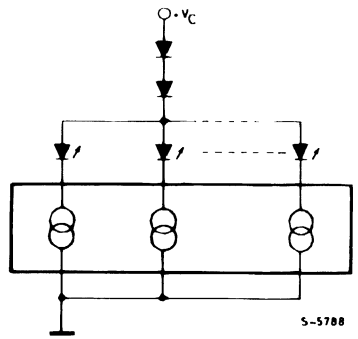
$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and P_{tot} limited.

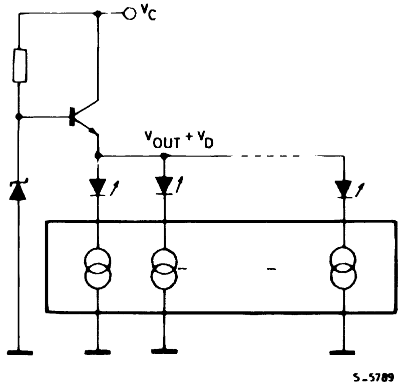
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

SGS-THOMSON
MICROELECTRONICS

M5482

LED DISPLAY DRIVER

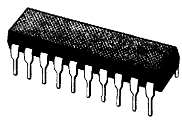
- 2 DIGIT LED DRIVER (15 segments)
- CURRENT GENERATOR OUTPUTS (no resistor required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples :

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION

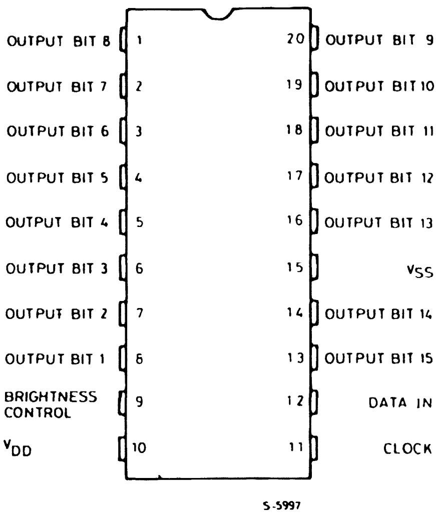
The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2 V maximum.



DIP-20
(Plastic 0.25)

ORDER CODE : M5482 B7

CONNECTION DIAGRAM



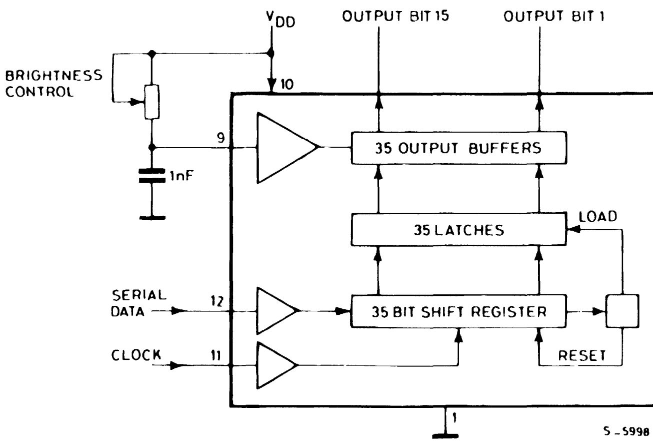
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		– 0.3 to 15	V
V_I	Input Voltage		– 0.3 to 15	V
$V_{O\ (off)}$	Off State Output Voltage		15	V
I_O	Output Sink Current		40	mA
P_{tot}	Total Package Power Dissipation	at 25 °C at 85 °C	1.5 800	W mW
T_j	Junction Temperature		150	°C
T_{op}	Operating Temperature Range		– 25 to 85	°C
T_{stg}	Storage Temperature Range		– 65 to 150	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM

Figure 1.



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} within operating range, V_{DD} = 4.75 V to 13.2 V, V_{SS} = 0 V,unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2 V			7	mA
V_I	Input Voltages Logical "0" Level Logical "1" Level	 ± 10 µA Input Bias 4.75 ≤ V_{DD} ≤ 5.25 V_{DD} > 5.25	 – 0.3 2.2 V_{DD} – 2		 0.8 V_{DD} V_{DD}	 V V V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750 µA	3		4.3	V
$V_{O(off)}$	Off State Output Voltage				13.2	V
I_O	Output Sink Current (note 3) Segment OFF Segment ON	 V_O = 3 V V_O = 1 V (note 4) Brightness In. = 0 µA Brightness In. = 100 µA Brightness In. = 750 µA	 0 2 12	 2.7 15	 10 10 4 25	 µA µA mA mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Notes : 1. Output matching is calculated as the percent variation from I_{MAX} + I_{MIN}/2.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.

The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.

A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

$T_j \equiv [(V_{OUT})(I_{LED})(\text{no.of segments}) + V_{DD} \cdot 7\ \text{mA}]\ (80\ °C/W) + T_{amb}$

where : T_j = junction temperature (150 °C max)
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
80 °C/W = thermal coefficient of the package
T_{amb} = ambient temperature

Figure 2 : Input Data Format.

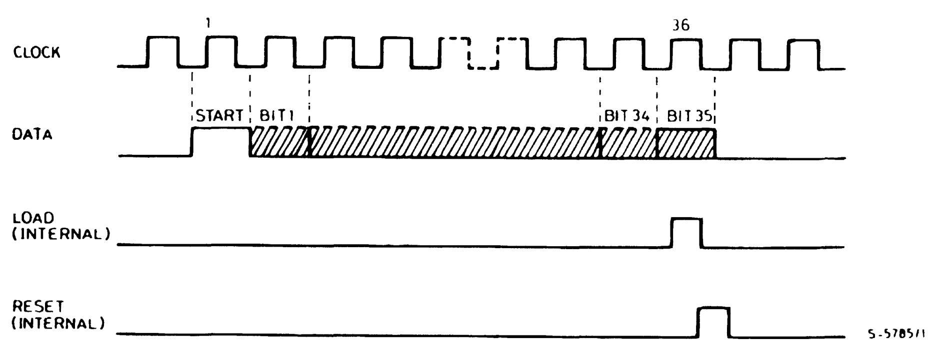


Figure 3 .

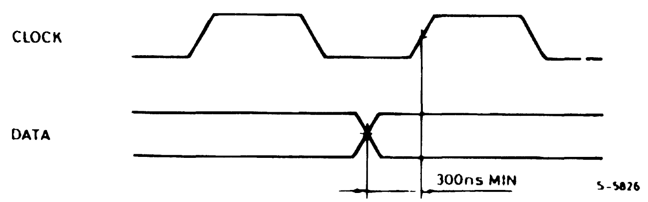


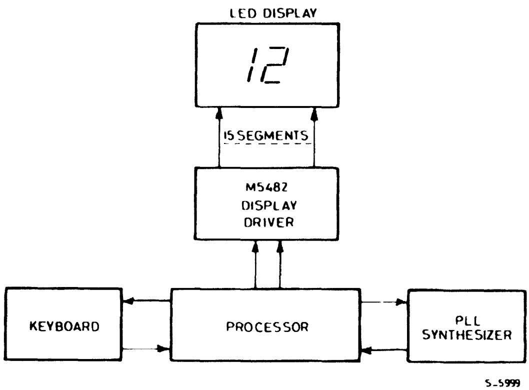
Figure 4 : Serial Data Bus / Outputs Correspondence.

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	START
5482	15	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	START

5451	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		START
5482	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X		START

TYPICAL APPLICATION

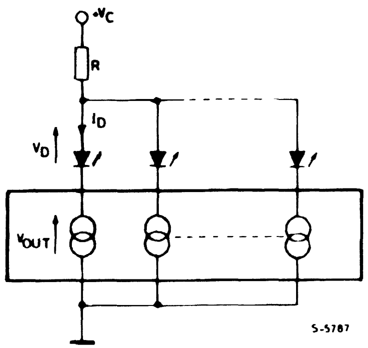
BASIC electronically tuned TV system.



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)



In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

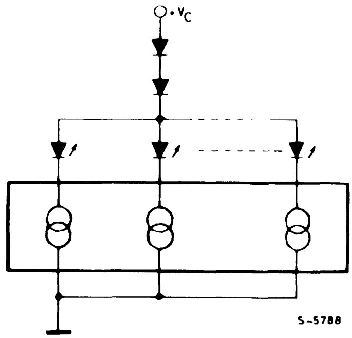
$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistors is reduced and P_{tot} limited.

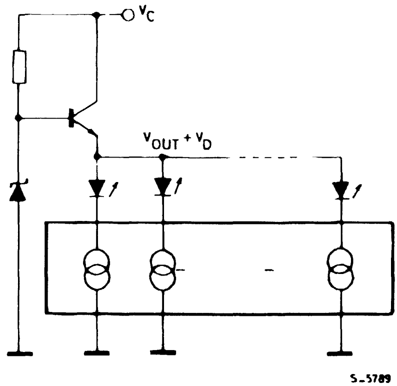
b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)



In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

CLOCK/CALENDAR WITH SERIAL S–BUS

ADVANCE DATA

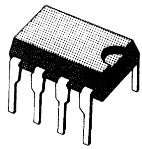
- CLOCK/CALENDAR WITH SERIAL S–BUS
- 32kHZ QUARTZ TIMEBASE
- COUNTERS FOR SEC ; MIN ; HRS ; DAY ; MONTH OR SEC ; MIN ; HRS ; DAY OF WEEK
- EXTREMELY LOW POWER CONSUMPTION IN STANDBY OPERATION (TYP. 5A)
- 8 PIN DIP PACKAGE
- INTEGRATED POWER FAIL DETECTION AND POWER-ON RESET
- PULSE OUTPUT FOR SECONDS
- CMOS PROCESS

DESCRIPTION

The integrated circuit M8716B contains a digital clock with a 32kHz quartz oscillator and a serial bus interface (S–Bus). The circuit is programmable to count seconds, minutes, hours, days and month or seconds, minutes, hours and day of the week.

This circuit is intended for use within a microcomputer system.

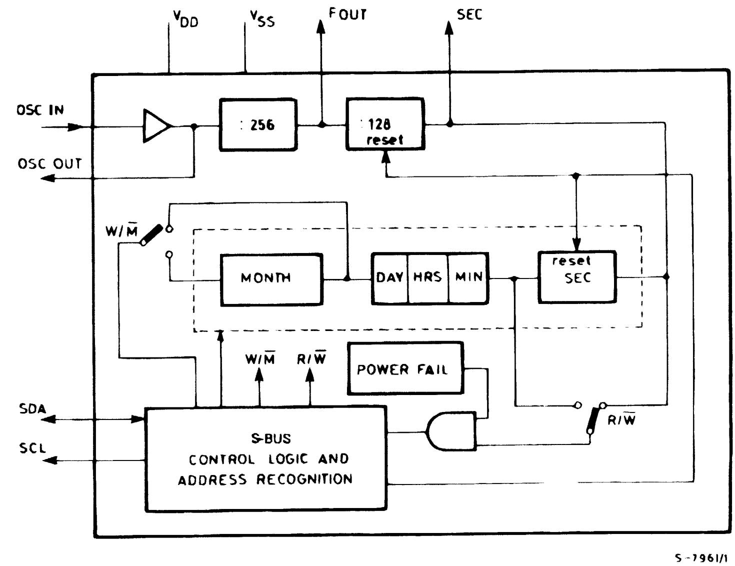
The M8716B is available in a 8 lead dual in-line plastic package.



B1
(Plastic Package)

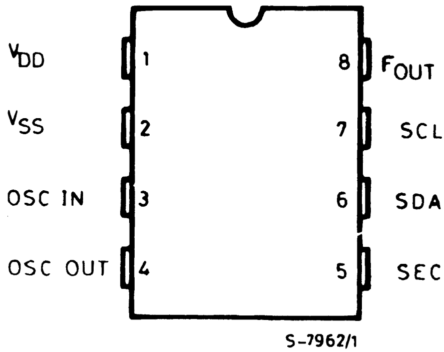
ORDER CODE : M8716A B1

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS

(T_A = 25°C : V_{DD} = 5V ; F_{OSC} = 32.768kHz if not otherwise specified).

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}	Supply Current				1	mA
V_{BAT}	Supply Voltage (standby operation)	No Data Transfer	2.0	2.4		V
I_{BAT}	Supply Current (standby operation)	Test Circuit V_{BAT} = 2.4V		5	15	µA
I_{IN}	Input Current SDA ; SCL	$V_{IN} = V_{DD}$			5	µA
		$V_{IN} = V_{SS}$			– 5	
I_{OUT}	Output Current SDA	V_{OL} = 0.4V	4			mA
I_{OUT}	Output Current F_{OUT}, SEC	V_{OUT} = 1V	0.1			mA
		V_{OUT} = 4V	– 0.1			
C_{OUT}	Oscillator Output-capacitance		16	20	24	pF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}-V_{SS}	Supply Voltage	– 0.3 to + 10	V
V_I/V_O	Input Voltage, Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Total Package Power Dissipation	300	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_A	Operating Temperature	0 to + 70	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GENERAL DESCRIPTION

The integrated circuit M8716B contains a digital clock counting seconds, minutes, hours, days and months or seconds, minutes, hours and days of the week as an option. A 32.768kHz quartz oscillator serves as time-base. This circuit is intended for use within a microcomputer system.

Writing (time setting) and reading of the counters is done via a serial interface (S–Bus). The micro-computer is used for controlling the data transfer and for generating the signals to drive a (7 segment) display. If a data transfer takes place between the M8716B and the microprocessor, a 5V supply voltage has to be provided. During standby the circuit is supplied by two NiCd-cells at a very low power consumption.

FUNCTIONAL DESCRIPTION

DIVIDERS AND COUNTERS

The oscillator frequency of 32.768kHz is first divided by 256 and then again by 128. The resulting output frequency of 1Hz then serves as clock pulse for the time counters.

The content of the counters for sec, min, hr, day and month of sec, min, hr, and day of week can be read or modified (written) via the S–Bus interface. During a "write" cycle only the content of the counters starting from the minutes counter is modified : the seconds counter and the seconds divider block are reset to zero.

Selection between "calendar" operation (display of day and month) and "day of week" operation (display of day of week 1 to 7) is done as follows :

If the second bit in the first data byte is "1" during a "write" operation, the counters are set for the mode "day of week".

If this bit remains at "0" during a "write" operation the calendar mode is selected. In this case, carry of the "day" counter is performed automatically at positions 28, 30 or 31, depending on the month. In case of a leap year the day 29 (of February) can be set by a "write" operation.

In this case, carry takes place on 3-1 (March 1st).

S–BUS INTERFACE GENERAL DESCRIPTION

Data transfer from the circuit M8716B to the microcomputer (reading) and vice versa (writing) takes place via the two lines SDA and SCL. Address and data are transmitted on SDA while at the same time clock pulses have to be provided on SCL for synchronization by the microcomputer.

S–BUS INTERFACE ADDRESSING

(see fig. 1...3)

A data transfer (reading or writing) is initiated by a start condition ("1" – > "0" transition on SDA while SCL remains at "1") and a subsequent address byte. By assigning a unique address to each circuit, several circuits may be connected to the S–Bus without interfering each other.

If the M8716B recognizes an address transmitted on the bus as its own address, the data transfer starts. The least significant bit of the address word controls the direction of data transfer (R/$\overline{W}$-control). If it is set to "0", data is transferred from the microcomputer to the circuit, i.e. the content of the time counters is modified. If it is set to "1" the time information is read out by the microcomputer. A data transmission between the microprocessor and M8716B must always be completed otherwise the clock content may be lost. This means that the "master" can't use the possibility to stop the transmission after a certain byte by not sending the acknowledge bit.

Even 2f M8716B can work at the frequency four DC UP to 100kHz, it is tested at a frequency of 30kHz. If a carry of the time counter should take place during a data transfer, the carry will be stored and made after the data transfer. As only one carry can be stored, the whole data transfer must not take a time longer than one second.

SYNCHRONIZATION

For easy of synchronization with an external time reference in case of small deviations (< ± 30sec), only the address (with R/W̄ = "0") has to be transmitted, followed immediately by a stop condition. No data is transmitted (see fig. 4). The second divider block (128Hz to 1Hz) and the seconds counter are reset. If the seconds counter was at position 30 ... 59, a carry to the minutes counter takes place in addition to the reset.

POWER FAIL

In case of total power fail an internal register is set to "0". This register disables the data of the watch. So in a read cycle the µP recognizes "0" of the watch content. This is a unique situation appearing only in case of a power fail. The power fail register is automatically reset by the first "write" command.

PULSE OUTPUTS F_{OUT}, SEC

The output frequency of the first divider block (128Hz) is provided on the pin F_{OUT} and facilitates adjustment of the oscillator frequency without loading (and detuning) the oscillator.

The output SEC (1 Hz) may be utilized for a blinking second indication.

Both pins F_{OUT} and SEC can also be used as input during the functional test. A Low impedance (50 to 100Ω) external signal source which overrides the internal output buffer can drive the circuit at a frequency higher than the normal rate. This allows to reduce test time.

Figure 1 : Complete Timing for an Address/-read ; Resp. Address/-write Cycle.

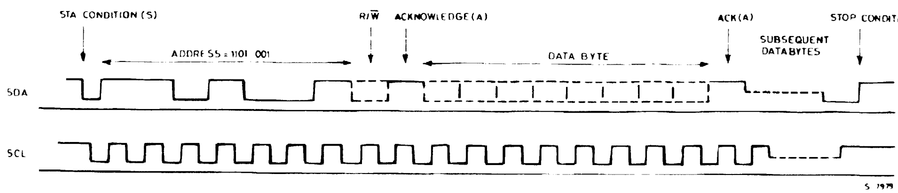


Figure 2a : Data Format for One Cycle Address/-read (with calendar).

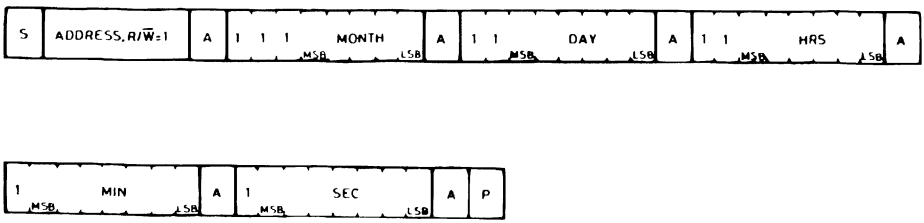


Figure 2b : Data Format for One Cycle Address/-write (with calendar).

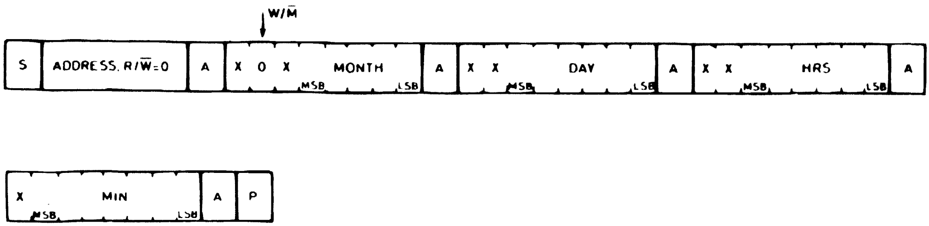


Figure 3a : Data Format for One Cycle Address/-read (with day of week indication).

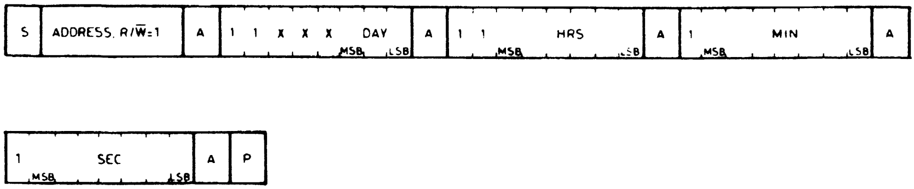


Figure 3b : Data Format for One Cycle Address/-write (with day of week indication).

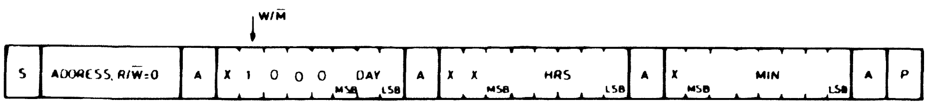


Figure 4 : Data Format for Synchronization (deviation < 30sec).

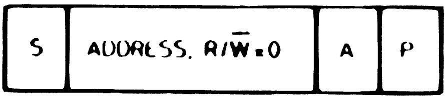


Figure 5 : Test Circuit.

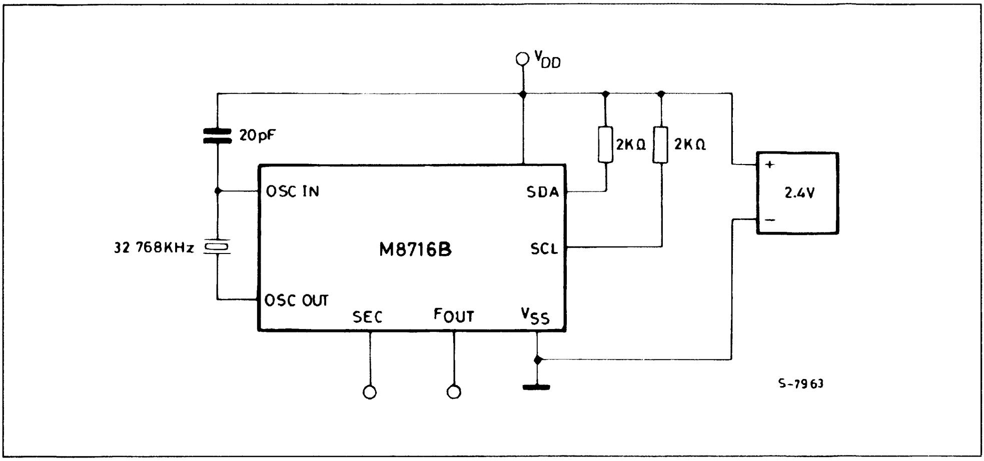
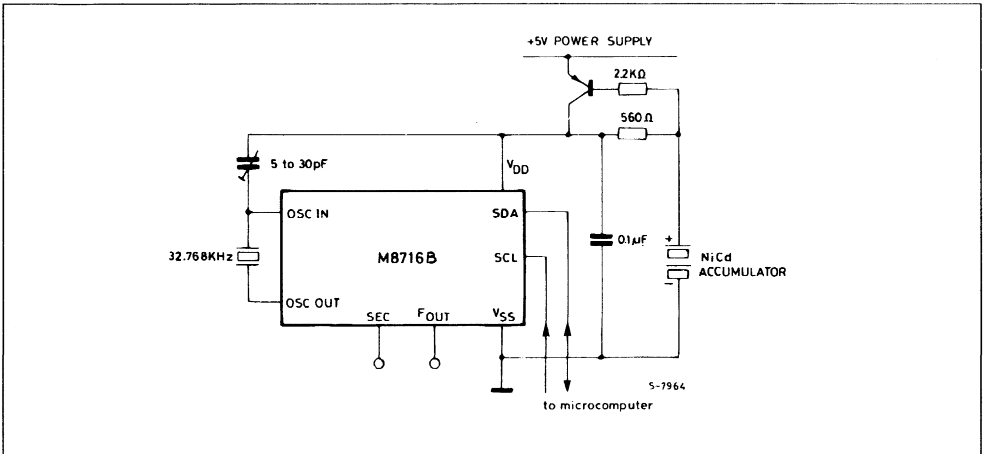


Figure 6 : Typical Application.



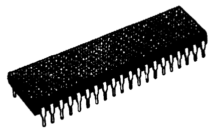
SGS-THOMSON
MICROELECTRONICS

ST6306/07/08
ST6316/17/18

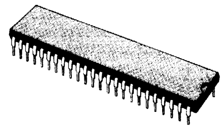
8-BIT HCMOS MCUs FOR TV FREQUENCY SYNTHESIS

ADVANCE DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 8192 BYTES
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 DIP PACKAGES
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL, ST6316/17/18 ONLY, ST6306/07/08 HAVE MORE I/Os)
- 20/22/24 (ST6306/07/08) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- 18/20/24 (ST6316/17/18) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/ I^2CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR
- THREE INTERRUPT VECTORS (IR, Timer 1 & 2)



PDIP-40



PDIP-48

- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- 1.625µS TCYCLE (with 8.0 MHz clock)
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 6-LEVEL STACK
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS.
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63 -HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS PC.

This is advance data on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 1 : ST6306/07/08 Pin Configurations

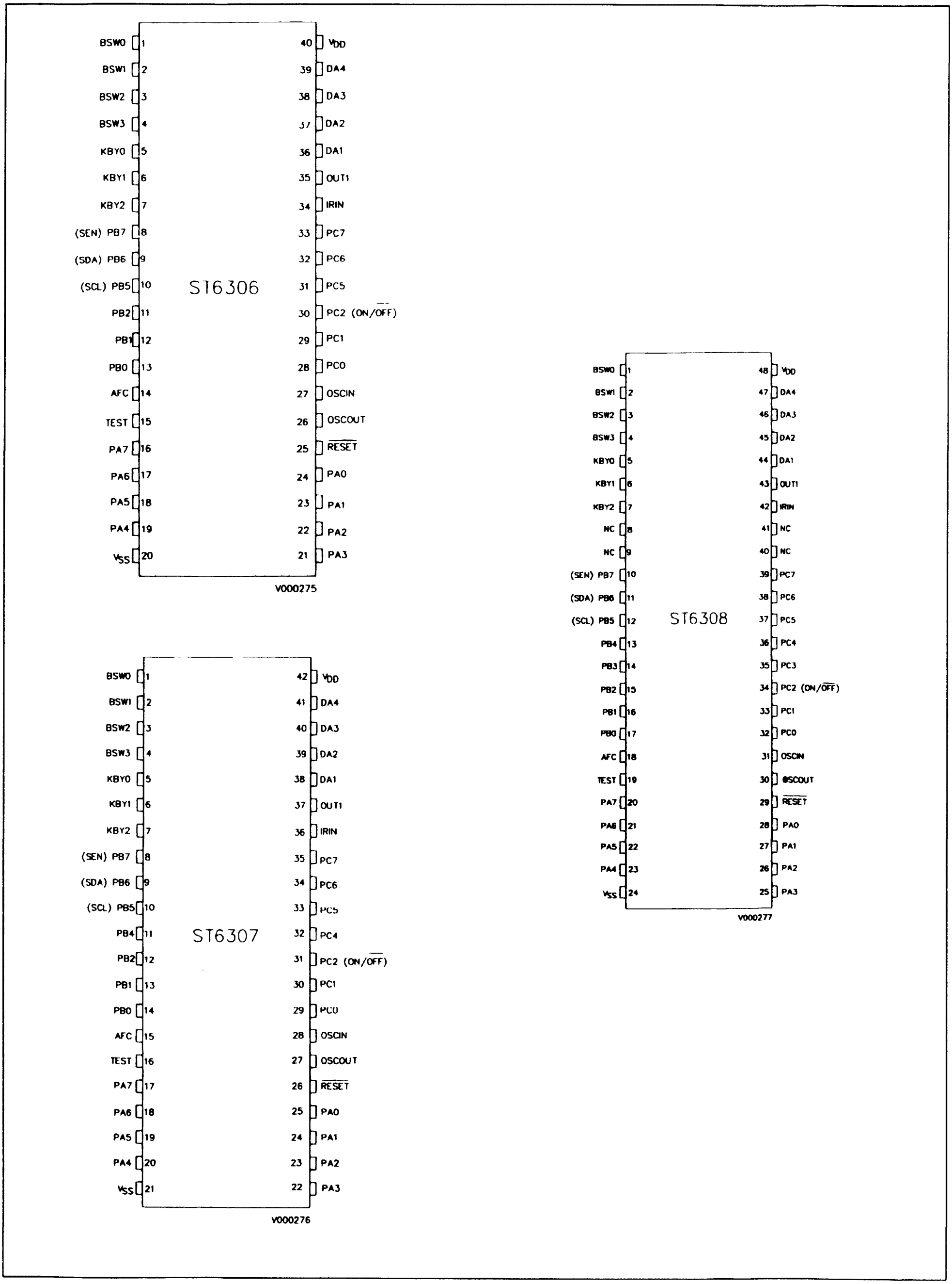
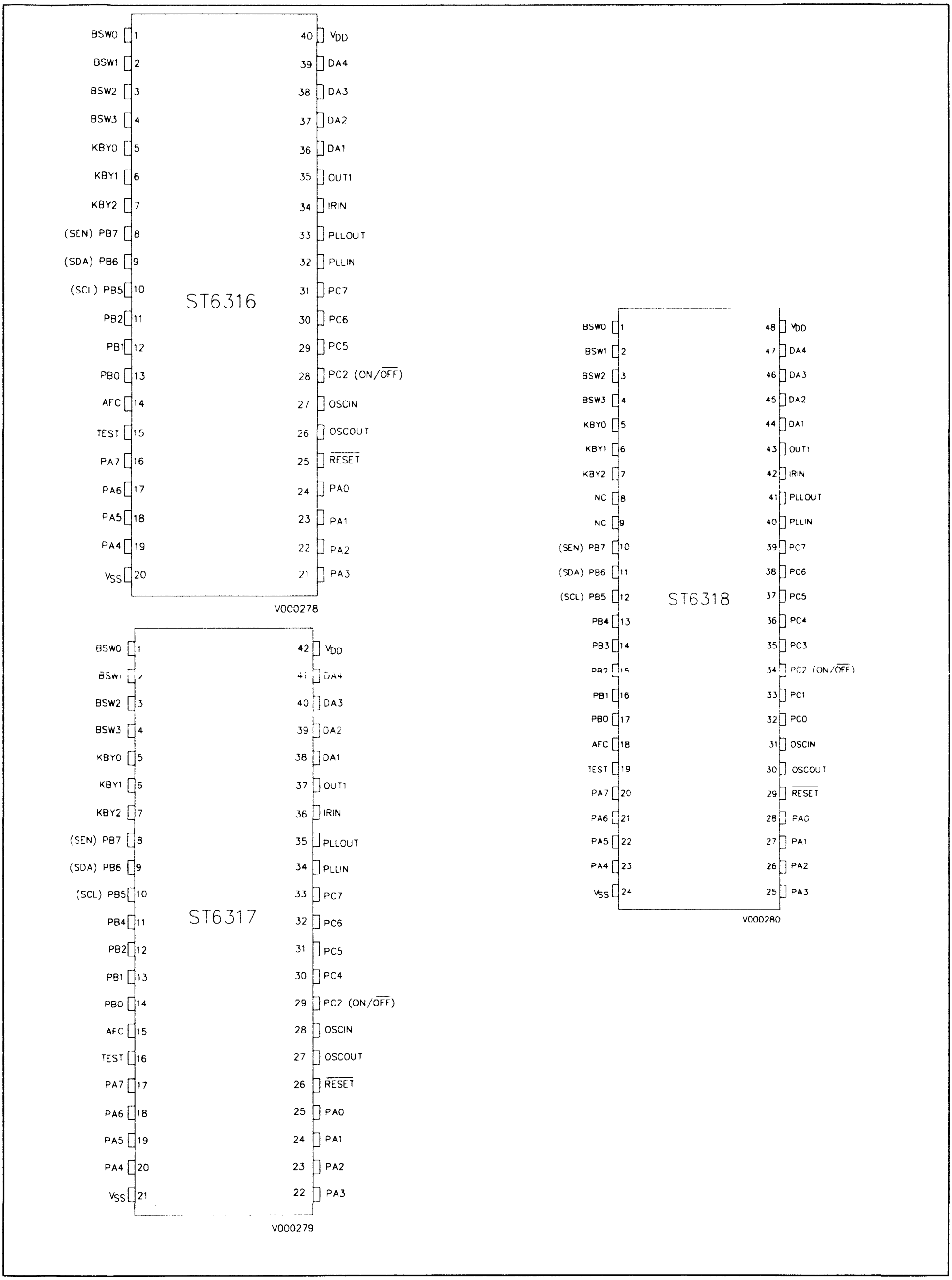


Figure 2 : ST6316/17/18 Pin Configurations



GENERAL DESCRIPTION

The ST6306/07/08 and ST6316/17/18 microcontrollers are powerful members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST6306/07/08 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 6-Bit PWM D/A Converter, an AFC A/D converter with 0.5V resolution. The ST6316/17/18 have the same configuration plus an on-chip 14/15 bit Phase Locked Loop peripheral (PLL) . In addition all these devices have 128 bytes of on-chip EEPROM.

Figure 3 : ST6306/07/08 System Description.

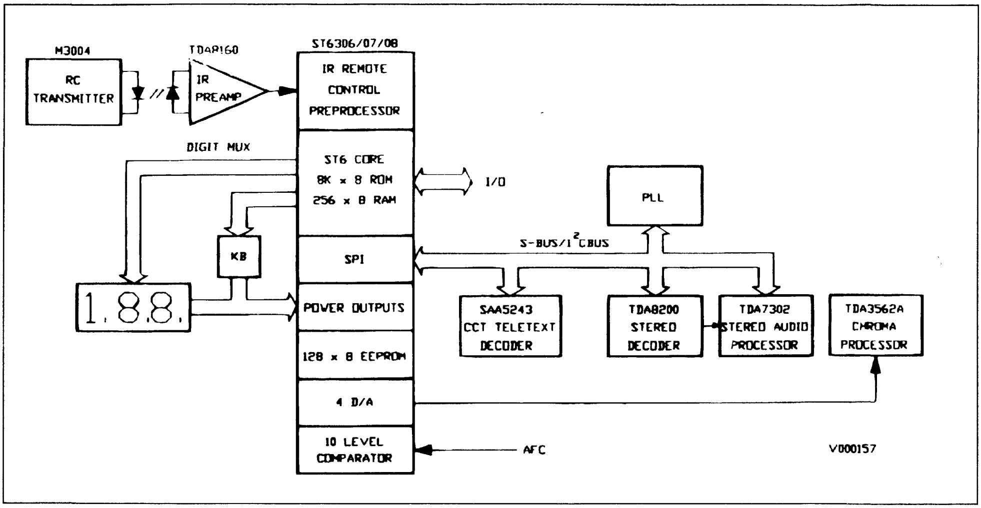
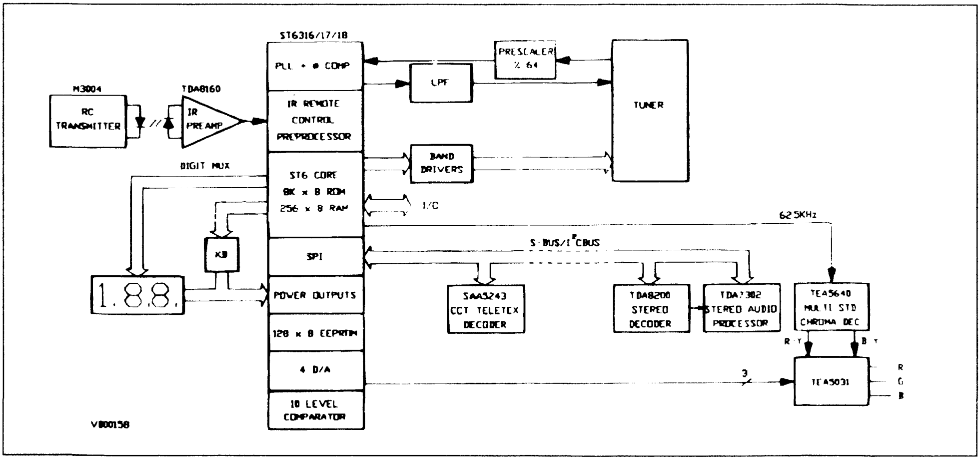


Figure 4 : ST6316/17/18 System Description.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a ceramic resonator or an external signal has to be connected between these two pins in order to allow the right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. A mask option allows the selection of a 4MHz or 8MHz oscillator frequency.

RESET. The active low RESET pin is used to restart the microcontroller from the beginning of its program.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode if kept high when Reset is active. This pin has to be connected to VSS for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has an open-drain (13.2V Max) output configuration with direct LED driving capability (30mA, 1V).

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PB5, PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCK), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). PB3 is not available on ST6307/17. PB3 and PB4 are not available on ST6306/16.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PC2 (12V Max) is also used as TV set On-Off switch. PC0 and PC1 are not available on ST6316/17 as these pins are connected to the PLL cell. PC3 is not available on ST 6307/17. PC3 and PC4 are not available on ST6306/16.

IRIN. This pin is the external interrupt input of the MCU and is directly connected to the infra-red signal pre-processor which allows, through a band pass filter, to reduce the number of interrupts sent to the Core. A mask option allows the direct connection of the interrupt pin to the Core Non maskable interrupt line.

DA1-DA4. These pins are the four PWM D/A outputs (32KHz repetition) of the 6-bit on-chip D/A converter. The PWM function can be disabled by software ; in this case these lines can be used as general purpose open-drain outputs (13.2V Drive).

OUT1. This pin is the 62.5KHz output available to drive multi-standard chroma processors. This function can be disabled by software allowing the use of this pin as general purpose open-drain output (13.2V drive).

AFC. This is the input of the on-chip 10 level A/D that can be used for AFC function. This pin is an high impedance input that can withstand signal with an amplitude up to 13.2V.

BSW0-BSW3. These outputs are provided to select up to 4 tuning bands. These pins have an open-drain (13.2V drive) output configuration.

KBY0-KBY2. These input pins are intended as common lines for keyboard scanning. They have CMOS level threshold and have on-chip 100Kohm pull-up resistor.

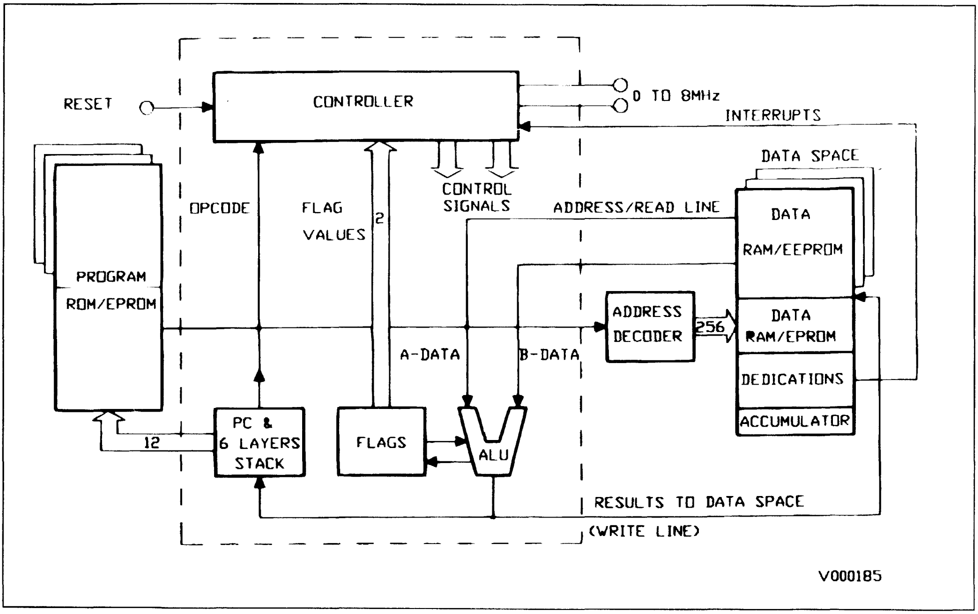
PLLIN. This is the PLL input pin. The signal coming from an external 64 divider is fed to PLLIN. Maximum input frequency is 16MHz and minimum required signal amplitude is 500mVpp. The PLL is not available in the ST6306/07/08 types.

PLLOUT. This is the PLL output pin. This three-state output generates tuning correction pulses at the comparison frequency of 976.5Hz (488.2 and 1.95KHz optionally selectable). The PLL is not available in the ST6306/07/08 types.

ST63XX CORE

The ultra small and fast Micro-Core of the ST63XX TV chips microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST63XX Core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. Three pairs of flags monitor the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 5 : ST63XX Core Block Diagram.



PROGRAM ROM PAGING

ST63XX has 12 address bits for program ROM, thus giving a program address space of 4 Kbytes. In the highest twelve bytes of the ROM are located the restart and INT vectors. To go beyond the 4K limit, the lower half of the program address space (0..7FFH) has been used as paged address space, the current page being selected by a banking register. Only the lower part of address space has been bank-switched because of interrupt (vectors and drivers) and common subroutines, that should be available all the time.

DATA ROM WINDOWING

Data ROM is physically the same ROM as for program space. Simply, it is possible to read as data all the program ROM space with the range 40H..7FH of the data address space and the contents of the Data ROM Window Register. The six least significant bits of data address space become the least significant address bits of the program ROM address to be build. This only when addressing the data space locations mentioned above. The bits coming out from Data ROM Window register become the most significant ones ; they are 6 if the program ROM is of 4Kbytes, 7 if 8Kbytes. So, when addressing location 40H of data space, and 0 is loaded in the register, the physical location addressed is at location 0.

PAGED RAM ADDRESS RANGE

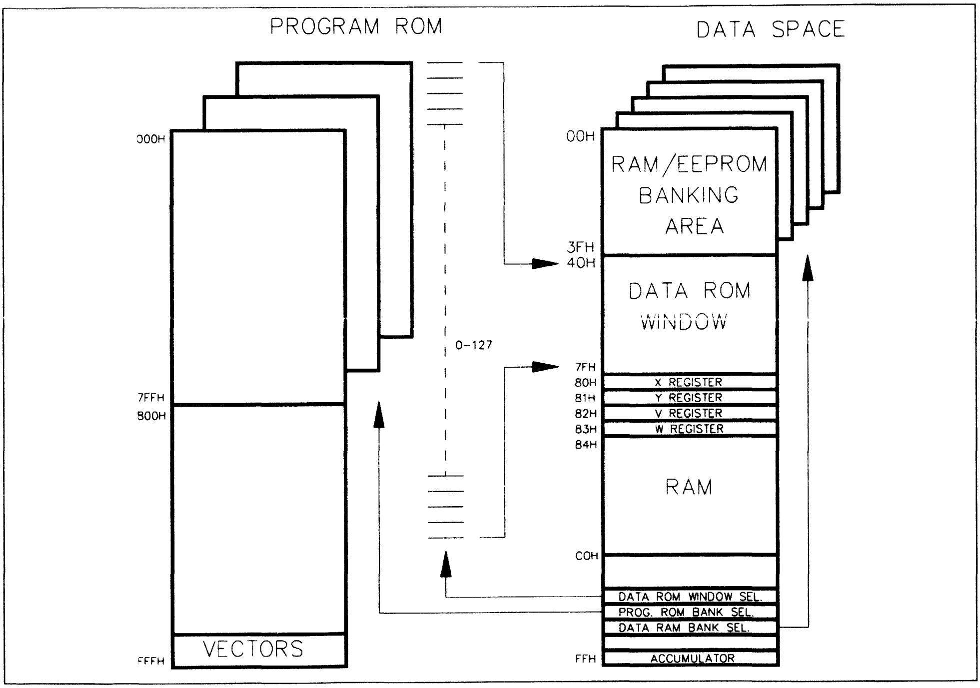
A 64 bytes range inside the data space is paged to allow extension of the RAM memory available for the user. Paged RAM address range can be switched to address up to 8 different 64 bytes pages, in which any kind of memory and/or additional control registers can be mapped. On ST6306/07/08 and ST6316/17/18 three pages are available. These 192 bytes plus 64 Bytes of non-paged RAM give a total of 256 RAM bytes available for the user.

EEPROM

128 bytes of EEPROM are available to store normalized TV audio and video user/factory values as well as 40 favorite programs. The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Any EEPROM location can be read just like any other data location, also in terms of access time.

A writing of an EEPROM location takes about 5msec and during this time the EEPROM is not accessible by the Core. Two programming modes are available : BYTE MODE (BMODE) and PARALLEL MODE (PMODE). The BMODE is the normal way to write the EEPROM and consists in accessing one byte per time. The PMODE consists in accessing up to 8 bytes per time.

Figure 6 : ST63XX Memory Addressing Description.



I/O PORTS

Each ST63XX general I/O port normally consists of eight identical cells, each containing a separately addressable data latch and data direction latch ; together they form an eight bit data register and an eight bit data direction register. The I/O uses two addresses of the data space, one for the data register and one for the data direction register. Each of the eight pins can be programmed independently as an input or as an output with various additional modes under control of the data direction register. When programmed as an input a pull-up resistor can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode ; this is defined during manufacture by a program ROM mask option. One I/O port (A) has an open-drain (13.2V drive) output configuration with high current drive capability for direct LED driving.

TIMERS

Each Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes : event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register. A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG

The digital watchdog consists of a down counter that can be used to provide a controlled recovery from a software upset. The check time can be set differently for different routines within the general program. After a reset the watchdog is automatically activated. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. When the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP. Deactivation of the watchdog is available as manufacturing mask option.

SPI

The SPI macrocell has been designed to be cost effective and very flexible in order to interface to the external peripherals generally present in TV applications that are often characterized by different serial input/output specifications (Audio Processors, Teletext Decoders, etc.). The reason of an hardware serial interface is that with the increasing features of the TV, in particular the newer teletext features and the greater diffusion of digital TV devices, it is necessary to be able to interface at speeds faster than those practical by software. The ST6 TV devices are designed with a serial peripheral interface which maintains the software SPI flexibility but adds hardware SPI configurations suitable for devices which typically require a greater exchange of data in the TV application. The three pins dedicated for serial data transfer (single master only) can be operated in the following ways : directly by software, as an S-BUS, as an I^2CBUS (two pins), and as an standard SPI (shift register). When using the hardware SPI, a fixed clock rate of 62.5kHz is provided which is considered a good value for TV applications.

6-BIT PWM D/A CONVERTER AND 62.5 OUTPUT

The D/A macrocell offers four PWM D/A outputs (31.2Khz repetition) with six bit resolution and with possibilities to disable the PWM in order to use the pins as standard open drain outputs. In addition a 62.5KHz output pin is available. Also this function which can be disabled and the line can be used as a standard open drain output.

AFC, KB, BAND SWITCH

This macrocell contains many dedicated functions for TV applications :

- An A/D converter with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution.
- A keyboard input register of three bits which provides three inputs lines dedicated to keyboard scanning. These lines are CMOS levels compatible with an on-chip 100Kohm pull-up resistor.
- Band switch select outputs. These pins are provided to select up to 4 tuning bands and have an open-drain (13.2V drive) output configuration.

PLL

This macrocell contains a phase-locked loop (PLL) synthesizer with a 14 bit (option 15-bit) programmable divider. The dividing ratio is given by the value loaded in the PLL data registers. The PLL operates with a tuning resolution frequency of 976.5Hz (488.2Hz and 1.95KHz available as options). The PLL input is capacitively coupled with the signal coming from an external 64 divider. The maximum input frequency is 16MHz and the minimum input voltage amplitude (peak to peak) is 0.5V. This on-chip peripherals is not available on ST6306/07/08.

INFRARED DIGITAL FILTER

The IR signal pre-processor is designed to be used with M3004 or M708 transmitters and with any other IR transmitter having a carrier frequency in the range 35.8-40KHz. (For details of the transmitters please refer to their specifications). The unique feature of this pre-processor is its band pass filter. It can distinguish the signal in the presence of extreme noise conditions and thus ensures a minimum number of interrupt the ST63XX core, leaving the latter to concentrate on other tasks. This celle can be bypassed by ROM mask option. In this case the INT pin is connected directly to the NMI of ST63 Core.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST63XX TV family is supported by a complete set of emulation devices. This set includes the ST63PXX piggyback devices for pin-to-pin replacement of all DIP masked devices.

The EMST63-HW/TVS hardware emulator and development system is also available offering powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST63XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS™ personal computers.

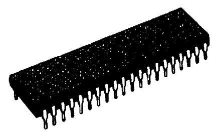
SGS-THOMSON MICROELECTRONICS

ST6326/27/28 ST6336/37/38

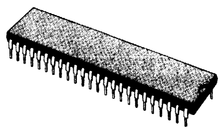
8-BIT HCMOS MCUs FOR TV FREQUENCY SYNTHESIS WITH OSD

ADVANCE DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 8192 BYTES
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 PIN DIP PACKAGES
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL, ST6336/37/38 ONLY, ST6326/27/28 HAVE MORE I/Os)
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR
- 18/20/24 (ST6326/27/28) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 6 (ST6326) OR 8 (ST6327/28) DIRECT LED DRIVING OUTPUTS
- 18/20/24 (ST6336/37/38) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 6 (ST6336) OR 8 (ST6337/38) DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/I^{2}CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR



PDIP-40



PDIP-48

- FOUR INTERRUPT VECTORS (IR, Timer 1 & 2, OSD VSYNC)
- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- 1.625µS TCYCLE (8.0 MHz clock)
- TRUE LIFO 6-LEVEL STACK
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™ PC

This is advance data on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 1 : ST6326/27/28 Pin Configurations.

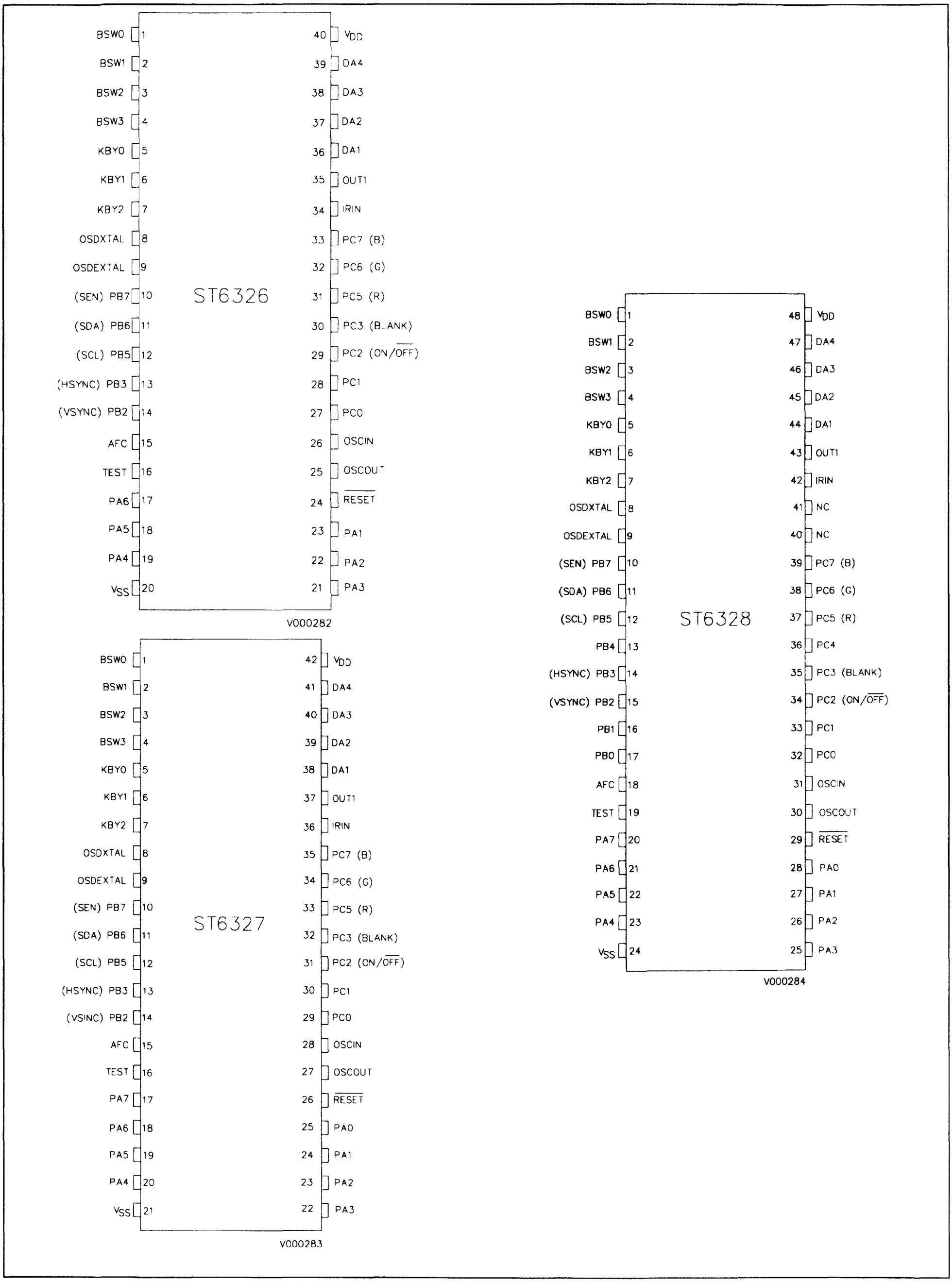
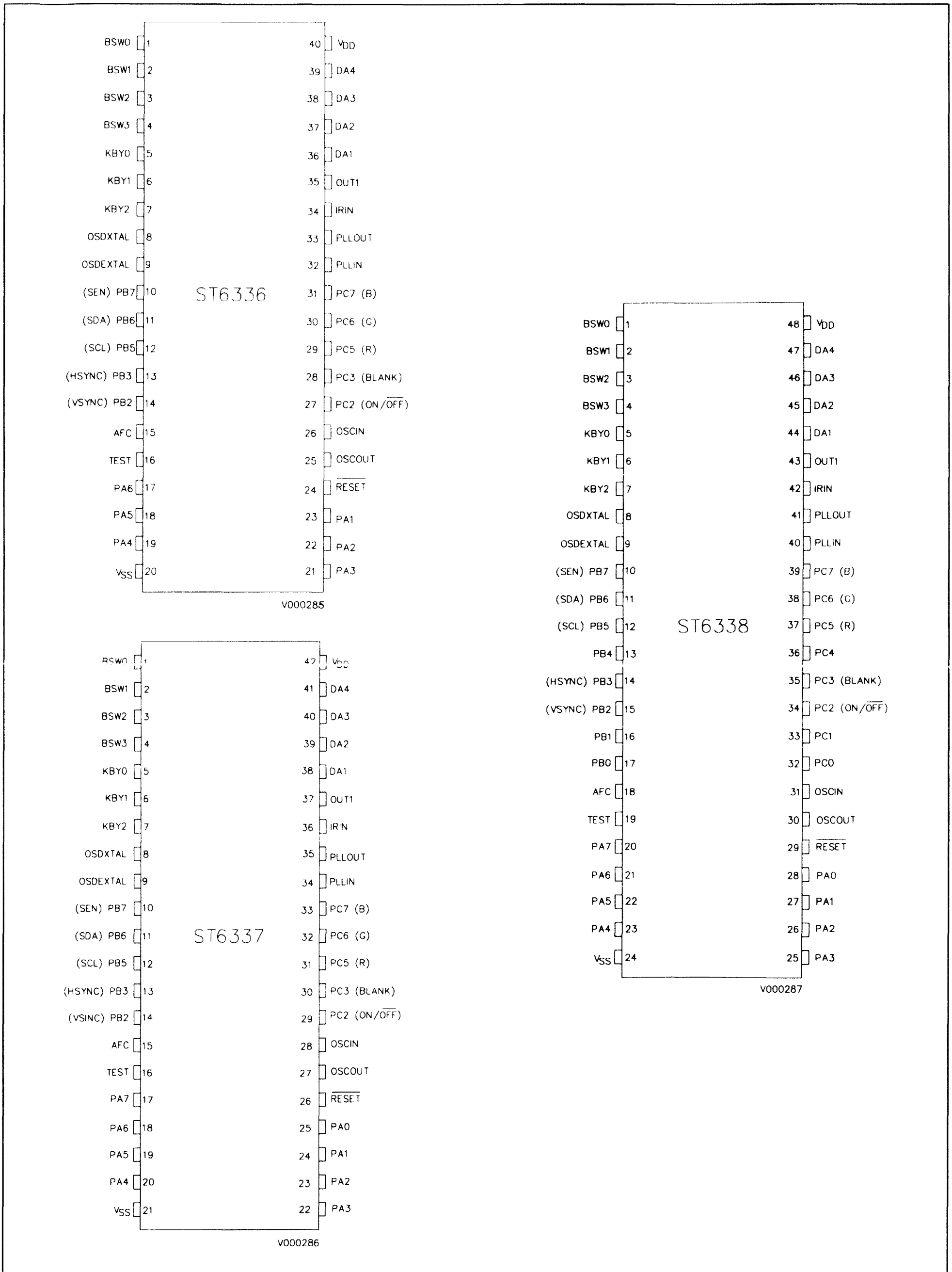


Figure 2 : ST6336/37/38 Pin Configurations.



GENERAL DESCRIPTION

The ST6326/27/28 and ST6336/37/38 microcontrollers are powerful members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST6326/27/28 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 5 lines by 15 columns On-screen display generator (OSD), four 6-Bit PWM D/A Converters, an AFC A/D converter with 0.5V resolution. The ST6336/37/38 have the same configuration plus an on-chip 14/15 bit Phase Locked Loop peripheral. In addition all these devices have 128 bytes of on-chip EEPROM.

Figure 3 : ST6326/27/28 System Description.

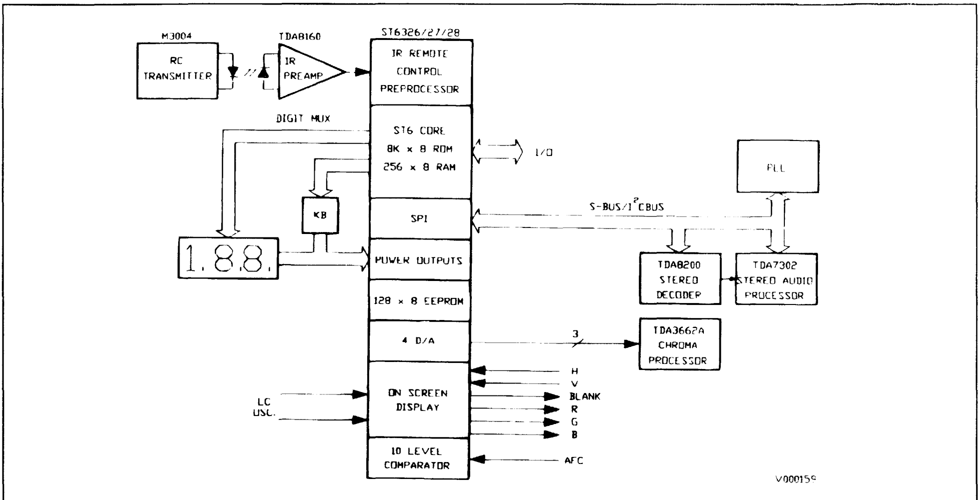
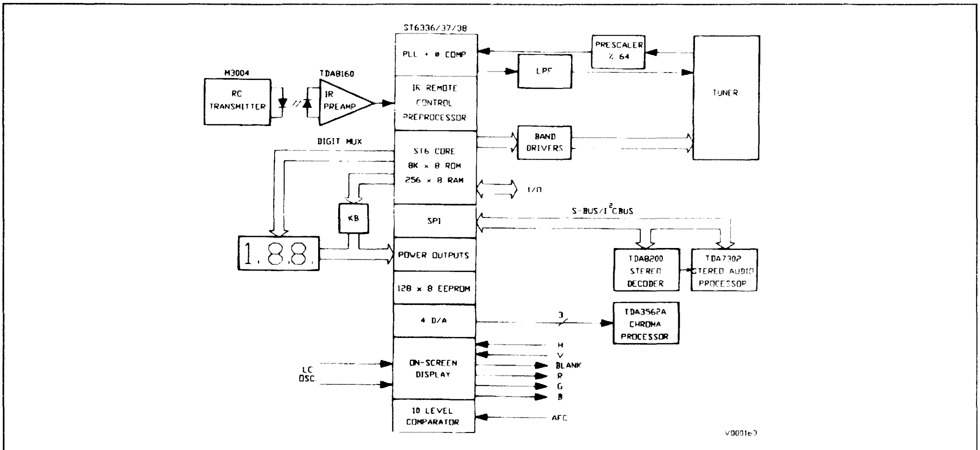


Figure 4 : ST6336/37/38 System Description.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a ceramic resonator or an external signal has to be connected between these two pins in order to allow the right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. A mask option allows the selection of a 4MHz or 8MHz oscillator frequency.

$\overline{\text{RESET}}$. The active low RESET pin is used to start the microcontroller from the beginning of its program.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode if kept high when Reset is active. This pin has to be connected to VSS for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has an open-drain (13.2V max) output configuration with direct LED driving capability (30mA, 1V). PA0 and PA7 are not available on ST6326/36.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option.

PB2 and PB3 lines are connected to the VSYNC and HSYNC control signals of the OSD cell; to provide the right signals to the OSD these I/O lines should be programmed in input mode and the user can read "on the fly" the state of VSYNC and HSYNC signals. PB2 is connected with the vertical synchronization signal VSYNC input. The active polarity of this signal is software controlled. PB3 is connected with the horizontal synchronization signal input HSYNC. Oscillator is synchronous with the change to low state. Oscillation stops while signal is in the high state. A ROM mask option is available to change the polarity of this signal.

PB5,PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCL), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). PB0, PB1 and PB4 are not available on ST6326/27/36/37.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PC3,PC5,PC6 and PC7 lines when in output modes are "ANDed" with the character and blank signals of the OSD cell. PC3 is connected with the OSD BLANK signal, PC5,PC6 and PC7 with the OSD R,G and B signals. These signals are active high. PC2 is also used as TV set On-Off switch (12V drive). PC0 and PC1 are not available on ST6336/37; PC4 is not available on ST6326/27/36/37.

IRIN. This pin is the external interrupt input of the MCU and is directly connected to the infra-red signal pre-processor which allows, through a band pass filter, to reduce the number of interrupts sent to the Core. A mask option allows the direct connection of the interrupt pin to the Core non maskable interrupt line.

DA1-DA4. These pins are the four PWM D/A outputs (32KHz repetition) of the 6-bit on-chip D/A converter. The PWM function can be disabled by software; in this case these lines can be used as general purpose open-drain outputs (13.2V drive).

OUT1. This pin is the 62.5KHz output available to drive multi-standard chroma processors. This function can be disabled by software allowing the use of this pin as general purpose open-drain output (13.2V drive).

AFC. This is the input of the on-chip 10 level A/D that can be used for the AFC function. This pin is an high impedance input that can withstand signal with an amplitude up to 13.2V.

BSW0-BSW3. These outputs are provided to select up to 4 tuning bands. These pins have an open-drain (13.2V drive) output configuration.

KBY0-KBY2. These input pins are intended as common lines for keyboard scanning. They have CMOS level threshold and have on-chip 100Kohm pull-up resistor.

PLLIN. This is the PLL input pin. The signal coming from an external 64 divider is fed to PLLIN. Maximum input frequency is 16MHz and minimum required signal amplitude is 500mVpp. The PLL peripheral is not available in the ST6326/27/28 types.

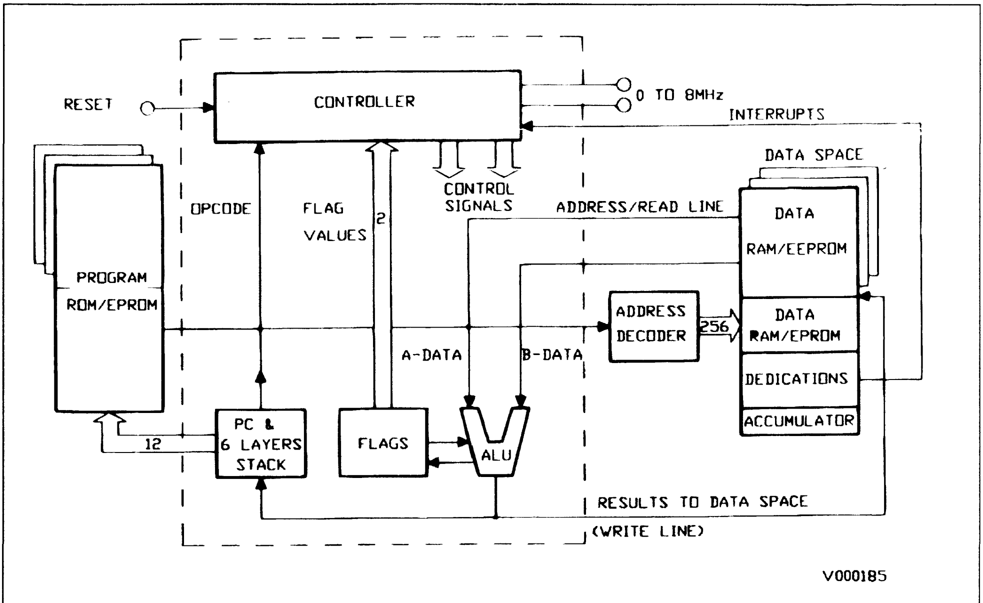
PLLOUT. This is the PLL output pin. This three-state output generates tuning correction pulses at the comparison frequency of 976.5Hz (488.2 and 1.95kHz optionally selectable). The PLL peripheral is not available in the ST6326/27/28 types.

ODSXTAL, OSDEXTAL. These pins are the OSD oscillator terminals. To these pins an oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

ST63XX CORE

The ultra small and fast Micro-Core of the ST63XX TV chips microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST63XX Core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. Three pairs of flags monitor the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 5 : ST63XX Core Block Diagram.



PROGRAM ROM PAGING

ST63XX has 12 address bits for program ROM, thus giving a program address space of 4 Kbytes. In the highest twelve bytes of the ROM are located the restart and INT vectors. To go beyond the 4K limit, the lower half of the program address space (0..7FFH) has been used as paged address space, the current page being selected by a banking register. Only the lower part of address space has been bank-switched because of interrupt (vectors and drivers) and common subroutines, that should be available all the time.

DATA ROM WINDOWING

Data ROM is physically the same ROM as for program space. Simply, it is possible to read as data all the program ROM space with the range 40H..7FH of the data address space and the contents of the Data ROM Window Register. The six least significant bits of data address space become the least significant address bits of the program ROM address to be build. This only when addressing the data space locations mentioned above. The bits coming out from Data ROM Window register become the most significant ones; they are 6 if the program ROM is of 4 Kbytes, 7 if 8 Kbytes. So, when addressing location 40H of data space, and 0 is loaded in the register, the physical location addressed is at location 0.

PAGED RAM ADDRESS RANGE

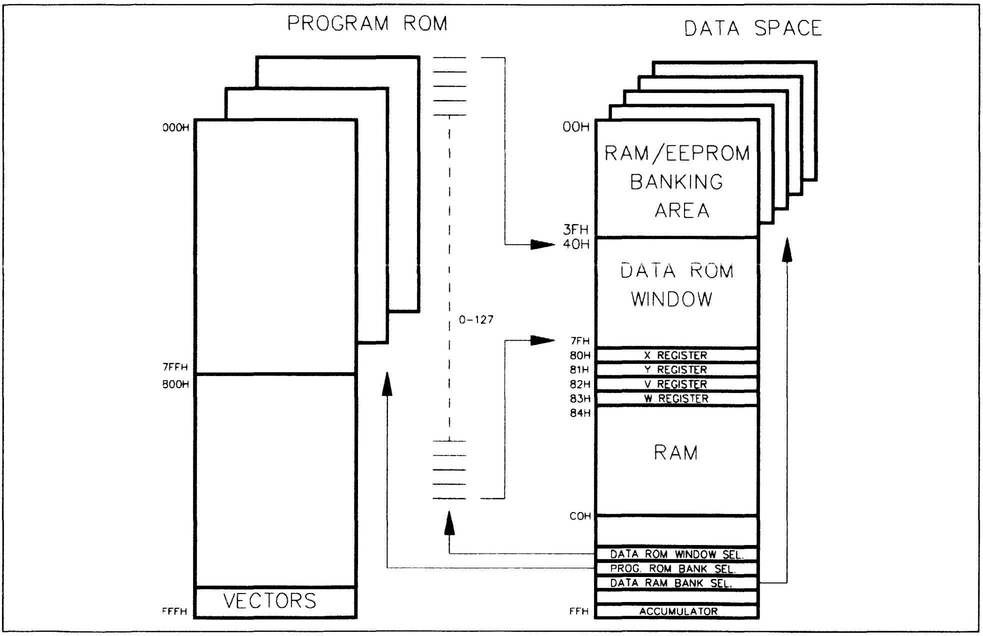
A 64 bytes range inside the data space is paged to allow extension of the RAM memory available for the user. Paged RAM address range can be switched to address up to 8 different 64 bytes pages, in which any kind of memory and/or additional control registers can be mapped. On ST6326/27/28 and ST6336/37/38 three pages of general purpose RAM plus two additional pages for ODS data/control registers are available. The 192 bytes of general purpose paged RAM plus 64 Bytes of non-paged RAM give a total of 256 RAM bytes available for the user.

EEPROM

128 bytes of EEPROM are available to store normalized TV audio and video user/factory values as well as 40 favorite programs. The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Any EEPROM location can be read just like any other data location, also in terms of access time.

A writing of an EEPROM location takes about 5 msec and during this time the EEPROM is not accessible by the Core. Two programming modes are available: BYTE MODE (BMODE) and PARALLEL MODE (PMODE). The BMODE is the normal way to write the EEPROM and consists in accessing one byte per time. The PMODE consists in accessing up to 8 bytes per time.

Figure 6 : ST63XX Memory Addressing Description.



I/O PORTS

Each ST63XX general I/O port normally consists of eight identical cells, each containing a separately addressable data latch and data direction latch; together they form an eight bit data register and an eight bit data direction register. The I/O uses two addresses of the data space, one for the data register and one for the data direction register. Each of the eight pins can be programmed independently as an input or as an output with various additional modes under control of the data direction register. When programmed as an input a pull-up resistor can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode; this is defined during manufacture by a program ROM mask option. One I/O port (A) has an open-drain (13.2V drive) output configuration with high current drive capability for direct LED driving.

TIMERS

Each Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes: event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register . A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG

The digital watchdog consists of a down counter that can be used to provide a controlled recovery from a software upset. The check time can be set differently for different routines within the general program. After a reset the watchdog is automatically activated. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. When the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP. Deactivation of the watchdog is available as manufacturing mask option.

ON-SCREEN DISPLAY

The ST63XX OSD is a macrocell belonging to the ST6 TV family. It is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST63XX OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and Blanking signals. The main characteristics of the cell are listed below:

- Number of display characters: 5 lines by 15 columns
- Number of character types: 64 characters
- Character size: Four character heights (18H, 36H 54H,72H), two available per screen, programmable by line
- Character format: 6x9 dots with character rounding function
- Character color: Eight colors available, programmable by word
- Display position: 64 horizontal positions by 2/fosc and 63 vertical positions by 4 H
- Word spacing: 64 positions programmable from 2/fosc to 128/fosc
- Line spacing: 63 positions programmable from 4 to 252 H.
- Background: No background, square background or fringe background programmable by word
- Background color: Two of eight colors available per screen, programmable by word.
- Display output: Three character data output terminals (R,G,B) and a Blank output terminal
- Display on/off: Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

SPI

The SPI macrocell has been designed to be cost effective and very flexible in order to interface to the external peripherals generally present in TV applications that are often characterized by different serial input/output specifications (Audio Processors, Teletext Decoders, etc.). The reason of an hardware serial interface is that with the increasing features of the TV, in particular the newer teletext features and the greater diffusion of digital TV devices, it is necessary to be able to interface at speeds faster than those practical by software. The ST6 TV devices are designed with a serial peripheral interface which maintains the software SPI flexibility but adds hardware SPI configurations suitable for devices which typically require a greater exchange of data in the TV application. The three pins dedicated for serial data transfer (single master only) can be operated in the following ways: directly by software, as an S-BUS™, as an I²CBUS™ (two pins), and as an standard SPI (shift register). When using the hardware SPI, a fixed clock rate of 62.5kHz is provided.

6-Bit PWM D/A CONVERTER and 62.5KHz output

The D/A macrocell offers four PWM D/A outputs (31.2kHz repetition) with six bit resolution and with possibilities to disable the PWM in order to use the pins as standard open drain outputs. In addition a 62.5 kHz output pin is available. Also this function can be disabled and the line can be used as a standard open drain output.

AFC, KB, Band Switch

This macrocell contains several dedicated functions for TV applications:

- An A/D converter with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5v to effectively double the resolution.
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INFRARED DIGITAL FILTER.

The IR signal pre-processor is designed to be used with M3004 or M708 transmitters and with any other IR transmitter having a carrier frequency in the range 35.8-40kHz. (For details of the transmitters please refer to their specifications). The unique feature of this pre-processor is its band pass filter. It can distinguish the signal in the presence of extreme noise conditions and thus ensures a minimum number of interrupt the ST63XX core, leaving the latter to concentrate on other tasks. This cell can be bypassed by ROM mask option. In this case the INT pin is directly connected to the NMI of ST63 Core.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST63XX TV family is completed with a set of emulation devices. This set includes the piggyback devices for pin-to-pin replacement of all DIP masked devices. In addition the ST63RT1 universal romless device is available (PLCC-84) for emulation of all the ST63XX devices. The universal romless can be used as stand alone emulation chip or in conjunction with the OSD romless emulation chip ST63RS1 (84 LLCC). The connection of an external OSD generator allows the emulation of customized charater sets.

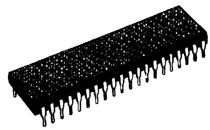
The EMST63-HW/TVS hardware emulator and development system is available, besides the piggyback devices, offering powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to shorten the total system development time of the final application. The ST63XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS™ personal computers.

ST6356/57/58

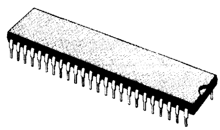
8-BIT HCMOS MCUs FOR TV VOLTAGE SYNTHESIS WITH OSD

ADVANCE DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 8192 BYTES
- DATA ROM : USER SELECTABLE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 DIP PACKAGES
- 14 BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (VS)
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR (OSD)
- 17/19/24 (ST6356/57/58) SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 6 (ST6356) OR 8 (ST6357/58) DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/I^{2}CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR
- FOUR INTERRUPT VECTORS (IR, Timer 1 & 2, OSD VSYNC)



PDIP-40

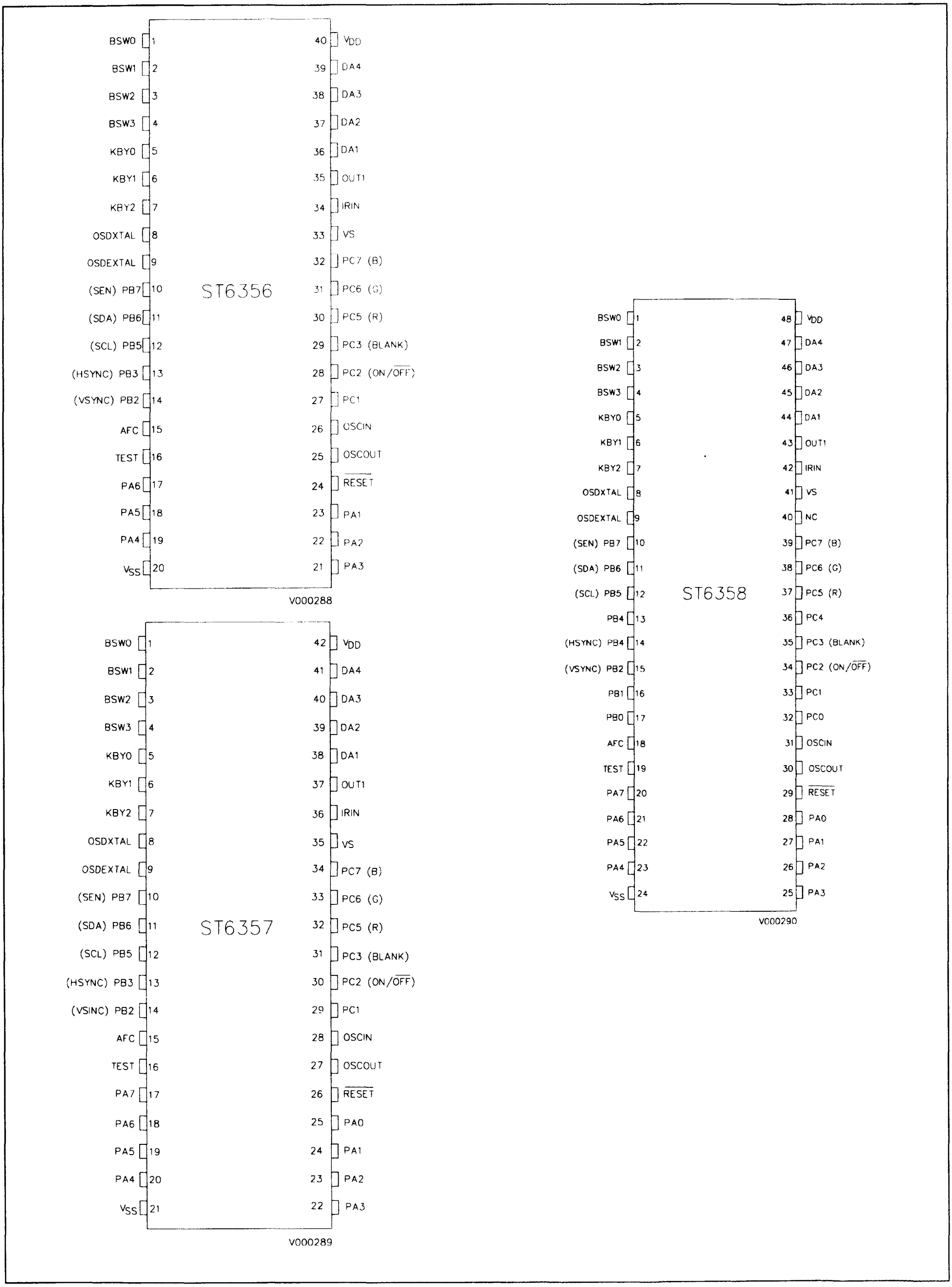


PDIP-48

- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- 1.625µS TCYCLE (8.0 MHz clock)
- TRUE LIFO 6-LEVEL STACK
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™PC

This advanced data on a new product now in development or undergoing eevaluation. Details are subject to change without notice.

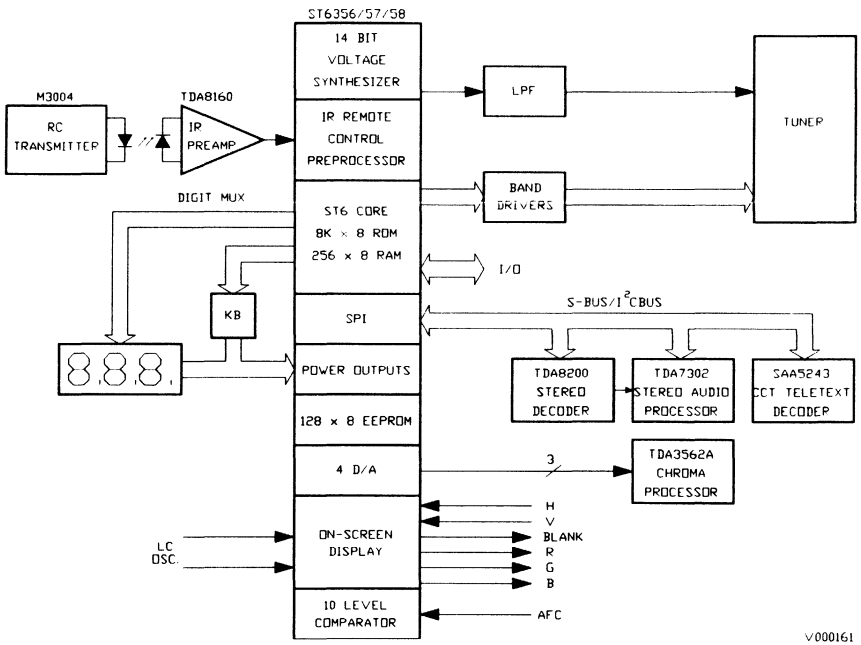
Figure 1 : ST6356/57/58 Pin Configurations



GENERAL DESCRIPTION

The ST6356/57/58 microcontrollers are powerful members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost trade-offs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The macrocells of the ST6356/57/58 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 5 lines by 15 columns On-screen display generator (OSD), four 6-Bit PWM D/A Converters, an AFC A/D converter with 0.5V resolution, a 14 bit Voltage synthesis tuning peripheral (VS). In addition all these devices have 128 bytes of on-chip EEPROM.

Figure 2 : ST6356/57/58 System Description.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are internally connected with the on-chip oscillator circuit. A crystal quartz, a ceramic resonator or an external signal has to be connected between these two pins in order to allow the right operating of the MCU. The OSCIN pin is the input pin, the OSCOUT pin is the output pin. A mask option allows the selection of a 4MHz or 8MHz oscillator frequency.

$\overline{\text{RESET}}$. The active low RESET pin is used to start the microcontroller from the beginning of its program.

TEST. The TEST (mode select) pin is used to place the MCU into special operating mode if kept high when Reset is active. This pin has to be connected to VSS for normal operation.

PA0-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has an open-drain (13.2V drive) output configuration with direct LED driving capability (30mA, 1V). PA0 and PA7 are not available on ST6356.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as input with or without internal pull-up resistor, or output. In output mode the push-pull or open-drain configuration is available as ROM mask option.

PB2 and PB3 lines are connected to the VSYNC and HSYNC control signals of the OSD cell ; to provide the right signals to the OSD these I/O lines should be programmed in input mode and the user can read "on the fly" the state of VSYNC and HSYNC signals. PB2 is connected with the vertical synchronization signal VSYNC input. The active polarity of this signal is software controlled. PB3 is connected with the horizontal synchronization signal input HSYNC. Oscillator is synchronous with the change to low state. Oscillation stops while signal is in the high state. A ROM mask option is available to change the polarity of this signal.

PB5, PB6 and PB7 lines when in output modes are "ANDed" with the SPI control signals. PB5 is connected with the SPI clock signal (SCK), PB6 with the SPI data signal (SDA) while PB7 is connected with SPI enable signal (SEN). PB0, PB1 and PB4 are not available on ST6356/57.

PC0-PC7. These 8 lines are organized as one I/O port (C). Each line may be configured under software control as input with or without internal pull-up resistor or output. In output mode the push-pull or open-drain configuration is available as ROM mask option. PC3, PC5, PC6 and PC7 lines when in output modes are "ANDed" with the character and blank signal of the OSD cell. PC3 is connected with the OSD BLANK signal, PC5, PC6 and PC7 with the OSD R, G and B signals. These signals are active high. PC2 is also used as TV set On-Off (12V drive) switch. PC0 and PC4 are not available on ST6356/57.

IRIN. This pin is the external interrupt input of the MCU and is directly connected to the infra-red signal pre-processor which allows, through a band pass filter, to reduce the number of interrupts sent to the Core. A mask option allows the direct connection of the interrupt pin to the Core non maskable interrupt line.

DA1-DA4. These pins are the four PWM D/A outputs (32KHz repetition) of the 6-bit on-chip D/A converter. The PWM function can be disabled by software ; in this case these lines can be used as general purpose open-drain outputs (13.2V drive).

OUT1. This pin is the 62.5KHz output available to drive multi-standard chroma processors. This function can be disabled by software allowing the use of this pin as general purpose open-drain output (13.2V drive).

AFC. This is the input of the on-chip 10 level A/D that can be used for the AFC function. This pin is an high impedance input that can withstand signal with an amplitude up to 13.2V.

BSW0-BSW3. These outputs are provided to select up to 4 tuning bands. These pins have an open-drain (12V drive) output configuration.

KBY0-KBY2. These inputs pins are intended as common lines for keyboard scanning. They have CMOS level threshold and have on-chip 100Kohm pull-up resistor.

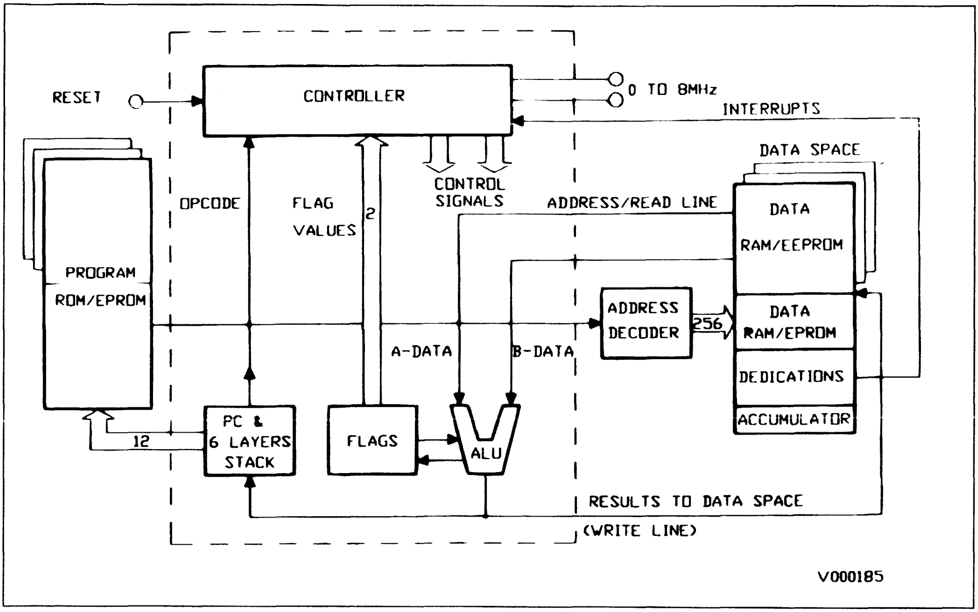
VS. This is the output pin of the on-chip 14-bit voltage synthesis tuning cell (VS). The tuning signal present at this pin gives an approximate resolution of 40KHz per step over the UHF band. This line is a push-pull output with standard drive.

ODSXTAL, OSDEXTAL. These pins are the OSD oscillator terminals. To this pins an oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

ST63XX CORE

The ultra small and fast Micro-Core of the ST63XX TV chips microcontrollers is designed to provide the economy of small die size through advanced HCMOS technologies. The ST63XX core can directly address 4 Kbyte of program memory with extension capability by 2 Kbyte bank addition. The directly addressable data space is 256 bytes sized with extension capability by 64 byte bank addition. The data ROM which is addressed in the data space is physically located in the program area. The core includes an 8-bit accumulator, two 8-bit index registers and a 12-bit program counter. These pairs of flags monitor the processor operations while a six levels LIFO hardware stack is available for subroutine & interrupt return address storage. One NMI and four normal interrupt vectors are available. STOP and WAIT modes are included to reduce overall power consumption.

Figure 3 : ST63XX Core Block Diagram.



PROGRAM ROM PAGING

ST63XX has 12 address bits for program ROM, thus giving a program address space of 4 Kbytes. In the highest twelve bytes of the ROM are located the restart and INT vectors. To go beyond the 4K limit, the lower half of the program address space (0...7FFH) has been used as paged address space, the current page being selected by a banking register. Only the lower part of address space has been bak-switched because of interrupt (vectors and drivers) and common subroutines, that should be available all the time.

DATA ROM WINDOWING

Data ROM is physically the same ROM as for program space. Simply, it is possible to read as data all the program ROM space with the range 40H..7FH of the data address space and the contents of the Data ROM Window Register. The six least significant bits of data address space become the least significant address bits of the program ROM address to the build. This only when addressing the data space locations mentioned above. The bits coming out from Data ROM Window register become the most significant ones ; they are 6 if the program ROM is of 4 Kbytes, 7 if 8 Kbytes. So, when addressing location 40H of data space, and 0 is loaded in the register, the physical location addressed is at location 0.

PAGED RAM ADDRESS RANGE

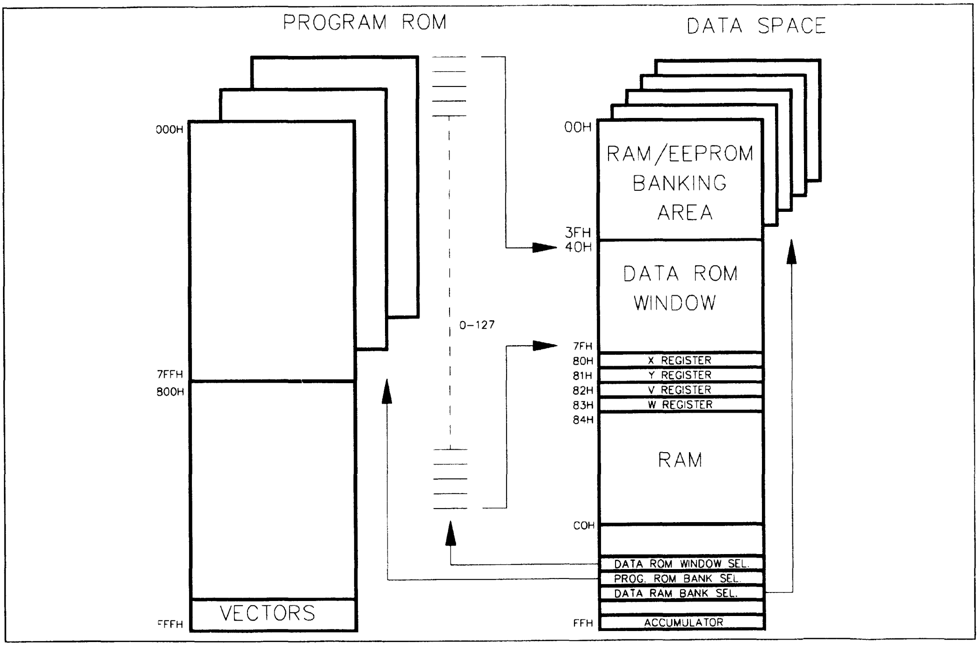
A 64 bytes range inside the data space is paged to allow extension of the RAM memory available for the user. Paged RAM address range can be switched to address up to 8 different 64 bytes pages, in which any kind of memory and/or additional control registers can be mapped. On ST6356/57/58 three pages of general purpose RAM plus two additional pages for ODS data/control registers are available. The 192 bytes of general purpose paged RAM plus 64 Bytes of non-paged RAM give a total of 256 RAM bytes available for the user.

EEPROM

128 bytes of EEPROM are available to store normalized TV audio and video user/factory values as well as 40 favorite programs. The EEPROM is physically organized in 32 byte modules (2 modules per page) and does not require dedicated instructions to be accessed in reading or writing. Any EEPROM location can be read just like any other data location, also in terms of access time.

A writing of an EEPROM location takes about 5msec and during this time the EEPROM is not accessible by the Core. Two programming modes are available : BYTE MODE (BMODE) and PARALLEL MODE (PMODE). The BMODE is the normal way to write the EEPROM and consists in accessing one byte per time. The PMODE consists in accessing up to 8 bytes per time.

Figure 4 : ST63XX Memory Addressing Description.



I/O PORTS

Each ST63XX general I/O port normally consists of eight identical cells, each containing a separately addressable data latch and data direction latch ; together they form an eight bit data register and an eight bit data direction register. The I/O uses two addresses of the data space, one for the data register and one for the data direction register. Each of the eight pins can be programmed independently as an input or as an output with various additional modes under control of the data direction register. When programmed as an input a pull-up resistor can be switched active under program control. When programmed as an output the I/O port will operate either in the push-pull mode or the open-drain mode ; this is defined during manufacture by a program ROM mask option. One I/O port (A) has an open-drain (13.2V drive) output configuration with high current drive capability for direct LED driving.

TIMERS

Each Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and a control logic that allows configuring the peripheral in three operating modes : event counter, input gated and output modes. The content of the 8-bit counter can be read/written in the Timer/Counter register. The state of the 7-bit prescaler can be read in the prescaler register. A maskable interrupt is associated with the end-of-count.

DIGITAL WATCHDOG

The digital watchdog consists of a down counter that can be used to provide a controlled recovery from a software upset. The check time can be set differently for different routines within the general program. After a reset the watchdog is automatically activated. Once the watchdog is enabled it can not be cleared by software without generating a Reset. The reset is prevented if the register is reloaded with the desired value before the watchdog register time-out. When the watchdog is active the STOP instruction is deactivated and a WAIT instruction is automatically executed instead of the STOP. Deactivation of the watchdog is available as manufacturing mask option.

ON-SCREEN DISPLAY

The ST63XX OSD is a macrocell belonging to the ST6 TV family. It is a CMOS LSI character generator which enable display of characters and symbols on the TV screen. The character rounding function enhances the readability of the characters. The ST63XX OSD receives horizontal and vertical synchronization signal and outputs screen information via R, G, B and Blanking signals. The main characteristics of the celle are listed below :

- Number of display characters : 5 lines by 15 columns
- Number of character types : 64 characters
- Character size : Four character heights (18H, 36H, 54H, 72H), two available per screen, programmable by line
- Charactyer format : 6x9 dots with character rounding function
- Character color : Eight colors available, programmable by word.
- Display position : 64 horizontal positions by 2/fosc and 63 vertical positions by 4H
- Word spacing : 64 positions programmable from 2/fosc to 128/fosc
- Line spacing : 63 positions programmable from 4 to 252H
- Background : No background, square background or fringe background programmable by word
- Background color : Two of eight colors available per screen, programmable by word.
- Display output : Three character data output terminals (R, G, B) and a blank output terminal
- Display on/off : Display data may be programmed on or off by word or entire screen. Entire screen may be blanked.

SPI

The SPI macrocell has been designed to be cost effective and very flexible in order to interface to the external peripherals generally present in TV application that are often characterized by different serial input/output specification (Audio Processors, Teletext Decoders, etc.). The reason of an hardware serial interface is that with the increasing features of the TV, in particular the newer teletext and the greater diffusion of digital TV devices, it is necessary to be able to interface at speeds faster than those practical by software. The ST6 TV devices are designed with a serial peripheral interface which maintains the software SPI flexibility but adds hardware SPI configurations suitable for devices which typically require a greater exchange of data in the TV application. The three pins dedicated for serial data transfer (single master only) can be operated in the following ways : directly by software, as an S-BUS™, as an I²CBUS™ (two pins), and as an standard SPI (shift register). When using the hardware SPI, a fixed clock rate of 62.5kHz is provided.

6-BIT PWM D/A CONVERTER AND 62.5KHz OUTPUT

The D/A macrocell offers four PWM D/A outputs (31.2Khz repetition) with six bit resolution and with possibilities to disable the PWM in order to use the pins as standard open drain outputs. In addition a 62.5kHz output pin is available. Also this function can be disabled and the line can be used as a standard open drain output.

AFC, KB, BAND SWITCH

This macrocell contains several dedicated functions for TV applications :

- An A/D converter with five levels at intervals of 1V from 1V to 5V. The levels can all be lowered by 0.5V to effectively double the resolution.
- A keyboard input register of three bits which provides three inputs lines dedicated to keyboard scanning. These lines are CMOS levels compatible with an on-chip 100Kohm pull-up resistor.
- Band switch select outputs. These pins are provided to select up to 4 tuning bands and have an open-drain (13.2V drive) output configuration.

VOLTAGE SYNTHESIS TUNING PERIPHERAL

The voltage synthesis tuning cell consists of a 14-bit counter ; the contents of this counter are converted using PWM and BRM techniques. The 14-bit gives 16384 steps which results in a resolution of approximately 2mV over a tuning voltage of 32V ; this corresponds to a tuning resolution of about 40KHz per step in UHF band (the actual value will depend on the characteristics of the tuner).

The tuning word consists of 14 bits contained in two dedicated registers. Course tuning (PWM) is performed using the seven MSBs, while the fine tuning (BRM) is performed using the data in the seven LSBs. With all zeros loaded the output is zero ; as the tuning voltage increases from all zeros, the number of pulses in one period increases to 128 with all pulses being the same width. For values larger than 128, the PWM takes over and the number of pulses in one period stays constant at 128, but the width changes. At the other end of the scale, when almost all ones are loaded, the pulses will start to link together and the number of pulses will decrease. When all ones are loaded, the output will be almost 100% high but will have a low pulse (1/16384 of the high pulse).

In the ST63XX VS macrocell, the clock frequency for the 14 bit reference counter is 2MHz from a 4MHz input clock (a program ROM mask option is available to enable a 2MHz option from an 8MHz clock).

INFRARED DIGITAL FILTER

The IR signal pre-processor is designed to be used with M3004 or M708 transmitters and with any other IR transmitter having a carrier frequency in the range 35.8-40KHz. (For details of the transmitters please refer to their specification). The unique feature of this pre-processor is its band pass filter. It can distinguish the signal in the presence of extreme noise conditions and thus ensures a minimum number of interrupt the ST63XX core, leaving the latter to concentrate on other tasks. This cell can be bypassed by ROM mask option. In this case the INT pin is directly connected to the NMI of ST63 Core.

DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST63XX TV family is completed with a comprehensive set of emulation devices. This set includes the piggyback device for pin-to-pin replacement of all DIP masked devices In addition the ST63RT1 universal romless device (PLCC-84) is available for emulation of all ST63XX devices. The universal romless can be used as stand alone emulation chip or in conjunction with the OSD romless emulation chip ST63RS1 (84 LLCC). The connection of an external OSD generator allows the emulation of customized character sets.

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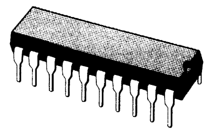
SGS-THOMSON MICROELECTRONICS

ST6398

ON-SCREEN CHARACTER GENERATOR

ADVANCE DATA

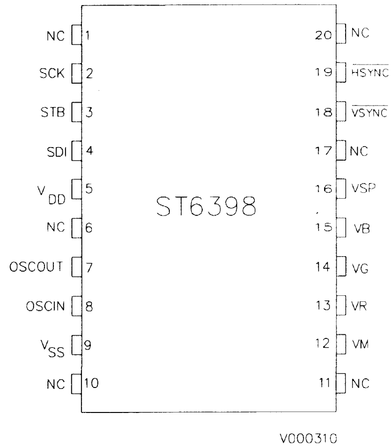
- ST63 TV FAMILY, STAND-ALONE OSD MACROCELL
- 3-WIRE SERIAL BUS INTERFACE
- HCMOS TECHNOLOGY
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4 TO 8MHZ CLOCK FREQUENCY
- 26 CHARACTERS BY 11 ROWS DISPLAY FORMAT
- SOFTWARE SELECTABLE DISPLAY POSITION
- 12H BY 18V DOTS CHARACTER MATRIX
- 8 COLOR VALUES (INCLUDING BLACK) PLUS TRANSPARENCY
- 256 ADDRESSABLE CHARACTER FONTS, 128 ROM AND 4 RAM BASIC CHARACTERS IMPLEMENTED
- 3 CHARACTER BACKGROUND TYPES, SELECTED ON A CHARACTER-BY-CHARACTER BASIS: TRANSPARENT, BGC0 OR BGC1 SOLID COLOR. THE BACKGROUND COLOR SET IS REDEFINABLE FOR THE WHOLE SCREEN
- ONE SOLID COLOR CHARACTER FOREGROUND, SELECTABLE IN A 4 FOREGROUND COLOR SET, SELECTED ON A CHARACTER-BY-CHARACTER BASIS. THE FOREGROUND COLOR IS DEFINABLE FOR THE WHOLE SCREEN. THE FOREGROUND BORDER CAN BE OUTLINED IN THE COLOR DEFINED FOR THE WHOLE SCREEN. THE FOREGROUND BORDER ENABLING IS DONE ON ROW-BY-ROW BASIS.
- INDIVIDUAL OFFSET CAN BE ADDED TO THE HORIZONTAL POSITION OF EACH ROW. THE VERTICAL POSITION OFFSET CAN BY SUPPLIED BY EITHER ADDING "N" LINES TO THE ROW OR SKIPPING THE "N" FIRST LINES



PDIP-20 (300-Mil)

- THE DISABLED ROW IS DISPLAYED IN THE SCREEN BACKGROUND COLOR AND TRANSPARENCY
- RASTER CONTROL: WHEN DISPLAY IS DISABLED THE FULL SCREEN IS DISPLAYED IN THE SCREEN BACKGROUND COLOR AND TRANSPARENCY; SCREEN COLOR SELECTABLE AMONG 8 VALUES PLUS TRANSPARENCY; DISABLED SCREEN, DISABLED ROWS AND TRANSPARENT CHARACTER BACKGROUNDS ARE DISPLAYED IN SCREEN COLOR; VME ENABLES THE CORRESPONDING TERMINAL OUTPUT TO MARK THE FOREGROUND PIXELS
- OSCILLATOR ENABLE/DISABLE FUNCTION
- 20 PIN DUAL IN LINE PACKAGE

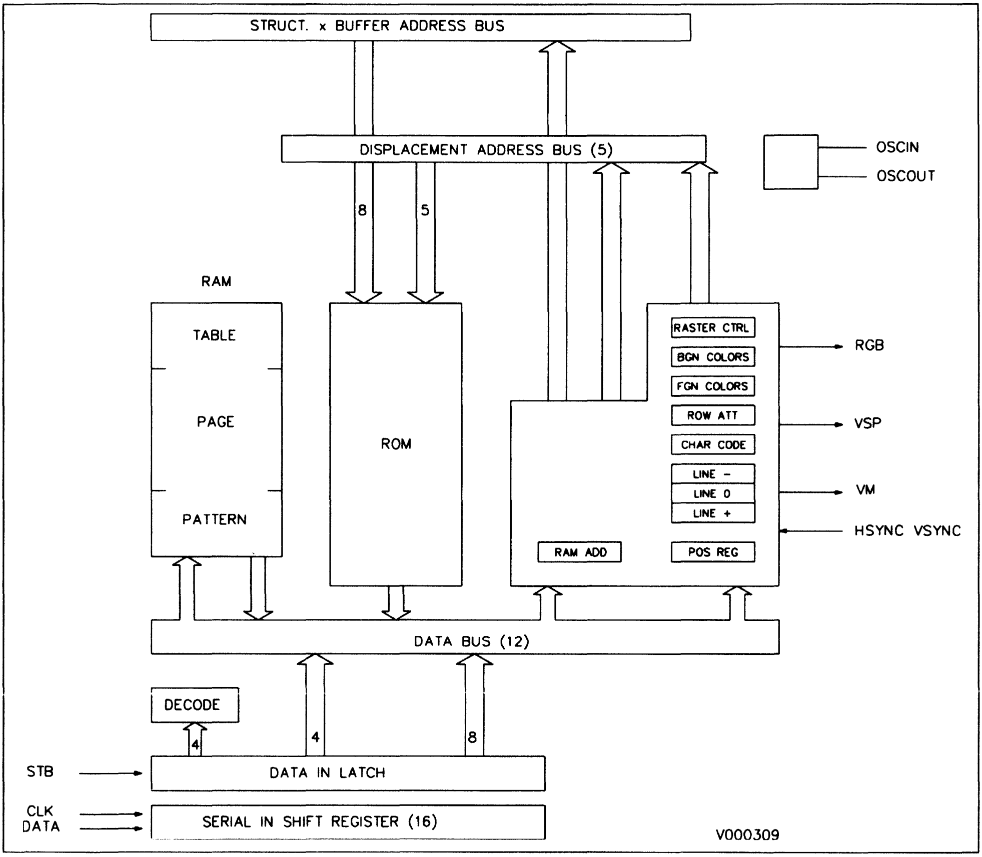
Figure 1 : ST6398 Pin Configurations.



GENERAL DESCRIPTION

The ST6398 is a stand-alone OSD generator macrocell belonging to the ST63 MCU family for TV application. Thanks to the on-chip three wire serial interface it can be easily connected to a microcontroller (ST63XX). The display character format is 26 characters x 11 rows with software selectable display position. The character matrix is 12H x 18V dots while 8 different character colors (including black) plus transparency can be selected. 256 different character fonts can be addressed with 128 ROM and 4 RAM based characters implemented. The character background is character-by-character selectable in three different modes: transparent, Background 0 or Background 1 solid color. The background color set is redefinable for the whole screen. The character foreground is character-by-character selectable out of a 4 color set. The foreground color set is redefinable for the whole screen. The foreground border may be outlined in a color defined for the whole screen. The foreground border enable is row-by-row based. An individual offset can be added to the horizontal position of each row while the vertical offset can be done either by adding "n" lines to the row or by skipping "n" first lines. When disable the row is displayed in the screen background color and transparency. The OSD oscillator can be enabled/disabled. The ST6398 is packaged in 20 pin dual-in-line package while the power supply is between 4.5V to 5.5V.

Figure 2 : ST6398 Block Diagram.



PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCIN and OSCOUT. These pins are the ST6398 oscillator terminals. To these pins an oscillation capacitor and coil network have to be connected to provide the right signal to the OSD.

SCK, SDI, STB. These pins are the serial clock, data and strobe pulse inputs of the 3-wire serial interface. Through these pins the ST6398 can be easily interfaced with the system microcontroller.

HSYNC, VSYNC. The HSYNC input pin receives the horizontal synchronization signal from the TV set while the VSYNC the vertical synchronization signal. The default active polarity is negative; the polarity of these pins is individually mask programmable.

VR, VG, VB. These output pins provides the pixel color signals (R,G,B) to the TV set. The default active polarity is positive; the polarity of these pins is individually mask programmable.

VSP. This output pin monitors the "solid" pixel signal. The default active polarity is positive; the polarity of this pin is individually mask programmable

VM. This output pin monitors the foreground output signal. The default active polarity is positive; the polarity of this pin is individually mask programmable

NC. These pins are usually not connected. These **MUST** not be connected to ground as they could be used for testing purposes.

8-BIT HCMOS PIGGYBACK MCUs FOR TV APPLICATIONS

ADVANCE DATA

- DEVICE TYPE :
  - ST63P06/7/8
  - ST63P16/7/8
  - ST63P26/7/8
  - ST63P36/7/8
  - ST63P56/7/8
- EMULATION OF ST63XX DIP MASKED DEVICES
- PIN TO PIN REPLACEMENT OF ALL ROM MASKED DEVICES
- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ CLOCK OPERATION
- PROGRAM ROM : 16K BYTES EXTERNAL
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 40/42 SHRINK/48 PIN DUAL-IN-LINE PIGGY-BACK CERAMIC PACKAGE
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL, ST63P16/7/8, ST63P36/7/8 ONLY)
- 14 BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (VS, ST63P56/7/8 only)
- SAME I/O PORT CONFIGURATION AS IN THE MASKED PRODUCTS, INCLUDING DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS I^2CBUS AND STANDARD SERIAL PROTOCOLS
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR (NOT AVAILABLE ON ST63P06/07/08 AND ST63P16/7/8)
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR
- THREE INTERRUPT VECTORS (IR, TIMER 1 & 2, ST63P06/7/8, ST63P16/7/8)
- FOUR INTERRUPT VECTORS (IR, TIMER 1 & 2, OSD VSYNC, ST63P26/7/8, ST63P36/7/8, ST63P56/7/8)
- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT AND BIT MANIPULATION INSTRUCTIONS
- 3.25µS TCYCLE (WITH 4.0 MHz CLOCK)
- TRUE LIFO 6-LEVEL STACK
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63 HW/TVS EMULATION AND DEVELOPMENT SYSTEM AND CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™ PC.

This is advance data on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 1 : ST63P06 - ST63P07 - ST63P08 Pin Configurations.

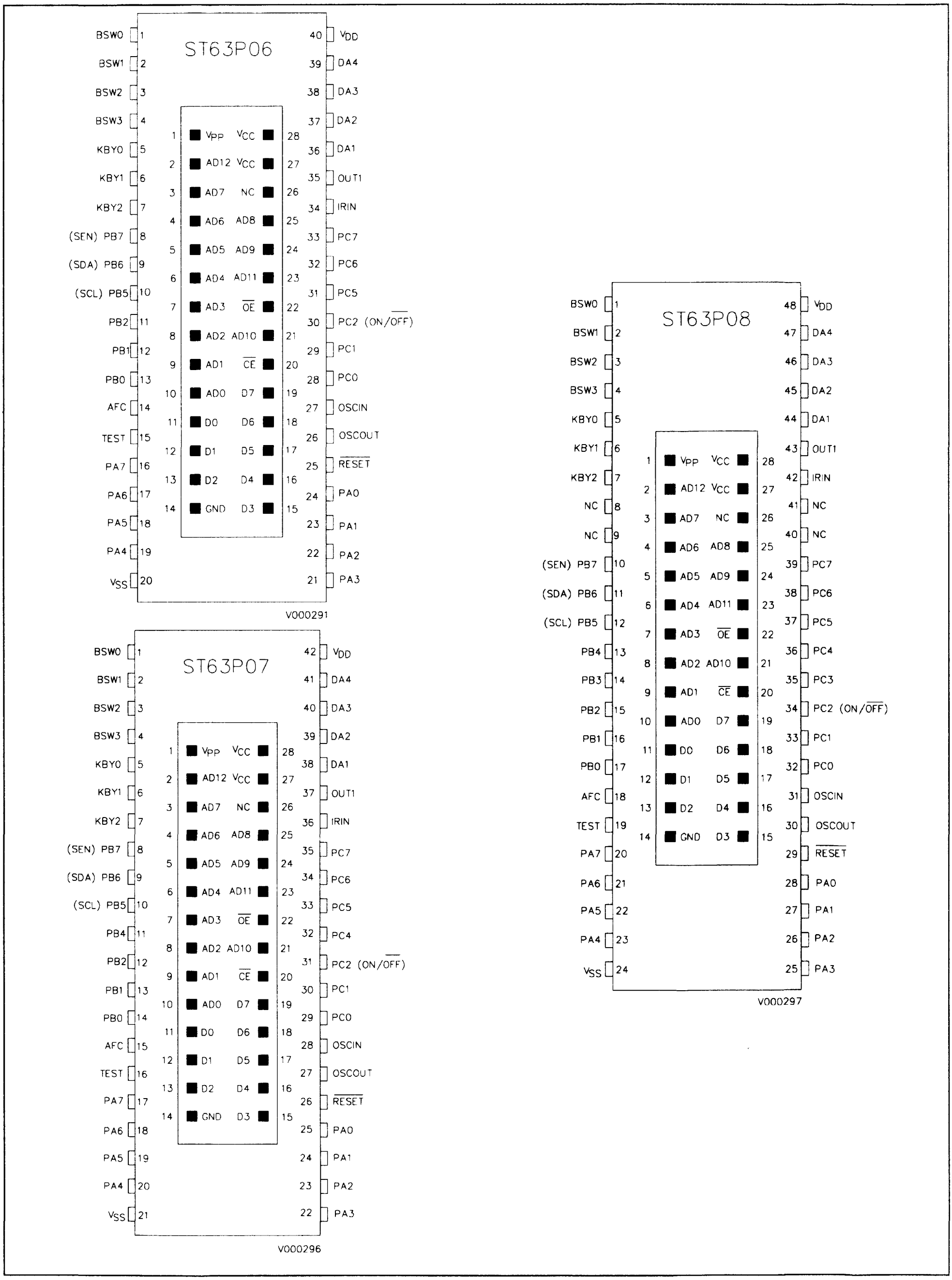


Figure 2 : ST63P16 - ST63P17 - ST63P18 Pin Configurations.

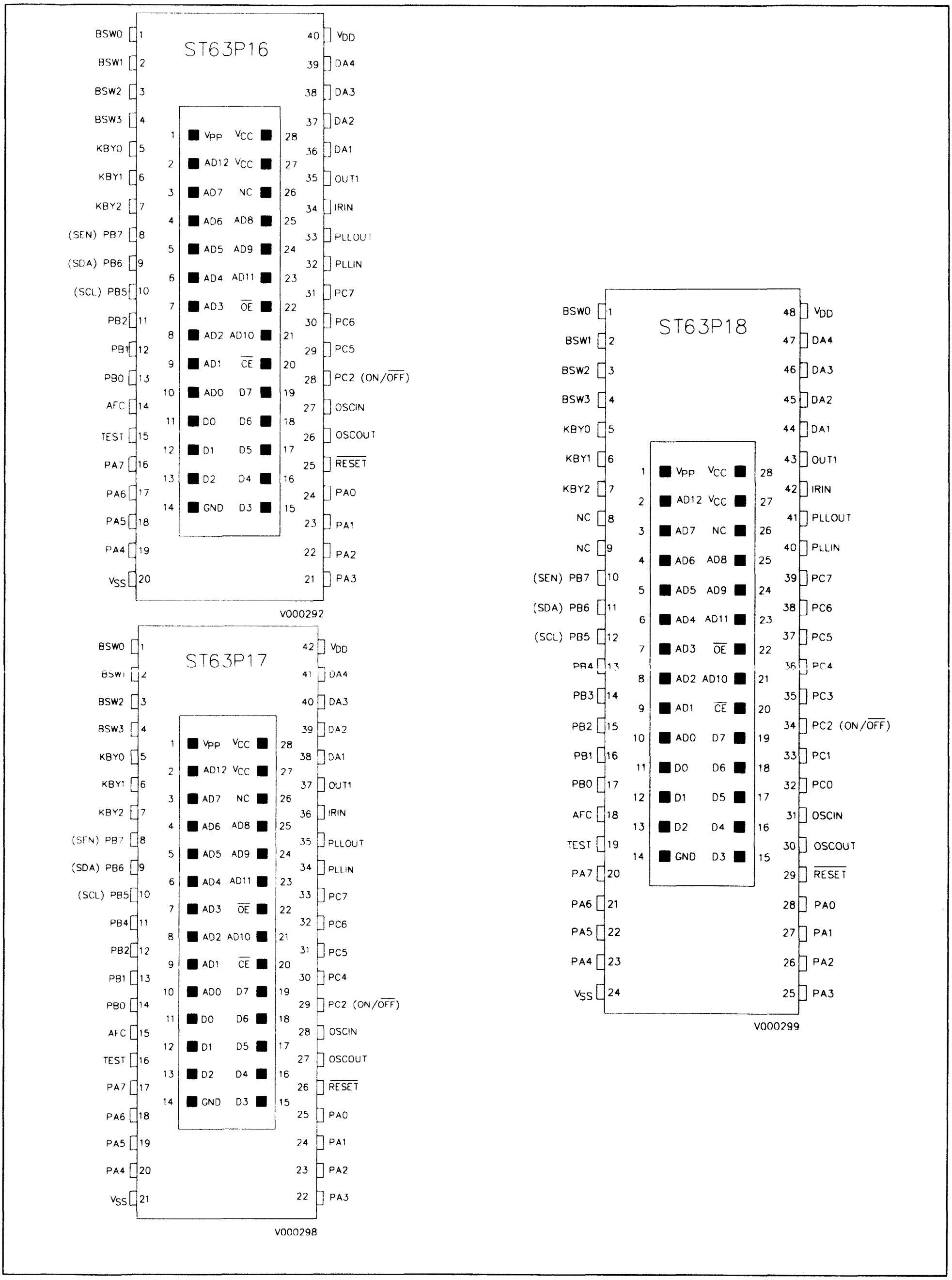


Figure 3 : ST63P26 - ST63P27 - ST63P28 Pin Configuration.

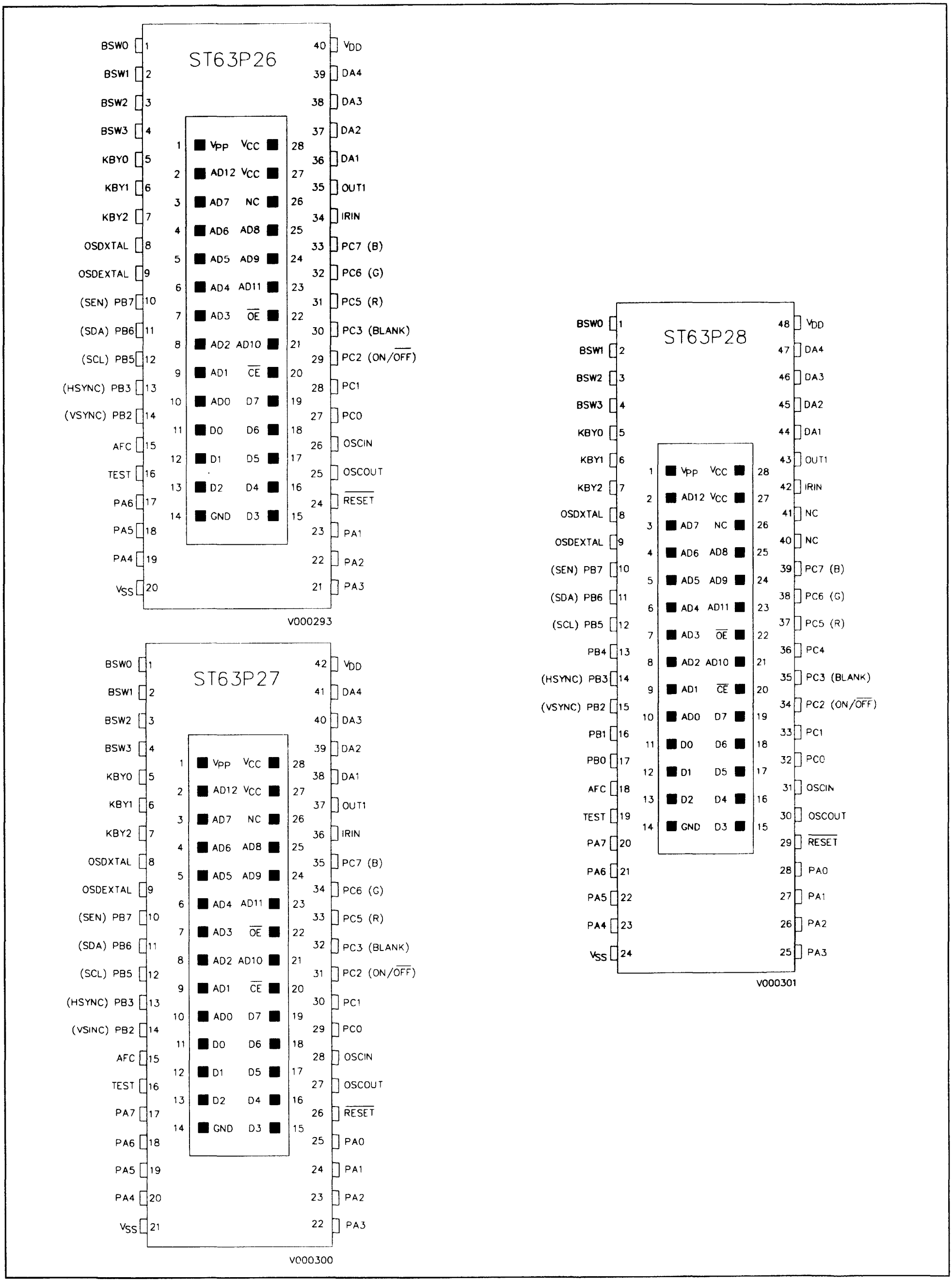


Figure 3 : ST63P36-ST63P37-ST63P38 Pin Configuration.

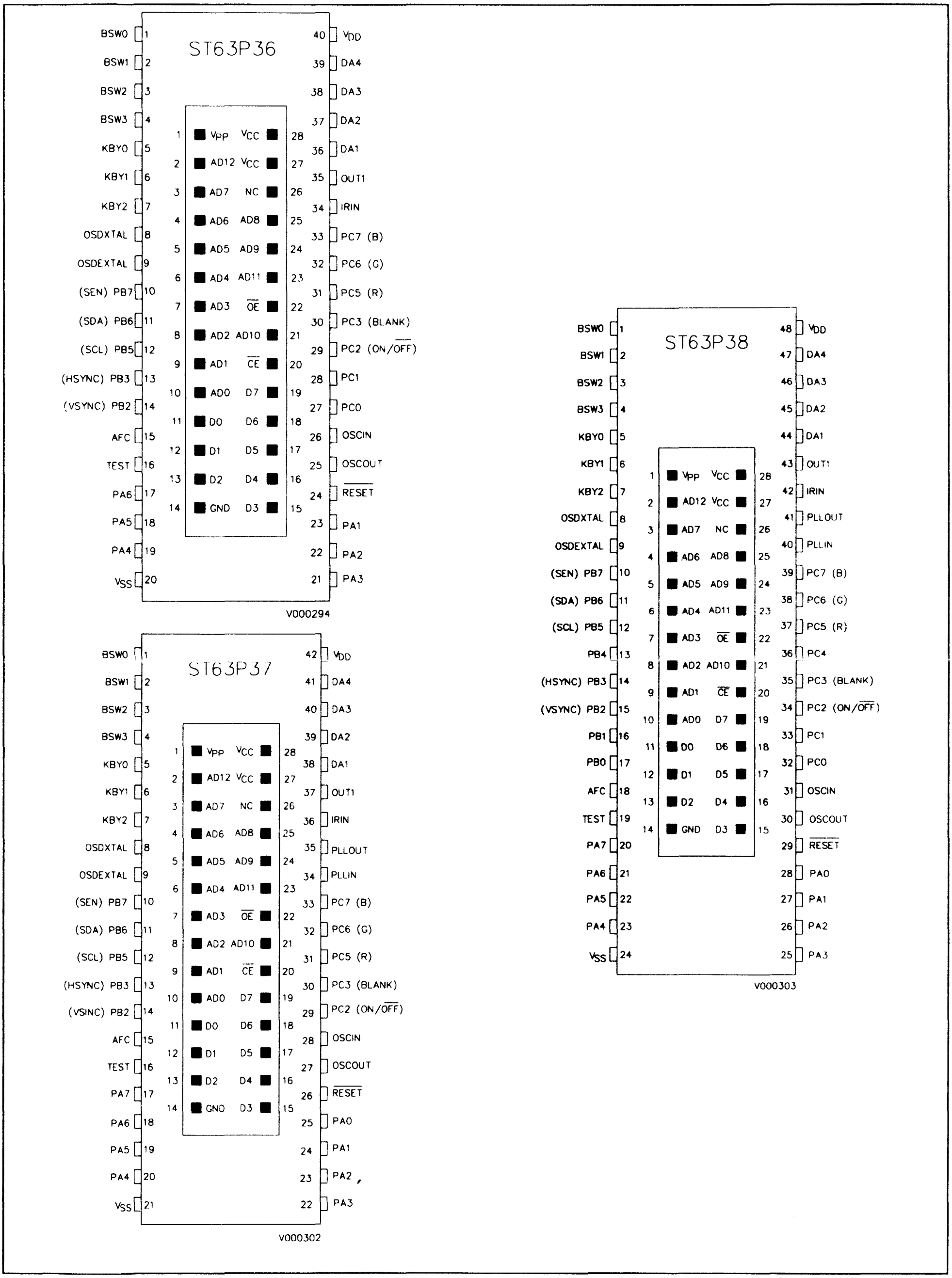
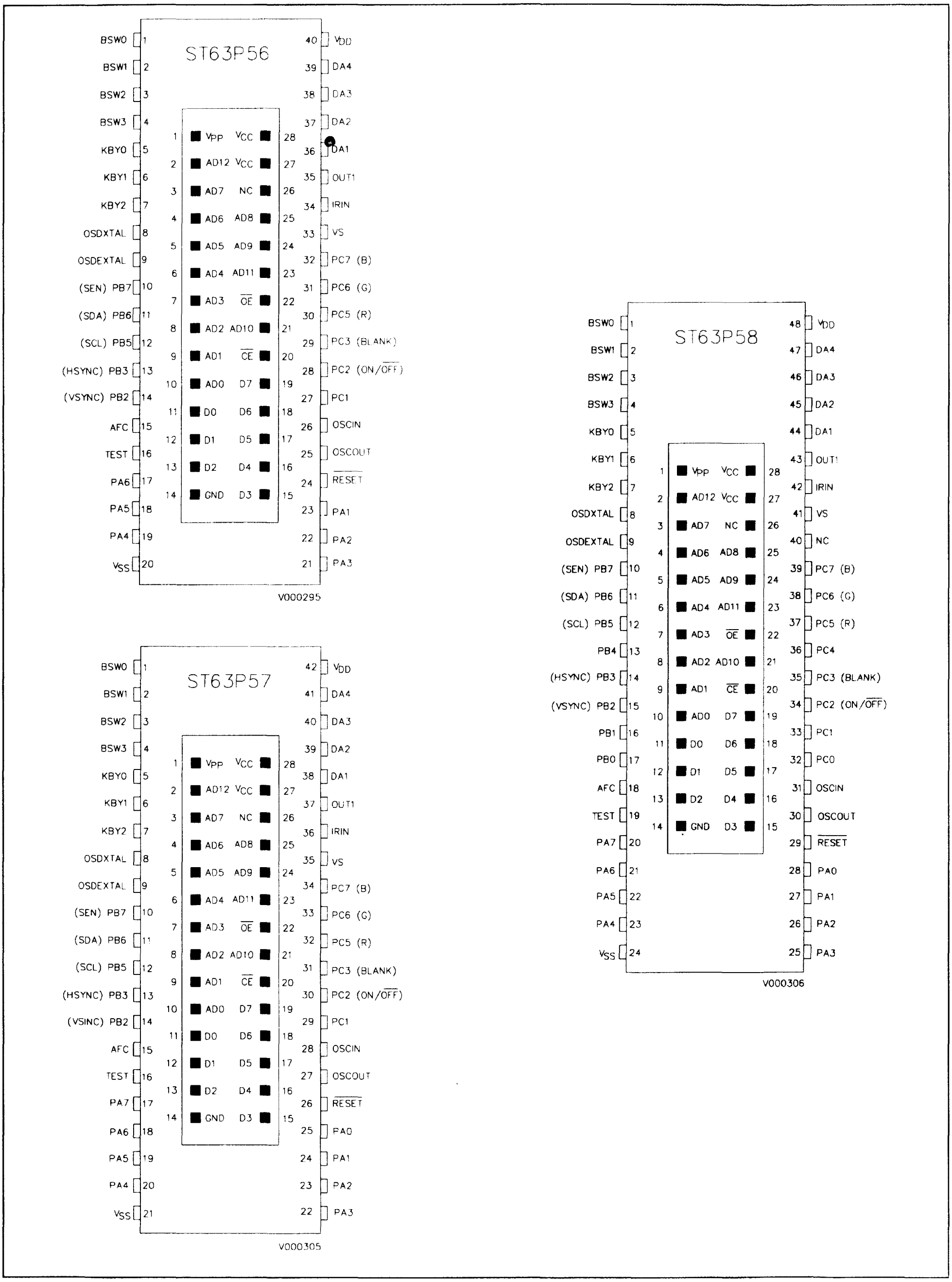


Figure 3 : ST63P56-ST63P57-ST63538 Pin Configurations.



GENERAL DESCRIPTION

The ST63PXX microcontrollers are piggyback members of the 8-bit HCMOS ST63XX family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost trade-offs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library.These peripherals are designed with the same Core technology giving full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. These piggyback devices have the same functions and pin configuration as all ROM ST63XX masked products. In the piggyback devices instead of on-chip program and data ROM, the relevant "address" and "data" lines are lead out to the 28 pin socket which is directly located on the top of the package, so that an external memory can be addressed. These piggyback devices can operate as an emulator to verify the user code, or for prototype/small volume production in order to test design concept before commitment is made to high volume production with masked ST63XX devices. The macrocells of the ST63PXX are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 5 lines by 15 columns On-screen display generator (OSD, not available on ST63P06/7/8, ST63P16/7/8), four 6-Bit PWM D/A Converters, an AFC A/D converter with 0.5V resolution, a 14 bit Phase Locked Loop peripheral (PLL, ST63P16/7/8, ST63P36/7/8 only), a 14 bit Voltage synthesis tuning peripheral (VS, ST63P56/7/8 only). In addition all these devices have 128 bytes of on-chip EEPROM. Refers to ST63XX masked devices datasheets for additional information.

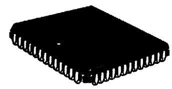
SGS-THOMSON MICROELECTRONICS

ST63RS1

8-BIT HCMOS ON-SCREEN DISPLAY ROMLESS MCU FOR TV APPLICATIONS

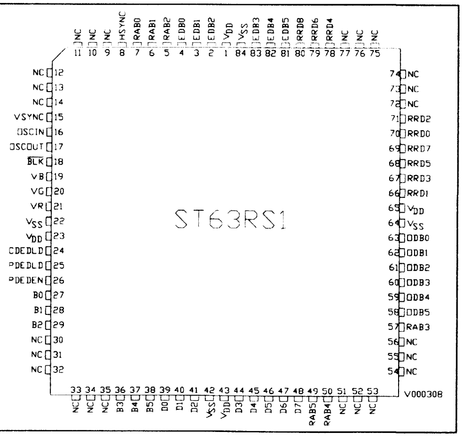
ADVANCE DATA

- ROMLESS OSD MACROCELL OF ST63XX TV FAMILY DEVICES
- CAN BE CONNECTED TO THE ST63RS1 UNIVERSAL ST63 ROMLESS DEVICE TO IMPLEMENT CUSTOM CHARACTER SETS
- 1.5μ HCMOS TECHNOLOGY
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 5 LINES BY 15 COLUMNS DISPLAY CHARACTERS
- 64 CHARACTERS TYPES
- FOUR DIFFERENT CHARACTER HEIGHTS (18H, 36H, 54H, 72H), TWO AVAILABLE PER SCREEN, PROGRAMMABLE BY LINE.
- 6X9 DOTS CHARACTER FORMAT WITH ROUNDING FUNCTION
- EIGHT COLORS AVAILABLE, PROGRAMMABLE BY WORD
- 64 HORIZONTAL DISPLAY POSITIONS BY 2/FOSC AND 63 VERTICAL POSITIONS BY 4H
- 64 WORD SPACING POSITIONS FROM 2/FOSC TO 128/FOSC
- 63 LINE SPACING POSITIONS PROGRAMMABLE FROM 4 TO 252 H
- BACKGROUND SET AS NO BACKGROUND, SQUARE BACKGROUND OR FRINGE BACKGROUND MODES, PROGRAMMABLE BY WORD
- TWO OF EIGHT BACKGROUND COLORS AVAILABLE, PROGRAMMABLE BY WORD
- THREE CHARACTER DATA OUTPUT PINS (R, G, B) AND BLANK OUTPUT PIN
- DISPLAY DATA MAY BE PROGRAMMED ON OR OFF BY WORD OR ENTIRE SCREEN. ENTIRE SCREEN MAY BE BLANKED



PLCC84

Figure 1 : ST63RS1 Pin Configuration.

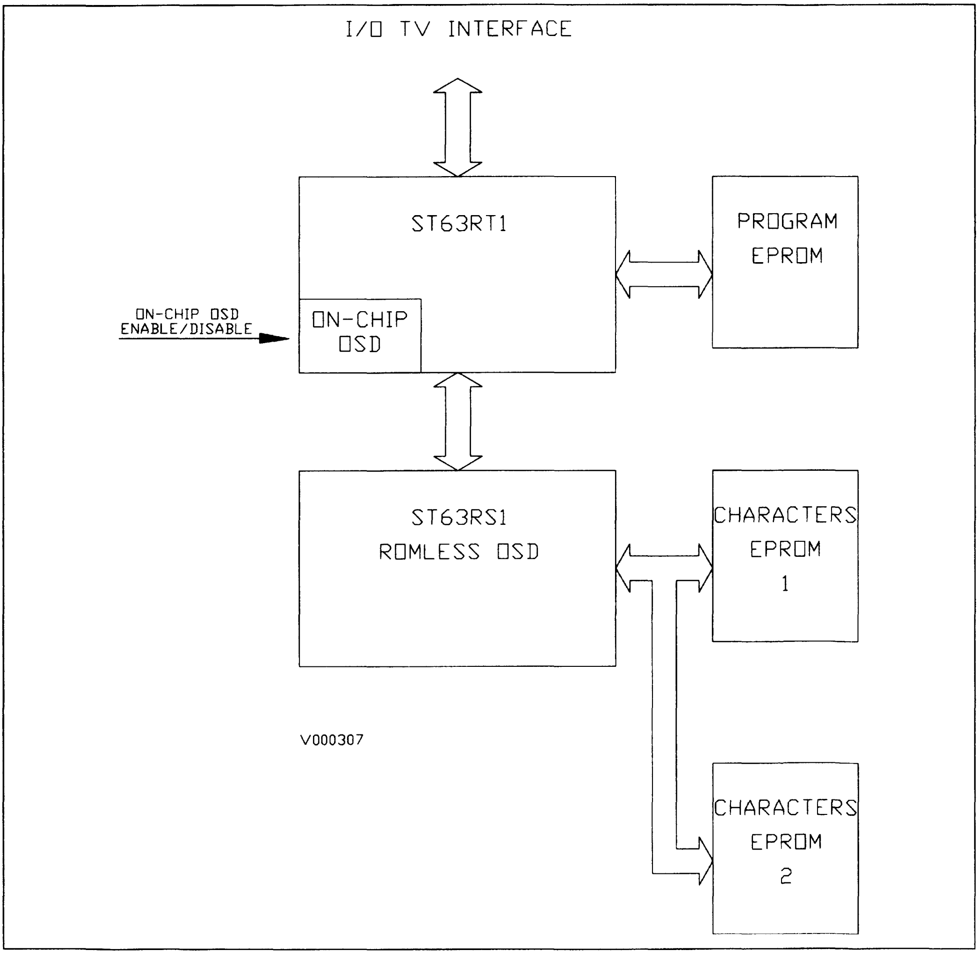


This is advance data on a new product now in development or undergoing evaluation. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST63RS1 romless On-screen display is a member of the 8-bit HCMOS ST63XX MCU family, a series of devices specially oriented to TV applications. This ST63RS1 macrocell is an HCMOS LSI character generator which enables display of characters and symbols on a TV screen. The character rounding function enhances the readability of the characters. The character set generated through the ST63RS1 is stored into two external memory EPROM devices (one for odd and one for even rows) in order to allow customized character configurations. The ST63RS1 receives horizontal and vertical synchronization signals and outputs screen information via R, G, B and Blanking dedicated pins. These devices can be used in conjunction with the ST63RT1 universal romless device to implement a complete TV set control thanks to the dedicated functions integrated into the ST63RT1. The ST63RT1 on-chip OSD should be disabled when on-screen driving is left to the external OSD. Figure 2 shows the system configuration using the ST63RT1 connected to the ST63RS1 in which the universal romless chip is devoted to the TV set control (tuning, IR decoding, etc) while the OSD romless chip is devoted to on-screen characters generation.

Figure 2 : ST63RS1 - ST63RT1 System Description.



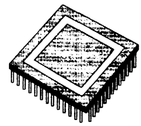
SGS-THOMSON MICROELECTRONICS

ST63RT1

8-BIT HCMOS UNIVERSAL ROMLESS MCU FOR TV APPLICATIONS

ADVANCE DATA

- UNIVERSAL ST63XX FAMILY EMULATION CHIP
- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 4.5 TO 5.5 V SUPPLY OPERATING RANGE
- 4MHZ OR 8MHZ CLOCK OPTIONS
- PROGRAM ROM : 16K BYTES EXTERNAL
- DATA ROM : USER SELECTABLE SIZE
- DATA RAM : 256 BYTES
- DATA EEPROM : 128 BYTES
- 120 CERAMIC PGA PACKAGE
- 14/15 BIT PHASE LOCKED LOOP PERIPHERAL (PLL)
- 14 BIT VOLTAGE SYNTHESIS TUNING PERIPHERAL (VS)
- ON-CHIP 5 LINES BY 15 COLUMNS ON-SCREEN-DISPLAY GENERATOR (OSD)
- THE ON-CHIP OSD CAN BE DISABLED ALLOWING DIRECT DRIVING OF AN EXTERNAL OSD GENERATOR (ST63RS1).
- 24 SOFTWARE PROGRAMMABLE GENERAL PURPOSE INPUTS/OUTPUTS, INCLUDING 8 DIRECT LED DRIVING OUTPUTS
- TWO TIMERS EACH INCLUDING AN 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER
- DIGITAL WATCHDOG FUNCTION
- SERIAL PERIPHERAL INTERFACE (SPI) SUPPORTING S-BUS/I^2CBUS AND STANDARD SERIAL PROTOCOLS
- FOUR 6-BIT PWM D/A CONVERTERS
- AFC A/D CONVERTER WITH 0.5V RESOLUTION
- INFRARED SIGNAL PRE-PROCESSOR



PGA120

- FOUR INTERRUPT VECTORS (IR, Timer 1 & 2, OSD VSYNC)
- ON-CHIP CLOCK OSCILLATOR
- ON-BOARD POWER-ON RESET CIRCUITRY
- ALL ROM TYPES ARE SUPPORTED BY PIN-TO-PIN PIGGYBACK VERSIONS.
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP AND BIT MANIPULATION INSTRUCTIONS
- 1.625µs TCYCLE (8.0 MHz clock)
- TRUE LIFO 6-LEVEL STACK
- THE DEVELOPMENT TOOL OF THE ST63XX MICROCONTROLLERS CONSISTS OF THE EMST63-HW/TVS EMULATION AND DEVELOPMENT SYSTEM CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN MS-DOS™ PC.

This is advance data on a new product now in development or undergoing evaluation. Details are subject to change without notice.

GENERAL DESCRIPTION

The ST63RT1 universal romless device is the emulation device of the 8-bit HCMOS ST63XX MCU family, a series of devices specially oriented to TV applications. Different packages and configurations are available to offer different performance/cost tradeoffs. All ST63XX members are based on a building block approach: to a common Core is associated a combination of on-chip peripherals (macrocells) available from a standard library. These peripherals are designed with the same Core technology providing full compatibility, short design and testing time. Many of these macrocells are specially dedicated to TV applications. The ST63RT1 romless device offers all the macrocells available on the different ST63 masked devices. On the ST63RT1 instead of on-chip program and data ROM, the relevant "address" and "data" lines are lead out so that an external memory can be addressed. The addressing capability of this device is 16K; in addition the on-chip OSD of the ST63RT1 can be disabled and an external OSD generator (ST63RS1) can be addressed to allow the generation of customized on-screen character sets.

The macrocells of the ST63RS1 are: two 8-bit counter with a 7-bit programmable prescaler (Timer), a Digital Watchdog Timer, a Serial Peripheral Interface (SPI), a 6-Bit PWM D/A Converter, an AFC A/D converter with 0.5V resolution, a 14/15 bit Phase Locked Loop peripheral (PLL), a 5 lines by 15 columns On-screen display generator (OSD) and a 14 bit Voltage synthesis tuning peripheral (VS). In addition 128 bytes of on-chip EEPROM are available.

Figure 1 : ST63RT1 Pin Assignment.

Pin Number	Function	Pin Number	Function	Pin Number	Function
A1	NC	F1	PC4	L1	NC
A2	RESET	F2	IDB4	L2	NC
A3	IDB6	F3	PC3/BLK	L3	NC
A4	PA2	F4	NA	L4	OUT1
A5	IDB7	F5	NA	L5	DA4
A6	AD0	F6	NA	L6	AD13
A7	AD1	F7	NA	L7	AD8
A8	D3	F8	NA	L8	AD5
A9	D2	F9	NA	L9	CDEDLD
A10	D0	F10	NA	L10	BSW3
A11	PA5	F11	PB0	L11	NC
A12	VDD	F12	PB1	L12	IAB3
A13	NC	F13	PB2/VSYN	L13	KBY0
B1	NC	G1	PC7/B	M1	NC
B2	NC	G2	PC5/R	M2	NC
B3	NC	G3	PC6/G	M3	DA1
B4	PA0	G4	NA	M4	DA3
B5	PA3	G5	NA	M5	VDD
B6	CE	G6	NA	M6	AD10
B7	D6	G7	NA	M7	AD9
B8	D4	G8	NA	M8	AD6
B9	D1	G9	NA	M9	AD2
B10	PA4	G10	NA	M10	BSW0
B11	PA6	G11	PB4	M11	NC
B12	NC	G12	PB5/SCL	M12	NC
B13	NC	G13	PB3/HSYN	M13	NC

Figure 1 : ST63RT1 Pin Assignment - Cont'ed

Pin Number	Function	Pin Number	Function	Pin Number	Function
C1	NC	H1	PLLIN	N1	NC
C2	NC	H2	IDB3	N2	IDB0
C3	NC	H3	PLLOUT	N3	DA2
C4	OSCOUT	H4	NA	N4	IAB5
C5	PA1	H5	NA	N5	AD12
C6	VSS	H6	NA	N6	AD11
C7	D7	H7	NA	N7	IAB4
C8	D5	H8	NA	N8	AD7
C9	IAB2	H9	NA	N9	AD4
C10	PA7	H10	NA	N10	AD3
C11	NC	H11	VSS	N11	BSW1
C12	NC	H12	PB7/SEN	N12	BSW2
C13	NC	H13	PB6/SDA	N13	NC
D1	PC0	J1	VS		
D2	IDB5	J2	IDB2		
D3	NC	J3	VSS		
D4	NA	J4	NA		
D5	NA	J5	NA		
D6	NA	J6	NA		
D7	NA	J7	NA		
D8	NA	J8	NA		
D9	NA	J9	NA		
D10	NA	J10	NA		
D11	NC	J11	KBY2		
D12	NC	J12	OSDOSCIN		
D13	TEST	J13	OSDOSCO		
E1	PC2-ON/$\overline{\text{OFF}}$	K1	IRIN		
E2	PC1	K2	IDB1		
E3	OSCIN	K3	NC		
E4	NA	K4	NA		
E5	NA	K5	NA		
E6	NA	K6	NA		
E7	NA	K7	NA		
E8	NA	K8	NA		
E9	NA	K9	NA		
E10	NA	K10	NA		
E11	PDEDLD	K11	NA		
E12	IAB1	K12	KBY1		
E13	AFC	K13	IAB0		

NC: Not Connected

NA: Not Available

Figure 2 : Frequency Synthesis TV System with External PLL.

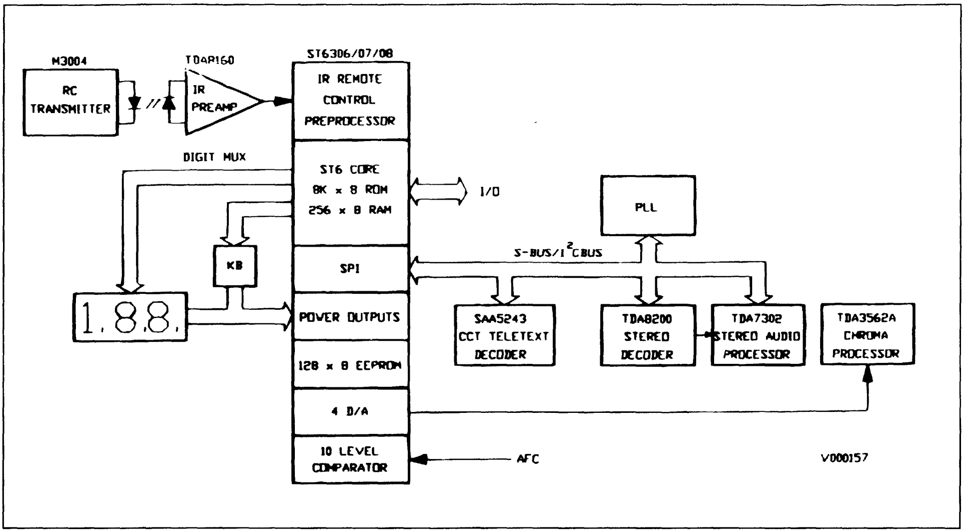


Figure 3 : Frequency Synthesis TV System with On-chip PLL and OSD.

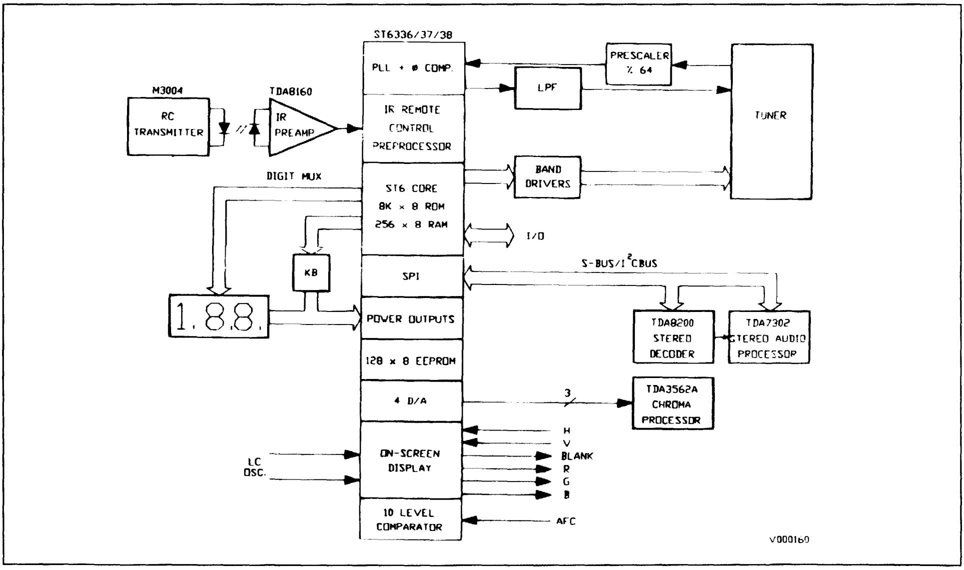


Figure 4 : Voltage Synthesis TV System with On-chip OSD.

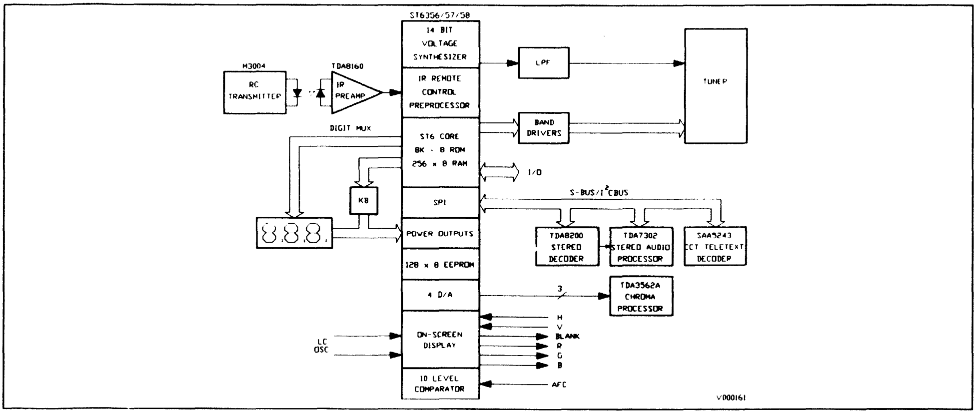
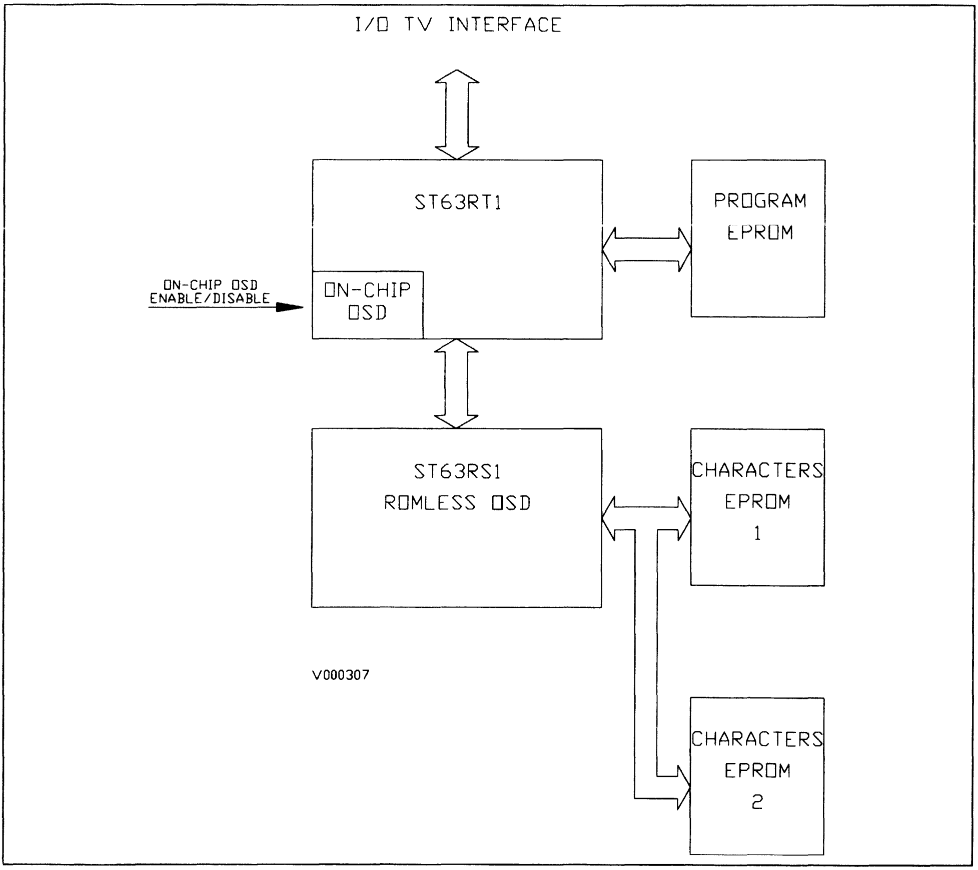


Figure 5 : ST63RT1 - ST63RS1 (OSD Generator) System Description.



SGS-THOMSON MICROELECTRONICS

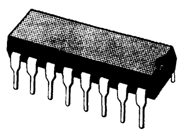
TBA920
TBA920S

LINE OSCILLATOR COMBINATION FOR TV SET

- SYNC-PULSE SEPARATION
- OPTIONAL NOISE INVERSION
- GENERATION OF A LINE FREQUENCY VOLTAGE BY MEANS OF AN OSCILLATOR
- PHASE COMPARISON BETWEEN SYNC-PULSE AND THE OSCILLATOR WAVEFORM
- PHASE COMPARISON BETWEEN THE OSCILLATOR WAVEFORM AND THE MIDDLE OF THE LINE FLY-BACK PULSE
- AUTOMATIC SWITCHING OF THE VARIABLE TRANSCONDUCTANCE AND THE VARIABLE TIME CONSTANT TO ACHIEVE NOISE SUPPRESSION AND, BY SWITCHING OFF, POSSIBILITY OF TAPE-VIDEO-REGISTERED REPRODUCTION
- SHAPING AND AMPLIFICATION OF THE OSCILLATOR WAVEFORM TO OBTAIN PULSES FOR THE CONTROL OF DRIVING STAGES IN HORIZONTAL, DEFLECTION CIRCUITS USING EITHER TRANSISTORS OR THYRISTORS

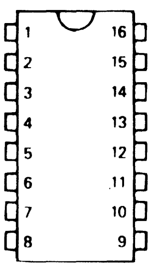
DESCRIPTION

The line oscillator combination TBA920 is a monolithic integrated circuit intended for the horizontal deflection of the black and white and colour TV sets picture tube.



TBA920-TBA920S
DIP16
(Plastic Package)

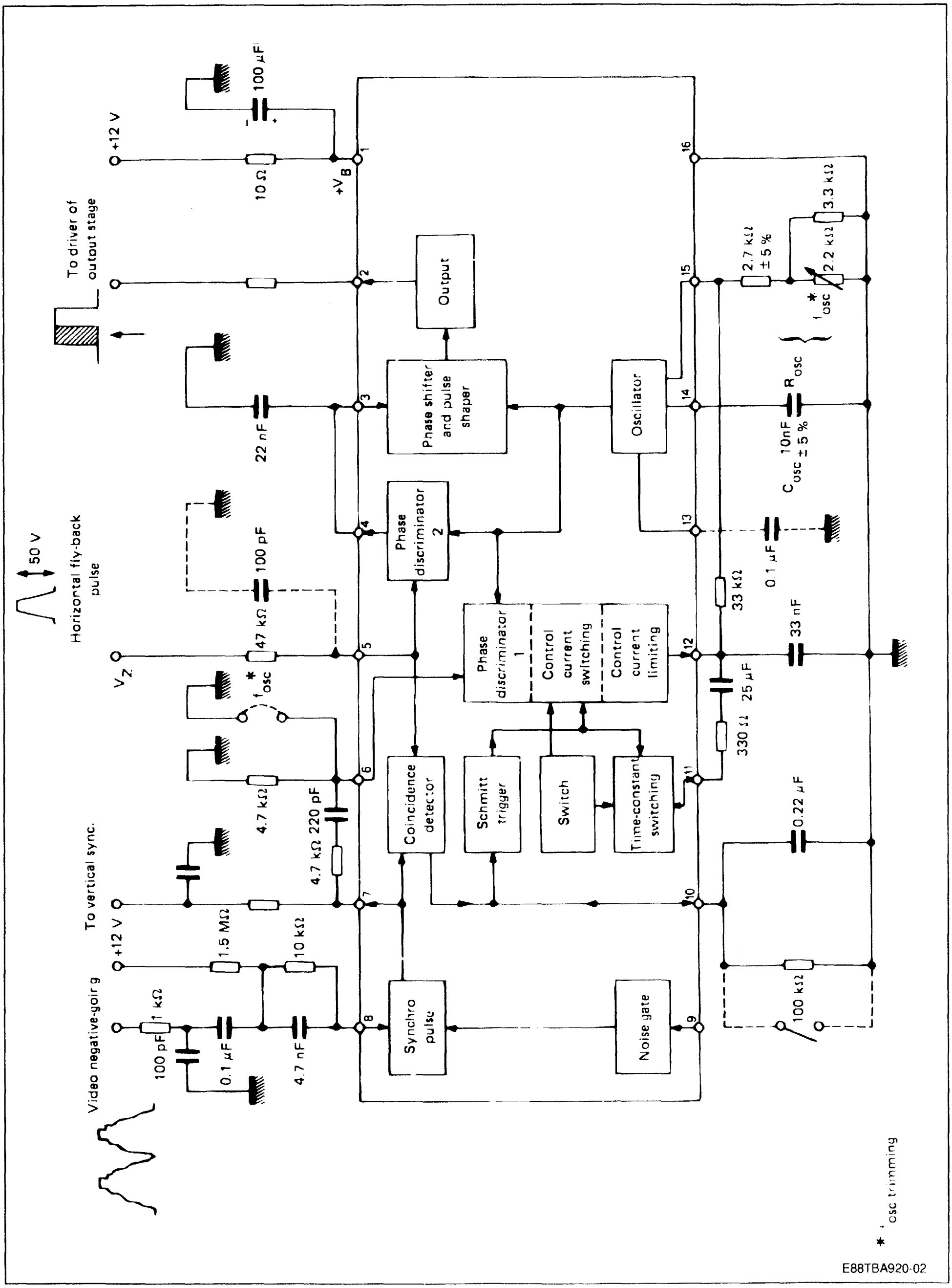
PIN CONNECTIONS



E88TBA920-01

1 - Positive supply
2 - Driver line stage pulse, driving an output stage
3 - Input control voltage for pulse width
4 - Phase discriminator output between fly-back pulse and oscillator
5 - Fly-back pulse input
6 - Synchro-pulse input
7 - Synchro pulse output
8 - Video signal input
9 - Noise gate input
10 - Switch emission-magnetoscope
11 - Time constant switch
12 - Oscillator control voltage loop
13 - Oscillator decoupling
14 - Tuning oscillator capacitor
15 - Oscillator control voltage
16 - Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage V_{1-16}	4 to 14	V
P_{tot}	Total Power Dissipation	600	mW
T_{amb}	Ambient Temperature	– 20 to 60	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 12 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_I	Video Signal (pin 8) Input Voltage (positive synchro–pulse)	1	3	7	V
I_I	Input Current			0.2	mA
I_I	Fly–back (pin 5) Input Current	0.1	1	2	mA
V_I	Input Voltage		± 0.8		V
Z_I	Input Resistance		0.4		kΩ
I_I	Noise Gate (pin 9) Input Current		20		µA
V_I	Input Voltage		0.7		V
V_O	Synchro Pulse (pin 7) Output Voltage	9	10		V
Z_O	Output Impedance on Rise Time		50		Ω
Z_O	Output Impedance on Fall Time		2.2		kΩ
I_O	Line Amplifier Output Current (peak to peak)		25	200	mA
V_O	Output Voltage	9	10		V
t_P	Output Pulse Duration (adjust by V_{3-16})	12		32	µs
	Fly–back Pulse Phase Control Delay accepted between output pulse and fly–back pulse	0		15	µs
I_O	Output Current During Fly–back Pulse		± 0.5		mA
	Line Oscillator (no synchronized) for 625 Lines		15625 ± 5 %		Hz
	At Supply Cut–off, without synchronized for 625 Lines		15625 ± 10 %		Hz
	Phase Control between Oscillator and Synchro–pulse • with Emission Pull in Range		± 1		kHz
	Keep in Range		± 1		kHz
S	Sensibility		3		kHz/µs
	• with Magnetoscope Keep in Range		± 350		Hz
	Pull in Range		± 350		Hz
S	Sensibility		± 1		kHz/µs
For TBA 9205 only					
ΔF_O	Oscillator (pin 14) Oscillator Frequency Spead R_{15-6} = 3.3 kΩ C_{14-16} = 10 nF		≤ 1.5		%
ΔF_O	Oscillator Frequency Range (figure 1 and 2)		± 5		%
Δt	Phase Position (pin 5-6) Phase spead between Front End Synch Pulse and Fly–back Pulse Center (figure 1)		≤ ± 0.4		µs

APPLICATION : EUROPEAN STANDARD 625 LINES

Figure 1.

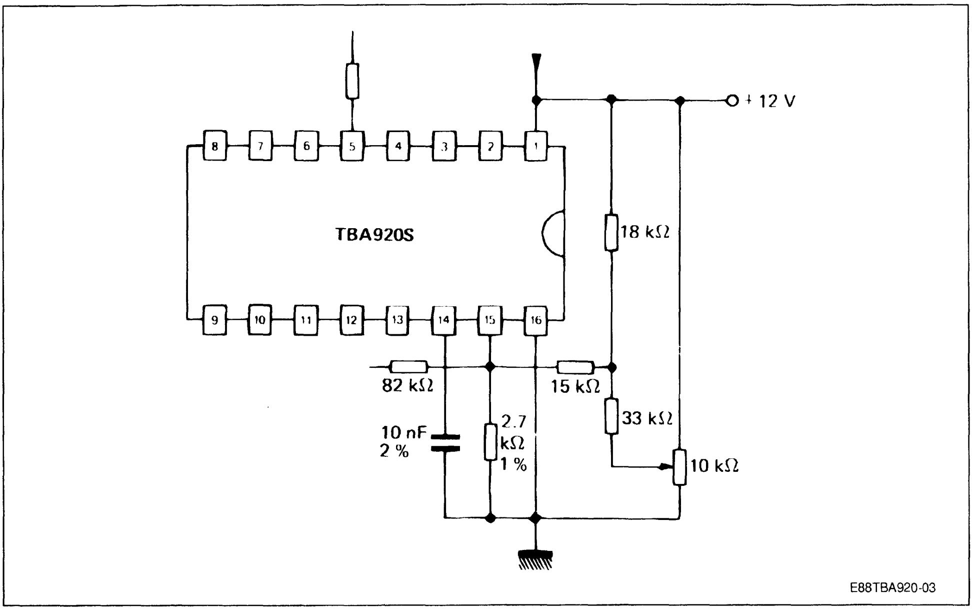
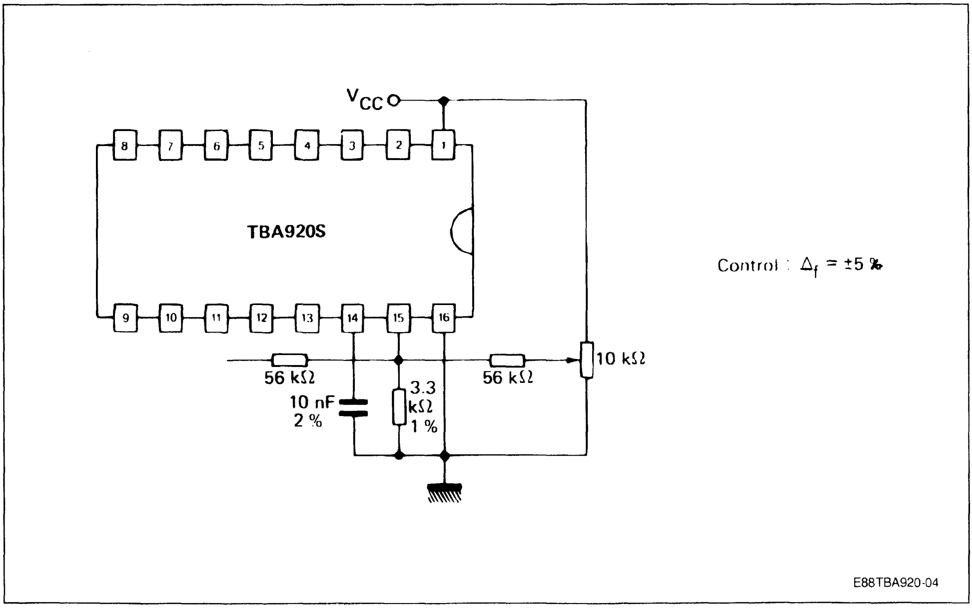
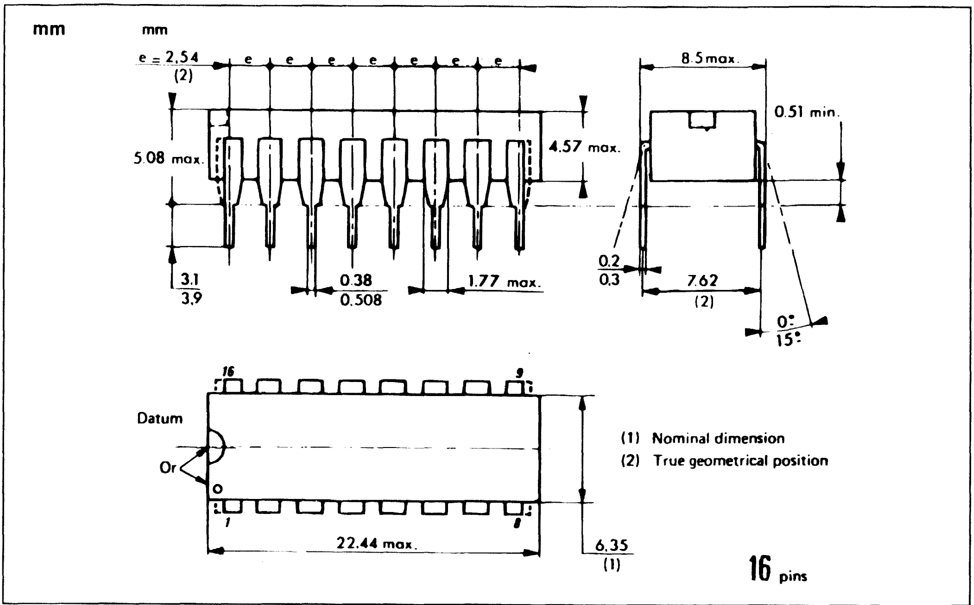


Figure 2.



PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP

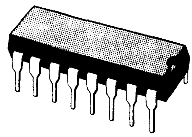


SGS-THOMSON MICROELECTRONICS

TDA440S

TV VIDEO IF SYSTEM

The functions incorporated are :
- GAIN CONTROLLED VISION IF AMPLIFIER
- SYNCHRONOUS DETECTOR
- AGC DETECTOR WITH GATING FACILITY
- AGC AMPLIFIER FOR PNP TUNER DRIVE WITH VARIABLE DELAY
- VIDEO PREAMPLIFIER WITH POSITIVE AND NEGATIVE OUTPUTS



DIP16

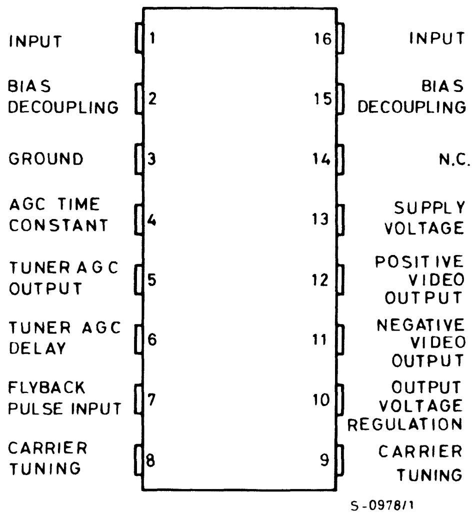
ORDER CODE : TDA440S

DESCRIPTION

The TDA440S is a monolithic integrated circuit in a 16-lead dual in-line plastic package.

It is intended for use in black and white and colour TV receivers.

CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 13)	15	V
V_5	Voltage at Pin 5	– 1 to 15	V
V_{10}	Voltage at Pin 10	3	V
V_{11}	Voltage at Pin 11 (with load connected to V_s)	8	V
I_{11}, I_{12}	Output Current	5	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	800	mW
T_{stg}	Storage Temperature	– 55 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range (pin 13)			10	12	15	V
I_s	Supply Current (pin 13)	V_s = 12 V			50		mA
$-I_{11}$ (1)	Output Current	V_s = 15 V	V_{11} = 8 V		1.6		mA
V_{11} (2)	Output Voltage	V_s = 12 V	$R_5 = \infty$			4.5	V
			R_5 = 0	7			V
V_{12} (2)	Output Voltage	V_s = 12 V	V_{11} = 5.5 V		5.6		V
$\frac{\Delta V_{11}}{\Delta V_s}$	Output Voltage Drift	V_s = 11 to 14 V			3.5		%

AC CHARACTERISTICS (refer to test circuit, V_s = 12 V, T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_5 (3)	Turner AGC Current	V_7 = 0 f_0 = 38.9 MHz	R_4 = 2.5 KΩ	6	9.5		mA
V_7	AGC Gating Pulse Input Peak Voltage	f = 15.6 KHz		– 1.5		– 5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i [4]	Input Sensitivity	$V_7 = 0$ $f_o = 38.9$ MHz $V_{11} = 3.3$ V Peak to Peak	100	150	220	µV
ΔV_i	AGC Range	$V_7 = 0$ $\Delta V_o = 1$ dB $f_o = 38.9$ MHz $V_{11} = 3.3$ V Peak to Peak	50	60		dB
V_o	Peak to Peak Output Voltage at Pin 11	$V_7 = 0$ $V_{11} = -5.5$ V $f_o = 38.9$ MHz V_i = See Note (5)	3.3	3.5	3.7	V
ΔV_o	Video Output Variation Over the AGC Range (0 to 5.5 MHz)	$V_7 = 0$ $\Delta V_i = 50$ dB $V_{11} = 3.3$ V Peak to Peak $f_o = 38.9$ MHz $f_m = 0$ to 5.5 MHz		1	2	dB
V_{11}, V_{12}	Sound IF a Video Output (5.5 MHz)	$V_7 = 0$ V_i = See Note (5) f_o (vision) = 38.9 MHz f_o (sound) = 33.4 MHz	30			mV
	Differential Error of the Output Voltage (B & W)	$V_7 = 0$ $f_o = 38.9$ MHz $V_{11} = 3.3$ V Peak to Peak			15	%
V_{11}, V_{12}	Video Carrier and Video Carrier 2nd Harmonic Leakage at Video Outputs	$V_7 = 0$ V_i = See Note (5) $f_o = 38.9$ MHz		15		mV
V_{11}, V_{12}	Video Carrier Leakage at Video Outputs			5		mV
B	Frequency Response (– 3 dB)		8	10		MHz
d_{im}	Intermodulation Products at Video Outputs	$V_7 = 0$ V_i = See Note (5) f_o (vision) = 38.9 MHz f_o (sound) = 33.4 MHz f_o (chroma) = 35.5 MHz		– 50	– 40	dB
R_i	Input Resistance (between pins 1 and 16)	$V_7 = 0$ V_i = See Note (5) $f_o = 38.9$ MHz		1.4		KΩ
C_i	Input Capacitance (between pins 1 and 16)			2		pF

Notes : 1. Current flowing out from pin 11 with the load connected to V = 8 V.
2. V_{11} and V_{12} are adjustable simultaneously by means of the resistance, or by a variable voltage ≤ 0.6 V, connected between pin 10 and ground.
3. Measured with an input voltage 10 dB higher than the V_i at which the tuner AGC current starts.
4. RMS values of the unmodulated video carrier (modulation down).
5. The input voltage V_i can have any value within the AGC range.

BLOCK DIAGRAM

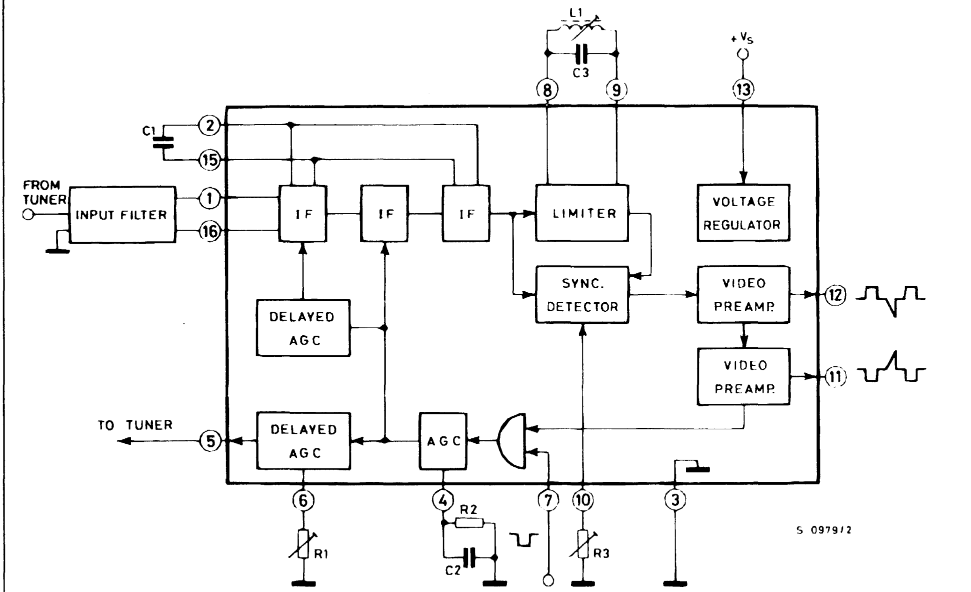
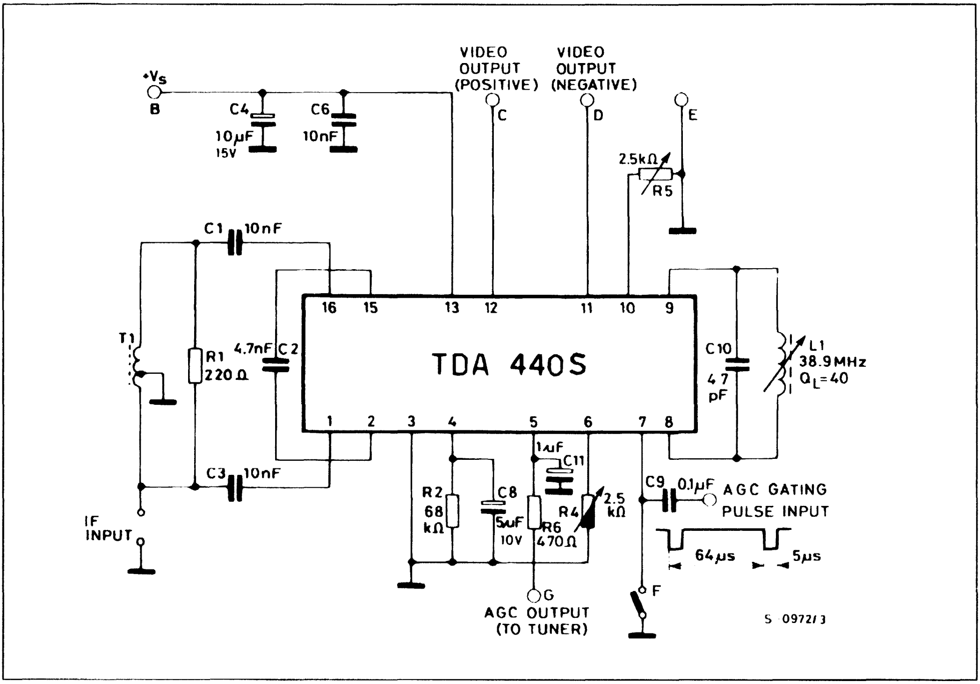


Figure 1 : AC Test Circuit.



Note : T1 = 50/200 W Balun transformer.
Vi = Input voltage between pins 1 and 16.

Figure 2 : AGC Voltage vs. Input Voltage Variation.

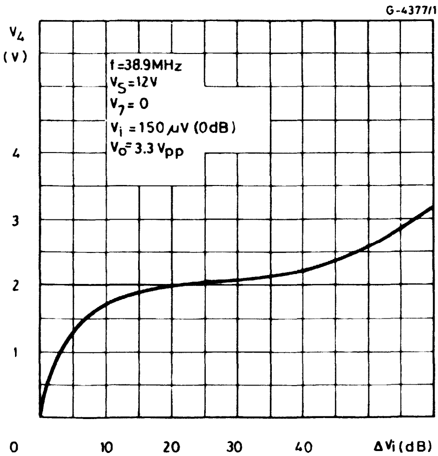


Figure 3 : Turner AGC Output Current vs. IF Gain Variation.

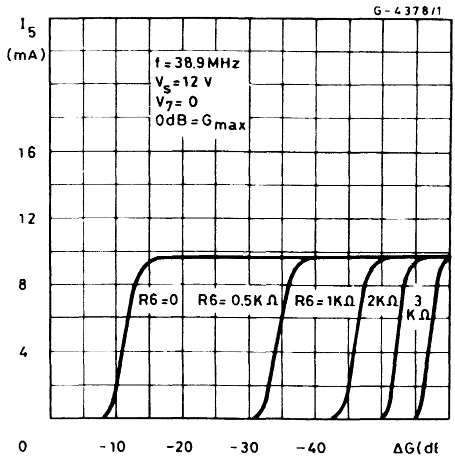
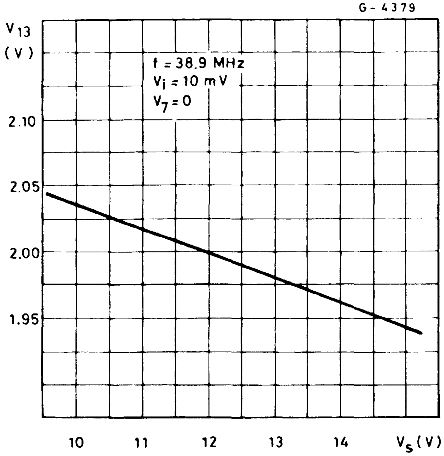


Figure 4 : Ouput Black Level vs. Supply Voltage.



APPLICATION INFORMATION

The TDA440S enables very compact IF amplifiers to be designed and provides the performance demanded by high quality receivers.

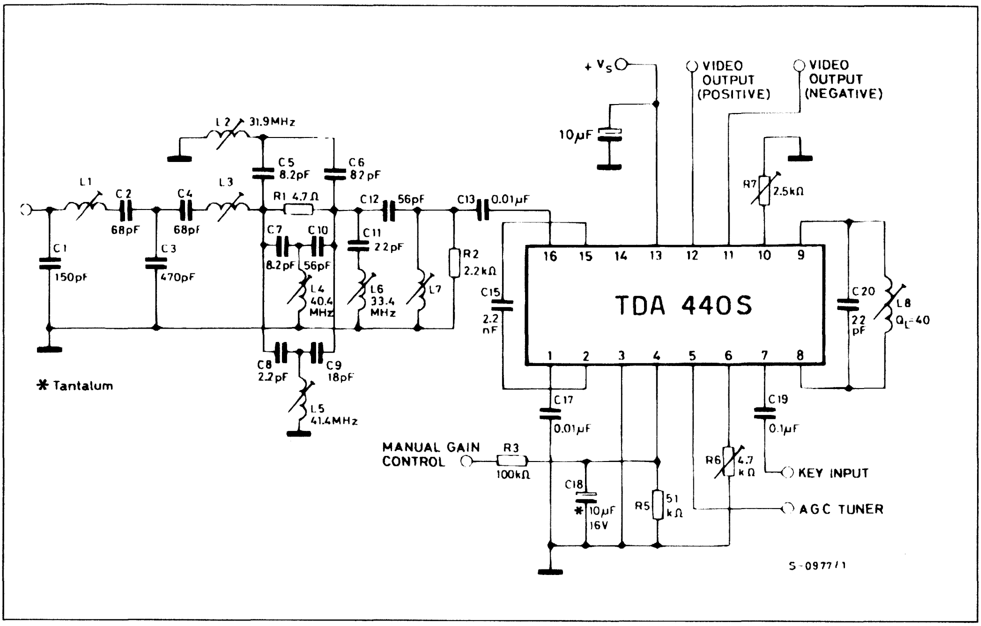
The input tuning-trapping circuitry and the detector network can be aligned independently with respect to each other.

The value of Q for the parallel tuned circuit between pin 8 and 9 is not critical, although the higher it is, the better is the chroma-sound beat rejection, but the tuning is more critical. Values of Q from 30 to 50 give good rejection with non-critical tuning.

The LC circuit between pins 8 and 9 is tuned to the vision carrier thus appreciably attenuating the sidebands. Hence a small amount of signal can be removed whose amplitude is almost constant over the whole working range of the AGC and it can be used to drive an AFC circuit.

The black level at the output is very stable against variations of V_S and of temperature : this enables the contrast control to be kept simple. The AGC is of the gated type and can take the top of the synchronism or the black level (back porch) as its reference : when the latter is used, the output black level is particularly stable.

Figure 5 : Typical Application Circuit.



L1 = 0.42 µH – Qo = 110 – 6 turns θ = 0.22 mm (close wound)
L2, L3, L7 = 0.3 µH – Qo = 110 – 5.5 turns θ = 0.22 mm (close wound)
L4 = 0.22 µH – Qo = 110 – 4.5 turns θ = 0.22 mm (close wound)
L5, L6 = 1 µH – Qo = 110 – 10 turns θ = 0.22 mm (close wound)
L8 = 1.2 µH – Qo = 110 – 10 turns θ = 0.22 mm(close wound)
L1 to L7 : coil former BR27/P, core GW 4 x 0.5 x 13 F 100 Neosid, Screening can BR 10/ST.

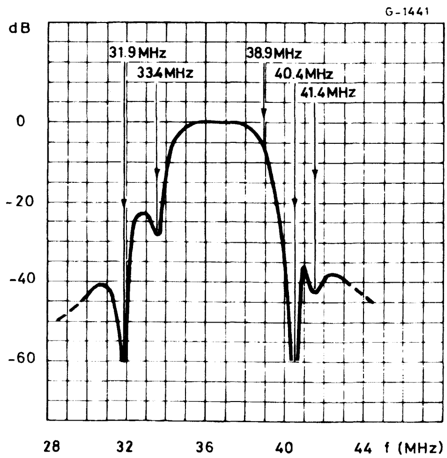
Typical Performances of the Fig. 5 Circuit.

Frequency response (fo vision = 38.9 MHz, fo sound = 33.4 MHz) standard CCIR

Sound carrier attenuation	28	dB
31.9 MHz trap attenuation	≥ 60	dB
40.4 MHz trap attenuation	≥ 56	dB
41.4 MHz trap attenuation	≥ 44	dB
AGC range	55	dB
Overall gain including IF filter and trap circuits (note 1)	86	dB
Intermodulation products over the whole AGC range (note 2)	– 55	dB

Notes :
1. The gain is measured at video output 3.3V peak to peak and is defined as peak to peak output voltage to RMS input voltage (modulation down).
2. Measured at 1.07 MHz, vision carrier level = 0 dB, chroma carrier level = – 6 dB, sound carrier level = – 6 dB.

Figure 6 : Overall Frequency Response of the Fig. 5 Circuit.

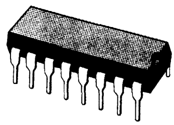


SGS-THOMSON
MICROELECTRONICS

TDA1170D

LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS



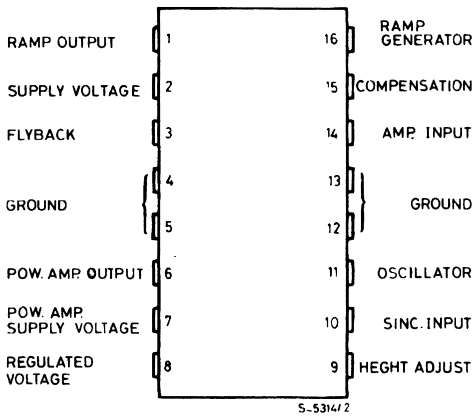
DIP16

ORDER CODE : TDA1170D

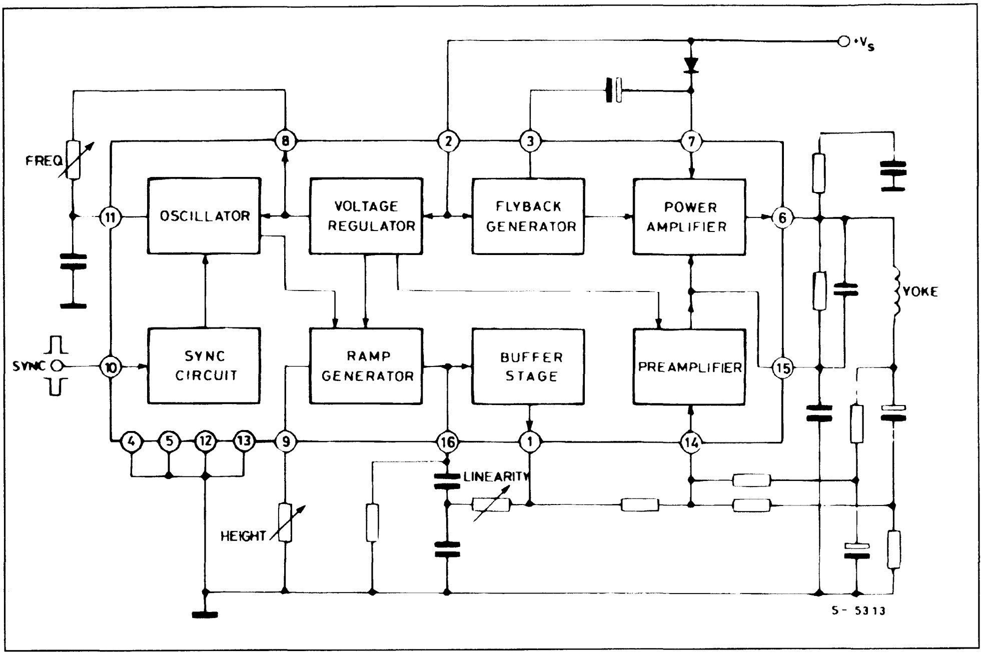
DESCRIPTION

The TDA 1170D is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise makes this device particularly suitable for use in monitors.** The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V6, V7	Flyback Peak Voltage	60	V
V14	Power Amplifier Input Voltage	+ 10 – 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2 msec	2	A
I_o	Output Peak Current at f = 50 Hz t ≤ 10 µsec	2.5	A
I_o	Output Prak Current at f = 50 Hz t > 10 µsec	1.5	A
I_3	Pin 3 DC Current at V6 < V2	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50 Hz, t_{fly} ≤ 1.5 msec	1.8	A
I_{10}	Pin 10 Current	± 20	mA
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 70 ° C (free air)	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-tab}$	Thermal Resistance Junction–pins	Max	14	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W(°)

(°) Obtained with pins 4, 5, 12, 13 soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_7	Pin 7 Quiescent Current	$I_6 = 0$		8	17	mA	1b
$-I_{11}$	Oscillator Bias Current	V11 = 1 V		0.1	1	µA	1a
$-I_{14}$	Amplifier Input Bias Current	V14 = 1 V		1	10	µA	1b
$-I_{16}$	Ramp Generator Bias Current	V16 = 0		0.02	0.3	µA	1a
$-I_{16}$	Ramp Generator Current	I_9 = 20 µA V16 = 0	18.5	20	21.5	µA	1b
$\frac{\Delta I_{16}}{I_{16}}$	Ramp Generator Non-linearity	ΔV16 = 0 to 12 V I_9 = 20 µA		0.2	1	%	1b
V_s	Supply Voltage Range		10		35	V	–
V1	Pin 1 Saturation Voltage to Ground	I_1 = 1 mA		1	1.4	V	–
V3	Pin 3 Saturation Voltage to Ground	I_3 = 10 mA		300	450	mV	1a
V6	Quiescent Output Voltage	V_s = 10 V R1 = 1 KΩ R2 = 1 KΩ	4.1	4.4	4.75	V	1a
		V_s = 35 V R1 = 3 KΩ R2 = 1 KΩ	8.3	8.8	9.45	V	1a
V6L	Output Saturation Voltage to Ground	$-I_6$ = 0.1 A		0.9	1.2	V	1c
		$-I_6$ = 0.8 A		1.9	2.3	V	1c
V6H	Output Saturation Voltage to Supply	I_6 = 0.1 A		1.4	2.1	V	1d
		I_6 = 0.8 A		2.8	3.2	V	1d
V8	Regulated Voltage at Pin 8		6.1	6.5	6.9	V	1b
V9	Regulated Voltage at Pin 9	I_9 = 20 µA	6.2	6.6	7	V	1b
$\frac{\Delta V8}{\Delta V_s}, \frac{\Delta V9}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	ΔV_s = 10 to 35 V		1		mV/V	1b
V14	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	–
R10	Pin 10 Input Resistance	V10 ≤ 0.4 V	1			MΩ	1a

Figure 1 : DC Test Circuit.

Figure 1a.

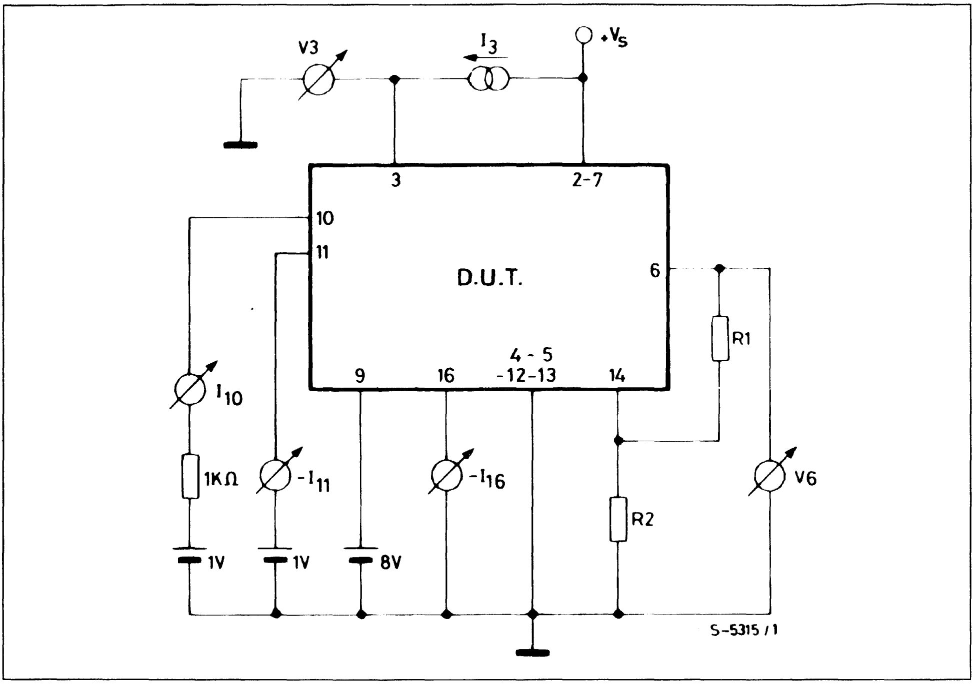


Figure 1b.

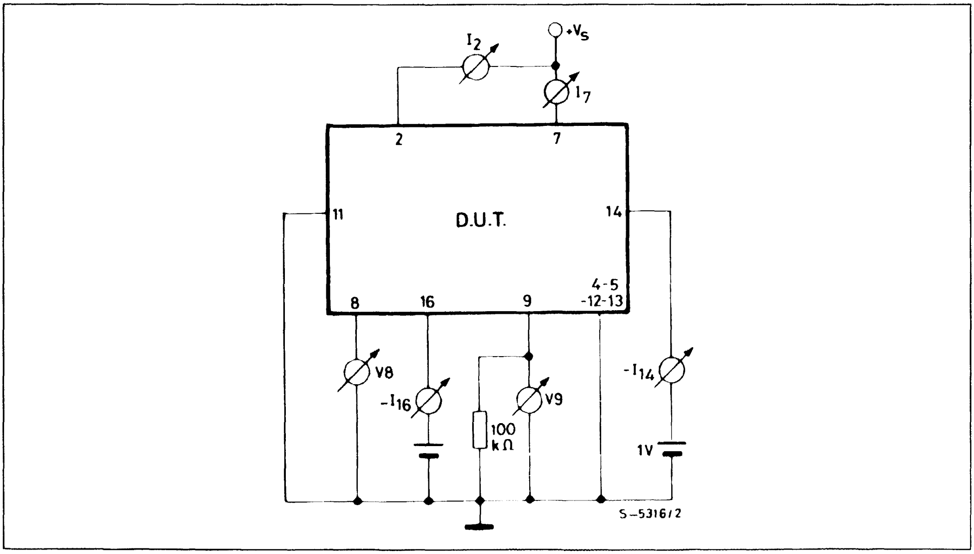


Figure 1c.

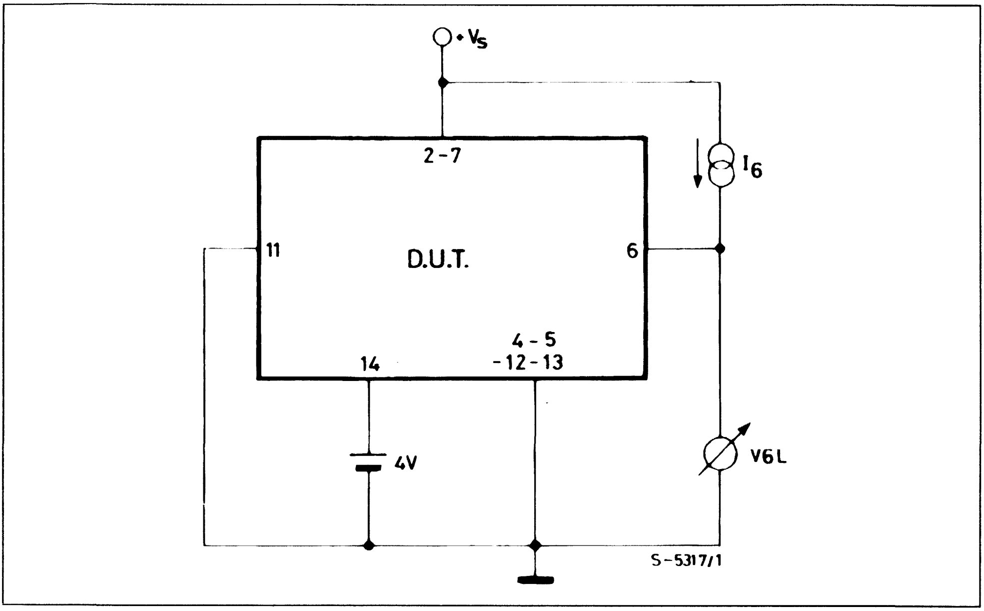
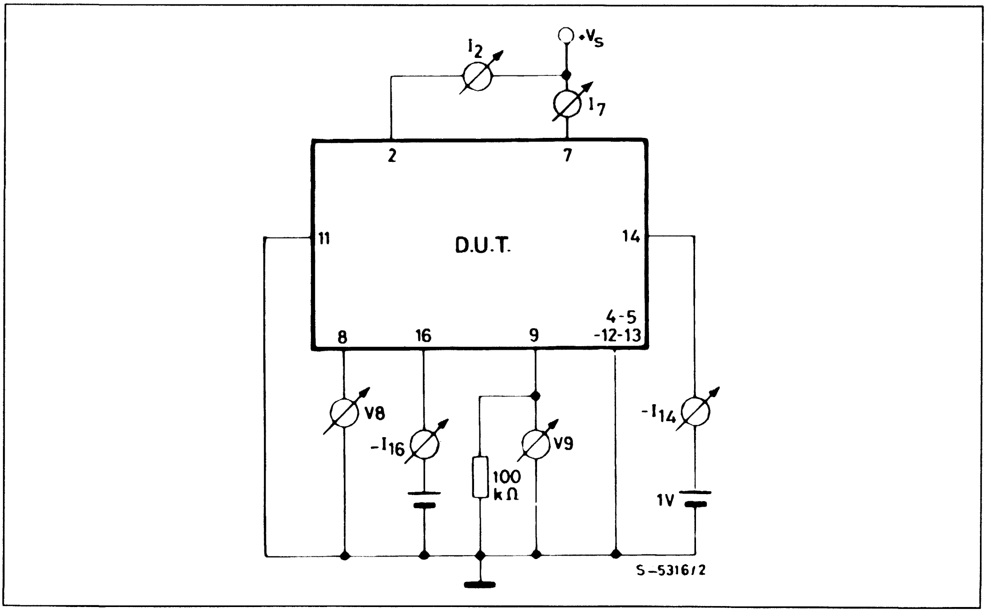


Figure 1d.



ELECTRICAL CHARACTERISTICS (refer to the AC test circuit, V_s = 22 V ; f = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 1 App		140		mA
I_{10}	Sync. Input Current (positive or negative)		500			μA
V6	Flyback Voltage	I_y = 1 App		45		V
t_{fly}	Flyback Time	I_y = 1 App		0.7		ms
V_{ON}	Peak to Peak Output Noise	Pin 11 Connected to GND			40	mVpp
f_o	Free Running Frequency	(P1 + R1) = 260 KΩ C2 = 0.1 μF		48.5		Hz
		(P1 + R1) = 300 KΩ C2 = 0.1 nF		42.2		Hz
Δf	Synchronization Range	I_8 = 0.5 mA	14			Hz
$\frac{\Delta f}{\Delta Vs}$	Frequency Drift with Supply Voltage	V_s = 10 to 35 V		0.005		Hz/V
$\frac{\Delta f}{\Delta T_{pins}}$	Frequency Drift vs. Pins 4, 5, 12 and 13 Temp.	T_{tab} = 40 to 120 °C		0.01		Hz/°C

Figure 2 : AC Test Circuit.

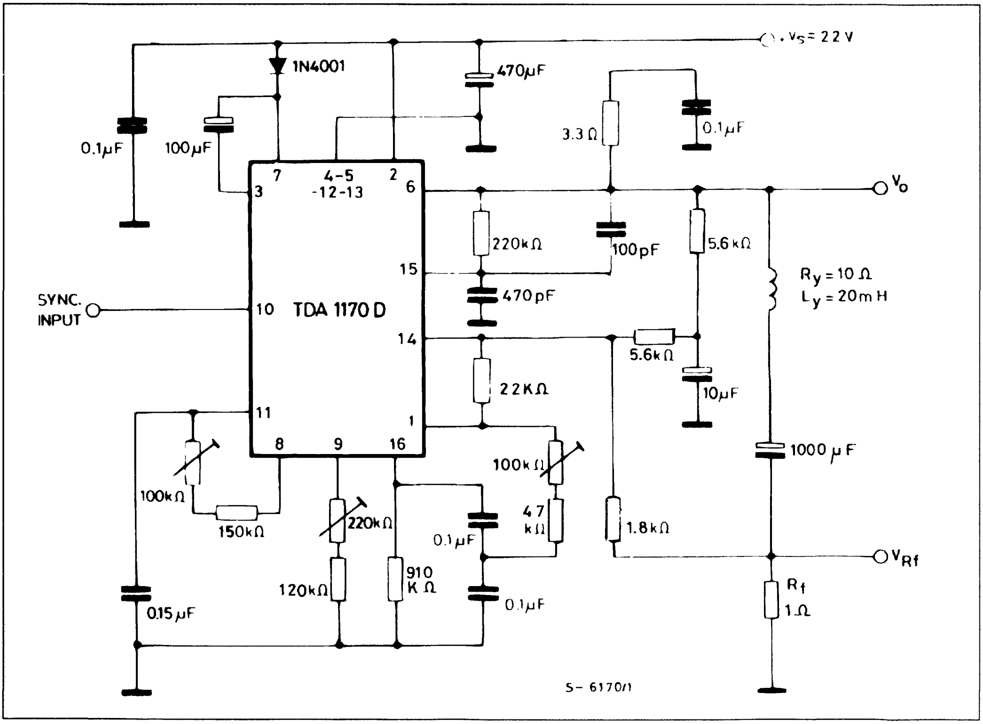


Figure 3 : Typical Application Circuit for Smal Screen B/W TV SET (Ry = 2.9 Ω, Ly = 6 mH, Iy = 1.1 App).

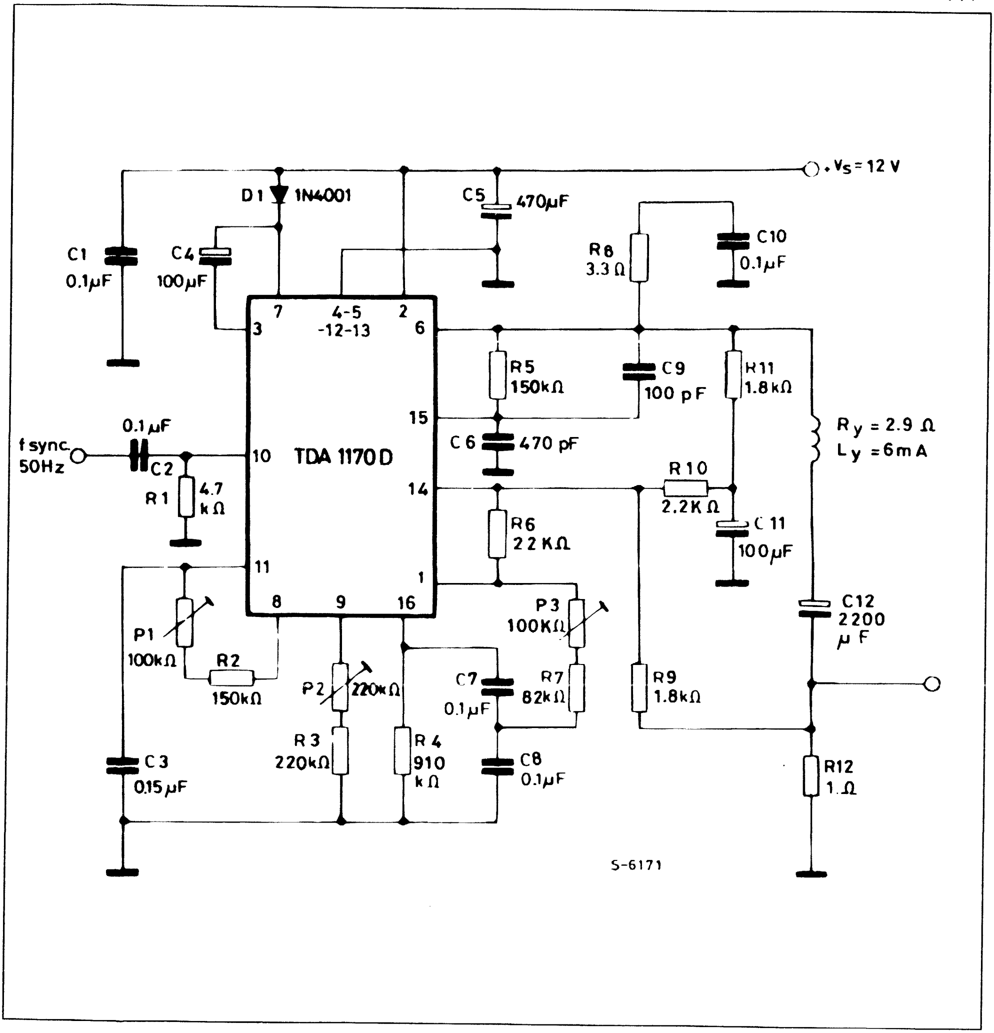
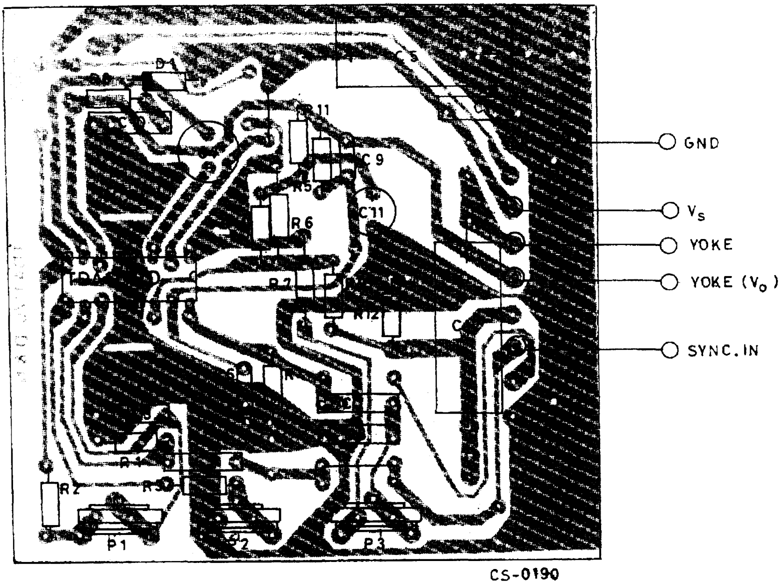


Figure 4 : P.C. Board and Components Layout of the Circuit of Fig. 3 (1 : 1 scale).



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 1170D can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

The diagram of figure 7 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 5 : Example of P.C. Board Copper Area which is Used as Heatsink.

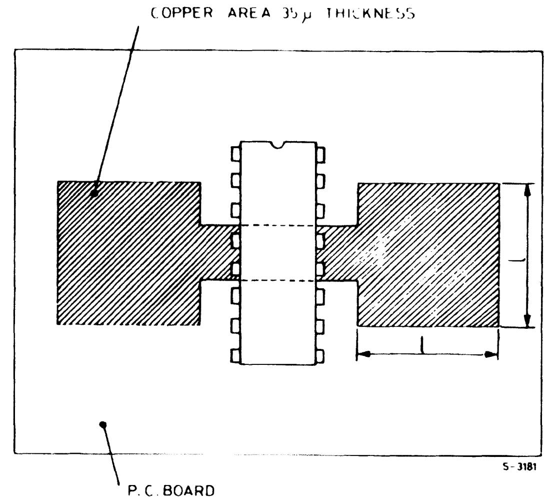


Figure 6 : External Heatsink Mounting Example.

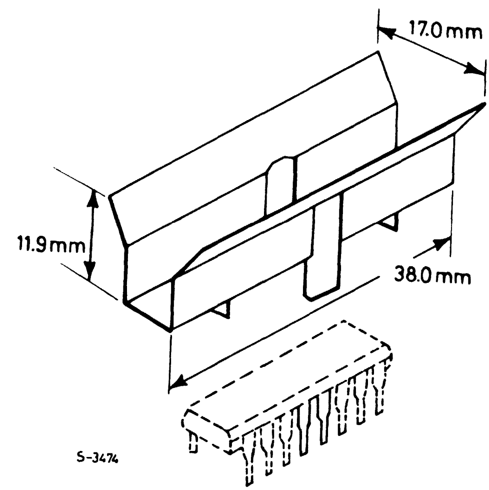


Figure 7 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l".

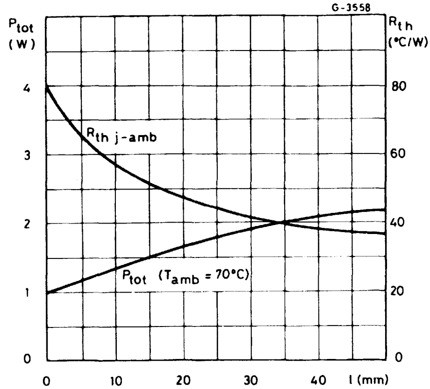
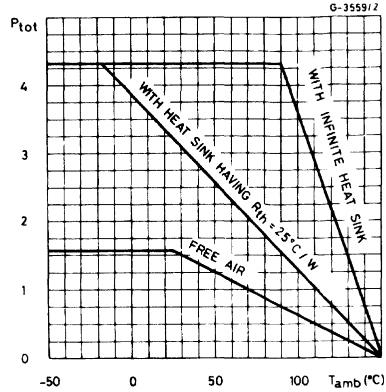


Figure 8 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



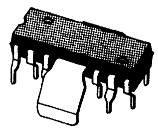
TDA1170N

LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

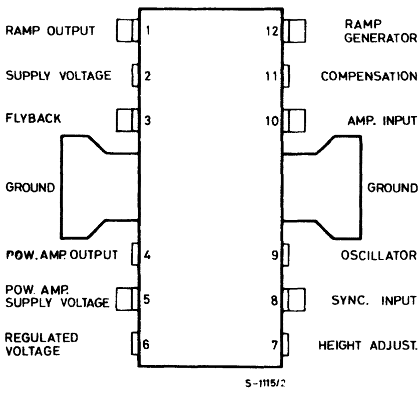
DESCRIPTION

The TDA 1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors. The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.



ORDER CODE : TDA 1170N

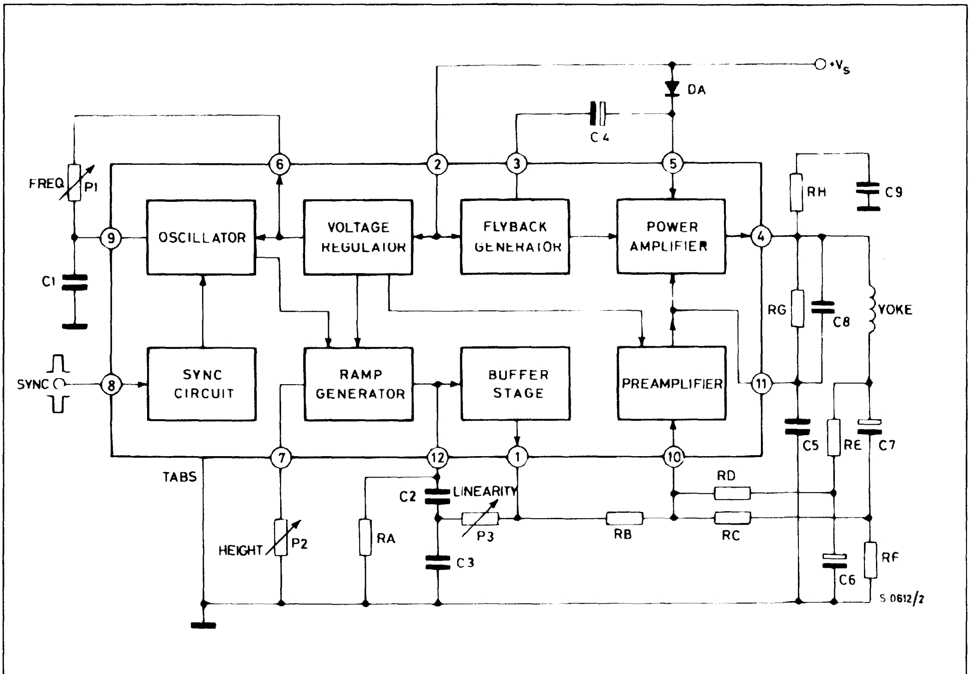
CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage at Pin 2	35	V
V4, V5	Flyback Peak Voltage	60	V
V10	Power Amplifier Input Voltage	{ + 10 – 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2 msec	2	A
I_o	output Peak Current at f = 50 Hz t ≤ 10 μsec	2.5	A
I_o	Output Peak Current at f = 50 Hz t > 10 μsec	1.5	A
I_3	pin 3 DC Current at V4 < V2	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50 Hz, t_{fly} ≤ 1.5 msec	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{tot}	Power Dissipation : at T_{ab} = 90 °C at T_{amb} = 80 °C (free air)	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal Resistance Junction-tab	Max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W(°)

(°) Obtained with tabs soldered to printed circuit wth minimized copper area.

ELECTRICAL CHARACTERISTICS (Refer to the test circuits, V_S = 35 V, Tamb = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	17	mA	1b
$-I_9$	Oscillator Bias Current	V9 = 1 V		0.1	1	µA	1a
$-I_{10}$	Amplifier Input Bias Current	V10 = 1 V		1	10	µA	1b
$-I_{12}$	Ramp Generator Bias Current	V12 = 0		0.02	0.3	µA	1a
$-I_{12}$	Ramp Generator Current	I_7 = 20 µA V12 = 0	18.5	20	21.5	µA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	ΔV12 = 0 to 12 V I_7 = 20 µA		0.2	1	%	1b
V_s	Supply Voltage Range		10		35	V	
V1	Pin 1 Saturation Voltage to Ground	I_1 = 1 mA		1	1.4	V	
V3	Pin 3 Saturation Voltage to Ground	I_3 = 10 mA		300	450	mV	1a
V4	Qiuescent output Voltage	V_s = 10 V R1 = 1 kΩ R2 = 1 kΩ	4.1	4.4	4.75	V	1a
		V_s = 35 V R1 = 3 kΩ R2 = 1 kΩ	8.3	8.8	9.45	V	1a
V4L	Output Saturation Voltage to Ground	$-I_4$ = 0.1 A		0.9	1.2	V	1c
		$-I_4$ = 0.8 A		1.9	2.3	V	1c
V4H	Output Saturation Voltage to Supply	I_4 = 0.1 A		1.4	2.1	V	1d
		I_4 = 0.8 A		2.8	3.2	V	1d
V6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V7	Regulated Voltage at Pin 7	I_7 = 20 µA	6.2	6.6	7	V	1b
$\frac{\lvert \Delta V6 \rvert}{\Delta V_s}; \frac{\Delta V7}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	ΔVs = 10 to 35 V		1		mV/V	1b
V10	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	
R8	pin 8 Input Resistance	V8 ≤ 0.4 V	1			MΩ	1a

Figure 1 : DC Test Circuits.

Figure 1a.

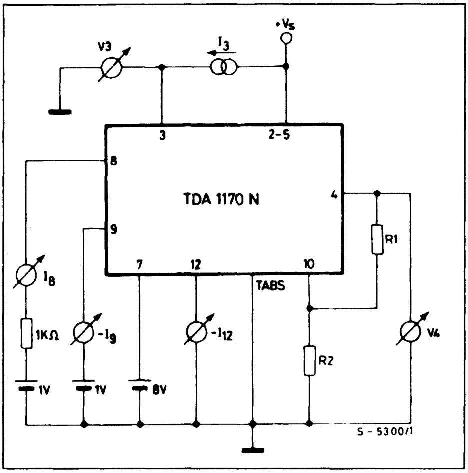


Figure 1b.

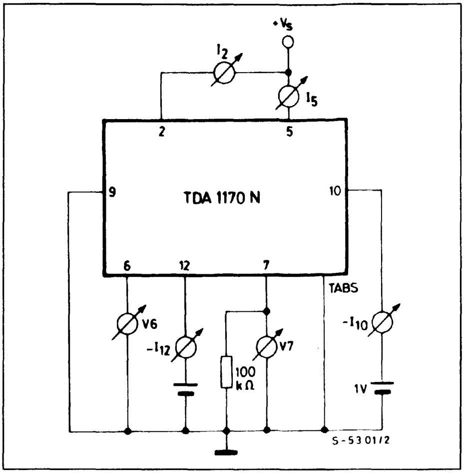


Figure 1c.

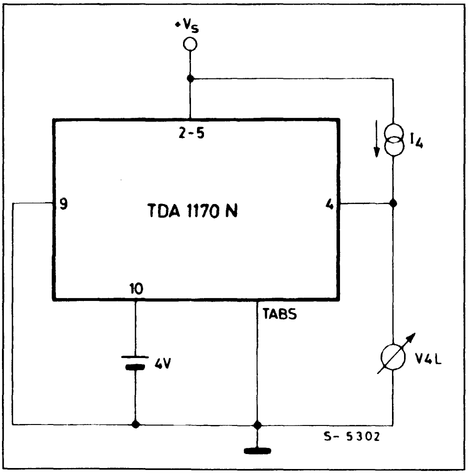
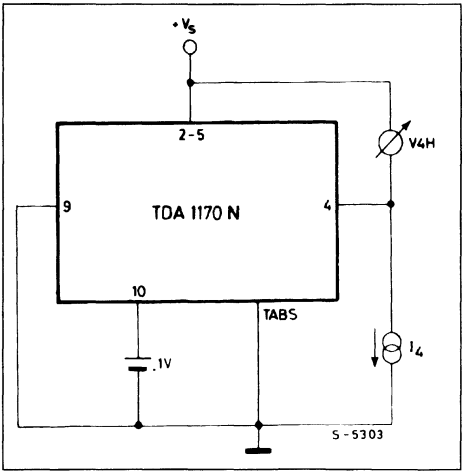


Figure 1d.



ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, V_s = 22 V ; F = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 1 App		140		mA
I_8	Sync. Input Current (positive or negative)		500			µA
V4	Flyback Voltage	I_y = 1 App		45		V
t_{fly}	Flyback Time	I_y = 1 App		0.7		ms
V_{ON}	Peak to Peak Output Noise	pin 9 Connected to GND			40	mVpp
f_o	Free Running Frequency	(P1 + R1) = 300 kΩ C2 = 0.1 µF		42.2		Hz
		(P1 + R1) = 260 kΩ C2 = 0.1 µF		48.5		Hz
Δf	Sychronization Range	I_8 = 0.5 mA	14			Hz
$\frac{\Delta f}{\Delta V_s}$	Frequency Drift with Supply Voltage	V_s = 10 to 35 V		0.005		Hz/V
$\frac{\lvert \Delta f \rvert}{\Delta T_{ab}}$	Frequency Drift with tab Temperature	T_{tab} = 40 to 120 °C		0.01		Hz/°C

Figure 2 : AC Test and Application Circuit for Large Screen B/W TV Set 10 Ω/20 mH/1 App.

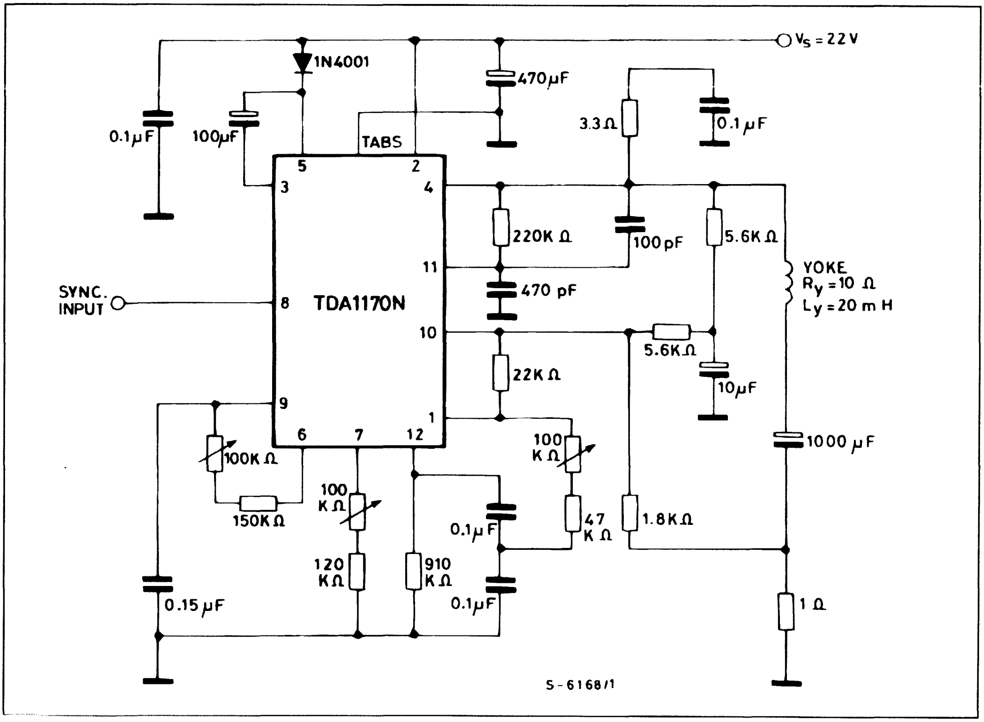


Figure 3 : Typical Application Circuit for Small Screen 90 ° TVC Set (R_Y = 15 Ω, L_Y = 30 mH, I_Y = 0.82 App).

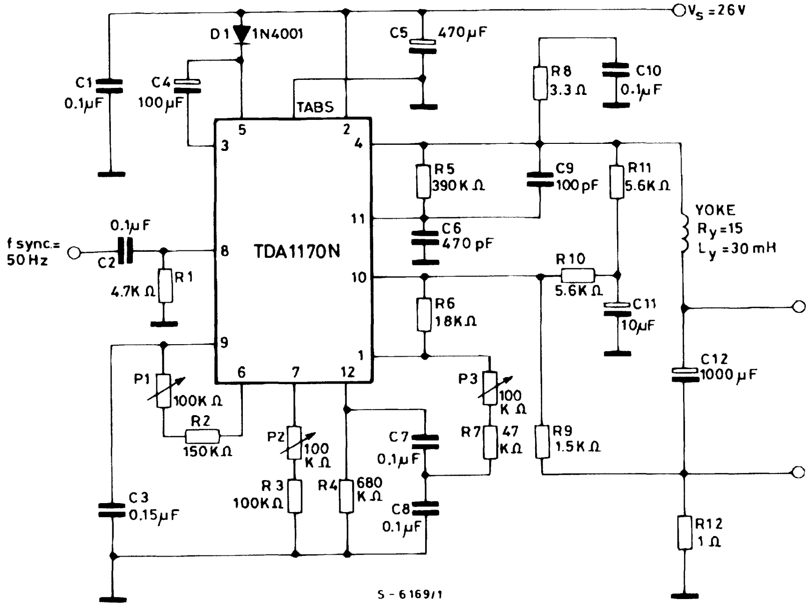
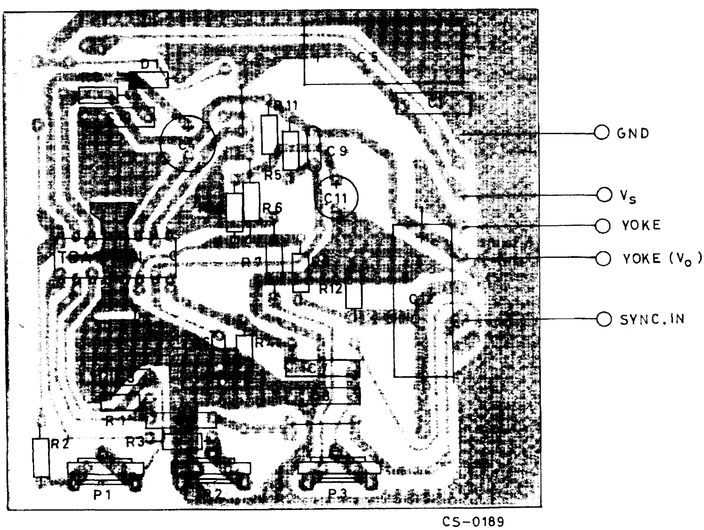


Figure 4 : P.C. Board and Components Layout of the Circuit of fig. 3 (1:1 scale).



MOUNTING INSTRUCTION

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

The junction to ambient thermal resistance can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

The diagram of fig. 7 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "e" of two equal square copper areas having a thicknessof 35 μ (1.4 mil).

Figure 5 : Exmple of P.C. Board Copper Area Used as Heatsink.

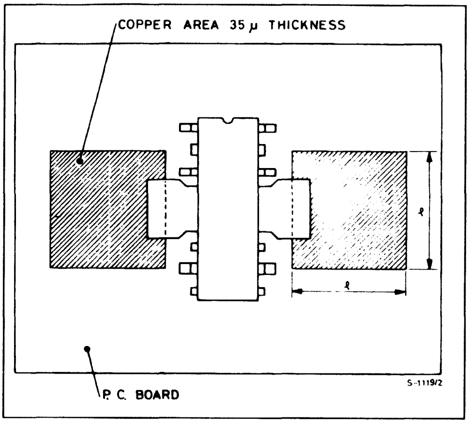


Figure 6 : Example of External heatsink.

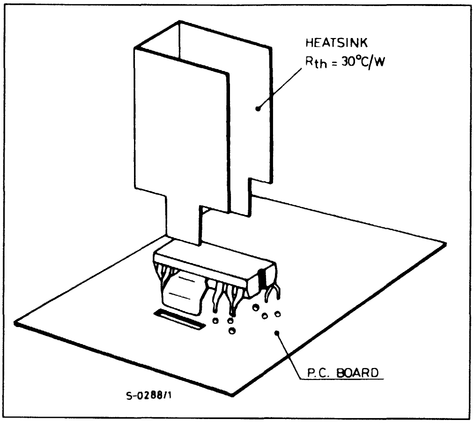


Figure 7 : Maximum Power Dissipation and Junctional Ambient Thermal Resistance vs. "e".

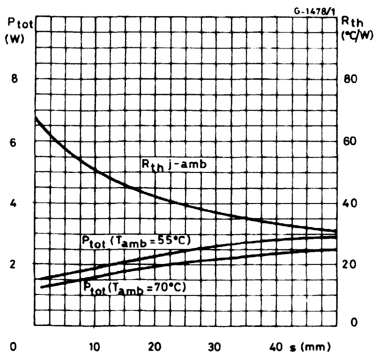
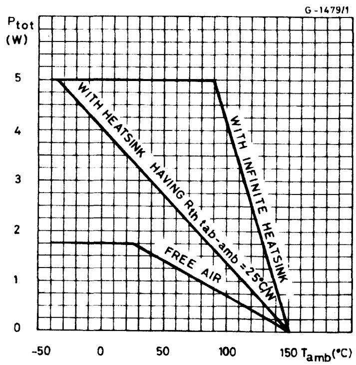


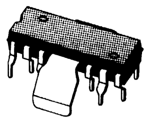
Figure 8 : Maximum Allowable Power Dissipation Versus Ambient Temperature.



TDA1170S

TV VERTICAL DEFLECTION SYSTEM

- SYNCHRONIZATION CIRCUIT
- OSCILLATOR AND RAMP GENERATOR
- HIGH POWER GAIN AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR



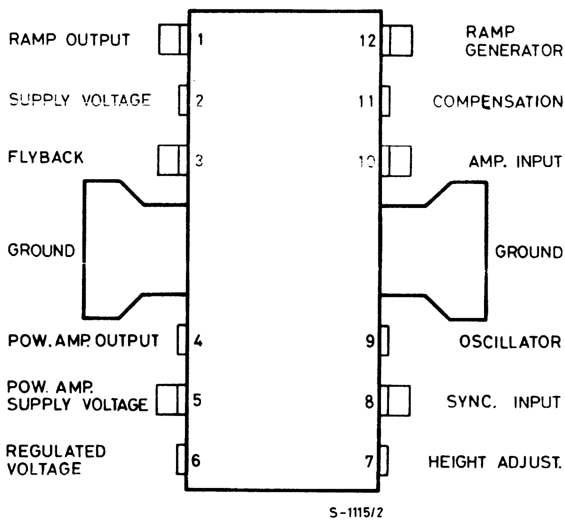
FIN DIP 12

ORDER CODES : TDA1170S

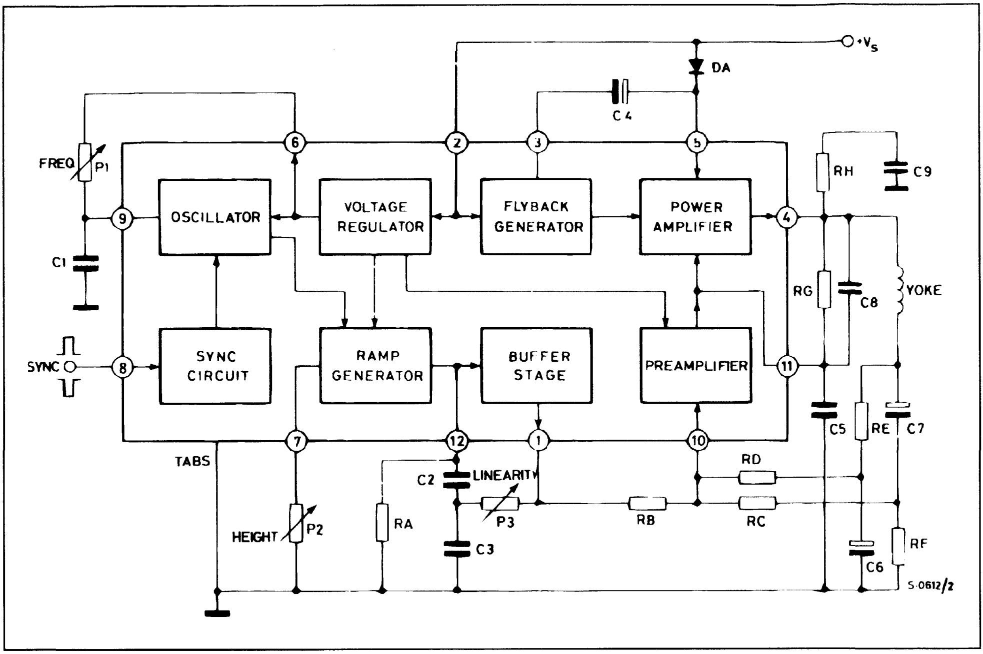
DESCRIPTION

The TDA1170S is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

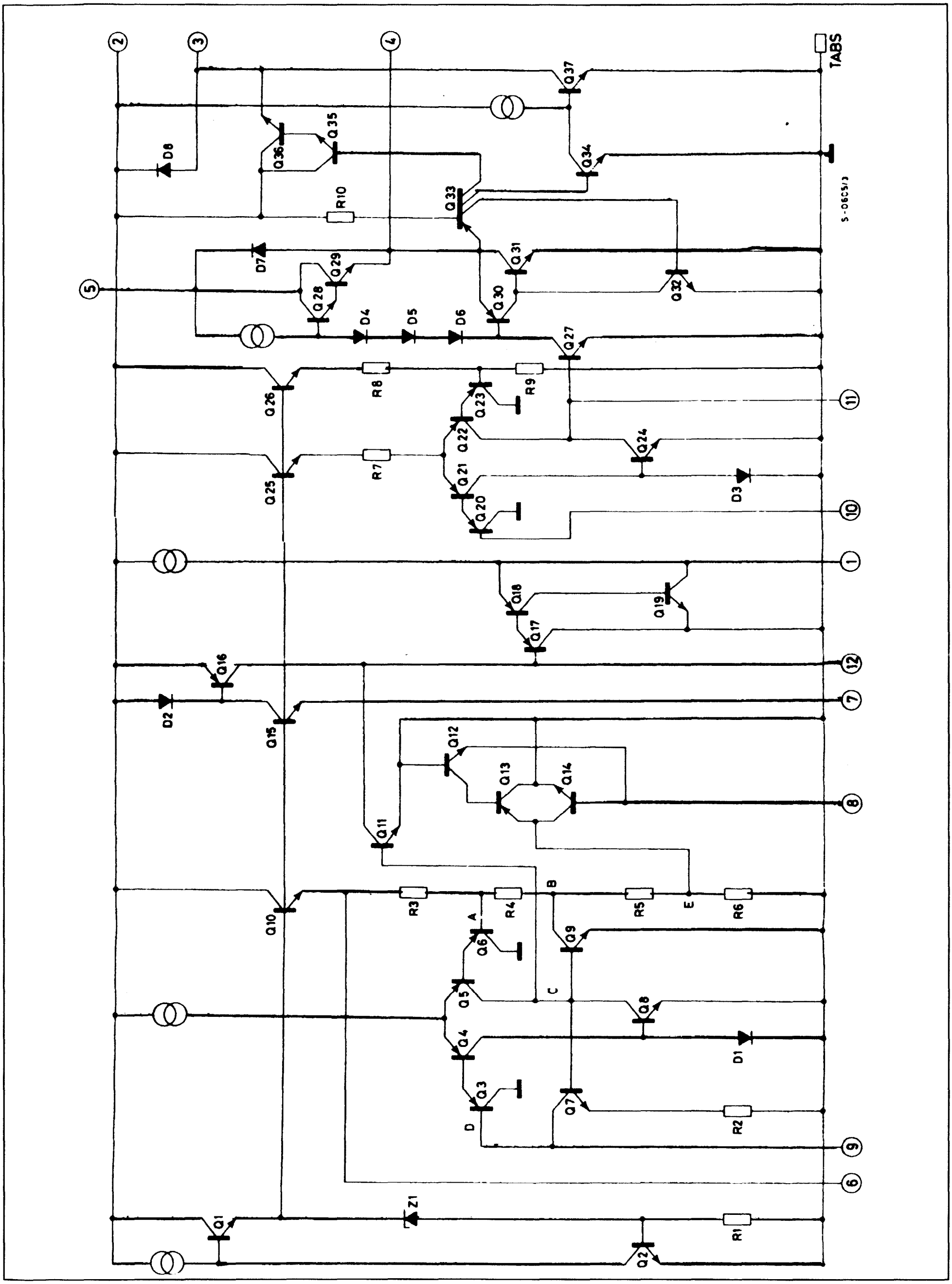
Symbol	Parameter		Value	Unit
V_S	Supply Voltage at Pin 2		35	V
V_4, V_5	Flyback Peak Voltage		60	V
V_{10}	Power Amplifier Input Voltage		+ 10 – 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2 msec		2	A
I_o	Output Peak Current at f = 50 Hz t ≤ 10 µsec		2.5	A
I_o	Output Peak Current at f = 50 Hz t > 10 µsec		1.5	A
I_3	Pin 3 DC Current at $V_4 < V_2$		100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50 Hz, t_{fly} ≤ 1.5 msec		1.8	A
I_8	Pin 8 Current		± 20	mA
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 80 ° C	TDA1170S	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature		– 40 to 150	°C

THERMAL DATA

			TDA1170S	TDA1170SH
$R_{th\ j-tab}$	Thermal Resistance Junction–tab	Max	12°C/W	10°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	70°C/W(°)	80°C/W

(°) Obtained with tabs soldered to printed circuit with minimized copper area.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_5	Pin 5 Quiescent Current	$I_4 = 0$		8	15	mA	1b
$-I_9$	Oscillator Bias Current	V_9 = 1 V		0.1	1	µA	1a
$-I_{10}$	Amplifier Input Bias Current	V_{10} = 1 V		0.1	1	µA	1b
$-I_{12}$	Ramp Generator Bias Current	$V_{12} = 0$		0.02	0.3	µA	1a
$-I_{12}$	Ramp Generator Current	I_7 = 20 µA $V_{12} = 0$	19	20	24	µA	1b
$\frac{\Delta I_{12}}{I_{12}}$	Ramp Generator Non-linearity	ΔV_{12} = 0 to 12 V I_7 = 20 µA		0.2	1	%	1b
V_s	Supply Voltage Range		10		36	V	–
V_1	Pin 1 Saturation Voltage to Ground	I_1 = 1 mA		1	1.4	V	–
V_3	Pin 3 Saturation Voltage to Ground	I_3 = 10 mA		1.7	2.6	V	1a
V_4	Quiescent Output Voltage	V_s = 10 V R_1 = 10 KΩ R_2 = 10 KΩ	4.1	4.4	4.75	V	1a
		V_s = 35 V R_1 = 30 KΩ R_2 = 10 KΩ	8.3	8.8	9.45	V	1a
V_{4L}	Output Saturation Voltage to Ground	$-I_4$ = 0.1 A		0.9	1.2	V	1c
		$-I_4$ = 0.8 A		1.9	2.3	V	1c
V_{4H}	Output Saturation Voltage to Supply	I_4 = 0.1 A		1.4	2.1	V	1d
		I_4 = 0.8 A		2.8	3.2	V	1d
V_6	Regulated Voltage at Pin 6		6.1	6.5	6.9	V	1b
V7	Regulated Voltage at Pin 7	I_7 = 20 µA	6.2	6.6	7	V	1b
$\frac{\Delta V_6}{\Delta V_s}$, $\frac{\Delta V_7}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	ΔV_s = 10 to 35 V		1		mV/V	1b
V_{10}	Amplifier Input Reference Voltage		2.07	2.2	2.3	V	–
R_8	Pin 8 Input Resistance	$V_8 \leq 0.4$ V	1			MΩ	1a

Figure 1 : DC Test Circuit.

Figure 1a.

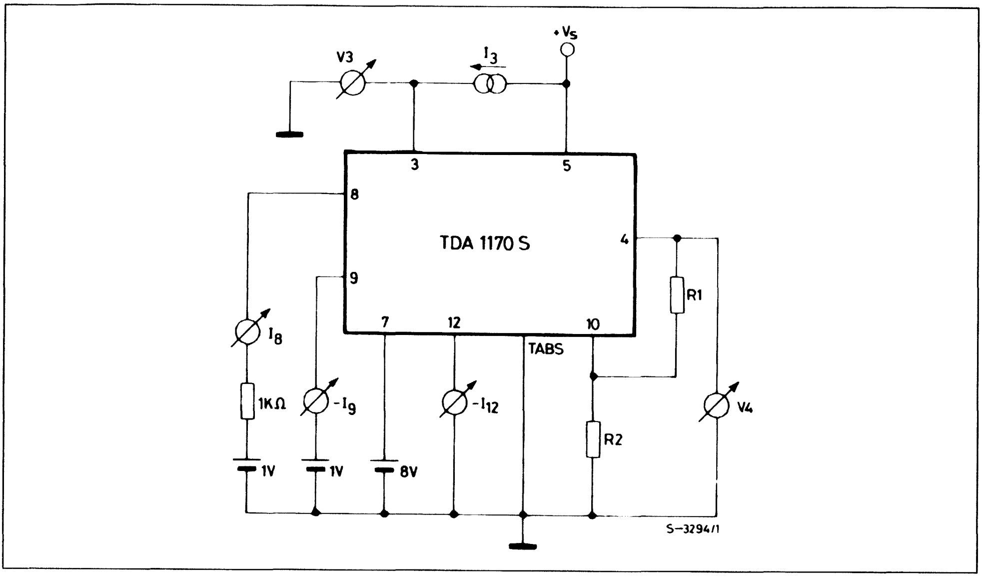


Figure 1b.

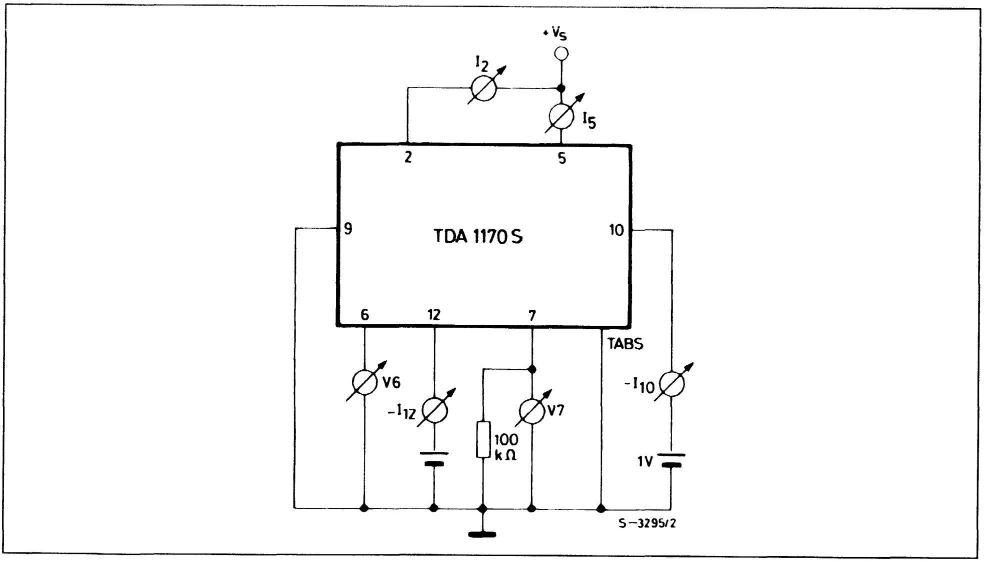


Figure 1c.

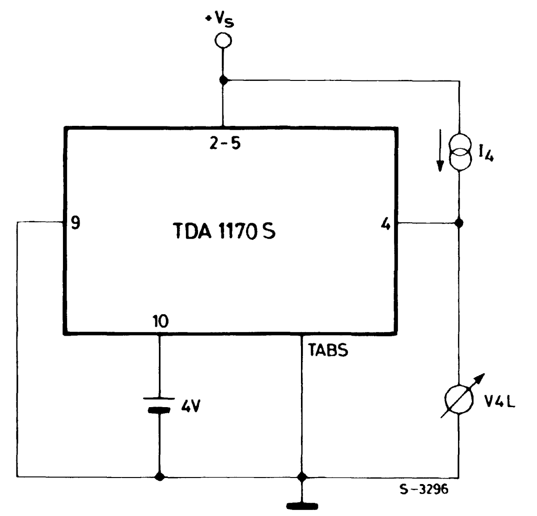
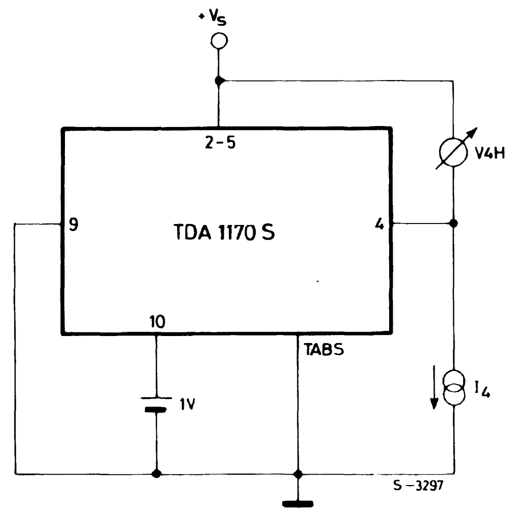


Figure 1d.



AC CHARACTERISTICS (refer to the test circuit, V_s = 25 V; f = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_s	Supply Current	I_y = 1 App		140		mA	2
I_8	Sync. Input Current (positive or negative)		500			µA	2
V_4	Flyback Voltage	I_y = 1 App		51		V	2
V_9	Peak to Peak Oscillator Sawtooth Voltage			2.4		V	2
t_{fly}	Flyback Time	I_y = 1 App		0.7		ms	2
f_o	Free Running Frequency	$(P_1 + R_1)$ = 300 KΩ C_2 = 0.1 µF		42.2		Hz	2
		$(P_1 + R_1)$ = 260 KΩ C_2 = 0.1 µF		52 48.5		Hz	2
Δf	Synchronization Range	I_8 = 0.5 mA	14			Hz	2
$\frac{\Delta f}{\Delta V_s}$	Frequency Drift with Supply Voltage	V_s = 10 to 35 V		0.005		Hz/V	2
$\left\lvert \frac{\Delta f}{\Delta T_{tab}} \right\rvert$	Frequency Drift with Tab Temperature	T_{tab} = 40 to 120 °C		0.01		Hz/°C	2

Figure 2 : AC Test Circuit.

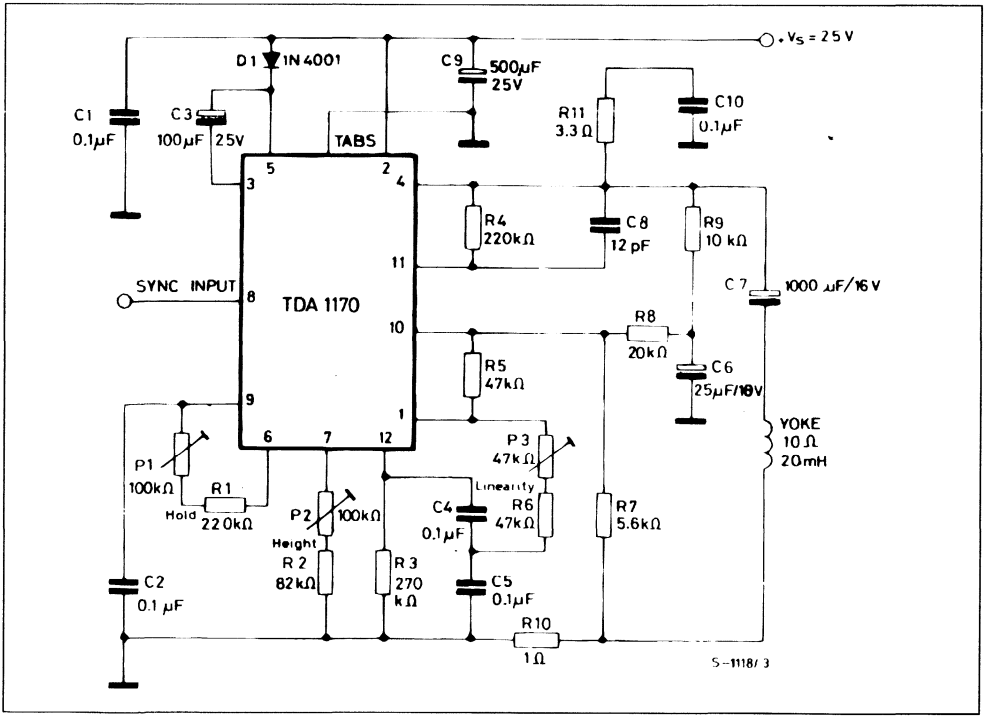
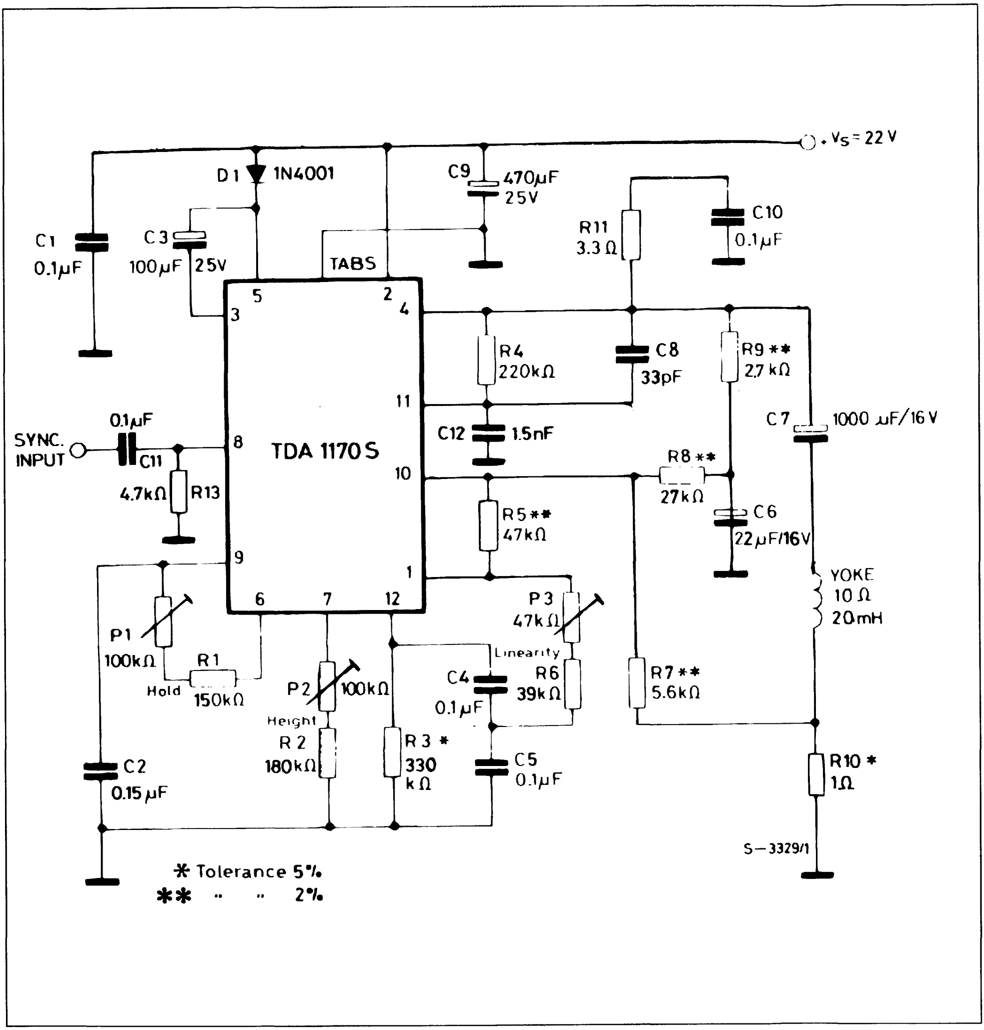


Figure 3 : Typical Application Circuit for Large Screen B/W TV SET (R_y = 10 Ω, L_y = 20 mH, I_y = 1 App).



TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	22	V
I_s	Supply Current	145	mA
t_{fly}	Flyback Time	0.7	ms
P_{tot}	TDA 1170S Power Dissipation	2.3	W
I_y	Maximum Scanning Current (peak to peak)	1.2	A

For safe working up to T_{amb} = 60 °C a heatsink of R_{th} = 14 °C/W is required.

TDA1170S

The junction to ambient thermal resistance of the TDA 1170S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 4) or to an external heatsink (fig. 5).

The diagram of fig. 6 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35 μ (1.4 mil).

Figure 4 : Example of P.C. Board Copper Area is Used as Heatsink.

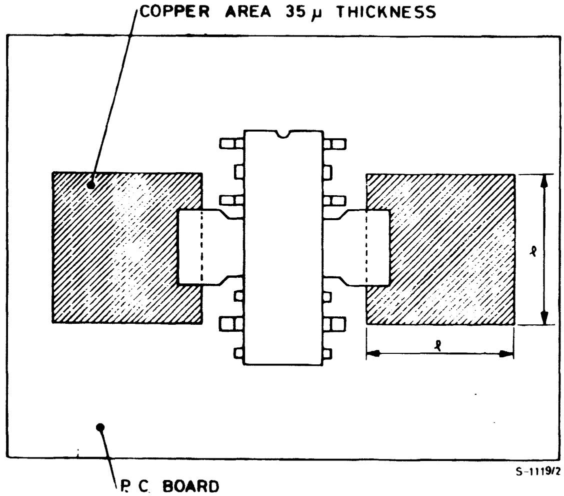


Figure 5 : Example of TDA 1170S with External Heatsink.

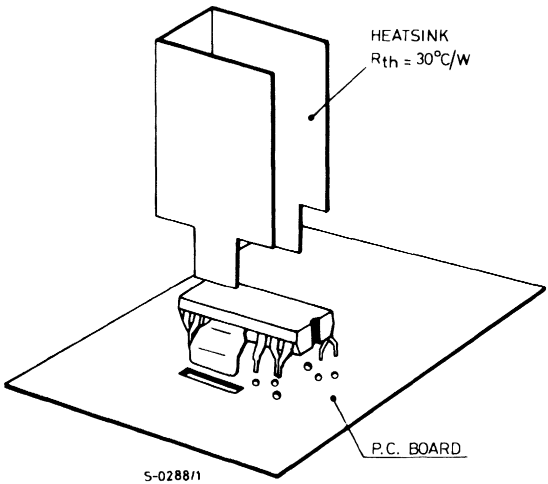


Figure 6 : Maximum Power Dissipation and Junctional-ambient Thermal Resistance vs. "S".

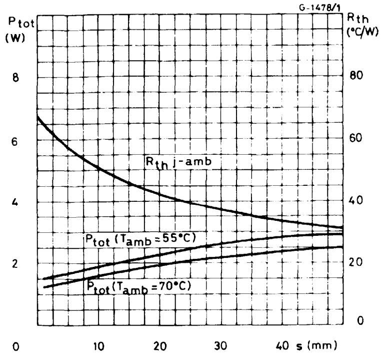


Figure 7 : Maximum Allowable Power Dissipation Versus Ambient Temperature.

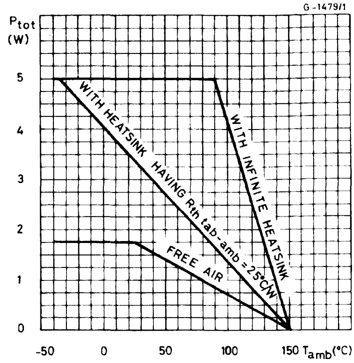
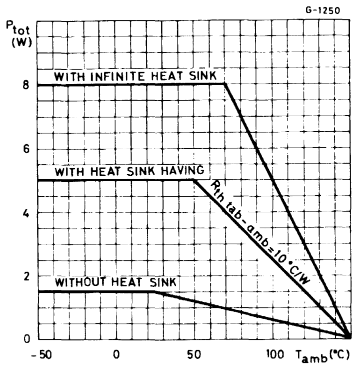


Figure 8 : Maximum Allowable Power Dissipation Versus Ambient Temperature.



SGS-THOMSON MICROELECTRONICS

TDA1180P

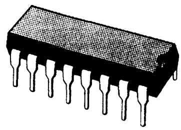
TV HORIZONTAL PROCESSOR

The TDA 1180P combines the following functions :

- NOISE GATED HORIZONTAL SYNC SEPARATOR
- NOISE GATED VERTICAL SYNC SEPARATOR
- HORIZONTAL OSCILLATOR WITH FREQUENCY RANGE LIMITER
- PHASE COMPARATOR BETWEEN SYNC PULSES AND OSCILLATOR PULSES (PLL)
- PHASE COMPARATOR BETWEEN FLYBACK PULSES AND OSCILLATOR PULSES (PLL)
- LOOP GAIN AND TIME CONSTANT SWITCHING (VCR)
- COMPOSITE BLANKING AND KEY PULSE GENERATOR
- PROTECTION CIRCUITS
- OUTPUT STAGES WITH HIGH CURRENT CAPABILITY

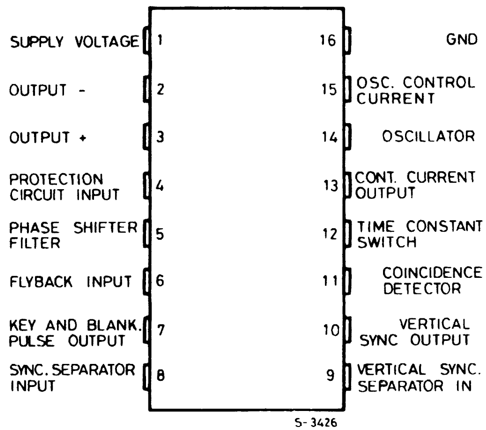
DESCRIPTION

The TDA 1180P is a horizontal processor circuit for b.w. and colour television receiver. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package.



ORDER CODE : TDA1180P

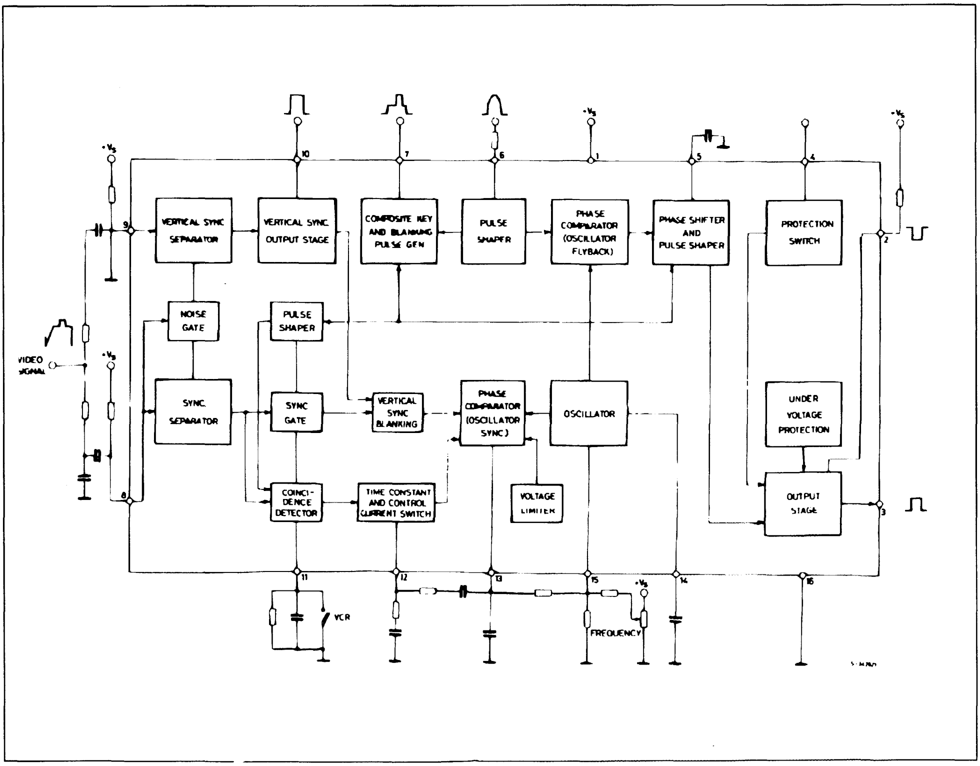
CONNECTION DIAGRAM (top view)



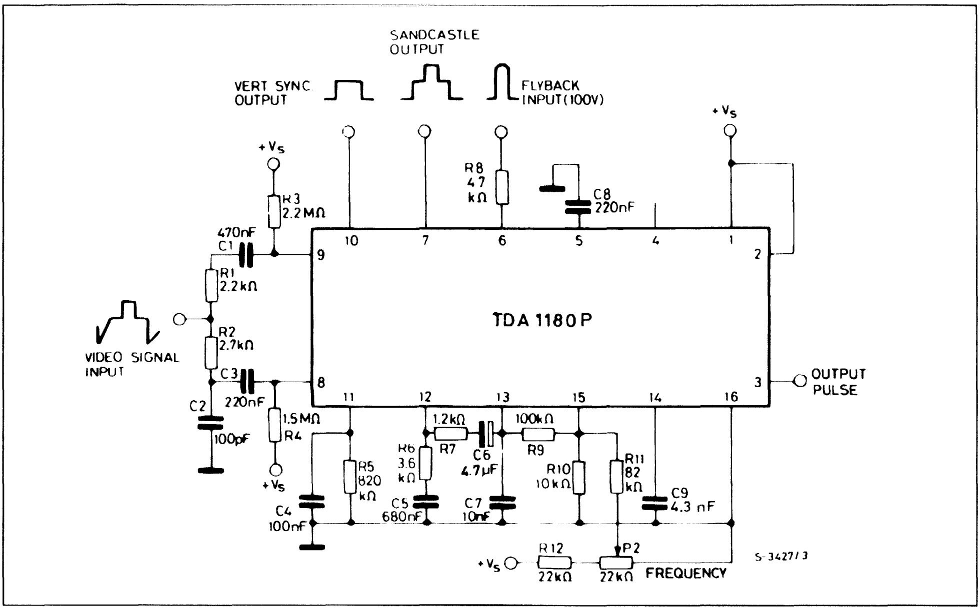
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	15	V
V_2	Voltage at Pin 2	18	V
V_4	Voltage at Pin 4	V_s	
V_8	Voltage at Pin 8	$\{V_s$ -6	V
V_9	Voltage at Pin 9	$\{+6$ -6	V
V_{11}	Voltage at Pin 11	V_s	
I_2	Pin 2 Peak Current	1	A
I_3	Pin 3 Peak Current	0.5	A
I_6	Pin 6 Current	30	mA
I_7	Pin 7 Current	20	mA
I_{10}	Pin 10 Current	30	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction–ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = 12 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range		9.5	12	13.2	V
I_s	Supply Current	$I_3 = 0$		42	52	mA
V_s	Supply voltage at which the output pulses (at pin 2 and 3) are switched off.				4	V

HORIZONTAL SYNC.SEPARATOR AND NOISE GATE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Peak to Peak Input Signal		1	3	6	V
V_8	Input Switching Voltage	I_8 = 80 µA		1.5		V
I_8	Input Switching Current	V_8 = 1.4 V		10		µA
I_8	Leakage Current	V_8 = – 5 V			1	µA

VERTICAL SYNC. SEPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Peak to Peak Input Signal		1	3	6	V
V_9	Input Switching Voltage	$I_9 = 80\ \mu A$		1.5		V
I_9	Input Switching Current	$V_9 = 1.4\ V$		5		µA
I_9	Leakage Current	$V_9 = -5\ V$			1	µA
V_{10}	Vertical Sync. Pulse Output Voltage	No Load at Pin 10	11			V
R_{10}	Output Resistance			10		KΩ
t_{LV}	Delay between Leading Edge of Input and Output Signals			17		µs
t_{TV}	Delay betwen Trailing Edge of Input and Output Signals			50		µs
t_V	Vertical Sync Pulse Duration			190		µs

PROTECTION CIRCUIT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_4	Input Voltage for Switching off the Output Pulses	Output Pulses OFF			0.5	V
		Output Pulses ON	1			
R_4	Input Resistance			200		KΩ
I_4	Input Current		5			µA

FLYBACK PULSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_6	Input Threshold Voltage of Blanking Generator			1.8		V
V_6	Input Threshold Voltage of Phase Comparator			7.6		V
I_6	Input Switching Current	$V_6 \geq 1.7\ V$		0.45		mA

OUTPUT PULSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_3	Peak to Peak Output Voltage	$I_3 = 150$ mApp		10		V
I_3	Output Current	$V_3 = 5\ V$		500		mA
R_3	Output Resistance	at Leading Edge of Output Pulse		3		Ω
		at Trailing Edge of Output Pulse		20		
t_p	Output Pulse Duration		20	22	26	µs

COMPOSITE BLANKING AND KEY PULSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{7K}	Key Pulse Output Peak Voltage		9	11		V
V_{7B}	Blanking Pulse Output Voltage		4.2	4.5	4.8	V
R_7	Output Resistance			100		Ω
t_{SK}	Phase Relation between Trailing Edge of Key Pulse and Middle of Sync Input Pulse			2.7		µs
t_K	Key Pulse Duration		3.5	3.8		µs
t_{fb}	Delay between Flyback Pulse and Blanking Pulse	V_6 = 1.7 V			0.2	µs

INTERNAL GATING PULSE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_g	Gating Pulse Duration			7.5		µs
t	Phase Relation between Middle of Sync Pulse and Trailing and Leading Edge of Gating Pulse			3.75		µs

COINCIDENCE DETECTOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{11}	Output Voltage	with Coincidence		6.8		V
		without Coincidence			4	
I_{11}	Peak Output Current			0.5		mA

VCR SWITCH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{11}	Input Voltage		0 to 4 or 8.5 to 12			V
$-I_{11}$	Output Current		35			µA
I_{11}	Output Current		0.4			mA

TIME CONSTANT SWITCH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{12}	Output Voltage			3		V
R_{12}	Output Resistance	4.5 V < V_{11} < 8 V V_{11} > 8.5 V or V_{11} < 4 V		100 40		Ω KΩ

OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{14}	Low Level Threshold Voltage			5.4		V
V_{14}	High Level Threshold Voltage			8.2		V
I_{14}	Charge Current			0.6		mA
I_{14}	Discharge Current			0.3		mA
V_{15}	Current Source Supply Voltage			3		V
I_{15}	Current Source Supply Current			0.3		mA
f_o	Free Running Frequency			15625		Hz
$\frac{\Delta f_o}{f_o}$	Adjustment Range			± 10		%
$\frac{\Delta f_o}{\Delta I_{15}}$	Frequency Control Sensitivity			52		$\frac{Hz}{\mu A}$
Δf_o	Frequency Change when V_s Drops to 4 V				± 10	%

OSCILLATOR–FLYBACK PULSE PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Control Voltage Range			9.4 to 8.2		V
I_5	Peak Control Current		– 0.6		+ 0.6	mA
I_5	Input Current (blocked phase detector)				5	μA
t_d	Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge			$t_p - t_f$		μs
$\frac{\Delta t}{\Delta t_d}$	Static Control Error				0.2	%

SYNC PULSE–OSCILLATOR PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{13}	Control Voltage Range			4.6 to 1.4		V
I_{13}	Control Peak Current		+ 2	– 2.2	– 2	mA
$\frac{\Delta f}{\Delta t}$	Phase Lock Loop Gain			2		$\frac{KHz}{\mu s}$
f	Catching and Holding Range			± 700		Hz

OVERALL PHASE RELATIONSHIP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_o	Phase Relation between Middle of Flyback Pulse and Middle of Sync Pulse			2.2		μs
$\frac{\Delta V_5}{\Delta t_o}$	Adjustment Sensitivity			65		$\frac{mV}{\mu s}$
$\frac{\Delta I_5}{\Delta t_o}$	Adjustment Sensitivity			16		$\frac{\mu A}{\mu s}$

Figure 1 : Vertical Sync. Output Pulse.

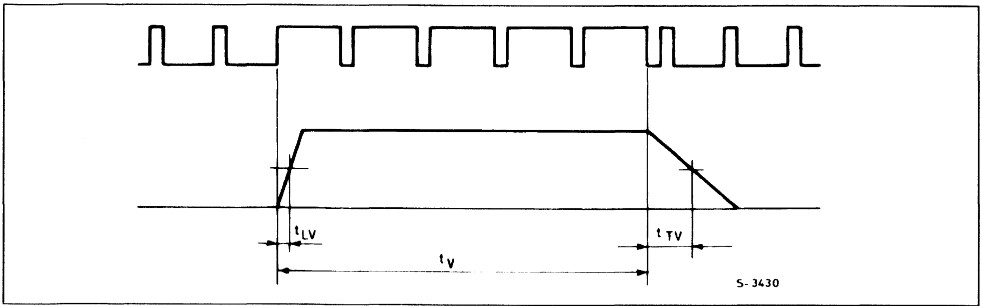


Figure 2 : Relationship of Main Waveform Phases.

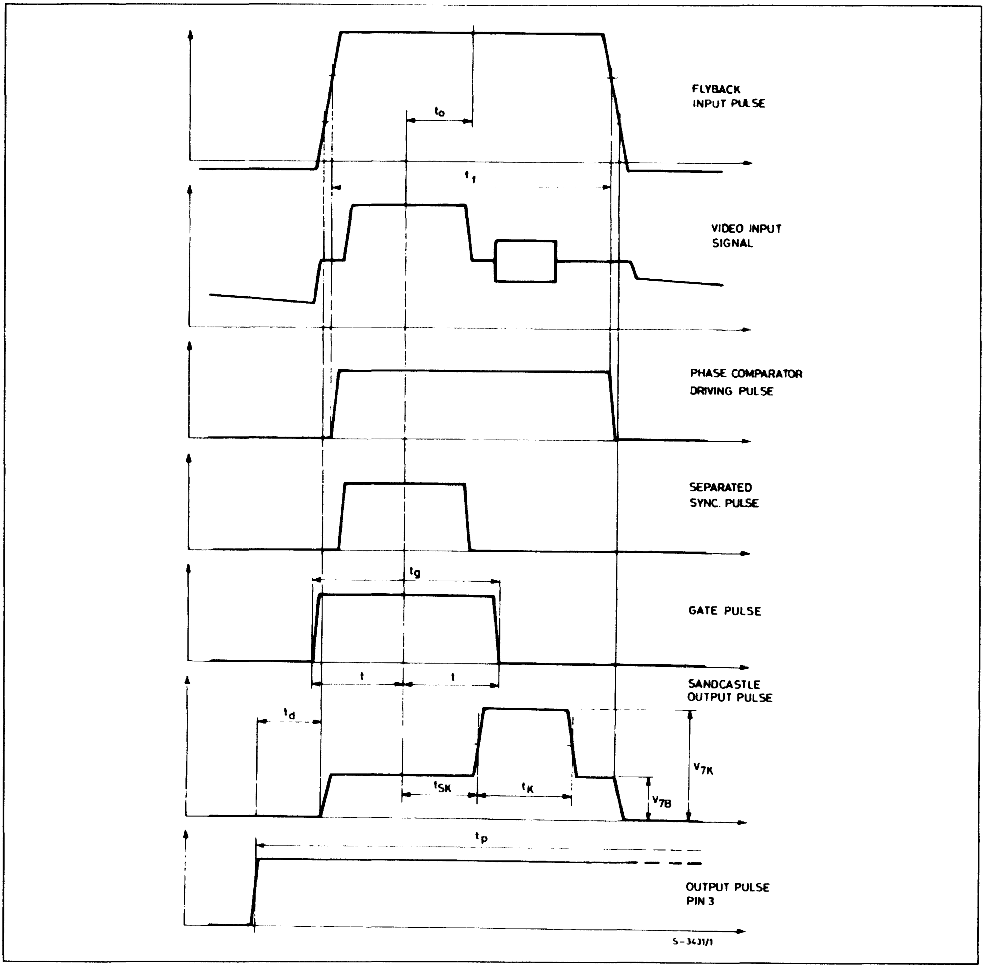


Figure 3 : Free Running Frequency vs. Supply Voltage.

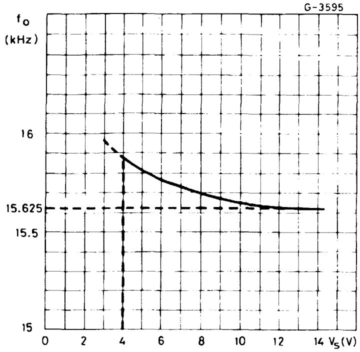


Figure 4 : Overall Phase Relation vs. Supply Voltage.

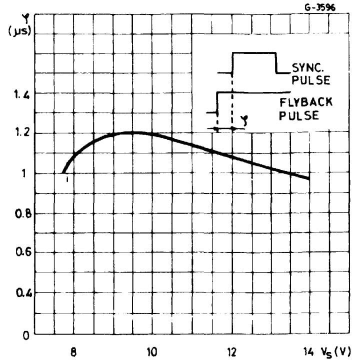
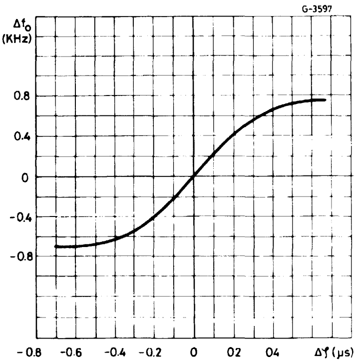


Figure 5 : Loop Gain.



APPLICATION INFORMATION

PIN 1 - POSITIVE SUPPLY

The operating supply voltage of the device ranges from 10 V to 13.2 V.

PIN 2 AND 3 - OUTPUT

The outputs of TDA 1180P are suitable for driving transistor output stages, they deliver positive pulse at pin 3 and negative pulse at pin 2.

The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.

The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.

Furthermore the output stages are internally protected against short circuit.

PIN 4 - PROTECTION CIRCUIT INPUT

By connecting pin 4 of the IC to earth the output pulses at pin 2 and 3 are shut off ; this function has been introduced to protect the final stages from overloads.

The same pulses are also shut off when the supply voltage falls below 4 V.

PIN 5 - PHASE SHIFTER FILTER

To compensate for the delay introduced by the line final stages, the flyback pulses to pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.

The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.

The maximum phase shift allowed is :

$$t_d = t_p - t_f$$

where t_f is the flyback pulse duration.

Pin 5 has high input and output resistance (current generator).

PIN 6 - FLYBACK INPUT

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.

The flyback input pulses are processed by a double threshold circuit ; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

PIN 7 - KEY AND BLANKING PULSE OUTPUT

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.

The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at pin 6.

The sum of the two signals (sandcastle pulse) is available on low impedance at output pin 7.

PIN 8 AND 9 - SYNC SEPARATORS INPUTS

The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.

The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.

PIN 10 - VERTICAL SYNC OUTPUT

The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.

The output impedance is typically 10 KΩ and the lowest amplitude without load is 11 V.

PIN 11 - COINCIDENCE DETECTOR

From the oscillator waveform a gate pulse 7 µs wide is taken whose phase position is centered on the horizontal syncronism.

The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.

This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.

When the two signals are not accurately aligned in time it means that the oscillator is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on pin 12 (small time constant of low-pass filter).

This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.

In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.

Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on pin 12 and reduces the sensitivity of the phase comparator.

In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.

To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting pin 11 to earth or to + V_s. The characteristics of the phase lock thus correspond to the lack of synchronization.

PIN 12 - TIME CONSTANT SWITCH, (see pin 11)

PIN 13 - CONTROL CURRENT OUTPUT

The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current I_{13} (proportional to the phase difference between the two signals) to pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.

The time constant of the filter can be switched between two values according to the impedance presented by pin 12.

The voltage limiter at the output of the phase comparator limits the voltage excursion on pin 13 and therefore the frequency range in which the oscillator remains held-in.

The output resistance of pin 13 is :
low when $V_{13} > 4.3$ V or $V_{13} < 1.6$ V
high when $1.6 \text{ V} < V_{13} < 4.3$ V.

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync, a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage ; inhibition remains even if the video signal is not present.

The free running frequency of the oscillator is determined by the values of the capacitor and of the resistor connected to pins 14 and 15 respectively.

To generate the line frequency output pulses, two theresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

PIN 14 - OSCILLATOR (see pin 13)

PIN 15 - OSCILLATOR CONTROL CURRENT INPUT (see pin 13)

PIN 16 - GROUND

Figure 6 : Application Circuit for Large Screen b.w. and Colour TV.

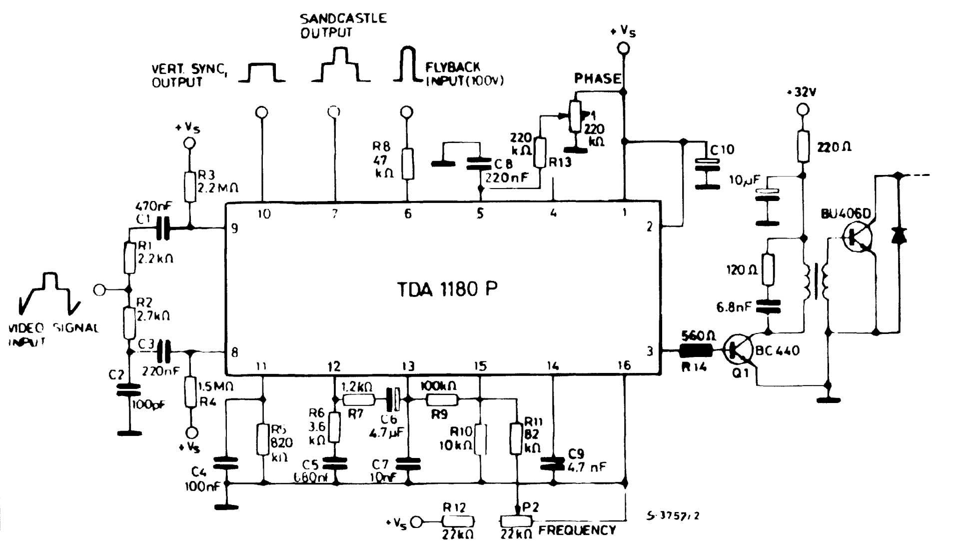


Figure 7 : P.C. Board and Component Layout for the Circuit in Figure 6 (1:1 scale).

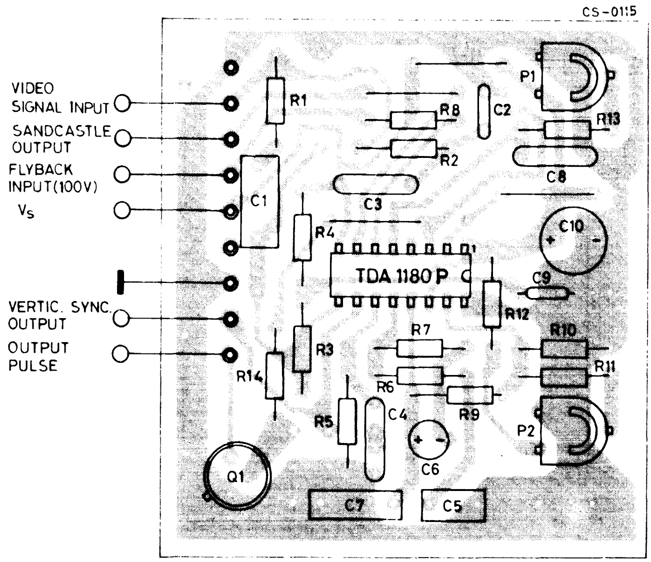


Figure 8 : Application Circuit for Small Screen b.w. TV.

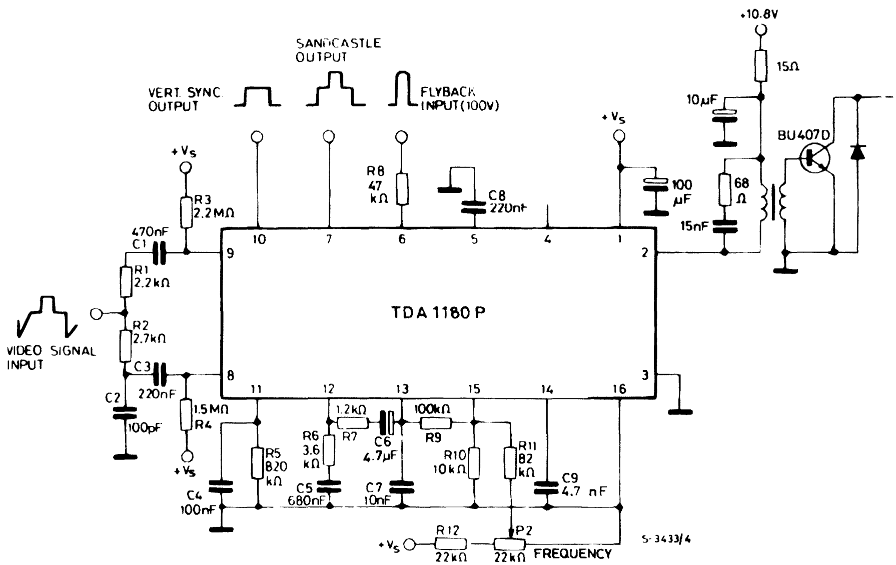
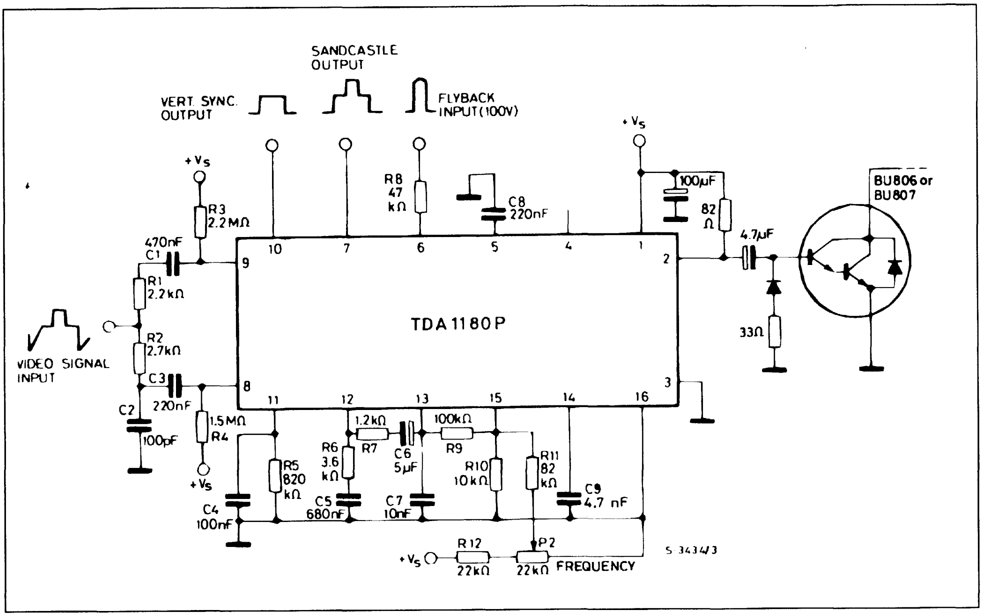


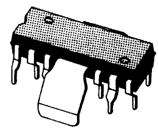
Figure 9 : Application Circuit for Darlington Output Stage.



COMPLETE TV SOUND CHANNEL

The TDA 1190Z is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It performs all the functions needed for the TV sound channel :

- IF LIMITER-AMPLIFIER
- ACTIVE LOW-PASS FILTER
- FM DETECTOR
- DC VOLUME CONTROL
- AF PREAMPLIFIER
- AF OUTPUT STAGE



FINDIP 12

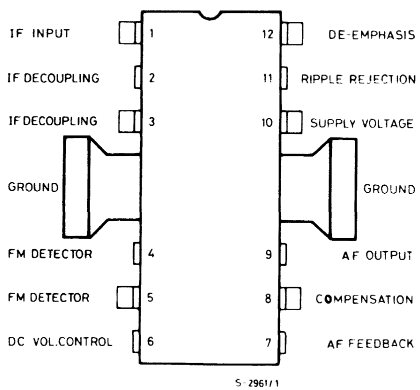
ORDER CODE : TDA1190Z

DESCRIPTION

The TDA 1190Z can give an output power of 4.2 W (d = 10 %) into a 16 Ω load at V_S = 24 V, or 1.5 W (d = 10 %) into an 8 Ω load at V_S = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.

The device has no irradiation problems, hence no external screening is needed.

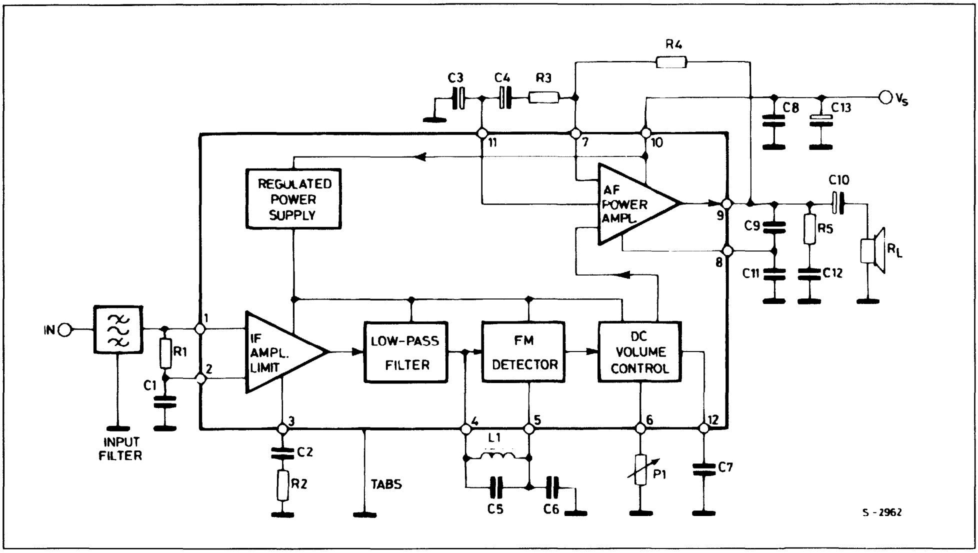
CONNECTION DIAGRAM (top view)



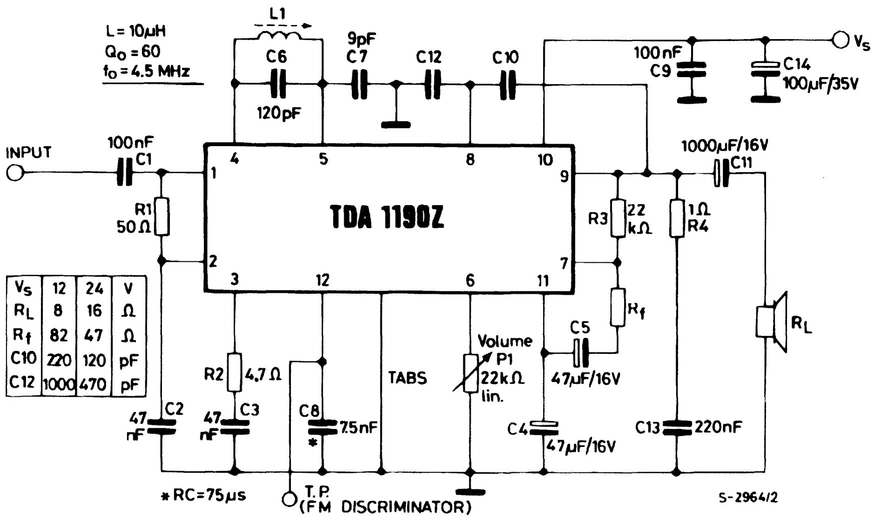
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 10)	28	V
V_i	Input Signal Voltage (pin 1)	1	V
I_o	Output Peak current (non-repetitive)	2	A
I_o	Output Peak Current (repetitive)	1.5	A
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 80 °C (free air)	5 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal Resistance Junction-tab	Max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70*	°C/W

* Obtained with tabs soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuit ; V_s = 24 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 10)		9		28	V
V_o	Quiescent Output Voltage (pin 9)	V_s = 24 V V_s = 12 V	11 5.1	12 6	13 6.9	V V
I_d	Quiescent Drain Current	P_l = 22 kΩ V_s = 24 V V_s = 12 V	11	22 19	45 40	mA mA
P_o	Output Power	d = 10 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 kHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		4.2 1.5		W W

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power	d = 2 % f_m = 400 Hz f_o = 4.5 MHz Δf = ± 25 kHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 3.5 1.4		 W W
V_i	Input Limiting Voltage (– 3 dB) at Pin 1	f_o = 4.5 MHz f_m = 400 Hz P_1 = 0 Δf = ± 7.5 kHz		40	100	µV
d	Distortion	P_o = 50 mW f_m = 400 Hz f_o = 4.5 MHz Δf = ± 7.5 kHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.75 1		 % %
B	Frequency Response of Audio Amplifier (– 3 dB)	R_L = 16 Ω C_{10} = 120 pF C_{12} = 470 pF P_1 = 22 kΩ R_f = 82 Ω R_f = 47 Ω		 70 to 12000 70 to 7000		 Hz Hz
V_o	Recovered Audio Voltage (pin. 12)	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δf = ± 7.5 kHz P_1 = 0		120		mV
AMR	Amplitude Modulation Rejection	V_i ≥ 1 mV f_o = 4.5 MHz f_m = 400 Hz Δ_f = ± 25 kHz m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i ≥ 1 mV V_o = 4 V f_o = 4.5 MHz f_m = 400 Hz Δf = ± 25 kHz	50	65		dB
R_f	External Feedback Resistance (between pins 7 and 9)				25	kΩ
R_i	Input Resistance (pin 1)	V_i = 1 mV f_o = 4.5 MHz		30		kΩ
C_i	Input Capacitance (pin 1)			5		pF
SVR	Supply Voltage Rejection	R_L = 16 Ω f_{ripple} = 120 Hz P_1 = 22 kΩ		46		dB
A	DC Volume Control Attenuation	P_1 = 12 kΩ		90		dB

Figure 1 : Relative Audio Output Voltage and Out-Noise vs. Input Signal.

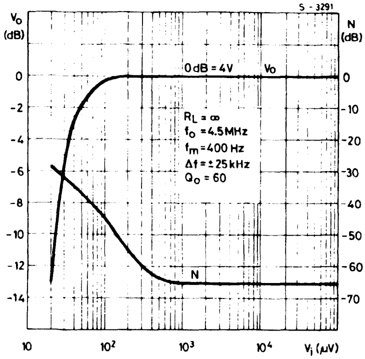


Figure 2 : Output Voltage Attenuation vs. DC Volume Control Resistance.

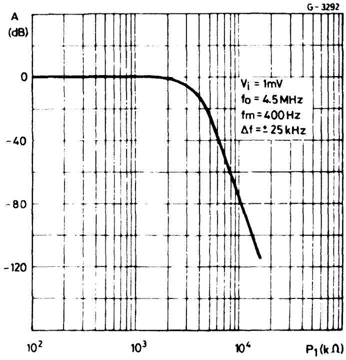


Figure 3 : Amplitude Modulation Rejection vs. Input Signal.

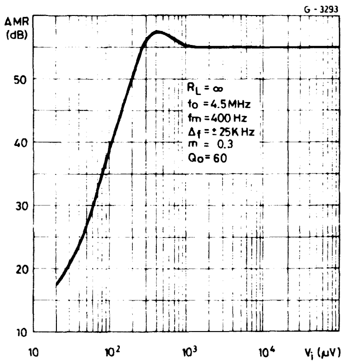


Figure 4 : Δ AMR vs. Tuning Frequency Change.

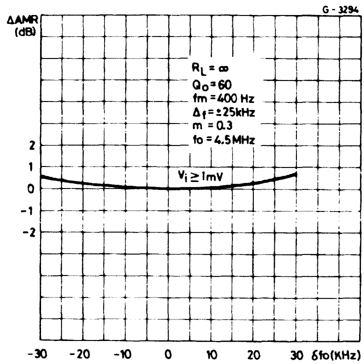


Figure 5 : Recovered Audio Voltage vs. Unloaded Q Factor of the Detector Coil.

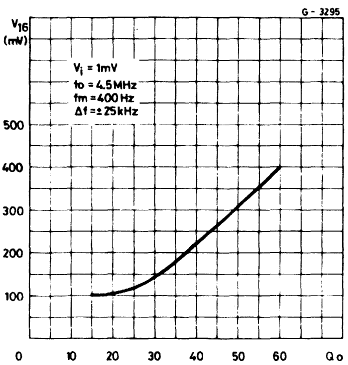


Figure 6 : Distortion vs. Output Power.

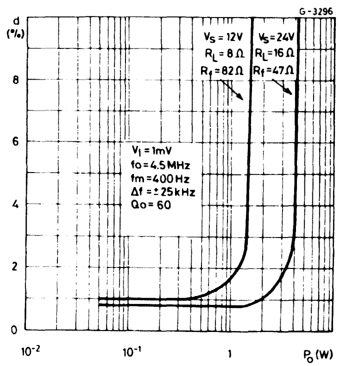


Figure 7 : Distortion vs. Frequency Deviation.

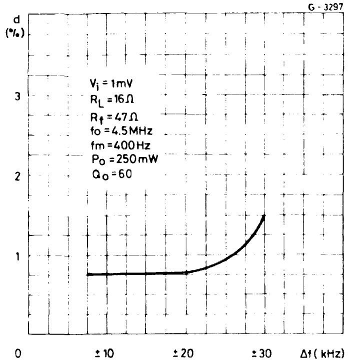


Figure 8 : Distortion vs. Tuning Frequency Change.

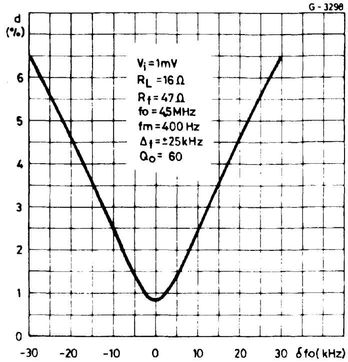


Figure 9 : Audio Amplifier Frequency Response.

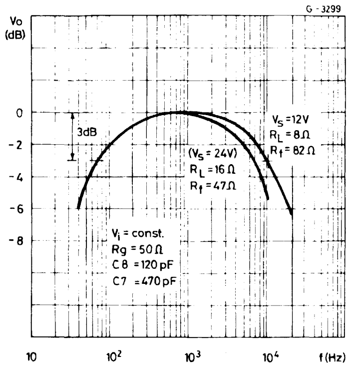


Figure 10 : Supply Voltage Ripple Rejection vs. Ripple Frequency.

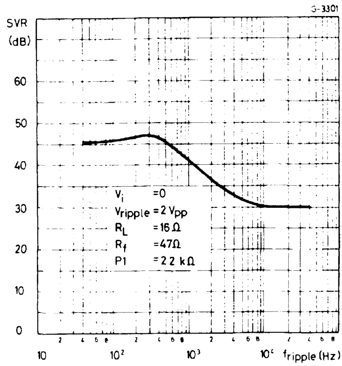


Figure 11 : Supply Voltage Ripple Rejection vs. Volume Control Attenuation.

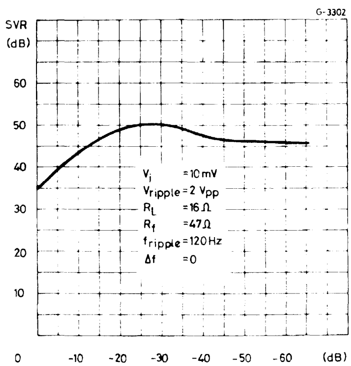


Figure 12 : Output Power vs. Supply Voltage.

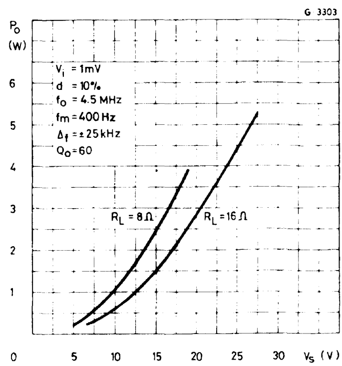


Figure 13 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).

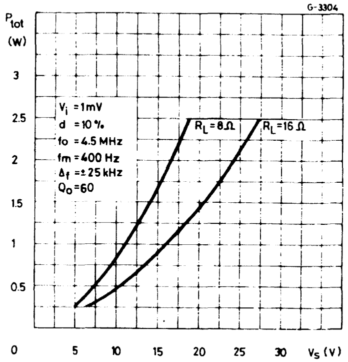


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

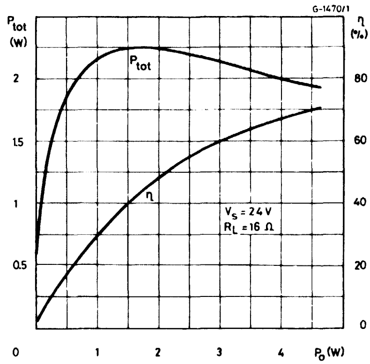
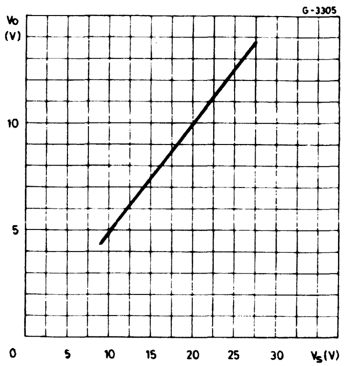


Figure 15 : Quiescent Output Voltage (pin 9) vs. Supply Voltage.



APPLICATION INFORMATION

The electrical characteristics of the TDA 1190Z remain almost constant over the frequency range of 4.5 to 6 MHz, therefore it can be used in all television standard (FM mod.). The TDA 1190Z has a high input impedance, so it can work with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 7, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier must enter into clipping.

The capacitor connected between pins 9 and 8 determines the upper cut-off frequency of the audio band. If larger bandwidth is required C_{10}, C_{12} must be reduced keeping C_{12}/C_{10} as in fig. 16.

The capacitor connected between pin 12 and ground, toghether with the internal resistor of 10 KΩ, forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by inductive load and the wires connecting the loudspeaker.

Figure 16 : Typical Application Circuit.

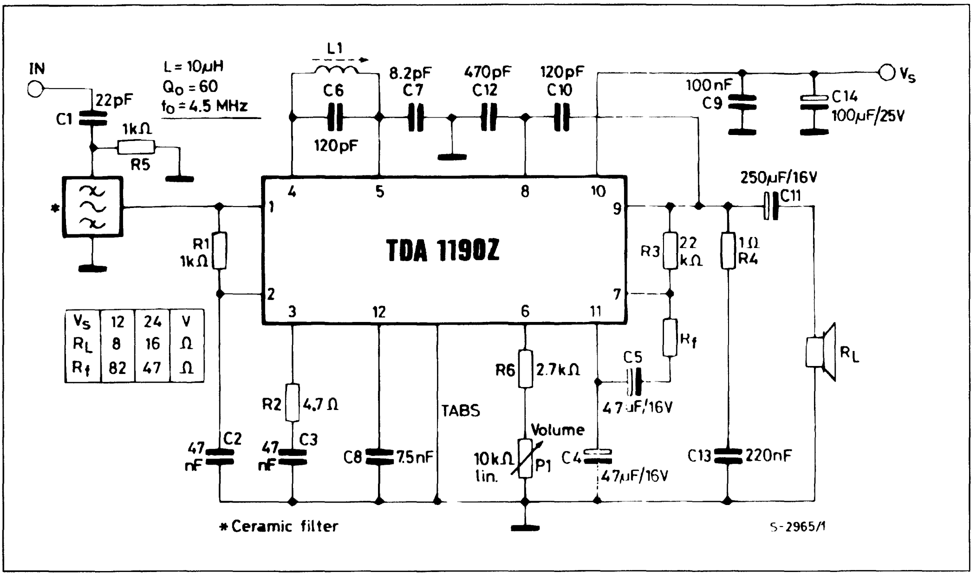
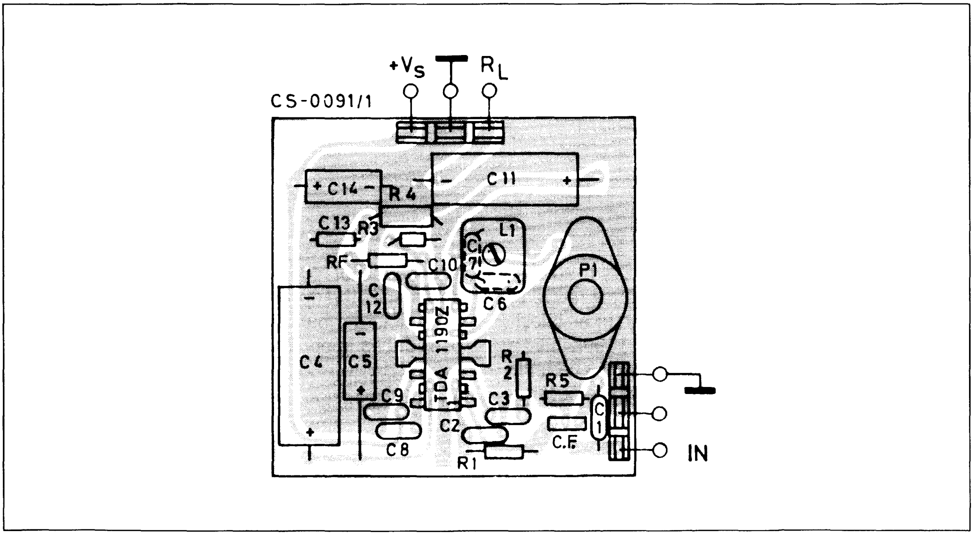


Figure 17 : P.C. Board and Component Layout of the Circuit Shown in Fig. 16.



MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA1190Z can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 18) or to an external heatsink (fig. 19).

The diagram of figure 20 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the tab temperature must not exceed 260 °C and the soldering time mumst not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 18 : Example of P.C. Board Copper Area Which is Used as Heatsink.

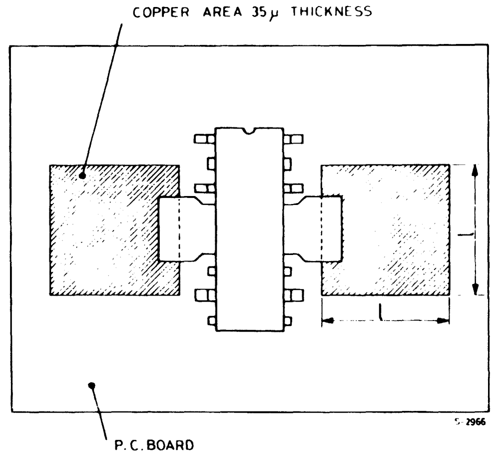


Figure 19 : External Heatsink Mounting Example.

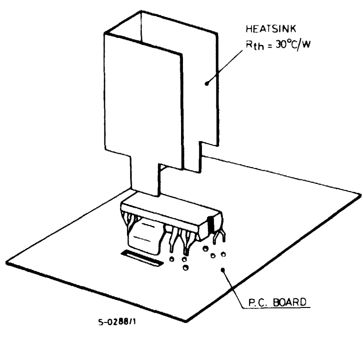


Figure 20 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l" .

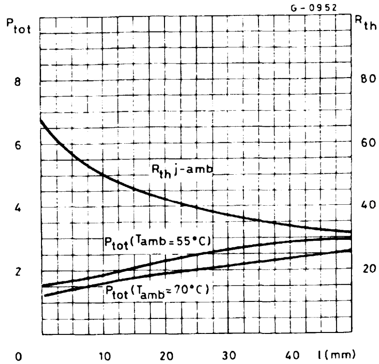
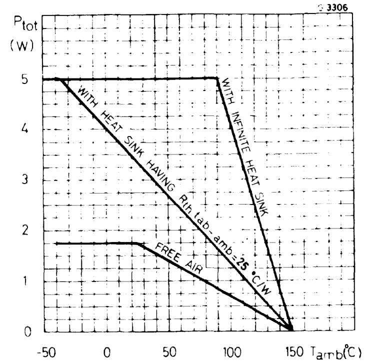


Figure 21 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



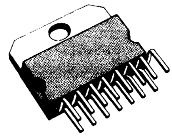
TDA1670A

VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

The functions incorporated are :

- SYNCHRONIZATION CIRCUIT
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER WITH HIGH CURRENT CAPABILITY
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT



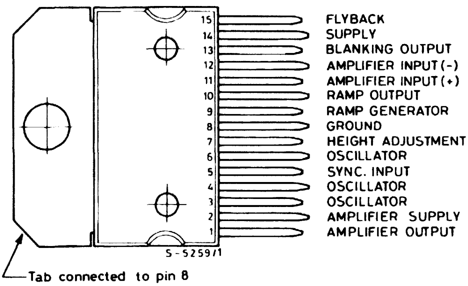
MULTIWATT-15

ORDER CODE : TDA1670A

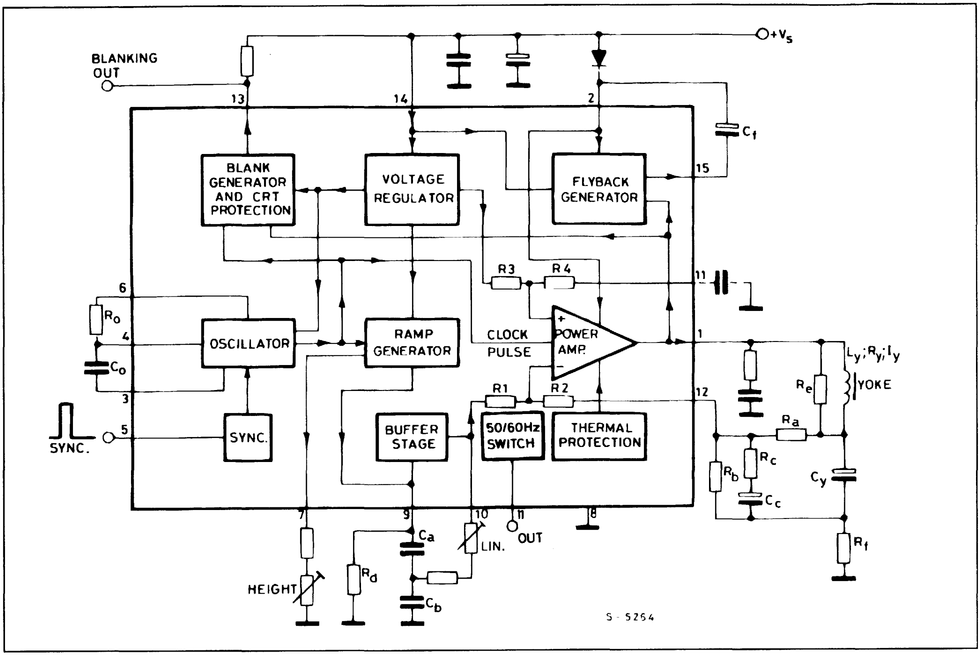
DESCRIPTION

The TDA 1670A is a monolithic integrated circuit in 15-lead Multiwatt ® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, BW TVs, monitors and displays.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



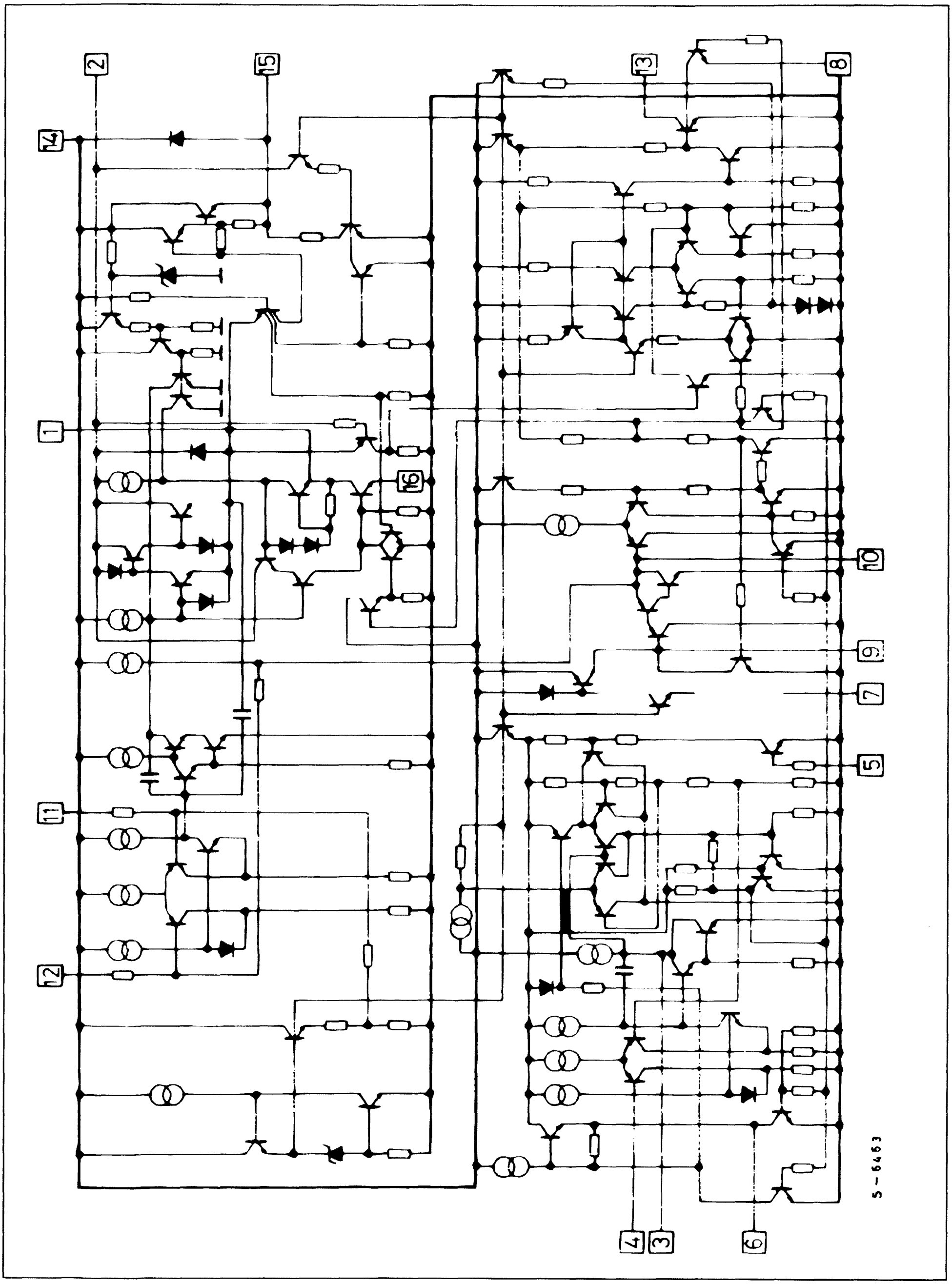
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 14	35	V
V_1, V_2	Flyback Peak Voltage	60	V
V_5	Sync. Input Voltage	20	V
V_{11}, V_{12}	Power Amplifier Input Voltage	V_s – 10	V
V_{13}	Voltage at Pin 13	V_s	
I_o	Output Current (non repetitive) at t = 2 msec	3	A
I_o	Output Peak Current at f = 50 Hz t > 10 µsec	2	A
I_o	Output Peak Current at f = 50 Hz t ≤ 10 µsec	3.5	A
I_{15}	Pin 15 Peak to Peak Flyback Current at f = 50 Hz, t_{fly} ≤ 1.5 msec	3	A
I_{15}	Pin 15 DC Current at $V_1 < V_{14}$	100	mA
P_{tot}	Maximum Power Dissipation at T_{case} ≤ 60 °C	30	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction–case	Max	3	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	40	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_s = 35 V, T_{amb} = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_1 = 0$		16	36	mA	1b
$-I_9$	Ramp Generator Bias Current	$V_9 = 0$		0.02	1	µA	1b
$-I_9$	Ramp Generator Current	$V_9 = 0$; $-I_7 = 20$ µA	18.5	20	21.5	µA	1b
$\left\|\frac{\Delta I_9}{I_9}\right\|$	Ramp Generator Non-linearity	ΔV_9 = 0 to 15 V $I_7 = 20$ µA		0.2	1	%	1b
I_{14}	Pin 14 Quiescent Current			25	45	mA	1b
V_1	Quiescent Output Voltage	$V_S = 35$ V ; $R_a = 2.2$ KΩ $R_b = 1$ KΩ	16.4	17.8	19.5	V	1a
		$V_s = 15$ V ; $R_a = 390$ Ω $R_b = 1$ KΩ	6.9	7.5	8.1	V	
V_{1L}	Output Saturation Voltage to Ground	$I_1 = 1.2$ A		1	1.4	V	1c
V_{1H}	Output Saturation Voltage to Supply	$-I_1 = 1.2$ A		1.6	2.2	V	1d
V_4	Oscillator Virtual Ground			0.45		V	1b
V_7	Regulated Voltage at Pin 7	$-I_7 = 20$ µA	6.3	6.6	7	V	1b
$\frac{\Delta V_7}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	ΔV_s = 15 to 35 V		1	2	mV/V	1b
V_{11}	Amplifier Input (+) Reference Voltage		4.1	4.4	4.7	V	1b
V_{13}	Blanking Output Saturation Voltage	$I_{13} = 10$ mA		0.35	0.5	V	1a
V_{15}	Pin 15 Saturation Voltage to Ground	$I_{15} = 20$ mA		1	1.5	V	1a

Figure 1 : DC Test Circuit.

Figure 1a.

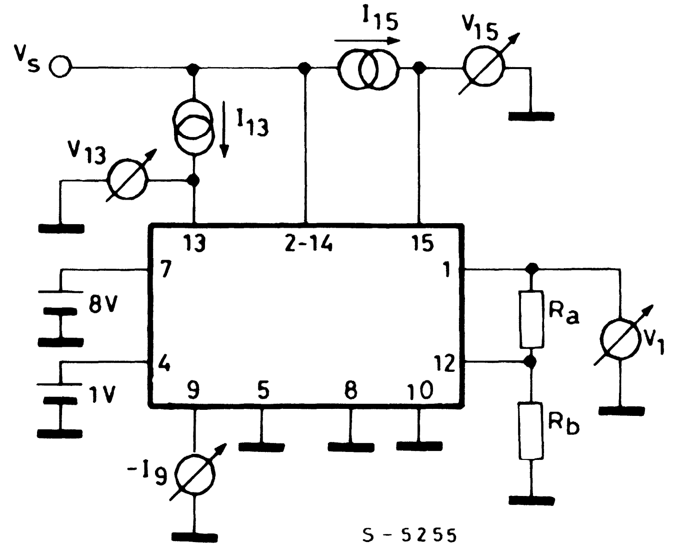


Figure 1b.

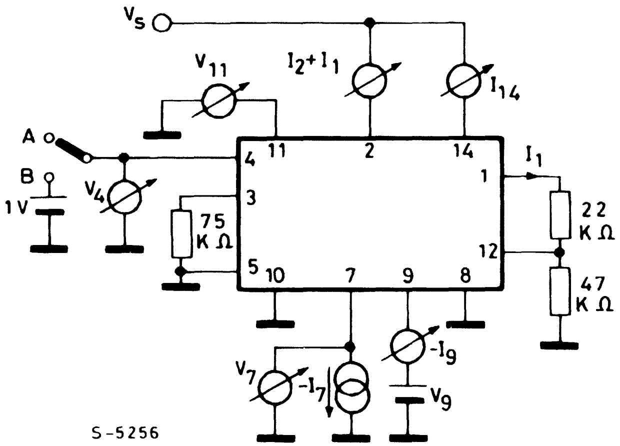


Figure 1c.

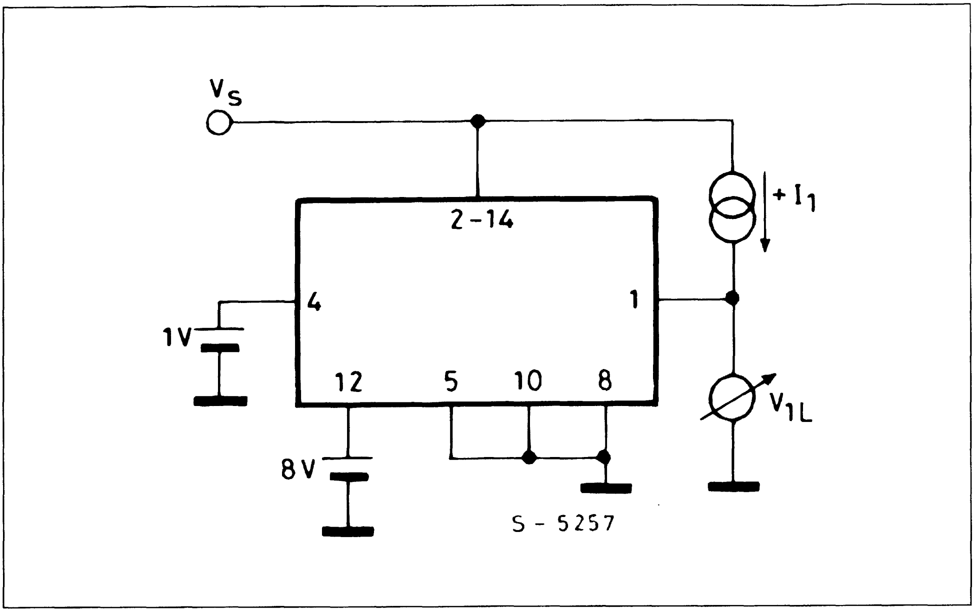
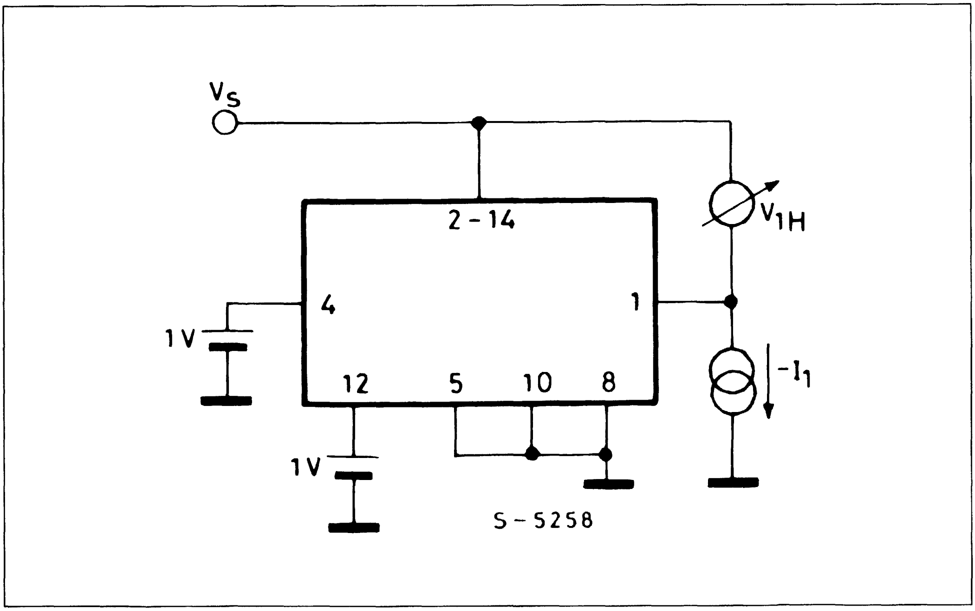


Figure 1d.



ELECTRICAL CHARACTERISTICS (refer to the A.C. test circuit of Fig. 2, T_{amb} = 25 °C, Vs = 24 V, f = 50 Hz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 2 App		295		mA
I_5	Sync. Input Current Required to Sync.		100			μA
V_1	Flyback Voltage	I_y = 2 App		50		V
V_3	Peak to Peak Oscillator Sawtooth Voltage	I_5 = 0		3.6		V
		I_5 = 100 μA		3.4		V
V_{10thL}	Start Scan Level of the Input Ramp			1.7		V
t_{fly}	Flyback Time	I_y = 2 App		0.6		ms
t_{blank}	Blanking Pulse Duration	f_o = 50 Hz T_j = 75 °C	1.33	1.4	1.47	ms
		f_o = 60 Hz T_j = 75 °C		1.17		ms
f_o	Free Running Frequency	R_o = 7.5 K C_o = 330 nF T_j = 75 °C	42	43.5	46	Hz
		R_o = 6.2 K C_o = 330 nF T_j = 75 °C		52.5		Hz
		R_o = 5.1 K C_o = 330 nF T_j = 75 °C		63.5		Hz
		R_o = 3.9 K C_o = 330 nF T_j = 75 °C		83		Hz
Δt	Synchronization Range	R_o = 7.5 K @ 50 Hz C_o = 330 nF	13.5	15		Hz
		R_o = 6.2 K @ 60 Hz C_o = 330 nF		17.5		Hz
		R_o = 5.1 K @ 70 Hz C_o = 330 nF		20.5		Hz
		R_o = 3.9 K @ 1000 Hz C_o = 330 nF		27.5		
T_{jso} Junction Temperature for Thermal Shutdown				140		°C

For other to use the following equation to calculate the approximate value of R_0 maintaining C_0 = 330 nF

$$R_0 = \frac{325 \cdot 10^3}{f_0}$$

Figure 2 : AC Test Circuit.

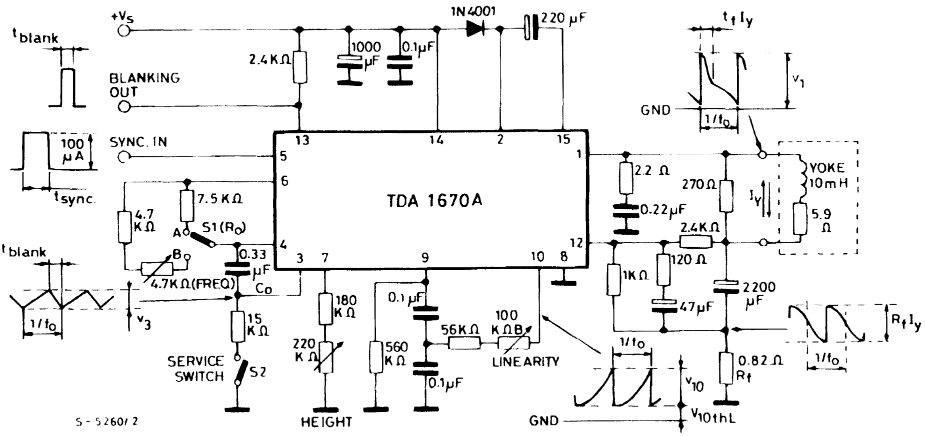
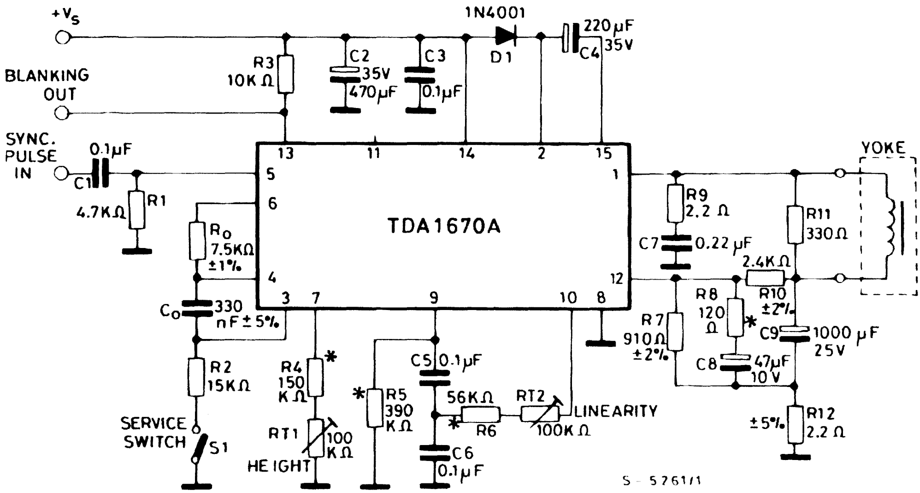


Figure 3 : Application Circuit for Smal Screen 90 % TVC Set (Ry = 15 Ω, Ly = 30 mH, ly = 0.82 App).



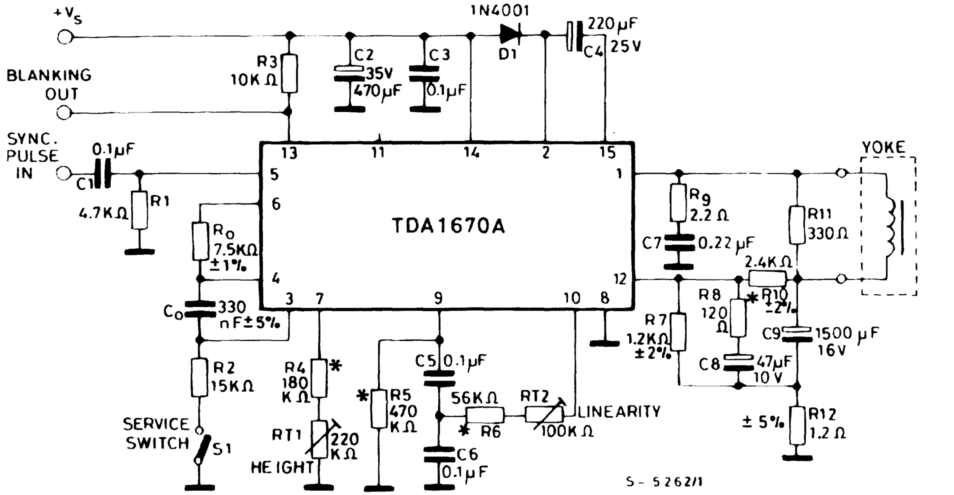
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum Supply Voltage	25	V
I_s	Supply Current	140	mA
t_{fly}	Flyback Time	0.7	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
$^*P_{tot}$	Power Dissipation	2.4	W
$^*R_{th\ heatsink}$	Thermal Resistance of the Heatsink For T_{amb} = 60 °C and $T_{j\ max}$ = 110 °C For T_{amb} = 60 °C and $T_{j\ max}$ = 120 °C	 13 16	 °C/W °C/W

* Worst case condition.

Figure 4 : Application Circuit for 110° TVC set (Ry = 9.6 Ω ; Ly = 24.6 mH ; Iy = 1.2 App).



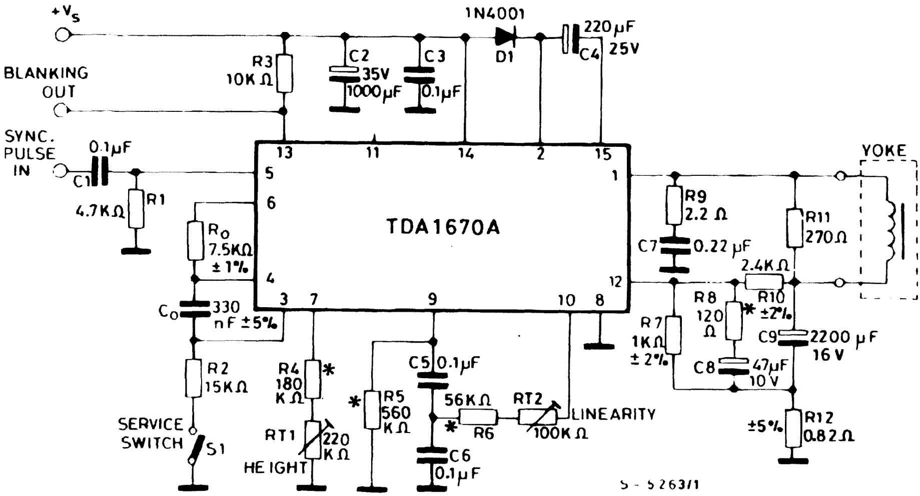
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum Supply Voltage	22.5	V
I_s	Supply Current	185	mA
t_{fly}	Flyback Time	1	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
*P_{tot}	Power Dissipation	2.7	W
*$R_{th\ heatsink}$	Thermal Resistance of the Heatsink For T_{amb} = 60 °C and $T_{j\ max}$ = 110 °C For T_{amb} = 60 °C and $T_{j\ max}$ = 120 °C	 11.5 14.5	 °C/W °C/W

* Worst case condition.

Figure 5 : Application Circuit for 110 ° TVC set (Ry = 5.9 Ω ; Ly = 10 mH ; Iy = 1.95 App).



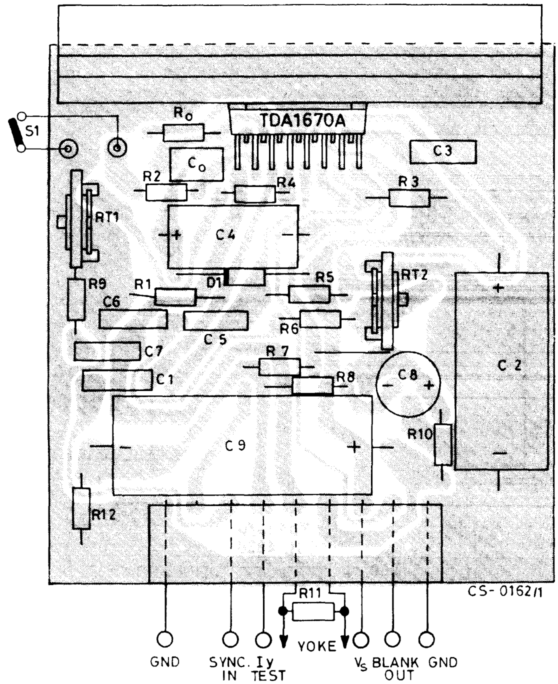
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_S	Minimum Supply Voltage	24	V
I_s	Supply Current	285	mA
t_{fly}	Flyback Time	0.6	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
*P_{tot}	Power Dissipation	4.3	W
*$R_{th\ heatsink}$	Thermal Resistance of the Heatsink For T_{amb} = 60 °C and $T_{j\ max}$ = 110 °C For T_{amb} = 60 °C and $T_{j\ max}$ = 120 °C	 6.5 8.5	 °C/W °C/W

* Worst case condition. ** See "Thermal considerations".

Figure 6 : P.C. Board and Components Layout for the ApplicationCircuits of fig. 3, 4 and 5 (1 : 1 scale).



APPLICATION INFORMATION (refer to the block diagram)

OSCILLATOR AND SYNC GATE
(clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches R_o high or low so allowing the charge or the discharge of C_o under constant current conditions.

The sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 4 is the inverting input of the amplifier used as integrator.

Pin 6 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 3 is the output of the amplifier.

Pin 5 is the input for sync pulses (positive).

RAMP GENERATOR AND BUFFER STAGE

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor ; a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

Pin 7 The resistance between pin 7 and ground defines the mirror current and than the height of the scanning.

Pin 9 is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.

Pin 10 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

POWER AMPLIFIER

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main during the trace period, and by the flyback generator circuit during the most part of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 12 is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 12 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

Pin 11 is the non-inverting input and it is not used. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.

This pin is only used on a quasi-bridge configuration.

Pin 1 is the output of the power amplifier and it drives the yoke by a negative slope current ramp. Re and the Boucherot cell are used to stabilize the power amplifier.

Pin 2 The supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main voltage V_S by a diode, while during the retrace time this pin is supplied from the flyback generator.

FLYBACK GENERATOR

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 2).

When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed : the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 15 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 2 (see pin 2).

BLANKING GENERATOR AND CRT PROTECTION

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. if the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 13 is an open collector output where the blanking pulse is available.

VOLTAGE REGULATOR

The main supply voltage V_S is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 14 is the main supply voltage input V_S (positive).

Pin 8 is the GND pin or the negative input of V_S.

Figure 7 : Output Saturation Voltage to Ground vs. Peak Output Current.

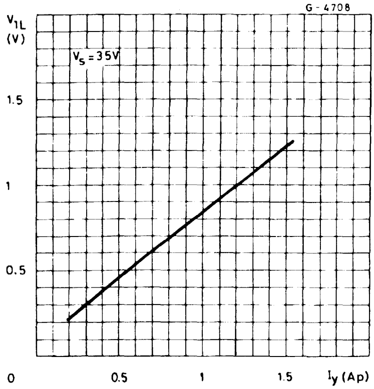


Figure 8 : Output Saruration Voltage to Supply vs. Output Peak Current.

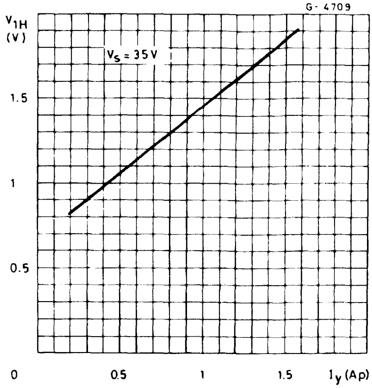
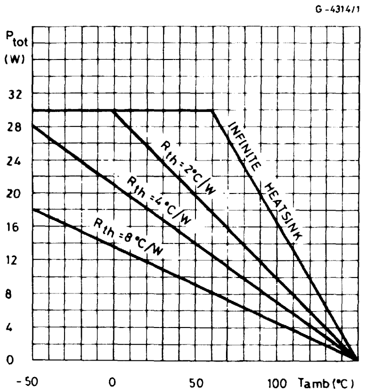


Figure 9 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

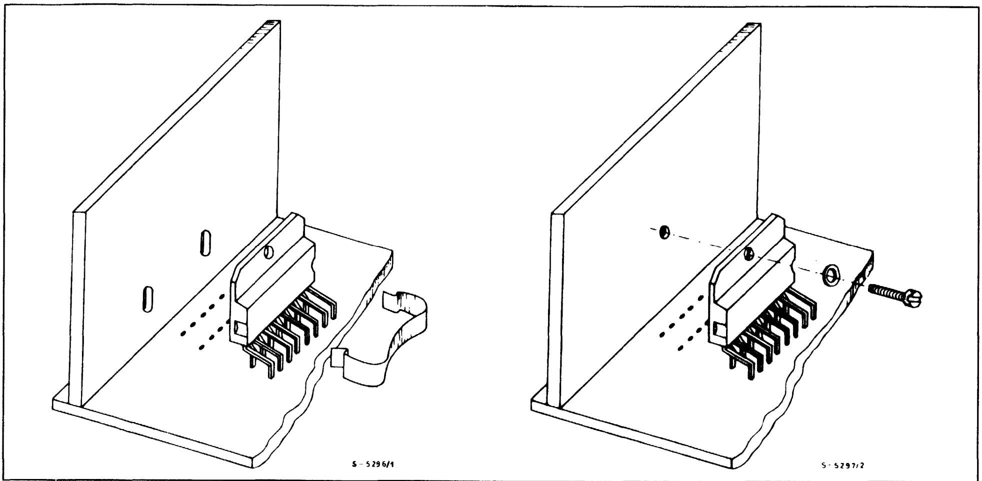


MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 10 : Mounting Example.



SGS-THOMSON MICROELECTRONICS

TDA1770A

VERTICAL DEFLECTION CIRCUIT

ADVANCE DATA

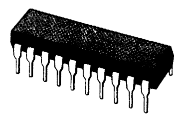
The functions incorporated are :
- SYNCHRONIZATION CIRCUIT
- PRECISION OSCILLATOR AND RAMP GENERATOR
- POWER OUTPUT AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT SCREEN PROTECTION CIRCUIT WHICH BLANKS THE BEAM CURRENT IN THE EVENT OF LOSS OF VERTICAL DEFLECTION CURRENT.

DESCRIPTION

The TDA 1770A is a monolithic integrated circuit in 20-lead plastic package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke.

It offers a wide range of applications in portable CTVs, BW TVs, monitors and displays.

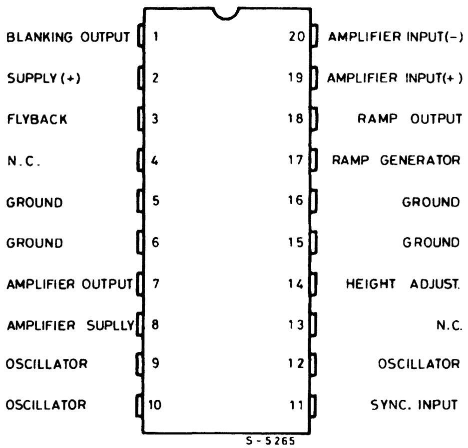
The TDA 1770 A is assembled in a new 20-lead plastic package which has 4 centre pins connected together and used for heatsinking.



DIP-20

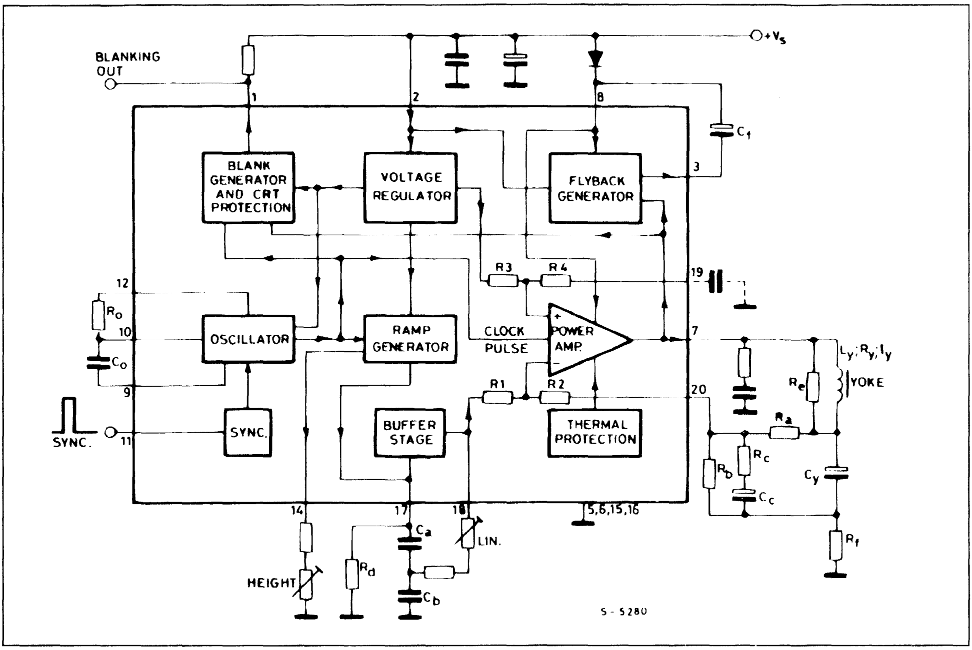
ORDER CODE : TDA1770A

CONNECTION DIAGRAM (top view)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 2	35	V
V_7, V_8	Flyback Peak Voltage	60	V
V_{11}	Sync. Input Voltage	20	V
V_{19}, V_{20}	Power Amplifier Input Voltage	V_S – 10	V
V_1	Voltage at Pin 1	V_s	
I_O	Output Current (non repetitive) at t = 2 msec	2	A
I_O	Output Peak Current at f = 50 Hz t > 10 µsec	1.2	A
I_O	Output Peak Current at f = 50 Hz t ≤ 10 µsec	2.2	A
I_3	Pin 3 Peak to Peak Flyback Current at f = 50 Hz, t_{fly} ≤ 1.5 msec	2	A
I_3	Pin 3 DC Current at $V_7 < V_2$	50	mA
P_{tot}	Maximum Power Dissipation : at T_{pins} ≤ 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 35 V, T_{amb} = 25 °C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current			25	45	mA	1b
I_8	Pin 8 Quiescent Current	$I_7 = 0$		16	36	mA	1b
$-I_{17}$	Ramp Generator Bias Current	$V_{17} = 0$		0.02	1	µA	1a
$-I_{17}$	Ramp Generator Current	$V_{17} = 0$; $-I_{14} = 20$ µA	18.5	20	21.5	µA	1b
$\left\|\frac{\Delta I_{17}}{I_{17}}\right\|$	Ramp Generator Non-linearity	$\Delta V_{17} = 0$ to 15 V $I_{14} = 20$ µA		0.2	1	%	1b
V_1	Blanking Output Saturation Voltage	$I_1 = 10$ mA		0.35	0.5	V	1b
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 20$ mA		1	1.5	V	1a
V_7	Quiescent Output Voltage	$V_s = 35$ V ; $R_a = 2.2$ KΩ $R_b = 1$ KΩ	16.4	17.8	19.5	V	1a
		$V_s = 15$ V ; $R_a = 390$ Ω $R_b = 1$ KΩ	6.9	7.5	8.1	V	
V_{7L}	Output Saturation Voltage to Ground	$I_7 = 0.7$ A		0.7	1	V	1c
V_{7H}	Output Saturation Voltage to Supply	$-I_7 = 0.7$ A		1.3	1.8	V	1d
V_{10}	Oscillator Virtual Ground			0.45		V	1a
V_{14}	Regulated Voltage at Pin 14	$-I_{14} = 20$ µA	6.3	6.6	7	V	1b
$\frac{\Delta V_{14}}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_s = 15$ to 35 V		1	2	mV/V	1b
V_{19}	Amplifier Input (+) Reference Voltage		4.1	4.4	4.7	V	1b

Figure 1 : DC Test Circuit.

Figure 1a.

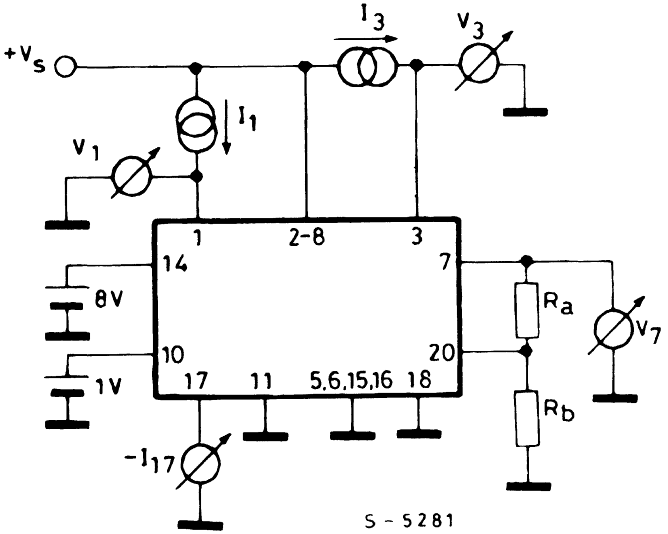


Figure 1b.

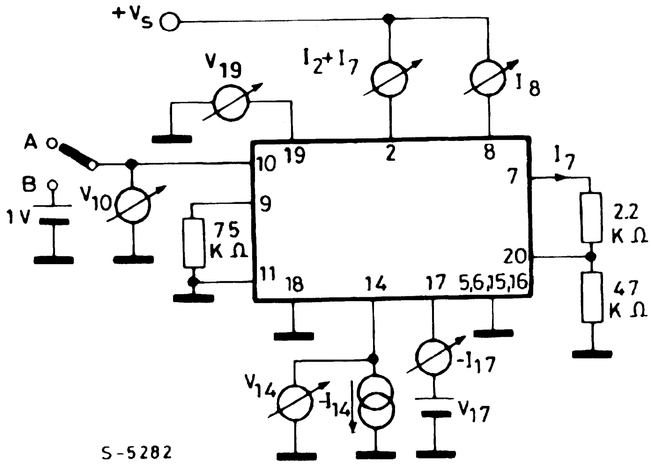


Figure 1c.

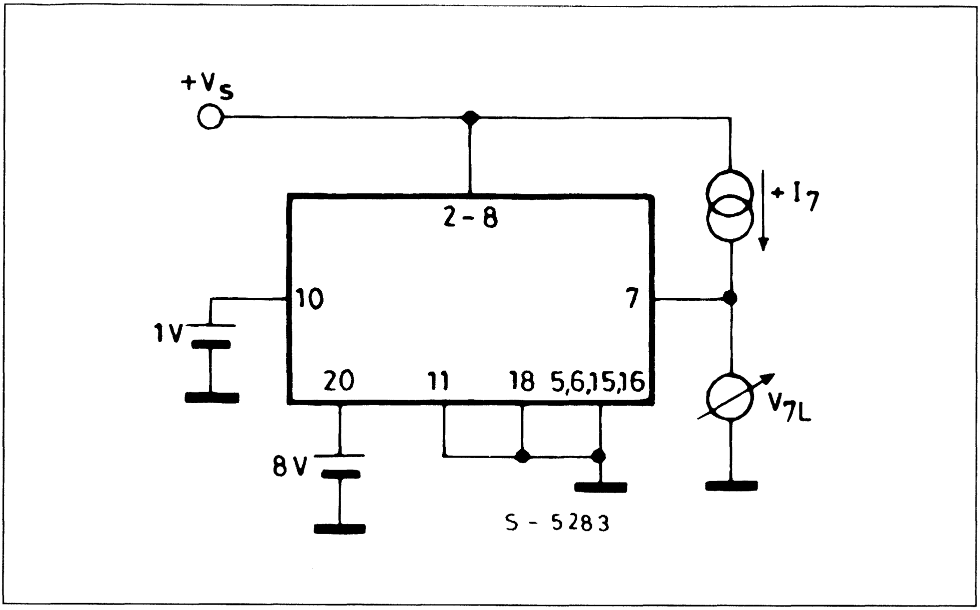
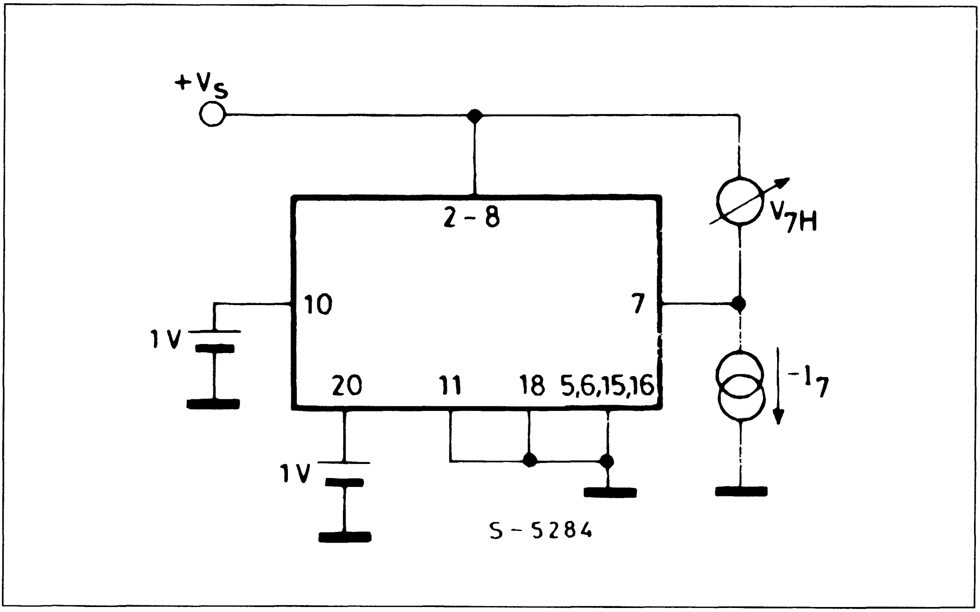


Figure 1d.



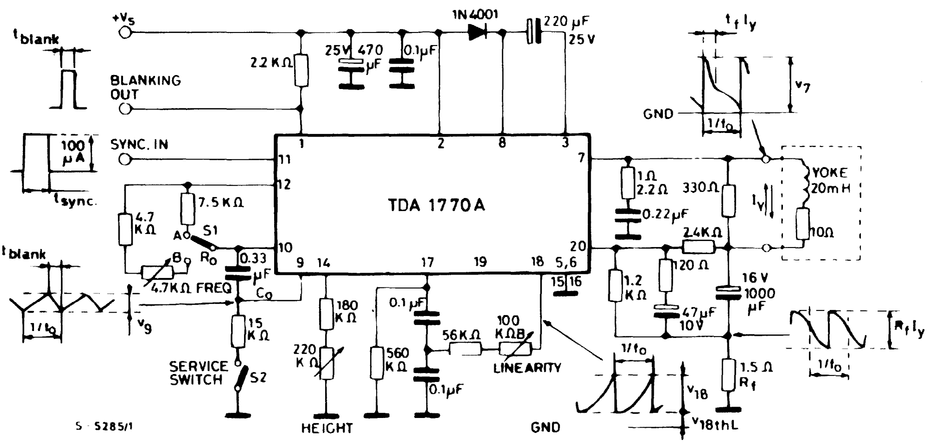
ELECTRICAL CHARACTERISTICS

(refer to the AC test circuit, V_s = 22 V, f = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

AC CHARACTERISTICS

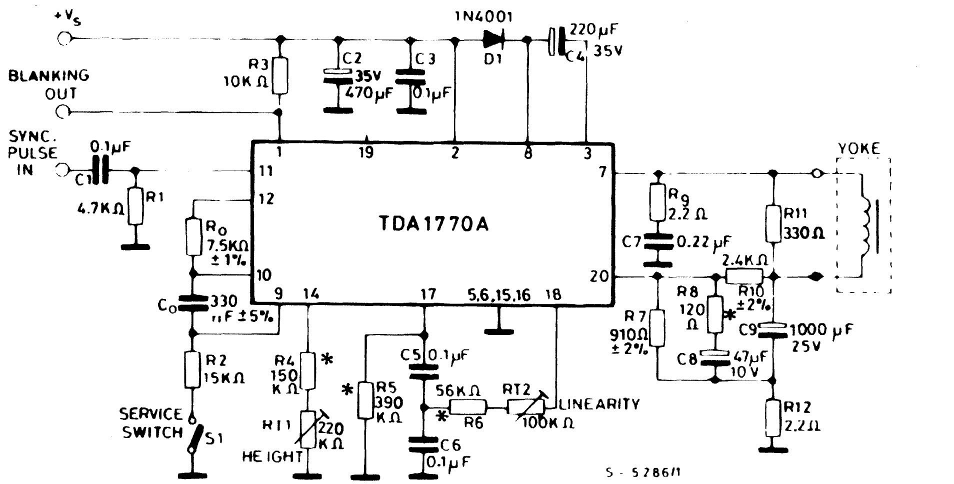
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 1 App		160		mA
I_{11}	Sync. Input Current		100			µA
V_7	Flyback Voltage	I_y = 1 App		42		V
V_9	Peak to Peak Oscillator Sawtooth Voltage	I_{11} = 0		3.6		V
		I_{11} = 100 µA		3.4		V
V_{18thL}	Starts Scan Level of the input Ramp			1.7		V
t_{fly}	Flyback Time	I_y = 1 App		0.75		msec
t_{blank}	Blanking Pulse Duration	f_o = 50 Hz T_j = 75 °C	1.33	1.4	1.47	ms
		f_o = 60 Hz T_j = 75 °C		1.17		ms
f_o	Free Running Frequency	R_o = 7.5 KΩ T_j = 75 °C C_o = 330 nF	42	43.5	46	Hz
		R_o = 6.2 KΩ T_j = 75 °C C_o = 330 nF		52.5		Hz
Δ_f	Synchronization Range	I_{11} = 100 µA T_j = 75 °C	14	16		Hz
T_j	Junction Temperature for Thermal Shut-down			145		°C

Figure 2 : AC Test Circuit.



SGS-THOMSON MICROELECTRONICS

Figure 3 : Typical Application Circuit for Smal Screen 90 ° TVC Set (Ry = 15 Ω, Ly = 30 mH, Iy = 0.82 App).



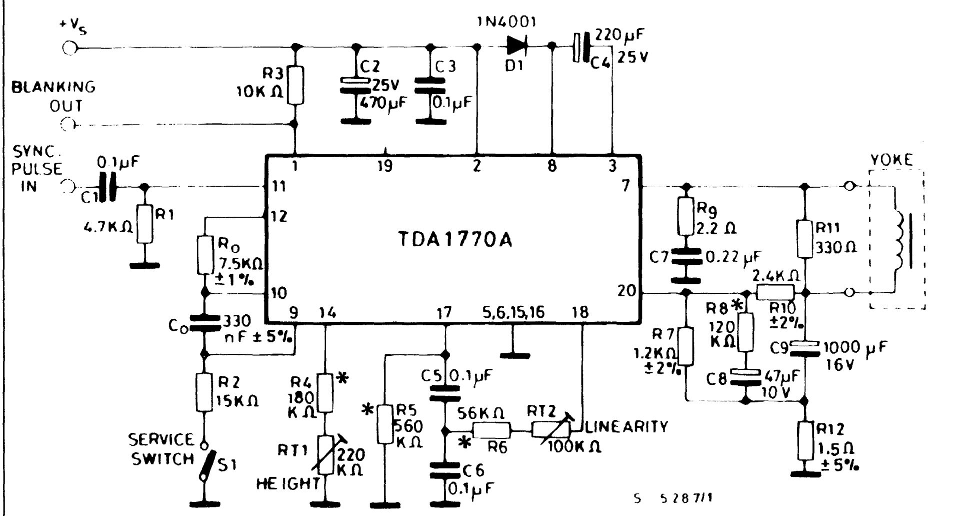
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_s	Minimum Supply Voltage	25	V
I_s	Supply Current	140	mA
t_{fly}	Flyback Time	0.7	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
*P_{tot}	Total Dissipation	2.4	W
*$R_{th\ heatsink}$**	Thermal Resistance of the Heatsink for T_{amb} = 60 °C and $T_{j\ max}$ = 130 °C	8	°C/W

* Worst case condition. ** See "Thermal considerations".

Figure 4 : Typical Application Circuit for B/W TV set (Ry = 10 Ω ; Ly = 20 mH ; Iy = 1 App).



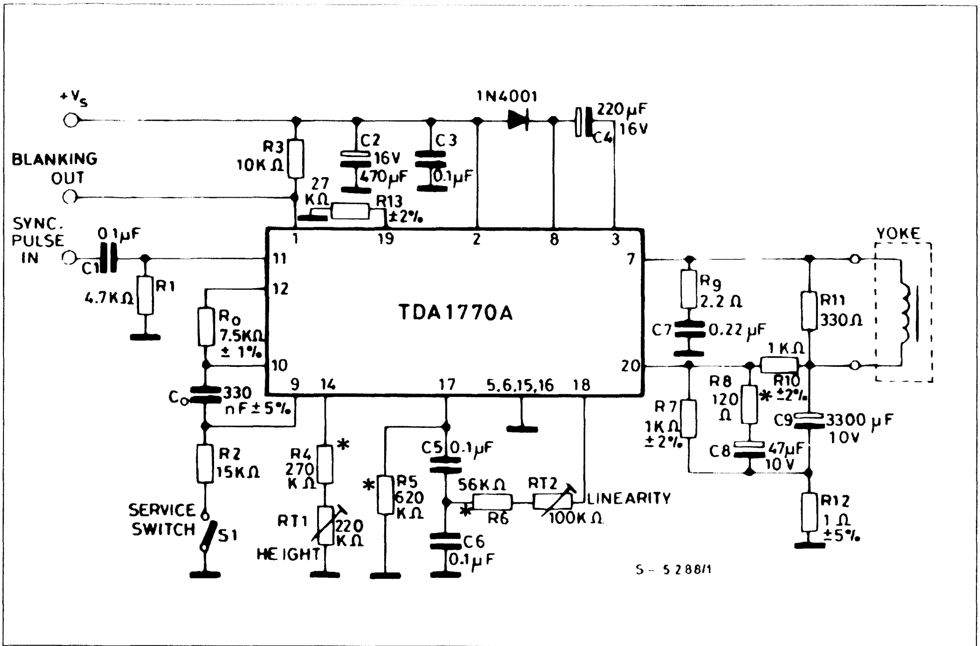
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_s	Minimum Supply Voltage	20	V
I_s	Supply Current	160	mA
t_{fly}	Flyback Time	0.75	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
*P_{tot}	Power Dissipation	2.1	W
*$R_{th\ heatsink}$**	Thermal Resistance of the Heatsink for T_{amb} = 60 °C and $T_{j\ max}$ = 130 °C	11	°C/W

* Worst case condition. ** See "Thermal considerations".

Figure 5 : Typical Application Circuit for Small Screen (Ry = 2.9 Ω ; Ly = 6 mH ; Iy = 1.1 App).



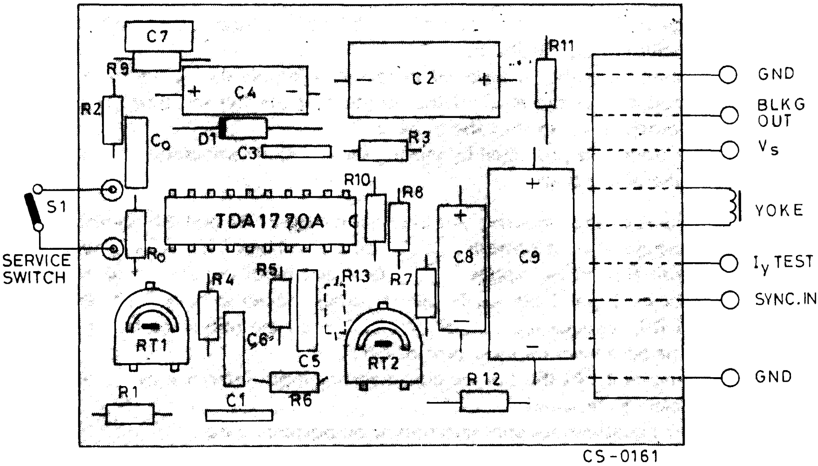
* The value depends on the characteristics of the CRT. The value shown is indicative only.

TYPICAL PERFORMANCE

Symbol	Parameter	Value	Unit
V_s	Minimum Supply Voltage	10.5	V
I_s	Supply Current	170	mA
t_{fly}	Flyback Time	0.45	msec
t_{blkg}	Blanking Time	1.4	msec
f_o	Free Running Frequency	43.5	Hz
*P_{tot}	Power Dissipation	1.25	W
*$R_{th\ heatsink}$**	Thermal Resistance of the Heatsink for T_{amb} = 60 °C and $T_{j\ max}$ = 130 °C	28	°C/W

* Worst case condition. ** See "Thermal considerations".

Figure 6 : P.C. Board and Components Layout for the ApplicationCircuits of fig. 3, 4 and 5 (1 : 1 scale).



APPLICATION INFORMATION (refer to the block diagram)

OSCILLATOR AND SYNC GATE (clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches Ro high or low so allowing the charge or the discharge of Co under constant current conditions.

The sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 10 is the inverting input of the amplifier used as integrator.

Pin 12 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

Pin 9 is the output of the amplifier.

Pin 11 is the input for sync pulses (positive).

RAMP GENERATOR AND BUFFER STAGE

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor, a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

Pin 14 The resistance between pin 14 and ground defines the current mirror current and than the height of the scanning.

Pin 17 is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.

Pin 18 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

POWER AMPLIFIER

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 20 is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 20 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

Pin 19 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.

This pin is used on a quasi-bridge configuration or on portable TVS.

Pin 7 is the output of the power amplifier and it drives the yoke by a negative slope current ramp Iy. Re and the Boucherot cell are used to stabilize the power amplifier.

Pin 8 the supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_S by a diode, while during the retrace time this pin is supplied from the flyback generator.

FLYBACK GENERATOR

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 2, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 8).

When the current across the yoke changes its direction, the output of the flyback generation falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed : the trace period restarts. The output of the power amplifier (pin 7) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 3 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 8 (see pin 8).

BLANKING GENERATOR AND CRT PROTECTION

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 1 is an open collector output where the blanking pulse is available.

VOLTAGE REGULATOR

The main supply voltage V_S is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 2 is the main supply voltage input V_S (positive).

Pin 5, 6, 15, 16 are the GND pins or the negative input of V_S.

THERMAL CONSIDERATIONS (a note referred to fig. 3, 4 and 5)

The shown value of case to ambient thermal resistance is the equivalent to three thermal resistances that are :

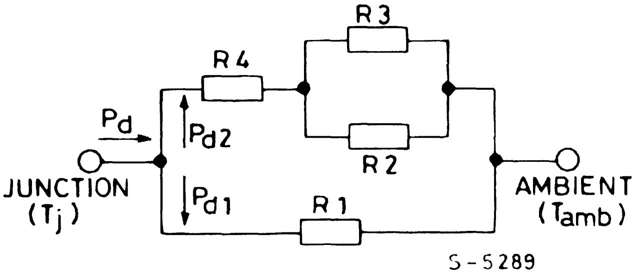
R1 – Thermal resistance junction to ambient of the device.

R2 – Thermal resistance of the p.c. copper side.

R3 – Thermal resistance of the auxiliary heatsink.

The circuit that contains these thermal resistances is shown on fig. 7 where R3 is the thermal resistance junction to pins of the device and Pd is the maximum dissipated power.

Figure 7 : Semiconductor Heatsink Thermal Circuit.



Since the thermal resistance R3 of the heatsink is defined from its physical and mechanical characteristics, it is necessary to define the required copper side on the p.c. board for the necessary R2 value. For instance, let's consider the application for the 90 ° yoke.
It is known :
$T_{j\,max} = 130\,°C$; $T_{amb\,max} = 60\,°C$; $R_{th\,c\text{-}amb} = 8\,°C/W$; $R_{th\,j\text{-}pins}$ (or R4) = 14 °C/W ; $R_{th\,j\text{-}amb} = 80\,°C/W$.

It can be calculated :

$$Pd = \frac{T_{j\,max} - T_{amb\,max}}{R_{th\,c\text{-}amb} + R_{th\,j\text{-}pins}} = \frac{130 - 60}{8 + 14} = 3.18\ W$$

Using an auxiliary heatsink of a thermal resistance R3 = 20 °C/W (including some losses), it can be easily calculated (see fig. 7) : R2 = 94 °C/W.

From fig. 9, it can be found : l ≥ 21 mm.

MOUNTING INSTRUCTIONS

The $R_{th\,j\text{-}amb}$ of the TDA 1770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 8) or to an external heatsink.

The diagram of figure 9 shows the R_{th} as a function of the side "l" of two equal square copper areas having a thickness of 35 µ (1.4 mils).
During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 8 : Example of P.C. Board Copper Area which is Used as Heatsink.

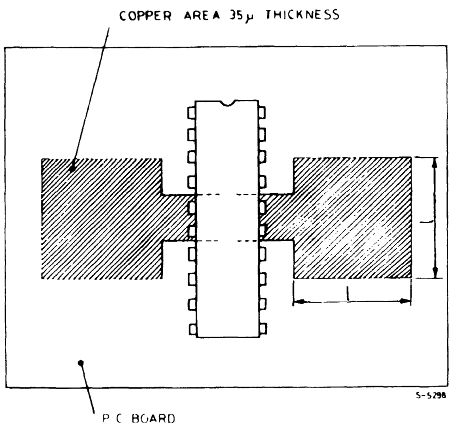


Figure 9 : Thermal Resistance of the P.C. Copper Side vs. Side "l".

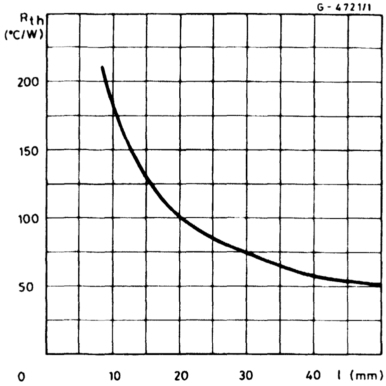
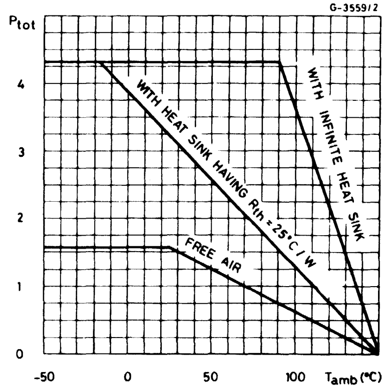
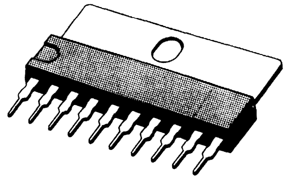


Figure 10 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



VERTICAL DEFLECTION CIRCUIT

- RAMP GENERATOR
- INDEPENDENT AMPLITUDE ADJUSTEMENT
- BUFFER STAGE
- POWER AMPLIFIER
- FLYBACK GENERATOR
- INTERNAL REFERENCE VOLTAGE
- THERMAL PROTECTION



SIL10

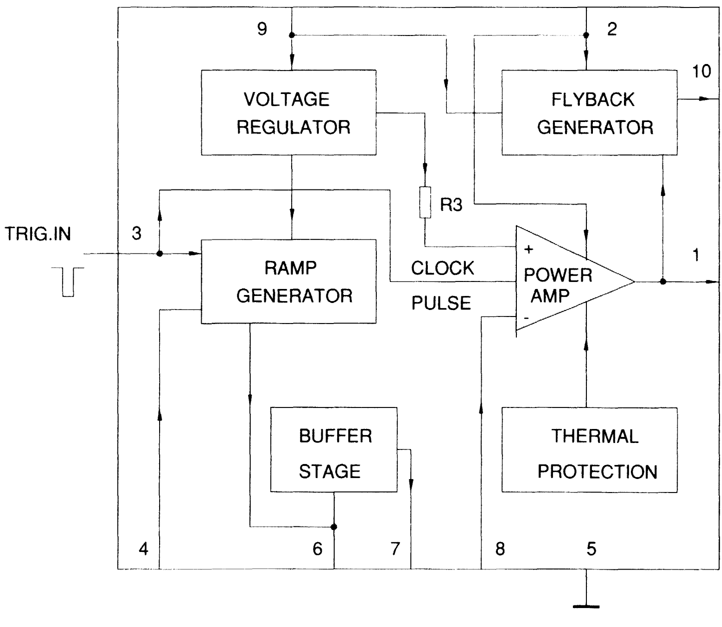
ORDER CODE : TDA1771

DESCRIPTION

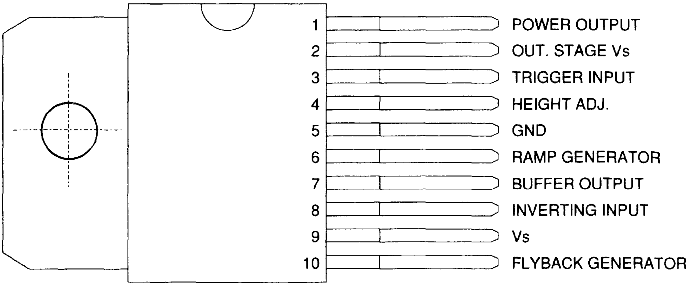
The TDA1771 is a monolithic integrated circuit in SIL-10 package.

It is a full performance and very efficient vertical deflection circuit intended for direct drive of a TV picture tube in Color and B & W television as well as in Monitor and Data displays.

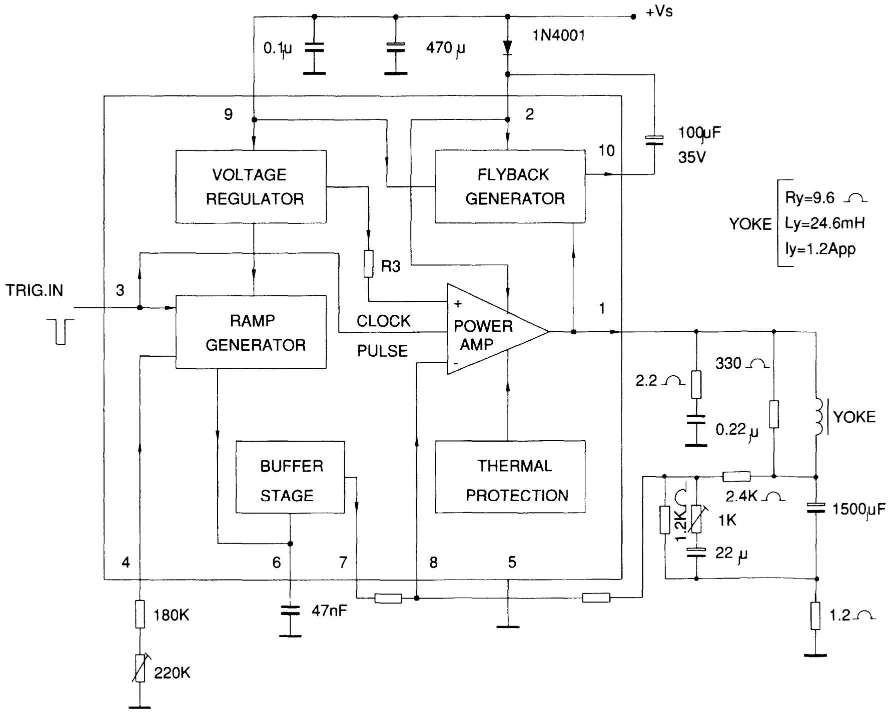
BLOCK DIAGRAM



PIN CONNECTIONS



APPLICATION CIRCUIT



DC ELECTRICAL CHARACTERISTICS (V_S = 35V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I_1 = 0 I_{10} = 0		16	36	mA
I_9	Pin 9 Quiescent Current	I_1 = 0 I_{10} = 0		15	30	mA
$-I_6$	Ramp Generator Bias Current	V_6 = 0			0.5	µA
$-I_6$	Ramp Generator Current	V_6 = 0 $-I_4$ = 20µA	18.5	20	21.5	µA
dI_6/I_6	Ramp Gener. Linearity	V_6 = 0 to 15V $-I_4$ = 20µA		0.2	1	%
V_1	Quiescent Output Voltage	R_a = 30k R_b = 10k V_S = 35V	17.0	17.8	18.6	V
		R_a = 6.8k R_b = 10k V_S = 15V	7.2	7.5	7.8	V
V_{1L}	Out Saturation Voltage to GND	I_1 = 0.5A		0.5	1	V
		I_1 = 1.2A		1	1.4	V
V_{1H}	Out Saturation Voltage to V_S	$-I_1$ = 0.5A		1.1	1.6	V
		$-I_1$ = 1.2A		1.6	2.2	V
V_4	Reference Voltage	$-I_4$ = 20µA	6.3	6.6	6.9	V
dV_4/V_S	Reference Voltage Drift Versus V_S	V_S = 10V to 35V		1	2	mV/V
dV_4/d_{I4}	Reference Voltage Drift Versus I_4	I_4 = 10µA to 30µA		1.5	2	mV/µA
V_r	Internal Ref. Voltage		4.26	4.40	4.54	V
Gv	Ouput Stage Open Loop Gain	f = 100Hz		60		dB
V_{fs}	V_{9-10} Saturation Voltage	$-I_{10}$ = 1.2A		1.5	2.5	V
V_{10}	Pin 10 Scanning Voltage	I_{10} = 20mA		1.7	3	V
V_3	Trigger Input Threshold	(see note 1)	2.6	3.0	3.4	V
I_3	Trigger Input Bias Current	V_{IN} = V_3 − 0.2V			30	µA
t_3	Trigger Input Width	(see note 2)	20	60	th	µS

AC ELECTRICAL CHARACTERISTICS (V_S = 24V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		30	V
I_1	Peak-to-peak Operating Current Range		0.4		2.5	A
I_S	Supply Current	I_Y = 2.4A_{pp}		315		mA
V_1	Flyback Voltage	I_Y = 2.4A_{pp}		51		V
V_7	Sawtooh Pedestall Voltage			1.85		V
T_{JS}	Junction Temp. for Thermal Shutdown			145		°C

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
V_1 , V_2	Flyback Peak Voltage	65	V
V_3	Trigger Input Voltage	20	V
V_8	Amplifier Input Voltage	GND to V_S	V
I_0	Output Peak to Peak Current (non repetitive t = 2ms)	6	A
I_0	Output Peak to Peak Current t > 10μs	4	A
I_{10}	Pin 10 DC Current at $V_1 < V_9$	100	mA
I_{10}	Pin 10 Peak to Peak Current @ t_{fly} < 1.5ms	3	A
P_{tot}	Total Power Dissipation @ T_{tab} = 60°C	9	W
T_S, T_J	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{TH(j\text{-}tab)}$	Thermal Resistance Junc.-tab	Max.	10	°C/W
$R_{TH(j\text{-}amb)}$	Thermal Resistance Junc.-amb	Max.	70	°C/W

APPLICATION NOTES

Notes : 1. The trigger input circuit can accept, with a metal option, positive and negative going input pulses.

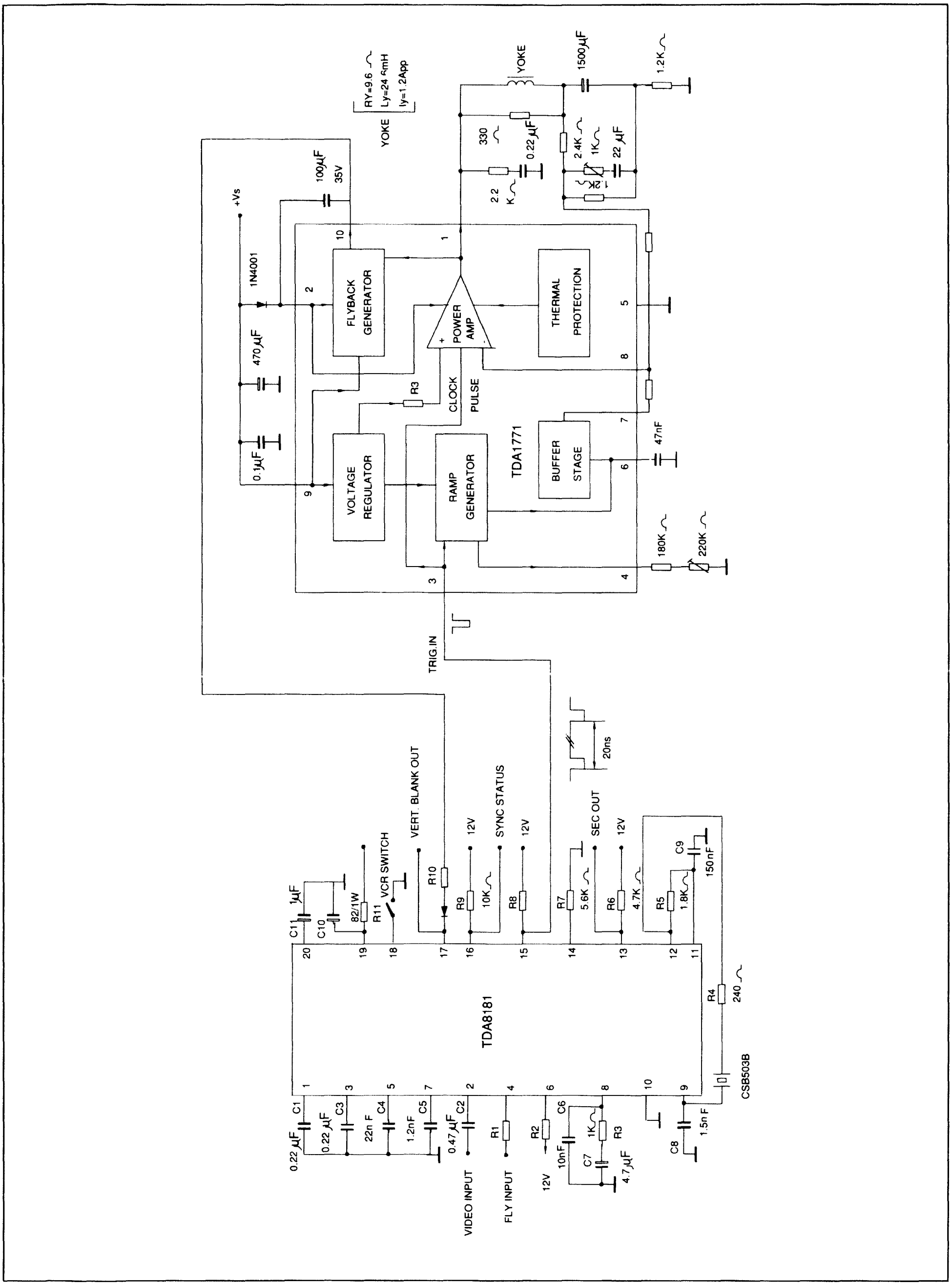
2.

$$th = \frac{1.2 * ts}{V_{PP}}$$

where : ts is the vertical period

V_{PP} is ramp amplitude at pin 6.

APPLICATION DIAGRAM

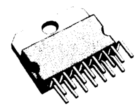


SGS-THOMSON
MICROELECTRONICS

TDA1872A

VERTICAL DEFLECTION CIRCUIT

- SYNCHRONIZATION CIRCUIT
- PRECISION OSCILLATOR AND RAMP GENERATOR
- 50/60Hz SYNCHRONIZATION IDENTIFICATION CIRCUIT WITH AUTOMATIC AMPLITUDE CORRECTION AND STATUS OUTPUT
- POWER OUTPUT AMPLIFIER WITH HIGH CURRENT CAPABILITY
- FLYBACK GENERATOR
- VOLTAGE REGULATOR
- PRECISION BLANKING PULSE GENERATOR
- THERMAL SHUT DOWN PROTECTION
- CRT PROTECTION CIRCUIT



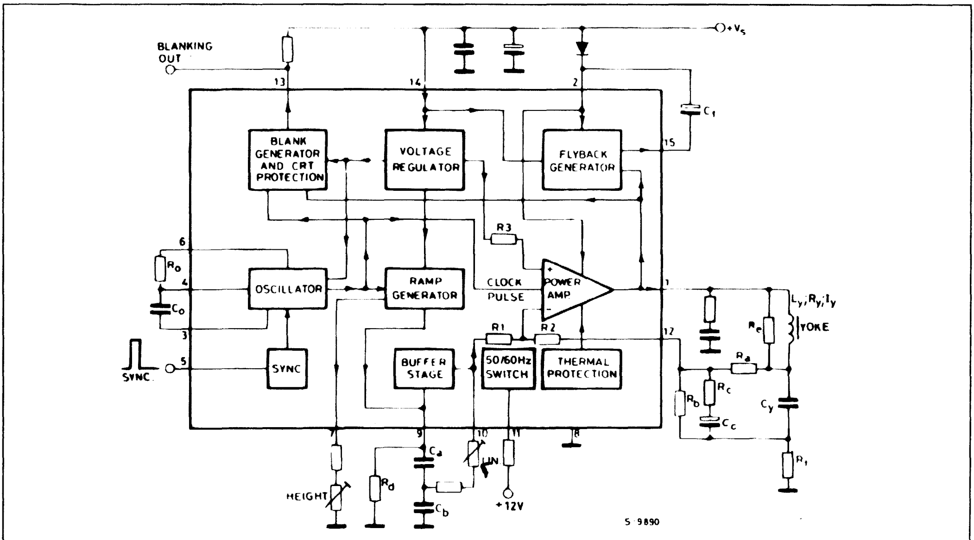
MULTIWATT
(15-lead)

ORDER CODE : TDA1872A

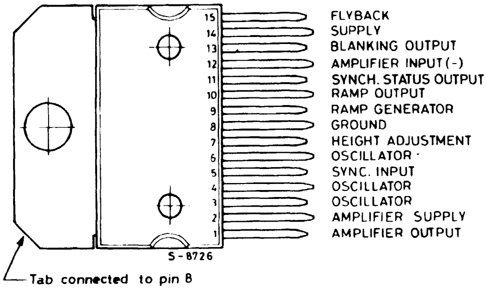
DESCRIPTION

The TDA1872A is a monolithic integrated circuit in 15 lead MULTIWATT package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110 degree color TV picture tubes.
It offers a wide range of applications also in portable CTVs, BW TVs, monitors and displays.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage at Pin 14	35	V
V_1, V_2	Flyback Peak Voltage	60	V
V_5	Synchronous Input Voltage	20	V
V_{12}	Power Amplifier Input Voltage	- 10 To V_s	V
V_{13}	Voltage at pin 13	V_s	
I_o	Output Current (non repetitive at t = 20ms)	3	A
I_o	Output Peak Current at f = 50Hz t > 10µs	2	A
I_o	Output Peak Current at f = 50Hz $t_{fly} \leq 1.5$ms	3.5	A
I_{15}	Pin 15 Peak to Peak Flyback Current at f = 50Hz $t_{fly} < 1.5$ms	3	A
I_{15}	Pin 15 DC Current at $V_1 < V_{14}$	100	mA
P_{tot}	Maximum Power Dissipation at $T_{case} \leq 60$°C	30	W
T_{stg}	Storage Temperature	- 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Junction-ambient	Max	40	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 35V, T_{amb} = 25°C, unless otherwise specified)

DC CHARACTERISTICS

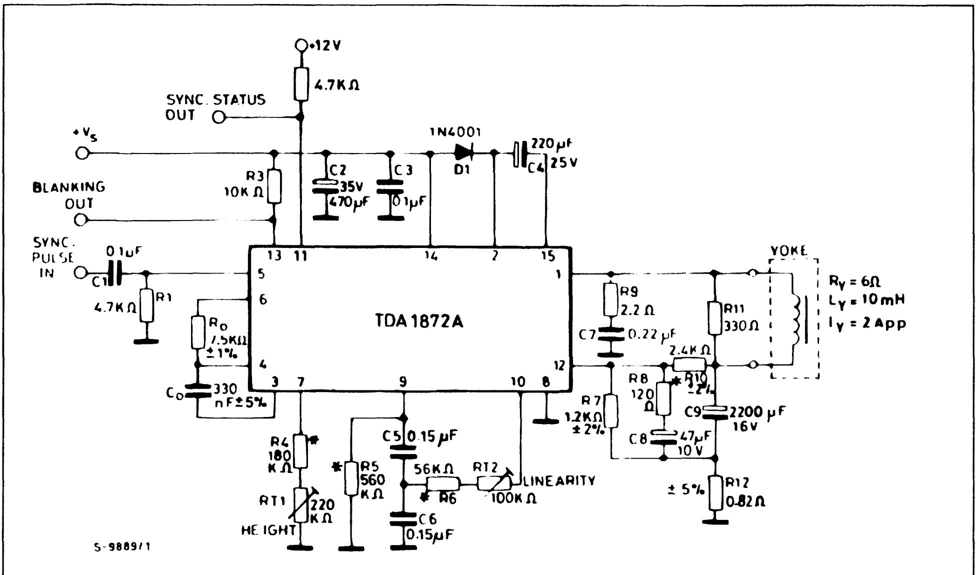
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_1 = 0$		20	40	mA	2b
$-I_9$	Ramp Generator Bias Current	$V_9 = 0$ $-I_7 = 0\mu A$		0.02	1	µA	2b
$-I_9$	Ramp Generator Current	V_9 = 0 to 15V $-I_7 = 20\mu A$	18.5	20	21.5	µA	2b
ΔI_9	Current Variation From 50 to 60Hz	$-I_7 = 20\mu A$	17.7	20	21.1	%	2b
$\left\lvert\frac{\Delta I_9}{I_9}\right\rvert$	Ramp Generator non Linearity	V_9 = 0 to 15V $-I_7 = 20\mu A$		0.2	1	%	2b
I_{14}	Pin 14 Quiescent Current			25	45	mA	2b
V_1	Quiescent Output Voltage	V_s = 35V R_a = 2.2KΩ R_b = 1KΩ	16.4	17.8	19.5	V	2a
		V_s = 15V R_a = 390Ω R_b = 1KΩ	6.9	7.5	8.1	V	
V_{1L}	Output Saturation Voltage to Ground	I_1 = 1.2A		1	1.4	V	2c
V_{1H}	Output Saturation Voltage to Supply	$-I_1$ = 1.2A		1.6	2.2	V	2d
V_4	Oscillator Virtual Ground			0.45		V	2b
V_7	Regulated Voltage at Pin 7	$-I_7 = 20\mu A$	6.3	6.6	6.9	V	2b
$\frac{\Delta V_7}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	ΔV_s = 15 to 35V		1	2	$\frac{mV}{V}$	2b
V_{13}	Blanking Output Saturation Voltage	I_{13} = 10mA		0.35	0.5	V	2a
V_{15}	Pin 15 Saturation Voltage to Ground	I_{15} = 20mA		1.2	1.8	V	2a

ELECTRICAL CHARACTERISTICS (Refer to the AC test circuits of fig.1, T_{amb} = 25°C, V_s = 24V, f = 50Hz, unless otherwise specified)

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 2A_{pp}		295		mA
I_5	Sync. Input Current Required to Sync.		100			μA
- I_7	Current at Pin 7	I_y = 2A_{pp}	36.3	38	39.7	μA
V_1	Flyback Voltage	I_y = 2A_{pp}		50		V
V_3	Peak to Peak Oscillator Sawtooth Voltage	I_5 = 0		3.6		V
		I_5 = 100μA		3.4		
V_{10thL}	Start Scan Level of the Input Ramp			1.85		V
t_{fly}	Flyback Time	I_y = 2A_{pp}		0.6		ms
t_{blank}	Blanking Pulse Duration	f_o = 50Hz T_j = 75°C	1.25	1.4	1.47	ms
		f_o = 60Hz T_j = 75°C		1.17		
f_o	Free Running Frequency	R_o = 7.5KΩ C_o = 330nF T_j = 75°C	41.5	44	46	Hz
		R_o = 6.2KΩ C_o = 330nF T_j = 75°C		52.5		Hz
Δf	Synchronization Range	I_5 = 100μA T_j = 75°C	19	20		Hz
V_{11}	Sync. Status Output	f = 50Hz or Unsynchronized			1.5	V
		f = 60Hz	10.5			
T_j	Junction Temperature for Thermal Shut-down			145		°C

Figure 1 : AC Test Circuit.



* The value depends on the characteristics of the CRT. The value shown is indicative only.

Figure 2 : DC Test Circuits.

Figure 2a.

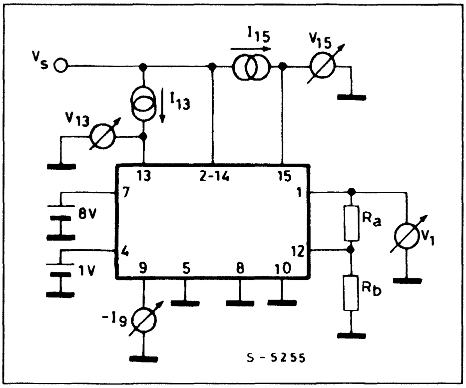


Figure 2b.

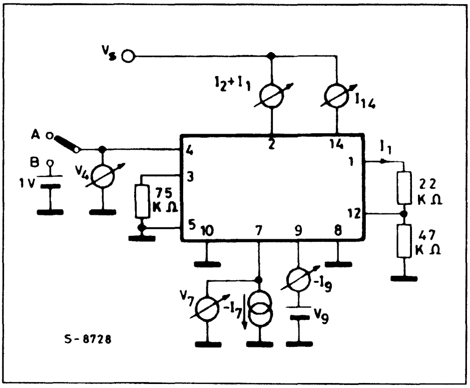


Figure 2 : DC Test Circuits (continued).

Figure 2c.

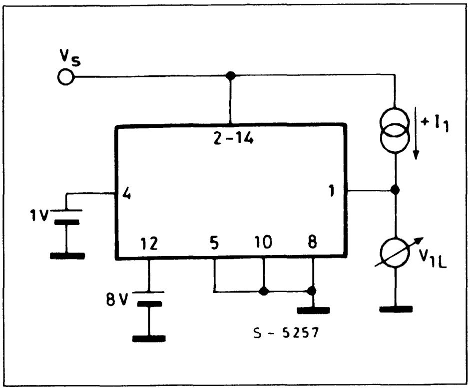


Figure 2d.

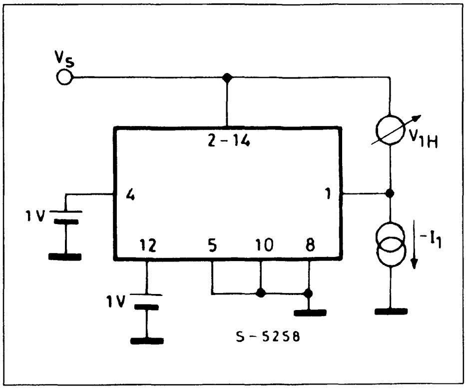
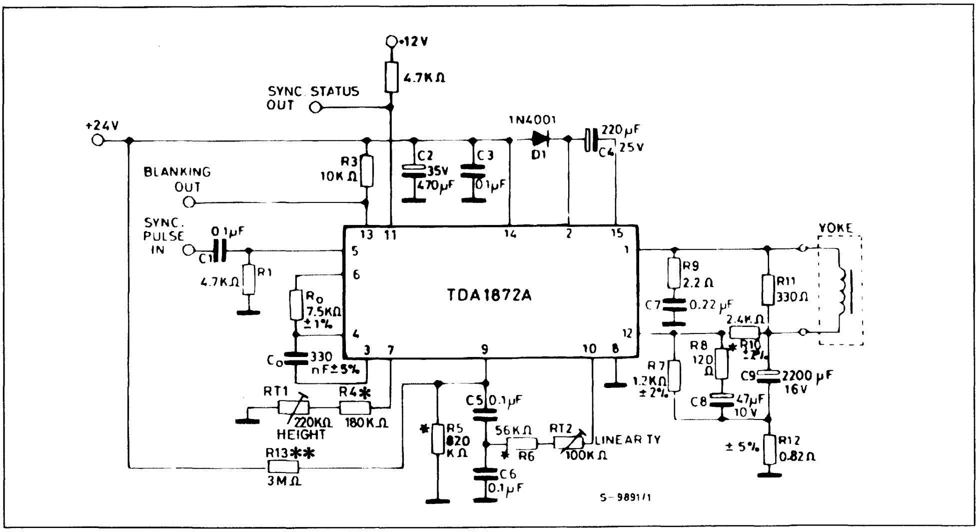
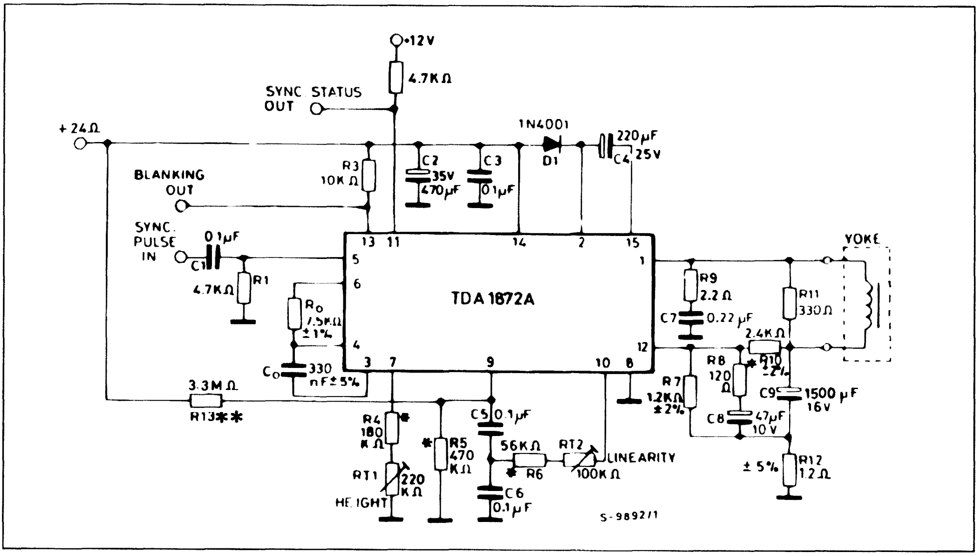


Figure 3 : Application Circuit Using Internal Ramp Generator (50 ÷ 60Hz ramp compensation) for 110° TVC set (R_T = 5.9Ω ; L_y = 10mH ; Iy = 1.95A_{pp}).



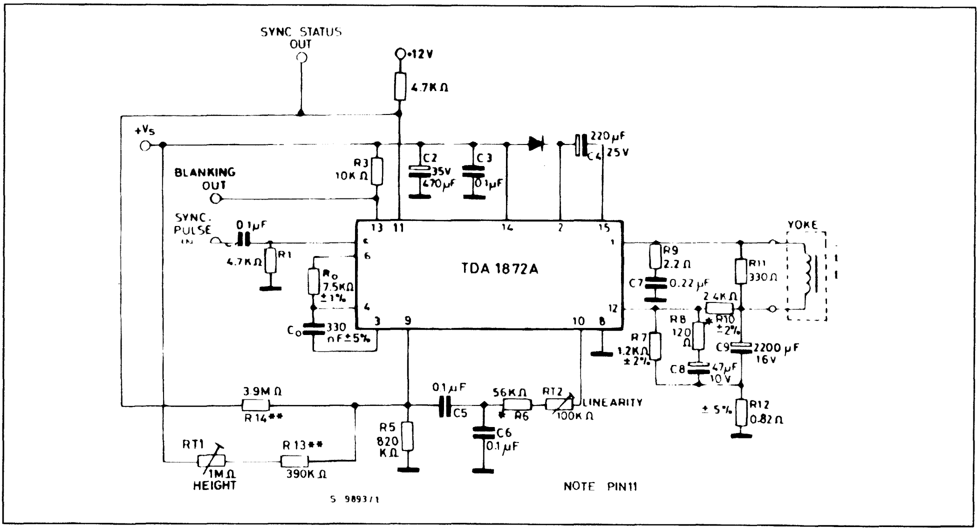
Note : Pin 11 must not be left floating.
* The value depends on the characteristics of the CRT. The value shown is indicative only.
** The value depends on the characteristics of the CRT and on the supply voltage.

Figure 4 : Applicaiton circuit (50 ÷ 60Hz ramp Compasation) for 110° RVC set (R_T = 9.6Ω ; L_y = 24.6mH ; I_y = 1.2A_{PP}).



Note : Pin 11 must not be left floating.
* The value depends on the characteristics of the CRT. The value shown is indicative only.
** The value depends on the characteristics of the CRT and on the supply voltage.

Figure 5 : Application Circuit Using External Ramp Generator (50 ÷ 60Hz ramp and pumping compensation).



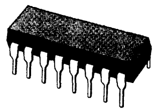
Note : Pin 11 must not be left floating.
* The value depends on the characteristics of the CRT. The value shown is indicative only.
** The value depends on the characteristics of the CRT and on the supply voltage.

SGS-THOMSON
MICROELECTRONICS

TDA1904

4 W AUDIO AMPLIFIER

- HIGH OUTPUT CURRENT CAPABILITY (up to 2 A)
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- SUPPLY VOLTAGE RANGE : 4 V TO 20 V



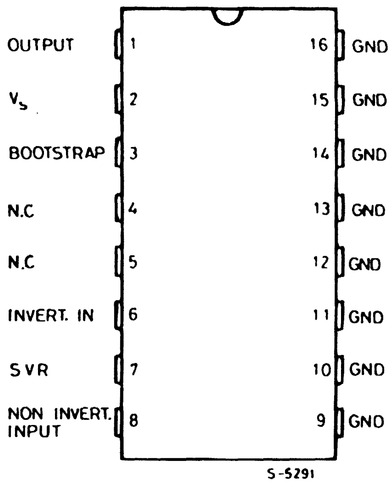
Powerdip
(8 + 8)

ORDER CODE : TDA1904

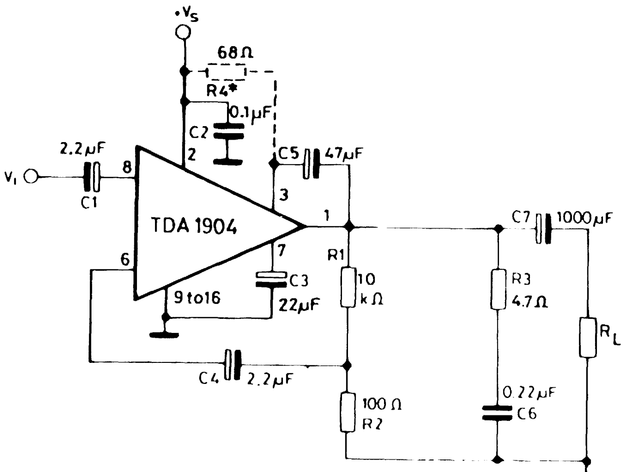
DESCRIPTION

The TDA1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in wide range of applications in portable radio and TV sets.

PIN CONNECTION (top view)



TEST AND APPLICATION CIRCUIT



(*) R4 is necessary only for $V_S < 6V$.

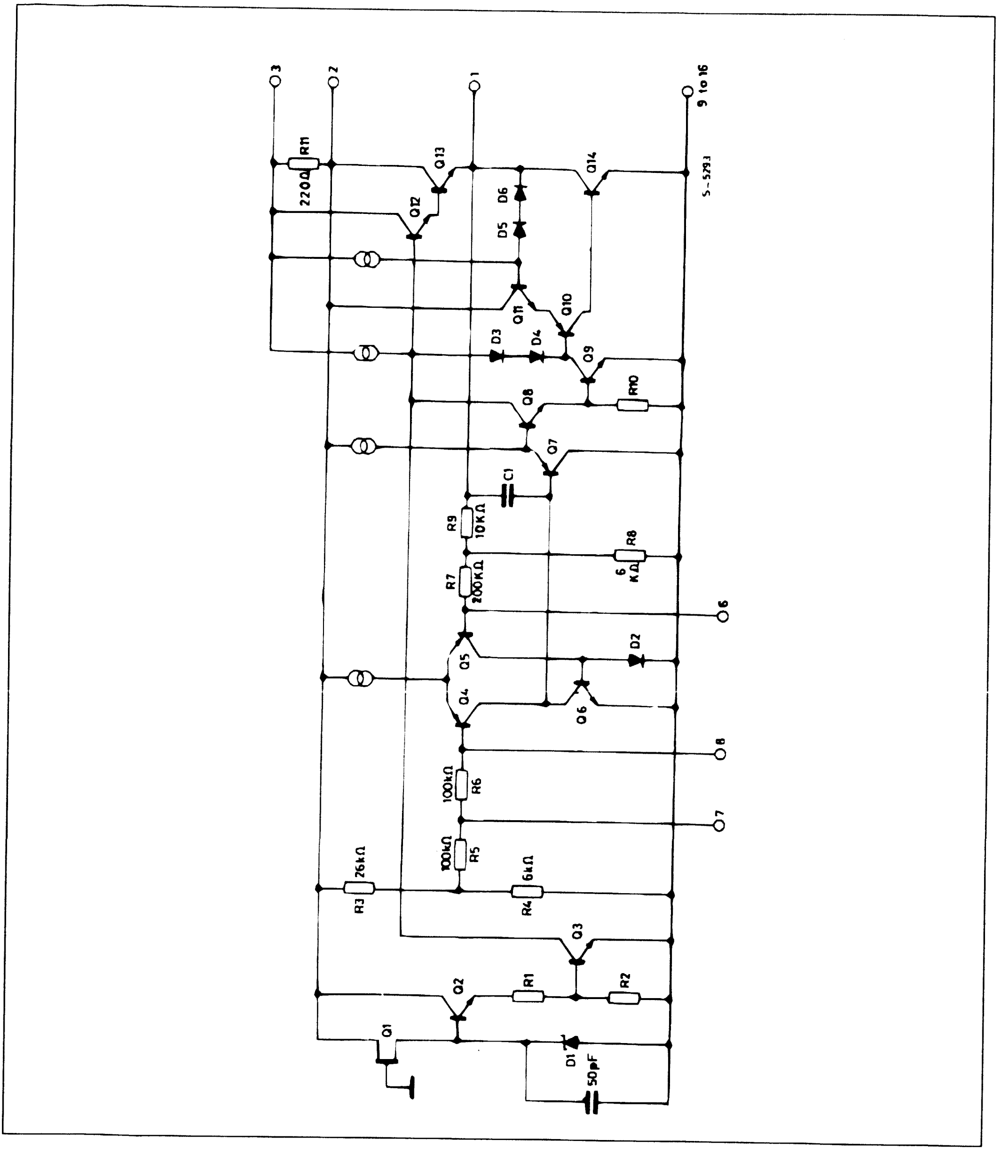
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	20	V
I_O	Peak Output Current (non repetitive)	2.5	A
I_O	Peak Output Current (repetitive)	2	A
P_{tot}	Total Power Dissipation at T_{amb} = 80 °C T_{pins} = 60 °C	1 6	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max.	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70	°C/W

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, R_{th} (heatsink) = 20 °C/W, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		4		20	V
V_o	Quiescent Output Voltage	V_s = 4 V V_s = 14 V		2.1 7.2		V
I_d	Quiescent Drain Current	V_s = 9 V V_s = 14 V		8 10	15 18	mA
P_o	Output Power	d = 10 % f = 1 KHz V_s = 9 V R_L = 4 Ω V_s = 14 V V_s = 12 V V_s = 6 V	 1.8 4 3.1 0.7	 2 4.5		W
d	Harmonic Distortion	f = 1 KHz R_L = 4 Ω V_s = 9 V Po = 50 mW to 1.2 W		0.1	0.3	%
V_i	Input Saturation Voltage (rms)	V_s = 9 V V_s = 14 V	0.8 1.3			V
R_i	Input Resistance (pin 8)	f = 1 KHz	55	150		kΩ
η	Efficiency	f = 1 KHz V_s = 9 V R_L = 4 Ω P_o = 2 W V_s = 14 V R_L = 4 Ω P_o = 4.5 W		 70 65		%
BW	Small Signal Bandwidth (– 3 dB)	V_s = 14 V R_L = 4 Ω		40 to 40,000		Hz
G_v	Voltage Gain (open loop)	V_s = 14 V f = 1 KHz		75		dB
G_v	Voltage Gain (closed loop)	V_s = 14 V R_l = 4 Ω f = 1 KHz P_o = 1 W	39.5	40	40.5	dB
e_N	Total Input Noise	R_g = 50 Ω (°) R_g = 10 kΩ		1.2 2	 4	µV
		R_g = 50 Ω (°°) R_g = 10 kΩ		2 3		µV
SVR	Supply Voltage Rejection	V_s = 12 V f_{ripple} = 100 Hz R_g = 10 kΩ V_{ripple} = 0.5 V_{rms}	40	50		dB
T_{sd}	Thermal Shut-down Case Temperature	P_{tot} = 2 W		120		°C

Note : (°) Weighting filter = curve A.
(°°) Filter with noise bendwidth : 22 Hz to 22 KHz.

Figure 1 : Test and Application Circuit.

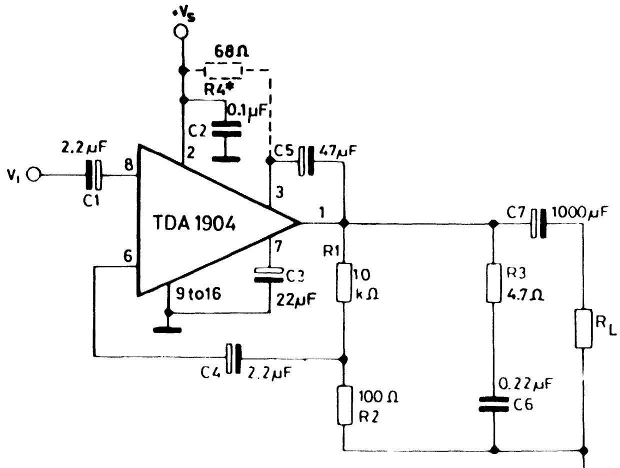
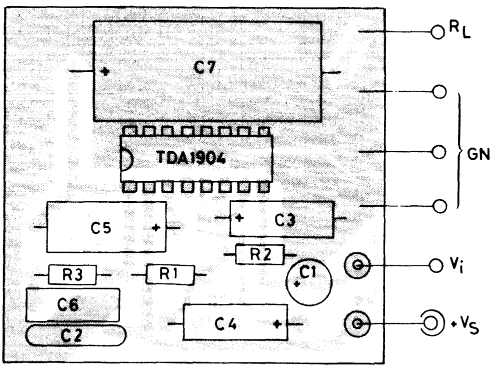


Figure 2 : P.C. Board and Components Layout of Figure 1 (1 : 1 scale).



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 1.

When the supply voltage V_S is less than 6 V, a 68 Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.

Different values can be used. The following table can help the designer.

Components	Reccom. Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value	Allowed Range	
					Min.	Max.
R_1	10 kΩ	Feedback Resistors	Increase of Gain.	Decrease of Gain. Increase Quiescent Current.	9 R_3	
R_2	100 Ω		Decrease of Gain.	Increase of Gain.		1 kΩ
R_3	4.7 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads.			
R_4	68 Ω	Increase of the Output Swing with Low Supply Voltage.			39 Ω	220 Ω
C_1	2.2 µF	Input DC Decoupling.	Higher Cost Lower Noise.	Higher Low Frequency Cutoff. Higher Noise.		
C_2	0.1 µF	Supply Voltage Bypass.		Danger of Oscillations.		
C_3	22 µF	Ripple Rejection	Increase of SVR Increase of the Switch-on Time.	Degradation of SVR.	2.2 µF	100 µF
C_4	2.2 µF	Inverting Input DC Decoupling.	Increase of the Switch-on Noise	Higher Low Frequency Cutoff.	0.1 µF	
C_5	47 µF	Bootstrap.		Increase of the Distortion at Low Frequency.	10 µF	100 µF
C_6	0.22 µF	Frequency Stability.		Danger of Oscillation.		
C_7	1000 µF	Output DC Decoupling.		Higher Low Frequency Cutoff.		

Figure 3 : Quiescent Output Voltage vs. Supply Voltage.

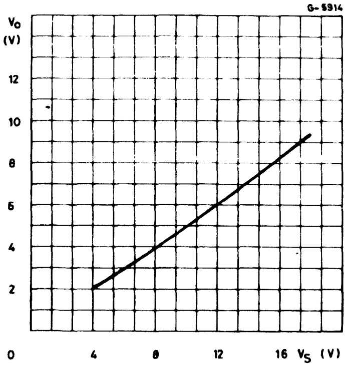


Figure 4 : Quiescent Drain Current vs. Supply Voltage.

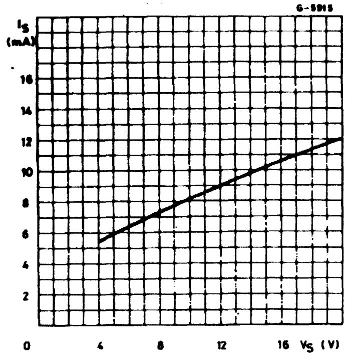


Figure 5 : Output Power vs. Supply Voltage.

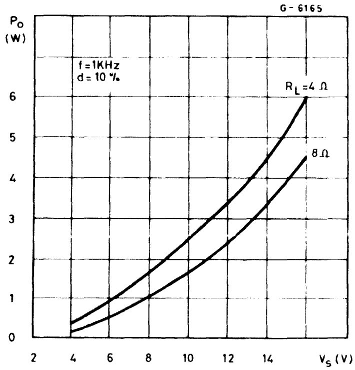


Figure 6 : Distortion vs. Output Power.

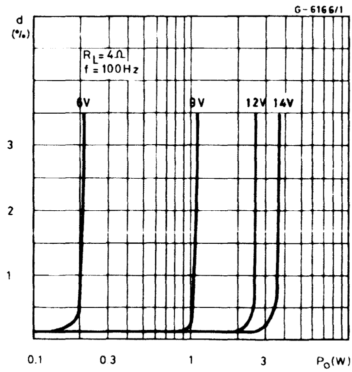


Figure 7 : Distortion Output Power.

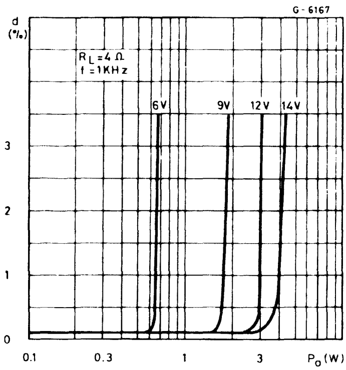


Figure 8 : Distortion vs. Output Power.

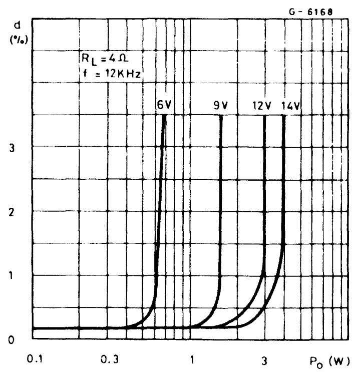


Figure 9 : Distortion vs. Output Power.

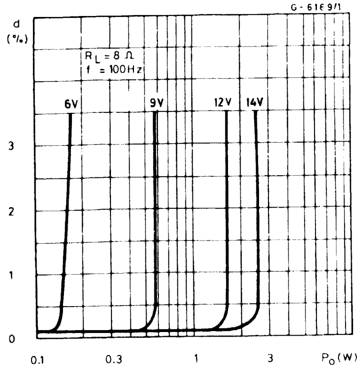


Figure 10 : Distortion vs. Output Power.

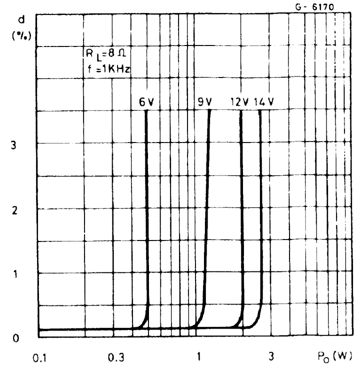


Figure 11 : Distortion vs. Output Power.

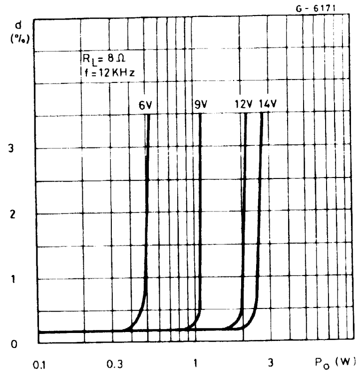


Figure 12 : Distortion vs. Frequency.

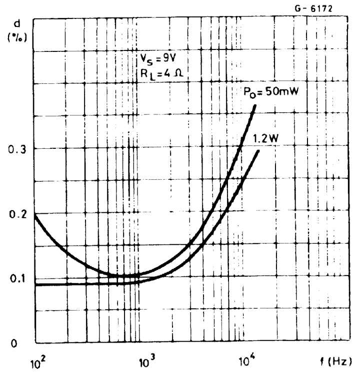


Figure 13 : Distortion vs. Frequency.

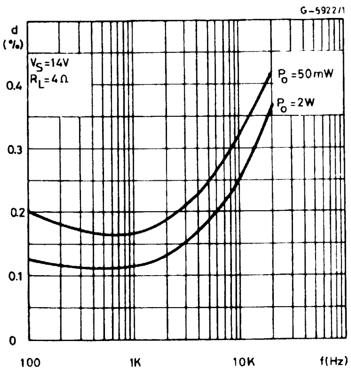


Figure 14 : Distortion vs. Frequency.

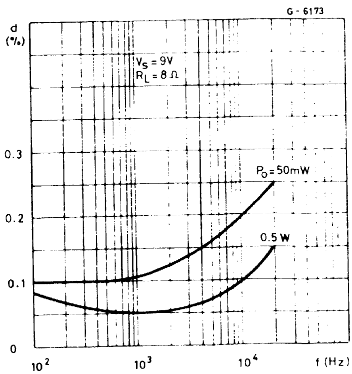


Figure 15 : Distortion vs. Frequency.

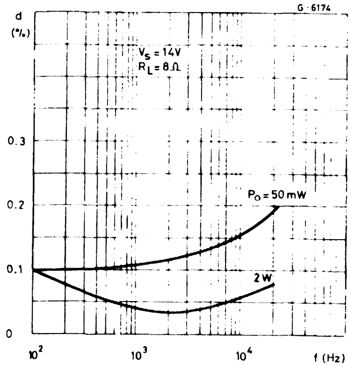


Figure 16 : Supply Voltage Rejection vs. Frequency.

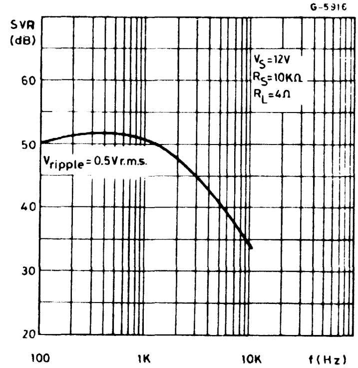


Figure 17 : Total Power Dissipation and Efficiency vs. Output Power.

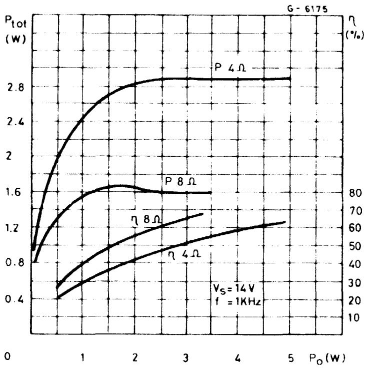


Figure 18 : Total Power Dissipation vs. Output Power.

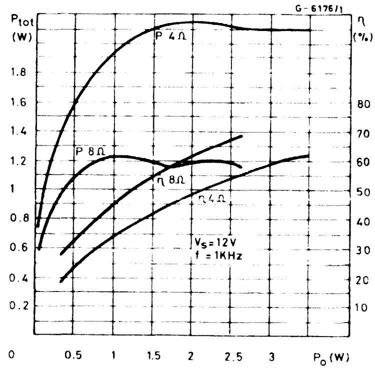


Figure 19 : Total Power Dissipation vs. Output Power.

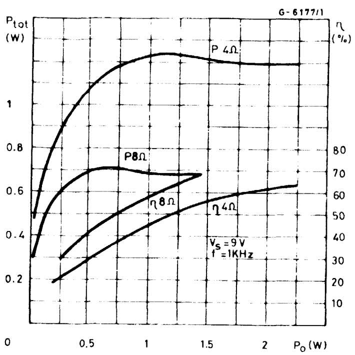
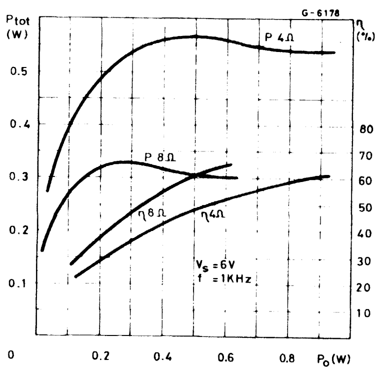


Figure 20 : Total Power Dissipation vs. Output Power.



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150 °C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increase up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

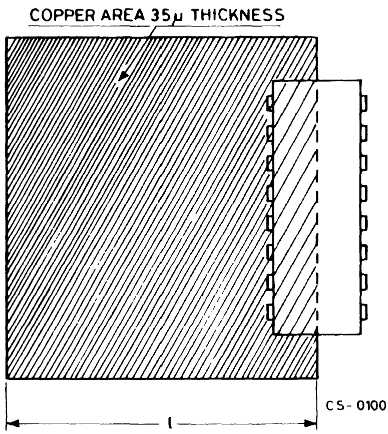
MOUNTING INSTRUCTION

The TDA1904 is assembled in the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 21 shows a PC board copper area used as a heatsink (l = 65 mm).

The thermal resistance junction-ambient is 35 °C.

Figure 21 : Example of Heatsink Using PC Board Copper (l = 65 mm).

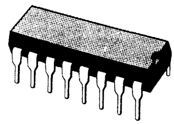


SGS-THOMSON MICROELECTRONICS

TDA1905

5 W AUDIO AMPLIFIER WITH MUTING

- MUTING FACILITY
- PROTECTION AGAINST CHIP OVER TEMPERATURE
- VERY LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- LOW "SWITCH-ON" NOISE
- VOLTAGE RANGE 4 V TO 30 V



Powerdip
(8 + 8)

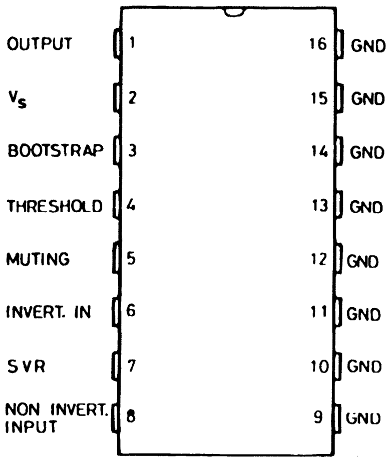
ORDER CODE : TDA1905

DESCRIPTION

The TDA1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.

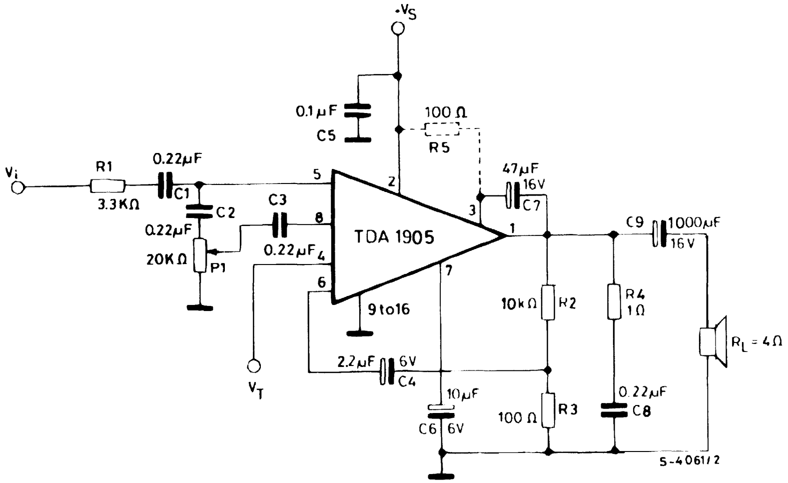
The TDA1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6 W and a thermal resistance of 15 °C/W (junction to pins).

PIN CONNECTION (top view)

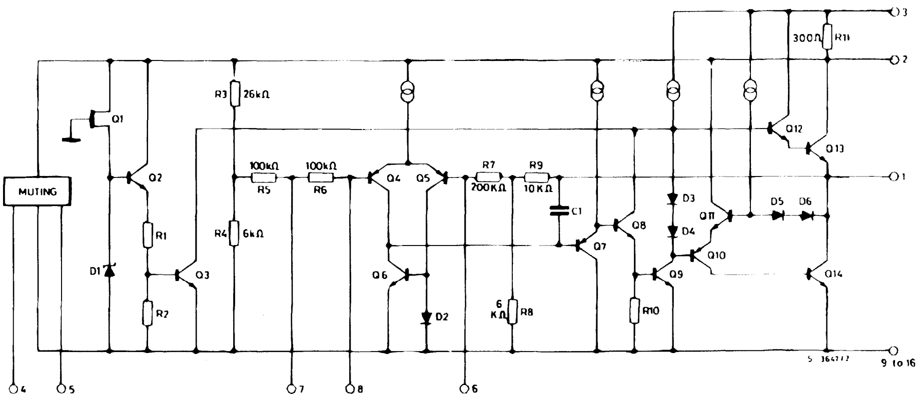


S-2913

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

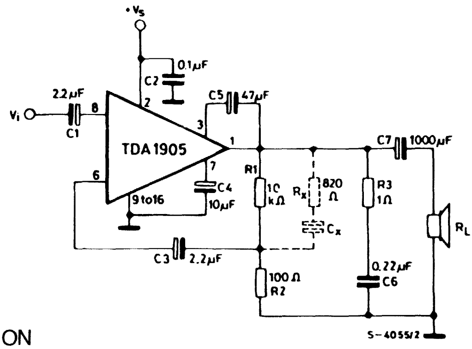
Symbol	Parameter	Value	Unit
V_s	Supply Voltage	30	V
I_o	Output Peak Current (non repetitive)	3	A
I_o	Output Peak Current (repetitive)	2.5	A
V_i	Input Voltage	0 to + V_s	V
V_i	Differential Input Voltage	± 7	V
V_{11}	Muting Threshold Voltage	V_s	V
P_{tot}	Power Dissipation at T_{amb} = 80 °C T_{case} = 60 °C	1 6	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

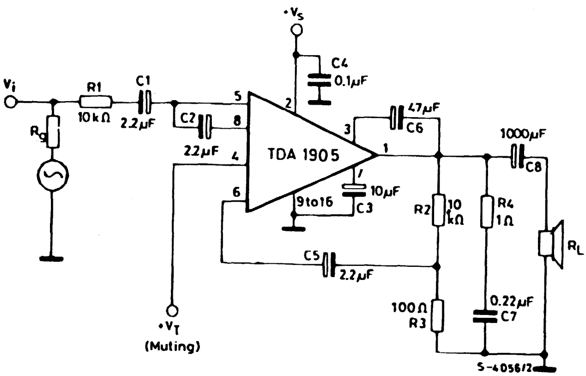
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max.	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-amb	Max.	70	°C/W

TEST CIRCUITS

WITHOUT MUTING



WITH MUTING FUNCTION



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, R_{th} (heatsink) = 20 °C/W, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		4		30	V
V_o	Quiescent Output Voltage	V_s = 4 V V_s = 14 V V_s = 30 V	1.6 6.7 14.4	2.1 7.2 15.5	2.5 7.8 16.8	V
I_d	Quiescent Drain Current	V_s = 4 V V_s = 14 V V_s = 30 V		15 17 21	 35	mA
$V_{CE\ sat}$	Output Stage Saturation Voltage	I_C = 1 A I_C = 2 A		0.5 1		V
P_o	Output Power	d = 10 % f = 1 KHz V_s = 9 V R_L = 4 Ω (*) V_s = 14 V R_L = 4 Ω V_s = 18 V R_L = 8 Ω V_s = 24 V R_L = 16 Ω	 2.2 5 5 4.5	 2.5 5.5 5.5 5.3		W
d	Harmonic Distortion	f = 1 KHz V_s = 9 V R_L = 4 Ω P_o = 50 mW to 1.5 W V_s = 14 V R_L = 4 Ω P_o = 50 mW to 3 W V_s = 18 V R_L = 8 Ω P_o = 50 mW to 3 W V_s = 24 V R_L = 16 Ω P_o = 50 mW to 3 W		 0.1 0.1 0.1 0.1		%
V_i	Input Sensitivity	f = 1 KHz V_s = 9 V R_L = 4 Ω P_o = 2.5 W V_s = 14 V R_L = 4 Ω P_o = 5.5 W V_s = 18 V R_L = 8 Ω P_o = 5.5 W V_s = 24 V R_L = 16 Ω P_o = 5.3 W		 37 49 73 100		mV
V_i	Input Saturation Voltage (rms)	V_s = 9 V V_s = 14 V V_s = 18 V V_s = 24 V	0.8 1.3 1.8 2.4			V
R_i	Input Resistance (pin 8)	f = 1 KHz	60	100		KΩ
I_d	Drain Current	f = 1 KHz V_s = 9 V R_L = 4 Ω P_o = 2.5 W V_s = 14 V R_L = 4 Ω P_o = 5.5 W V_s = 18 V R_L = 8 Ω P_o = 5.5 W V_s = 24 V R_L = 16 Ω P_o = 5.3 W		 380 550 410 295		mA
η	Efficiency	f = 1 KHz V_s = 9 V R_L = 4 Ω P_o = 2.5 W V_s = 14 V R_L = 4 Ω P_o = 5.5 W V_s = 18 V R_L = 8 Ω P_o = 5.5 W V_s = 24 V R_L = 16 Ω P_o = 5.3 W		 73 71 74 75		%

(*) With an external resistor of 100 Ω between pin 3 and $+V_s$.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BW	Small Signal bandwidth (– 3 dB)	V_s = 14 V R_L = 4 Ω P_o = 1 W	40 to 40,000			Hz
G_v	Voltage Gain (open loop)	Vs = 14 V f = 1 KHz		75		dB
G_v	Voltage Gain (closed loop)	V_s = 14 V R_L = 4 Ω f = 1 KHz P_o = 1 W	39.5	40	40.5	dB
e_N	Total Input Noise	R_g = 50 Ω R_g = 1 kΩ (°) R_g = 10 kΩ		1.2 1.3 1.5	4.0	µV
		R_g = 50 Ω R_g = 1 kΩ (°°) R_g = 10 kΩ		2.0 2.0 2.2	6.0	µV
S/N	Signal to Noise Ratio	V_s = 14 V, P_o = 5.5 W, R_L = 4 Ω: R_g = 10 kΩ (°) R_g = 0		90 92		dB
		R_g = 10 kΩ (°°) R_g = 0		87 87		dB
SVR	Supply Voltage Rejection	V_s = 18 V R_L = 8 Ω f_{ripple} = 100 Hz R_g = 10 kΩ V_{ripple} = 0.5 V_{rms}	40	50		dB
T_{sd}	Thermal Shut-down Case Temperature (*)	P_{tot} = 2.5 W		115		°C

MUTING FUNCTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TOFF}	Muting-off Threshold Voltage (pin 4)		1.9		4.7	V
V_{TON}	Muting-on Threshold Voltage (pin 4)		0		1.3	V
			6.2		V_s	V
R_5	Input Resistance (pin 5)	Muting-off	80	200		kΩ
		Muting-on		10	30	Ω
R_4	Input Resistance (pin 4)		150			kΩ
A_T	Muting Attenuation	R_g + R_1 = 10 kΩ	50	60		dB

Notes : (°) Weighting filter = curve A.
(°°) Filter with noise bandwidth : 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31.

Figure 1 : Quiescent Output Voltage vs. Supply Voltage.

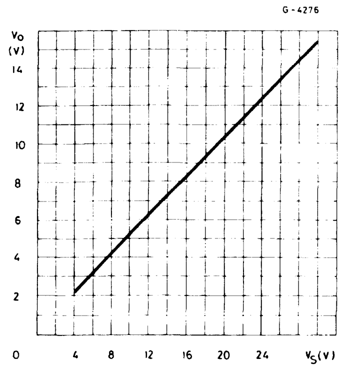


Figure 2 : Quiescent Drain Current vs. Supply Voltage.

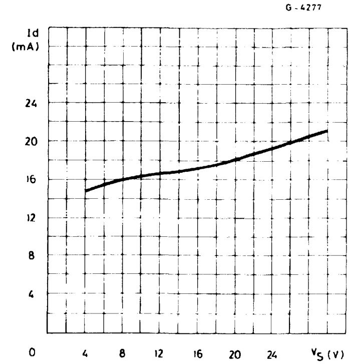


Figure 3 : Output Power vs. Supply Voltage.

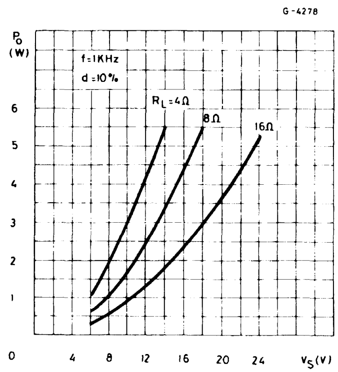


Figure 4 : Distortion vs. Output Power (R_L = 16 Ω).

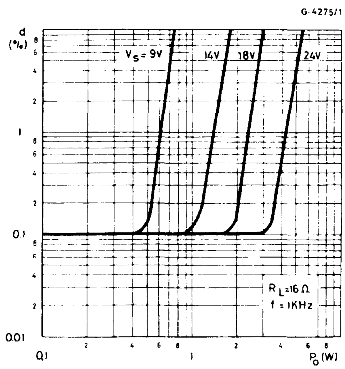


Figure 5 : Distortion vs. Output Power (R_L = 8 Ω).

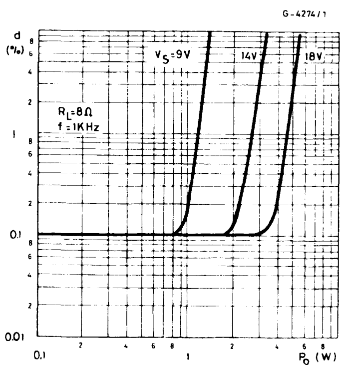


Figure 6 : Distortion vs. Output Power (R_L = 4 Ω).

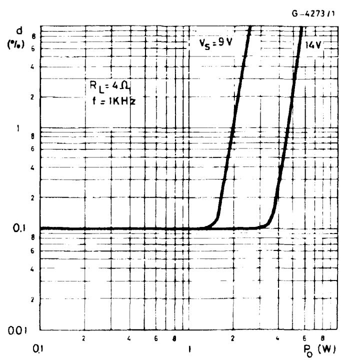


Figure 7 : Distortion vs. Frequency (R_L = 16 Ω).

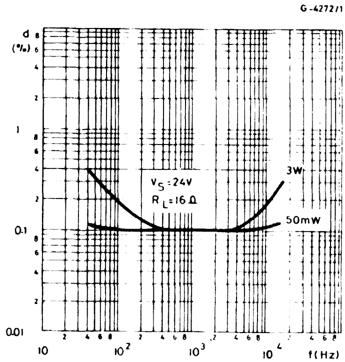


Figure 8 : Distortion vs. Frequency (R_L = 8 Ω).

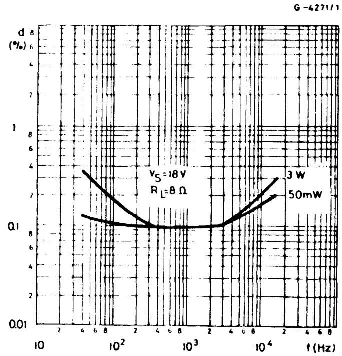


Figure 9 : Distortion vs. Frequency (R_L = 4 Ω).

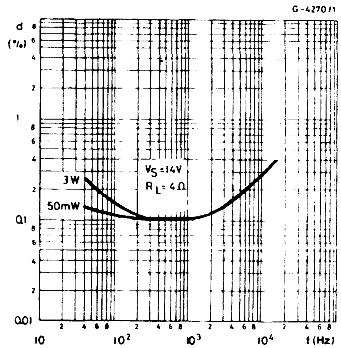


Figure 10 : Open Loop Frequency Response.

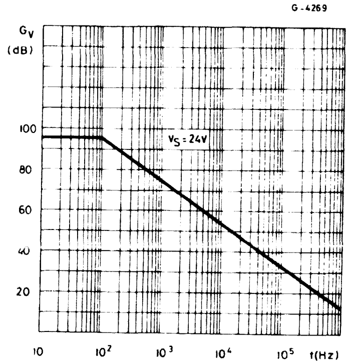


Figure 11 : Output Power vs. Input Voltage.

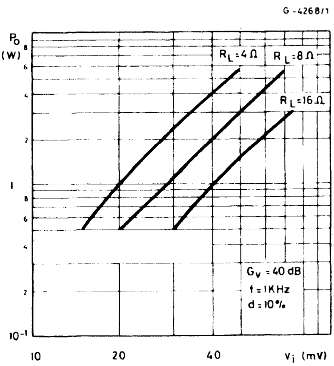


Figure 12 : Value of Capacitor Cx vs. Bandwidth (BW) and Gain (G_V).

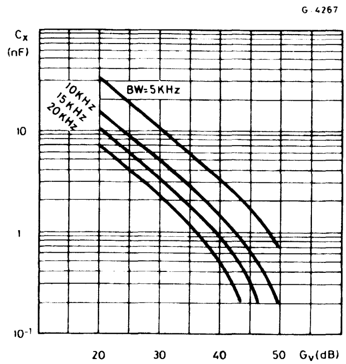


Figure 13 : Supply Voltage Rejection vs. Voltage Gain (ref. to the Muting circuit).

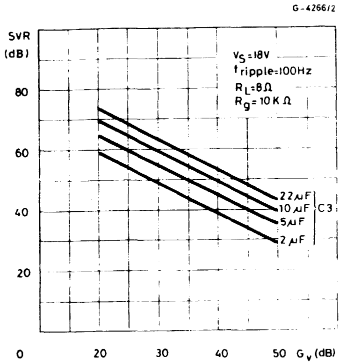


Figure 14 : Supply Voltage Rejection vs. Source Resistance.

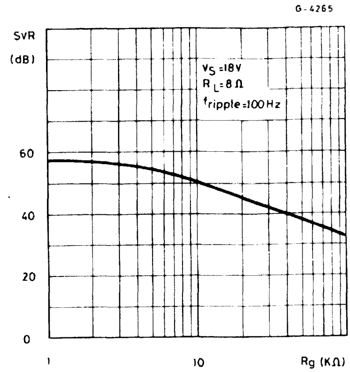


Figure 15 : Max Power Dissipation vs. Supply Voltage (sine wave operation).

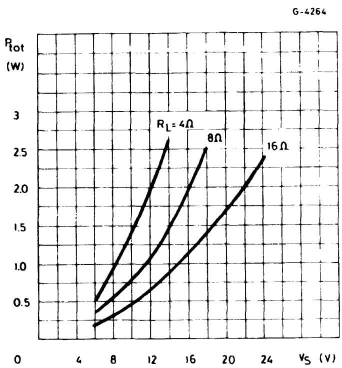


Figure 16 : Power Dissipation and Efficiency vs. Output Power.

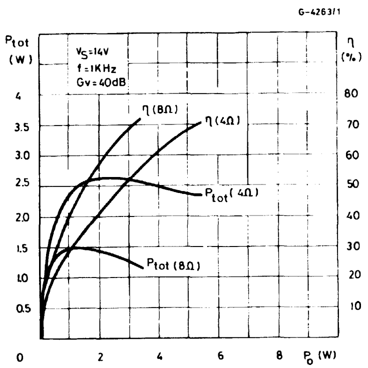


Figure 17 : Power Dissipation and Efficiency vs. Output Power.

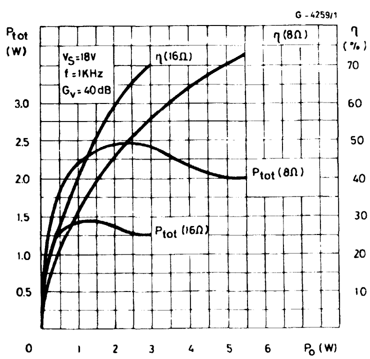
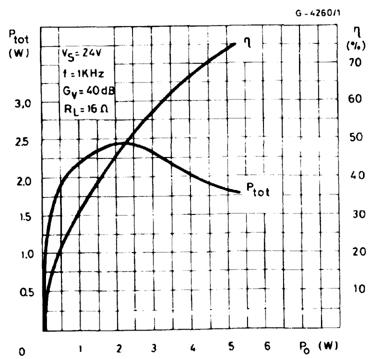
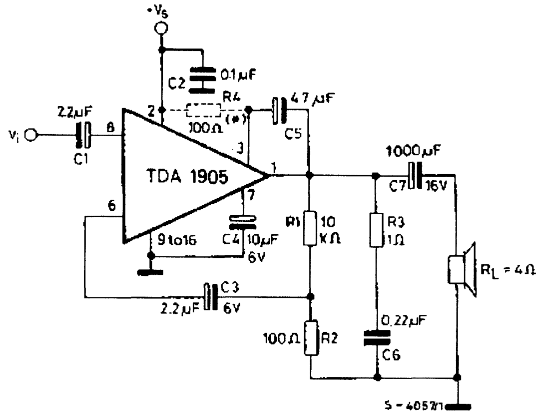


Figure 18 : Power Dissipation and Efficiency vs. Output Power.



APPLICATION INFORMATION

Figure 19 : Application Circuit without Muting.



(*) R_4 is necessary only for $V_s < 10$ V.

$P_o = 5.5$ W (d = 10 %)

$I_d = 0.55$ A

$G_v = 40$ dB

Figure 20 : PC Board and Components Layout of the Circuit of Figure 19 (1 : 1 scale).

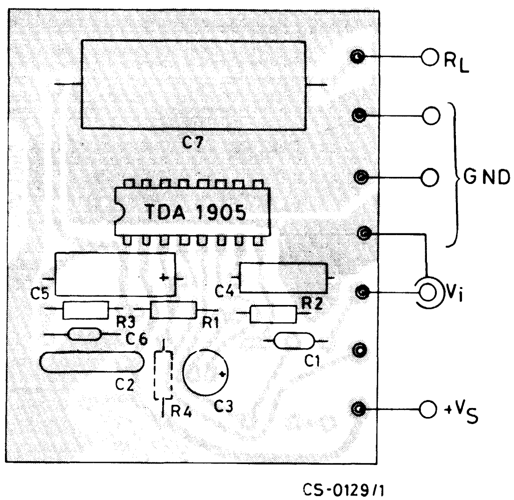


Figure 21 : Application Circuit with Muting.

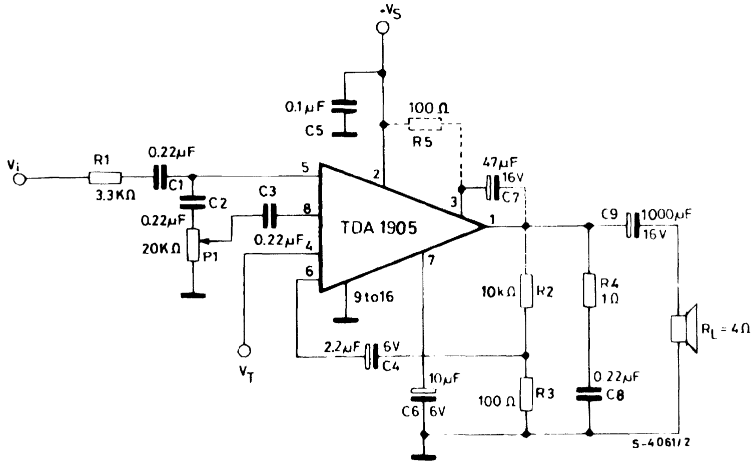


Figure 22 : Delayed Muting Circuit.

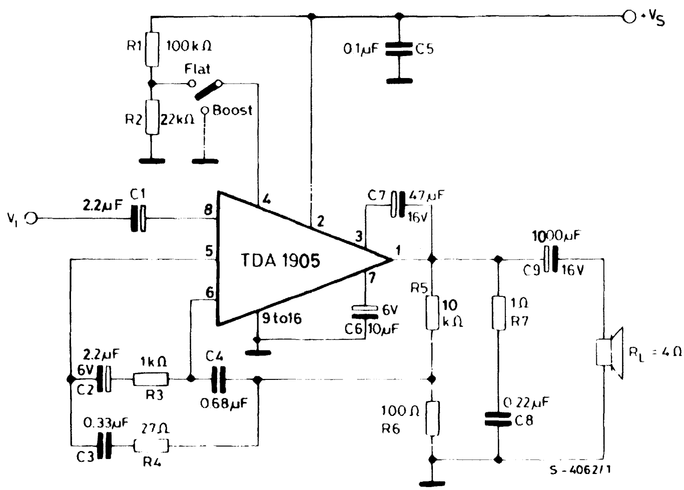


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Figure 23 : Low-cost Application Circuit without Boostrap.

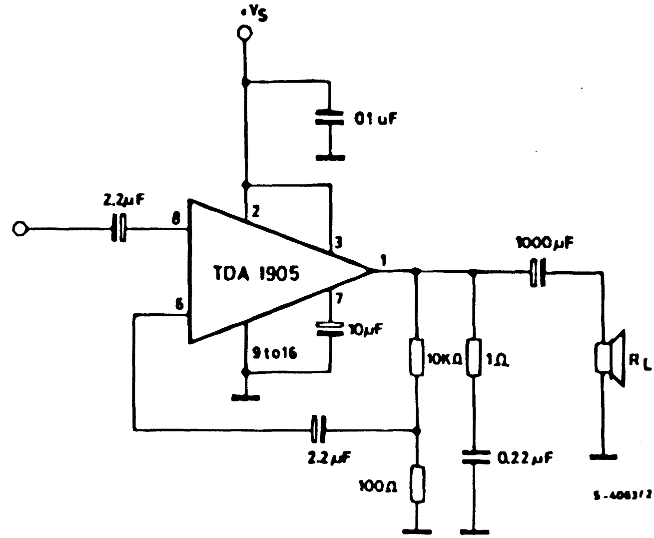


Figure 24 : Output Power vs. Supply Voltage (circuit of fig. 23).

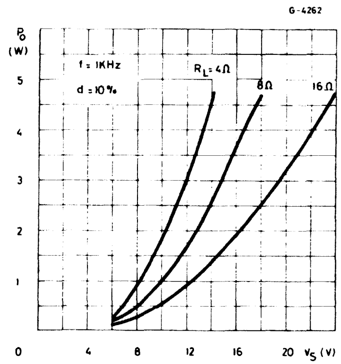


Figure 25 : Two Position DC Tone Control Using Change of Pin 5 Resistance (muting function).

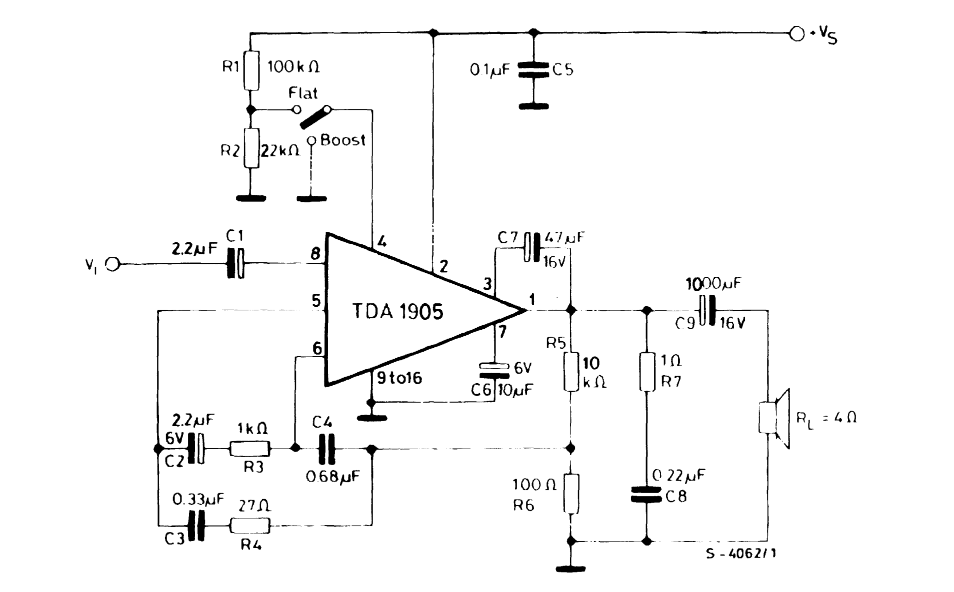


Figure 26 : Frequency Response of the Circuit of figure 25..

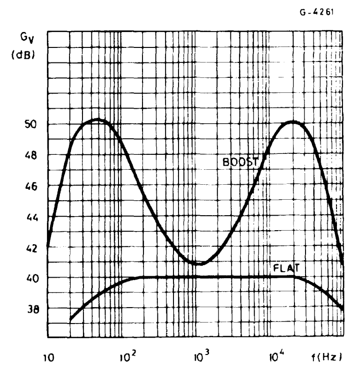


Figure 27 : Bass Bomb Tone Control Using Change of Pin 5 Resistance (muting function).

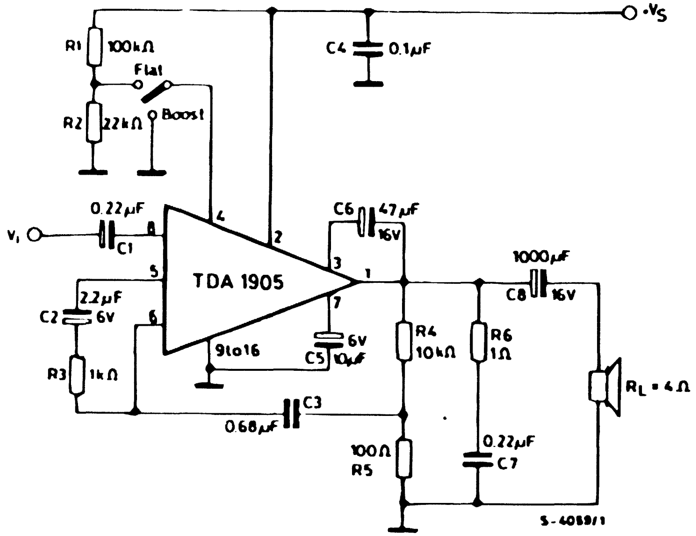
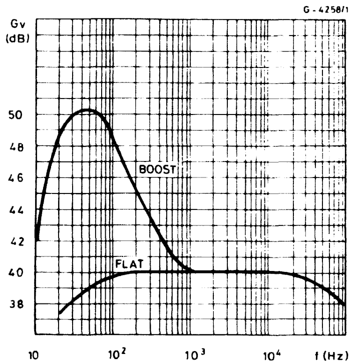


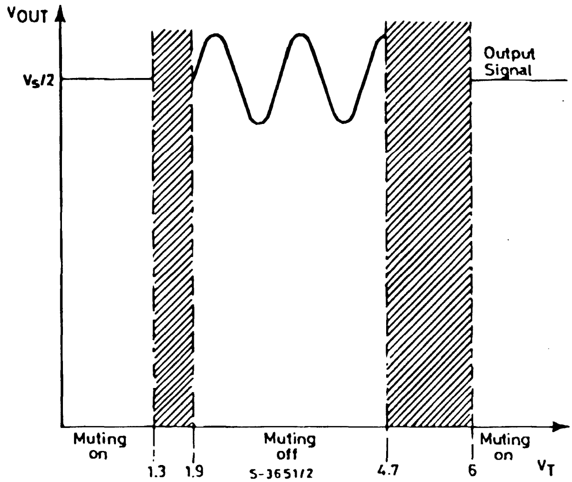
Figure 28 : Frequency Response of the Circuit of Figure 27.



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage V_T to pin 4, as shown in fig.29

Figure 29 .

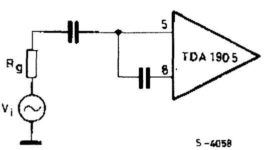


The input resistance at pin 5 depends on the threshold voltage V_T at pin 4 and is typically:

$R_5 = 200\ K\Omega$ @ $1.9\ V \leq V_T \leq 4.7\ V$ muting-off

$R_5 = 10\ \Omega$ @ $0V \leq V_T \leq 1.3\ V$, $6\ V \leq V_T \leq V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression:



$$A_T = \frac{V_i}{V_8} = \frac{R_g + (\frac{R_8 \cdot R_5}{R_8 + 5})}{(\frac{R_8 \cdot R_5}{R_8 + R_5})}$$

where $R_8 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.

A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 4 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig.22).
- during switching at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 5 can be useful in many application and two examples are shown in fig.25 and 27, where it has been used to change the feedback network, obtaining 2 different frequency response.

APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 21.

When the supply voltage V_S is less than 10 V, a 100 Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.

Different values can be used. The following table can help the designer.

Component	Raccom. Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value	Allowed Range Min.	Allowed Range Max.
$R_g + R_1$	10 KΩ	Input Signal Imped. for Muting Operation	Increase of the Attenuation in Muting-on Condition. Decrease of the Input Sensitivity.	Decrease of the Attenuation in Muting-on Condition.		
R_2	10 KΩ	Feedback Resistors	Increase of Gain	Decrease of Gain Increase Quiescent Current.	9 R_3	
R_3	100 Ω		Decrease of Gain	Increase of Gain		1 KΩ
R_4	1Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads.			
R_5	100 Ω	Increase of the Output Swing with Low Supply Voltage.			47	330
P_1	20 KΩ	Volume Potentiometer	Increase of the Switch-on Noise	Decrease of the Input Impedance and of the Input Level	10 KΩ	100 KΩ
C_1 C_2 C_3	0.22 μF	Input DC Decoupling.	Higher Cost Lower Noise.	Higher Low Frequency Cutoff. Higher Noise.		
C_4	2.2 μF	Inverting Input DC Decoupling.	Increase of the Switch-on Noise.	Higher Low Frequency Cutoff.	0.1 μF	
C_5	0.1 μF	Supply Voltage Bypass.		Danger of Oscillations.		
C_6	10 μF	Ripple Rejection	Increase of SVR Increase of the Switch-on Time	Degradation of SVR	2.2 μF	100 μF
C_7	47 μF	Bootstrap.		Increase of the Distortion at Low Frequency.	10 μF	100 μF
C_8	0.22 μF	Frequency Stability.		Danger of Oscillation.		
C_9	1000 μF	Output DC Decoupling.		Higher Low Frequency Cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the T_j cannot be higher than 150 °C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 32 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 30 : Output Power and Drain Current vs. Case Temperature.

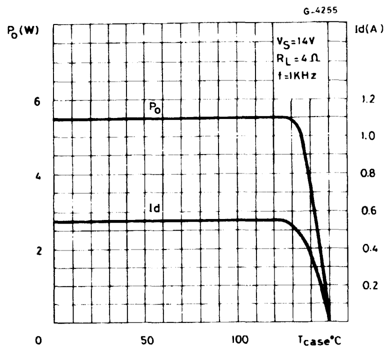


Figure 31 : Output Power and Drain Current vs. Case Temperature.

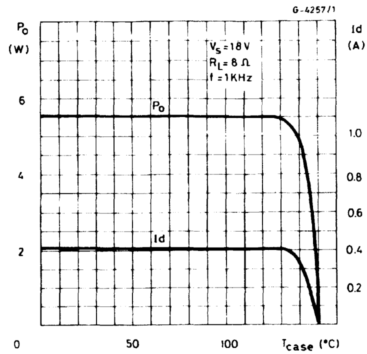
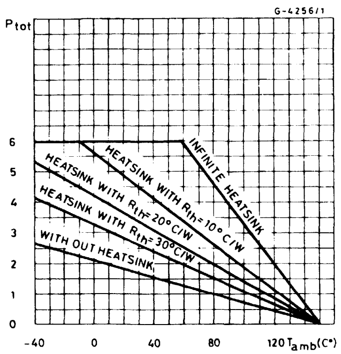


Figure 32 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



MOUNTING INSTRUCTION : See TDA1904.

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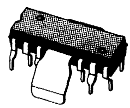
TDA1908

8 W AUDIO AMPLIFIER

- FLEXIBILITY IN USE WITH A MAX OUTPUT CURRENT OF 3 A AND AN OPERATING SUPPLY VOLTAGE RANGE OF 4 V TO 30 V
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- SOFT LIMITING IN SATURATION CONDITIONS
- LOW "SWITCH-ON" NOISE
- LOW NUMBER OF EXTERNAL COMPONENTS
- HIGH SUPPLY VOLTAGE REJECTION
- VERY LOW NOISE



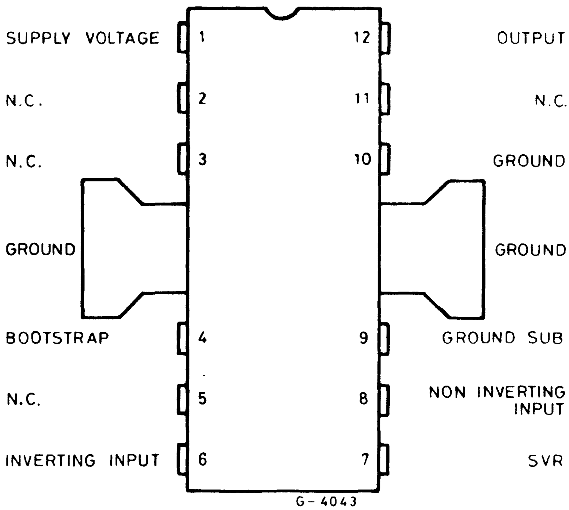
FINDIP
(Plastic 0.4)

ORDER CODE : TDA1908

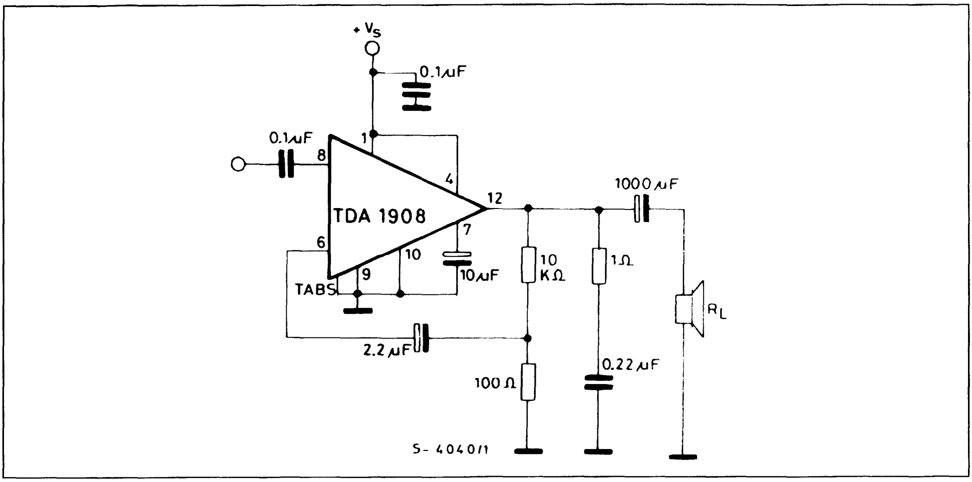
DESCRIPTION

The TDA1908 is a monolithic integrated circuit in 12 lead quad in-line plastic package intended for low frequency power applications. The mounting is compatible with the old types TBA800, TBA810S, TCA830S and TCA940N.

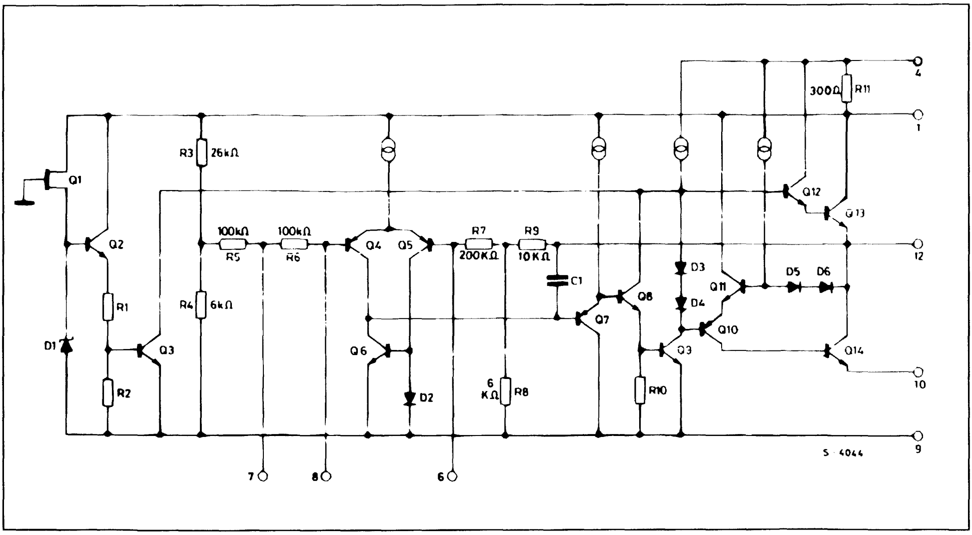
CONNECTION DIAGRAM (top view)



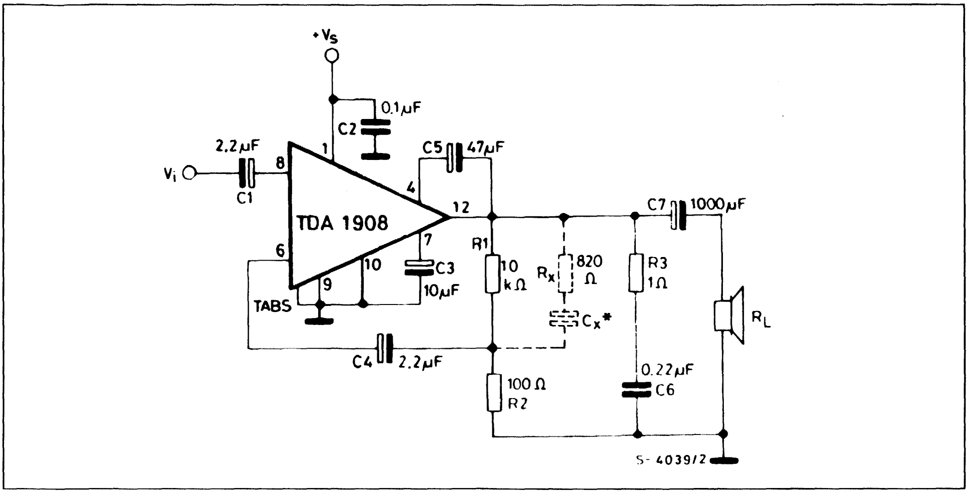
APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	30	V
I_o	Output Peak Current (non repetitive)	3.5	A
I_o	Output Peak Current (repetitive)	3	A
P_{tot}	Power Dissipation : at T_{amb} = 80 °C at T_{amb} = 90 °C	1 5	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}tab}$	Thermal Resistance Junction-tab	Max	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	(°) 70	°C/W

(°) Obtained with tabs soldered to printed circuit board with min copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, R_{th} (heatsink) = 8 °C/W, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		4		30	V
V_o	Quiescent Output Voltage	V_s = 4 V V_s = 18 V V_s = 30 V	1.6 8.2 14.4	2.1 9.2 15.5	2.5 10.2 16.8	V
I_d	Quiescent Drain Current	V_s = 4 V V_s = 18 V V_s = 30 V		15 17.5 21	 35	mA
V_{CEsat}	Output Stage Saturation Voltage (each output transistor)	I_C = 1 A I_C = 2.5 A		0.5 1.3		V
P_o	Output Power	d = 10 % f = 1 kHz V_s = 9 V R_L = 4 Ω V_s = 14 V R_L = 4 Ω V_s = 18 V R_L = 4 Ω V_s = 22 V R_L = 8 Ω V_s = 24 V R_L = 16 Ω	 7 6.5 4.5	 2.5 5.5 9 8 5.3		W
d	Harmonic Distortion	f = 1 kHz V_s = 9 V R_L = 4 Ω P_o = 50 mW to 1.5 W V_s = 18 V R_L = 4 Ω P_o = 50 mW to 4 W V_s = 24 V R_L = 16 Ω P_o = 50 mW to 3 W		 0.1 0.1 0.1		%
V_i	Input Sensitivity	V_s = 9 V R_L = 4 Ω P_o = 2.5 W V_s = 14 V R_L = 4 Ω P_o = 5.5 W V_s = 18 V R_L = 4 Ω P_o = 9 W V_s = 22 V R_L = 8 Ω P_o = 8 W V_s = 24 V R_L = 16 Ω P_o = 5.3 W		37 52 64 90 110		mV
V_i	Input Saturation Voltage (rms)	V_s = 9 V V_s = 14 V V_s = 18 V V_s = 24 V	0.8 1.3 1.8 2.4			V
R_i	Input Resistance (pin 8)	f = 1 kHz	60	100		KΩ
I_s	Drain Current	f = 1 kHz V_s = 14 V R_L = 4 Ω P_o = 5.5 W V_s = 18 V R_L = 4 Ω P_o = 9 W V_s = 22 V R_L = 8 Ω P_o = 8 W V_s = 24 V R_L = 16 Ω P_o = 5.3 W		 570 730 500 310		mA
η	Efficiency	V_s = 18 V f = 1 kHz R_L = 4 Ω P_o = 9 W		72		%
BW	Small Signal Bandwidth (– 3 dB)	V_s = 18 V R_L = 4 Ω P_o = 1 W	40 to 40 000			Hz
G_v	Voltage Gain (open loop)	f = 1 kHz		75		dB
G_v	Voltage Gain (closed loop)	V_s = 18 V R_L = 4 Ω f = 1 kHz P_o = 1 W	39.5	40	40.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
e_N	Total Input Noise	(°)	R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ		1.2 1.3 1.5	 4.0	µV
		(°°)	R_g = 50 Ω R_g = 1 KΩ R_g = 10 KΩ		2.0 2.0 2.2	 6.0	µV
S/N	Signal to Noise Ratio	V_s = 18 V P_o = 9 W R_L = 4 Ω	R_g = 10 KΩ R_g = 0 (°)		92 94		dB
			R_g = 10 KΩ R_g = 0 (°°)		88 90		dB
SVR	Supply Voltage Rejection	V_s = 18 V f_{ripple} = 100 Hz	R_L = 4 Ω R_g = 10 KΩ	40	50		dB
T_{sd}	Thermal Shut-down Junction Temperature (*)				145		°C

Note : (°) Weighting filter = curve A.
(°°) Filter with noise bandwith : 22 Hz to 22 KHz.

Figure 1 : Quiescient Output Voltage vs. supply Voltage.

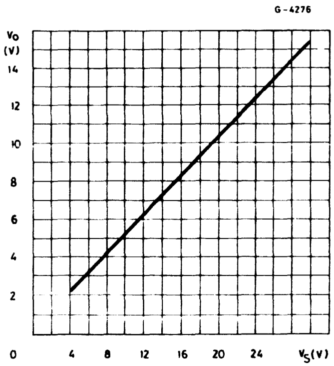


Figure 2 : Quiescent Drain Current vs. Supply Voltage.

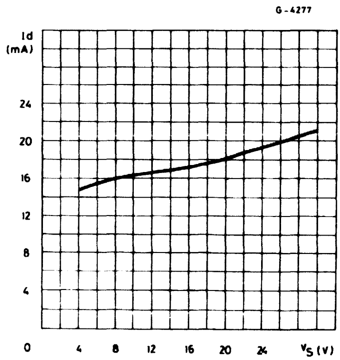


Figure 3 : Output Power vs. Supply Voltage.

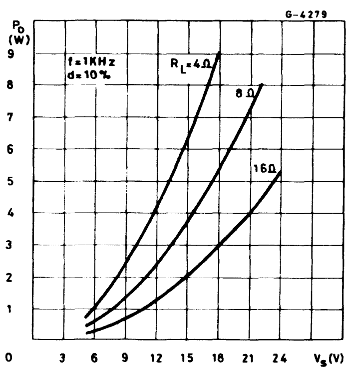


Figure 4 : Distortion vs. Output power (R_L = 16 Ω).

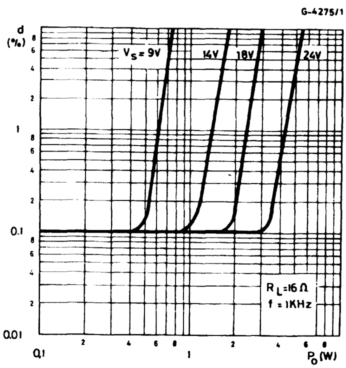


Figure 5 : Distortion vs. Output power (R_L = 8 Ω).

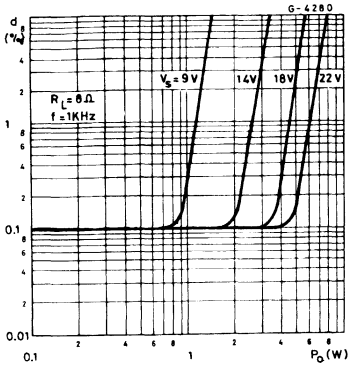


Figure 6 : Distortion vs. Output Power (R_L = 4 Ω).

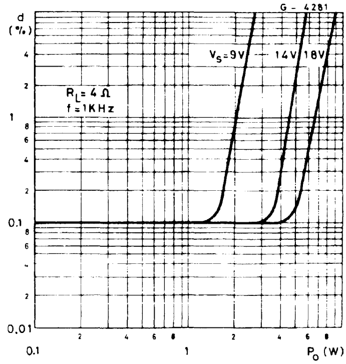


Figure 7 : Distortion vs. Frequency (R_L = 16 Ω).

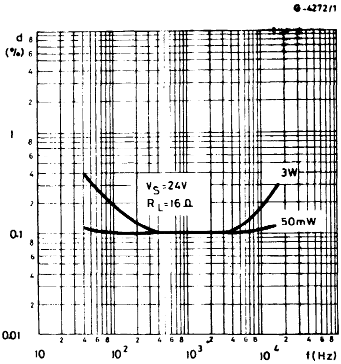


Figure 8 : Distortion vs. Frequency (R_L = 8 Ω).

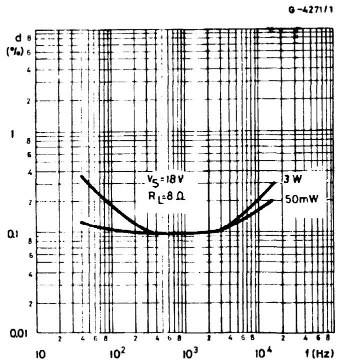


Figure 9 : Distortion vs. Frequency (R_L = 4 Ω).

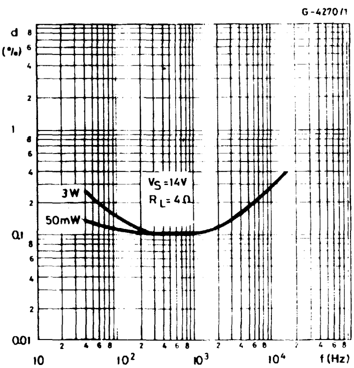


Figure 10 : Open Loop Frequency Response.

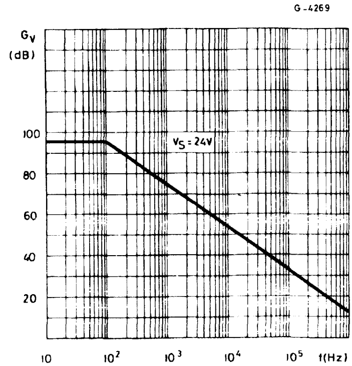


Figure 11 : Output power vs. Input Voltage.

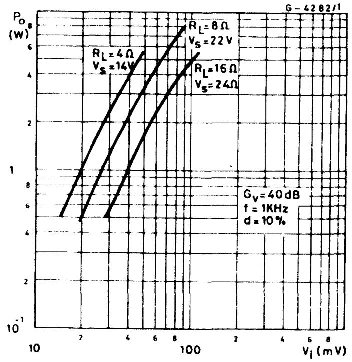


Figure 12 : Values of Capacitor C_x Versus Gain and Bw.

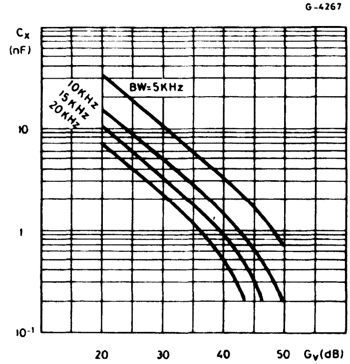


Figure 13 : Supply Voltage Rejection vs. Voltage Gain.

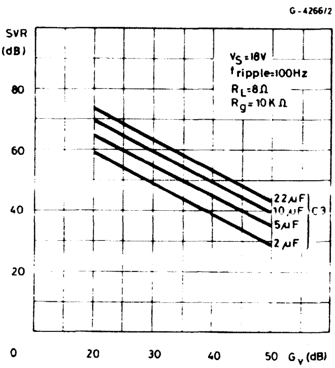


Figure 14 : Supply Voltage Rejection vs. Source Resistance..

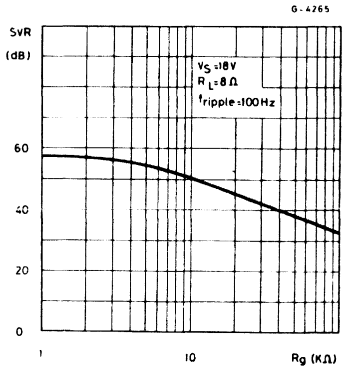


Figure 15 : Max Power Dissipation vs. Supply Voltage.

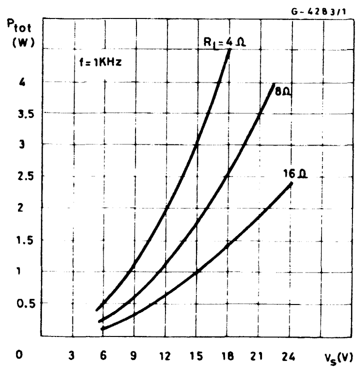


Figure 16 : Power Dissipation and Efficiency vs. Output Power (V_S = 14 V).

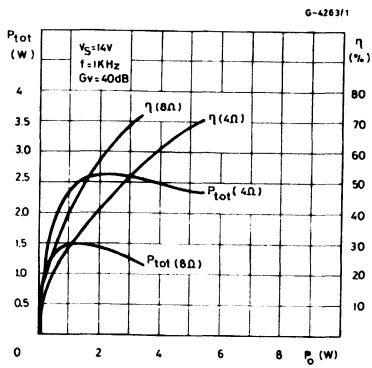


Figure 17 : Power Dissipation and Efficiency vs. Output Power (V_S = 18 V).

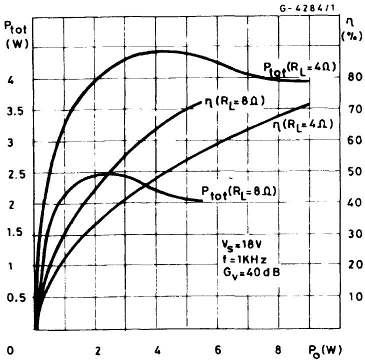
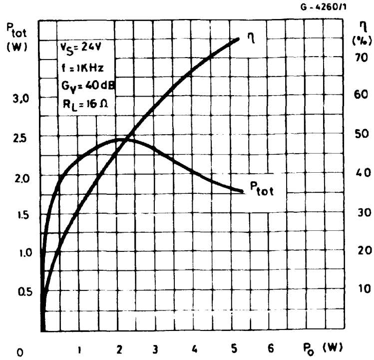
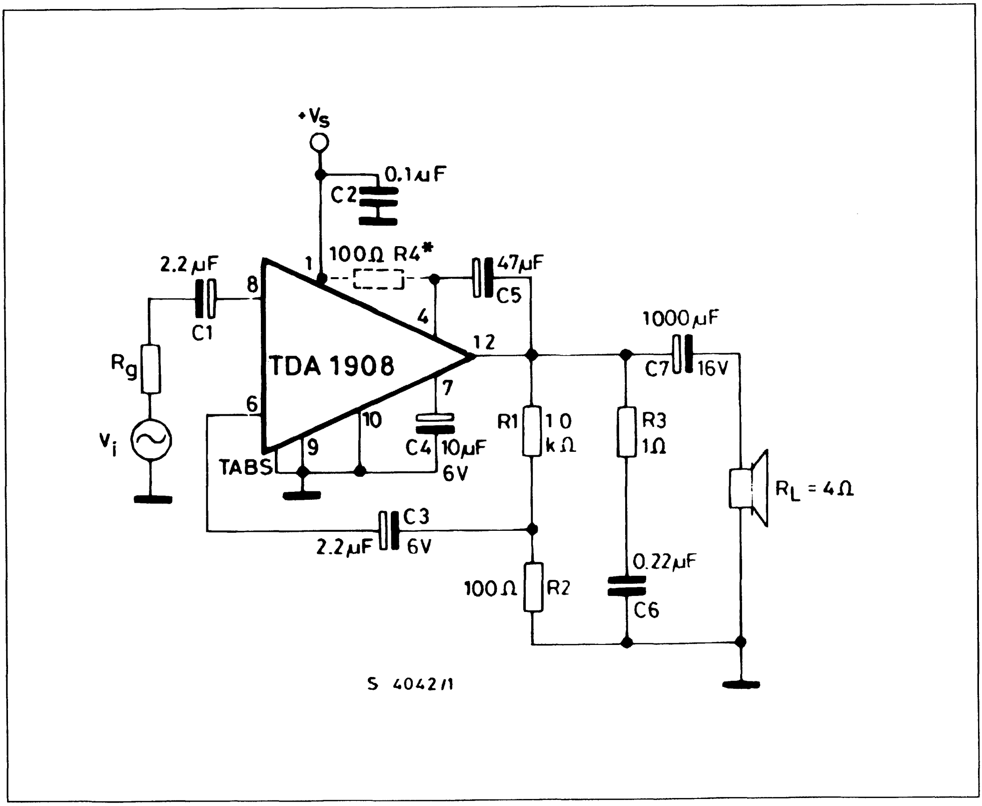


Figure 18 : Power Dissipation and Efficiency vs. Output Power (V_S = 24 V).



APPLICATION INFORMATION

Figure 19 : Application Circuit with Bootstrap.



* R4 is necessary when V_S is less than 10 V.

Figure 20 : P.C. Board and Component Layout of the Circuit of Fig. 19 (1 : 1 scale).

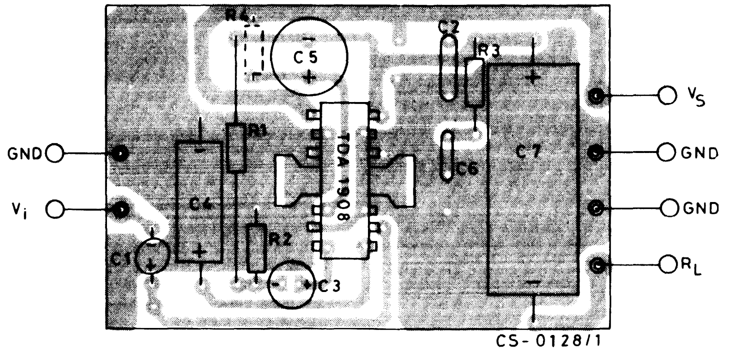


Figure 21 : Application Circuit without Bootstrap.

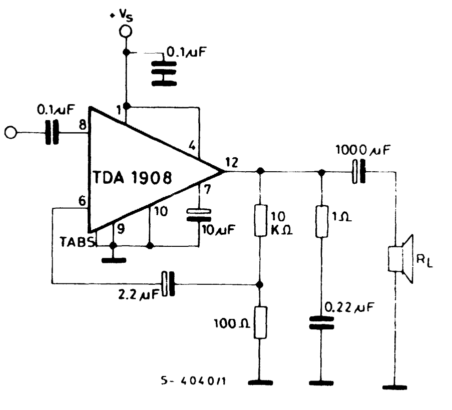


Figure 22 : Output Power vs. Supply Voltage (circuit of fig. 21).

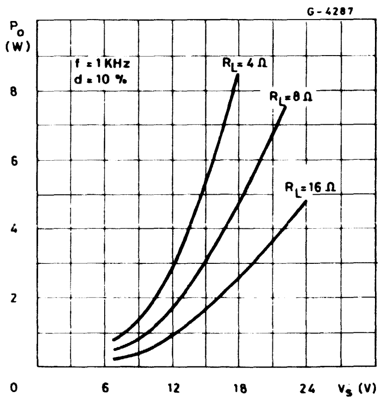
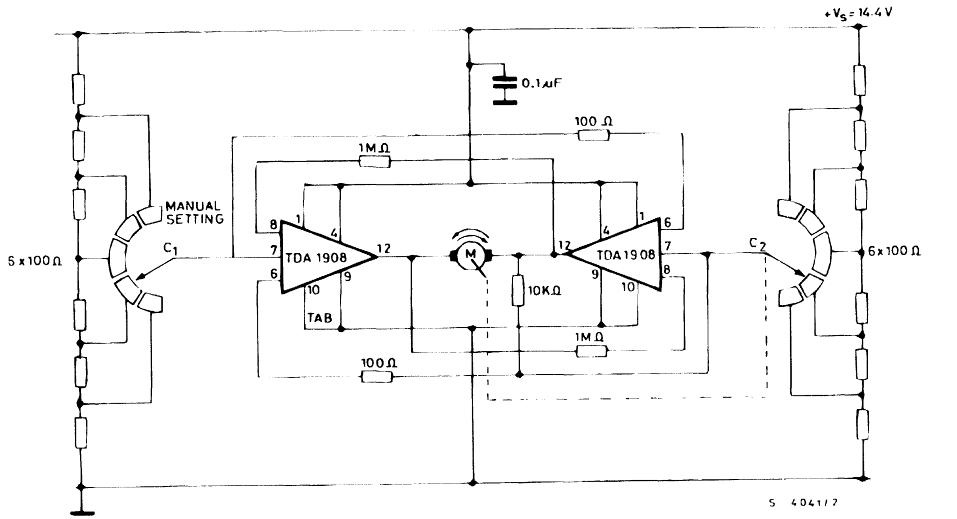


Figure 23 : Position Control for Car Headlights.



APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 19.

When the supply voltage V_s is less than 10 V, a 100 Ω resistor must be connected between pin 1 and pin 4 in order to obtain the maximum output power.

Different values can be used. The following table can help the designer.

Component	Raccom. Value	Purpose	Larger than Raccomanded Value	Smaller than Raccomanded Value	Allowed Range	
					Min.	Max.
R_1	10 KΩ	Close Loop Gain Setting.	Increase of Gain.	Decrease of Gain. Increase Quiescent Current.	9 R_2	
R_2	100 Ω	Close Loop Gain Setting.	Decrease of Gain.	Increase of Gain.		$R_1/9$
R_3	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads.			
R_4	100 Ω	Increasing of Output Swing with Low V_S.			47 Ω	330 Ω
C_1	2.2 μF	Input DC Decoupling.	Lower Noise	Higher Low Frequency Cutoff. Higher Noise.	0.1 μF	
C_2	0.1 μF	Supply Voltage Bypass.		Danger of Oscillations.		
C_3	2.2 μF	Inverting Input DC Decoupling.	Increase of the Switch-on Noise	Higher Low Frequency Cutoff.	0.1 μF	
C_4	10 μF	Ripple Rejection.	Increase of SVR. increase of the Switch-on Time.	Degradation of SVR.	2.2 μF	100 μF
C_5	47 μF	Bootstrap		Increase of the Distortion at Low Frequency	10 μF	100 μF
C_6	0.22 μF	Frequency Stability		Danger of Oscillation		
C_7	1000 μF	Output DC Decoupling.		Higher Low Frequency Cutoff.		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150 °C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increase up to 150 ° C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 26 shows the dissipable power as a function of ambient temperature for different thermal resistance.

Figure 24 : Output Power and Drain Current vs. Case Temperature.

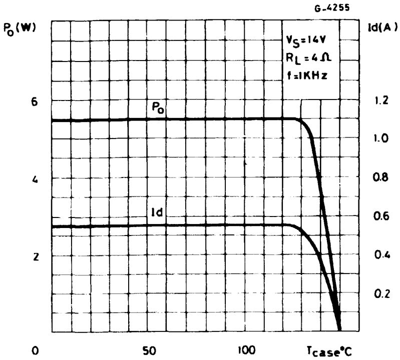


Figure 25 : Output Power and Drain Curent vs. Case Temperature.

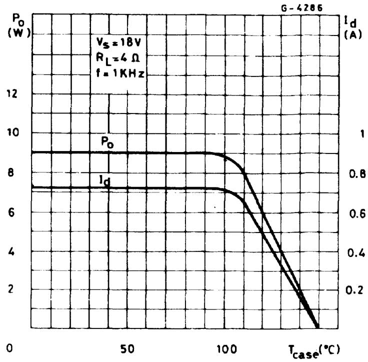
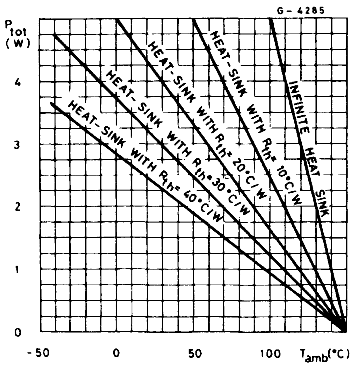


Figure 26 : Maximum Power Dissipation vs. Ambient Temperature.



MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to a copper area on the PC board (see fig. 27).

During soldering, tab temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

Figure 27 : Mounding Example.

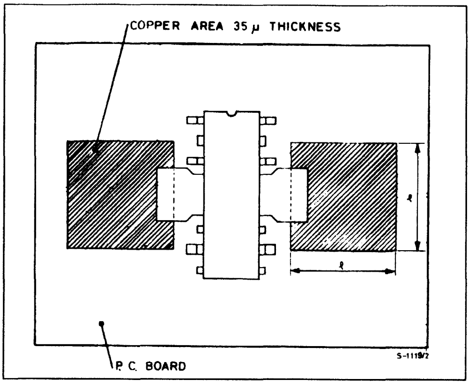
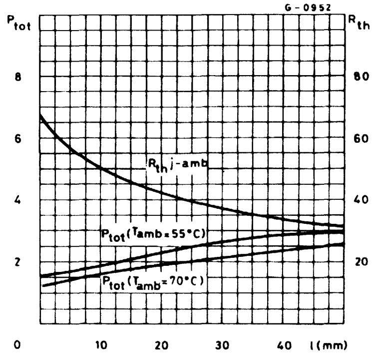


Figure 28 : Maximum Power Dissipation and Thermal Resistance vs. Side "∝".

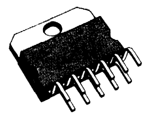


10W AUDIO AMPLIFIER WITH MUTING

- MUTING FACILITY
- PROTECTION AGAINST CHIP OVER TEMPERATURE
- VERY LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- LOW "SWITCH-ON" NOISE

The TDA1910 is assembled in MULTIWATT® package that offers :

- EASY ASSEMBLY
- SIMPLE HEATSINK
- SPACE AND COST SAVING
- HIGH RELIABILITY.



Multiwatt 11

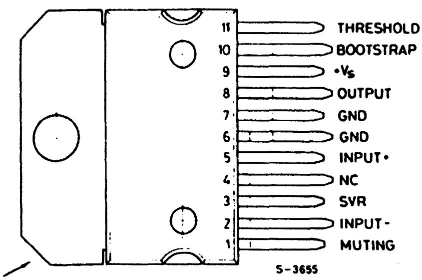
ORDER CODE : TDA1910

DESCRIPTION

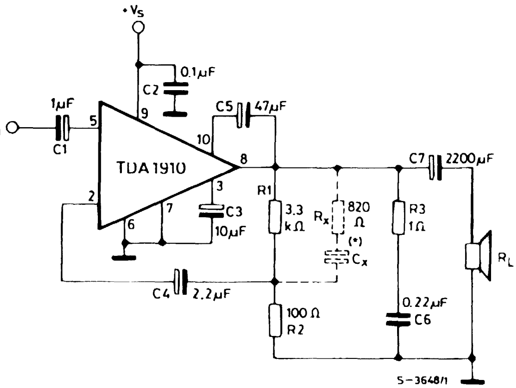
The TDA1910 is a monolithic integrated circuit in MULTIWATT® package, intended for use in Hi-Fi audio power applications, as high quality TV sets.

The TDA1910 meets the DIN 45500 (d = 0.5 %) guaranteed output power of 10 W when used at 24V/4Ω At 24V/8Ω the output power is 7W min.

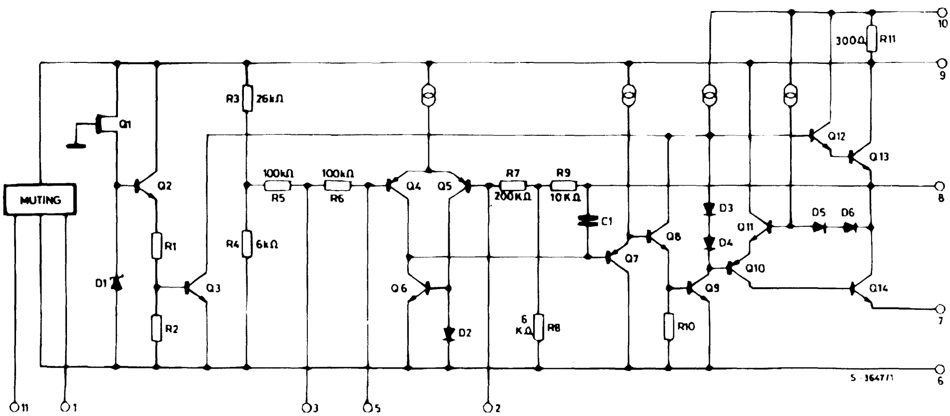
PIN CONNECTION (top view)



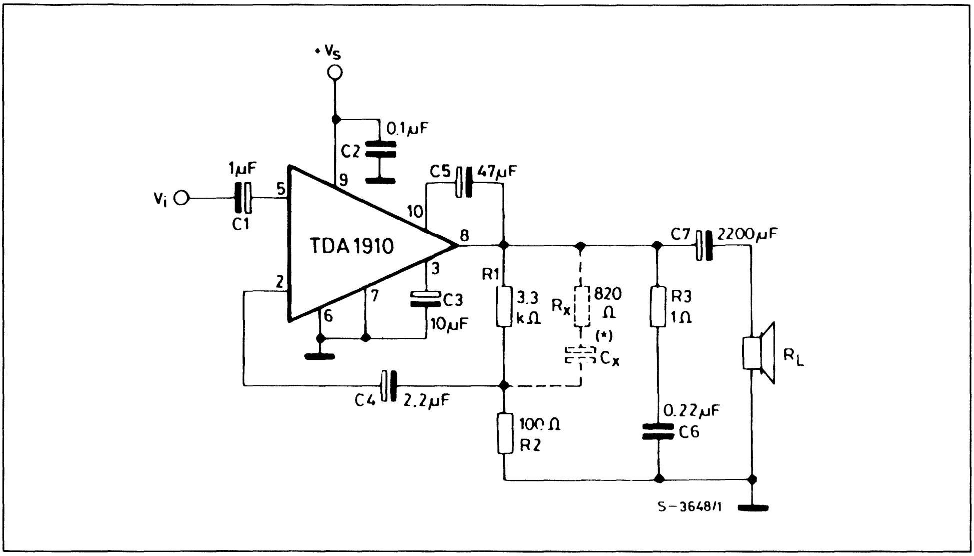
TEST CIRCUIT



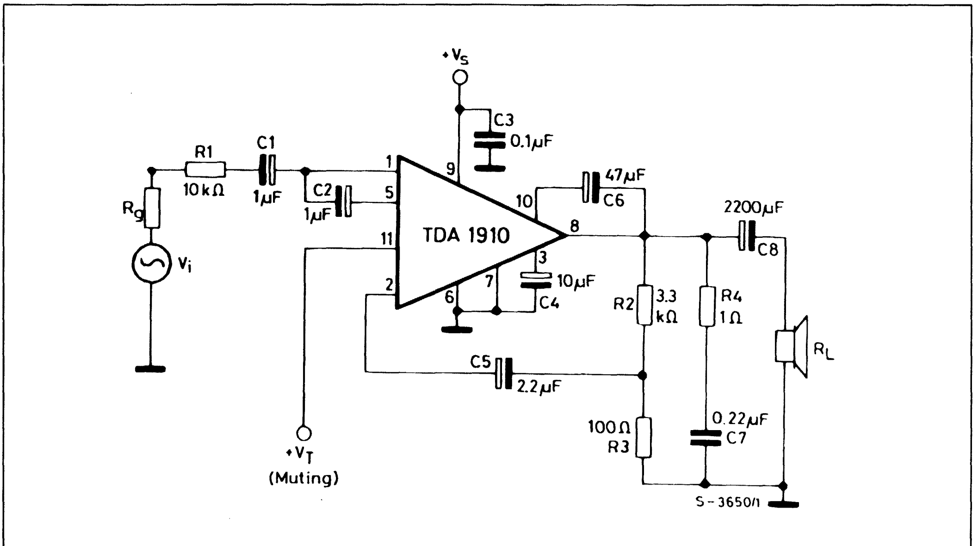
SCHEMATIC DIAGRAM



TEST CIRCUIT



MUTING CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	30	V
I_o	Output Peak Current (non repetitive)	3.5	A
I_o	Output Peak Current (repetitive)	3.0	A
V_i	Input Voltage	0 to + V_s	V
V_i	Differential Input Voltage	± 7	V
V_{11}	Muting Threshold Voltage	V_s	V
P_{tot}	Power Dissipattion at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_{amb} = 25 °C, R_{th} (heastsink) = 4 °C/W, unless otherwisse specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		30	V
V_o	Quiescent Output Voltage	V_s = 18 V V_s = 24 V	8.3 11.5	9.2 12.4	10 13.4	V
I_d	Quiescent Drain Current	V_s = 18 V V_s = 24 V		19 21	32 35	mA
$V_{CE\ sat}$	Output Stage Saturation Voltage	I_C = 2 A		1		V
		I_C = 3 A		1.6		
P_o	Output Power	d = 0.5 % f = 40 to 15, 000 Hz V_s = 18 V R_L = 4 Ω V_s = 24 V R_L = 4 Ω V_s = 24 V R_L = 8 Ω	 6.5 10 7	 7 12 7.5		W
		d = 10 % f = 1 kHz V_s = 18 V R_L = 4 Ω V_s = 24 V R_L = 4 Ω V_s = 24 V R_L = 8 Ω	 8.5 15 9	 9.5 17 10		W
d	Harmonic Distortion	f = 40 to 15, 000 Hz V_s = 18 V R_L = 4 Ω P_o = 50 mW to 6.5 W V_s = 24 V R_L = 4 Ω P_o = 50 mW to 10 W V_s = 24 V R_L = 8 Ω P_o = 50 mW to 7 W		 0.2 0.2 0.2	 0.5 0.5 0.5	%
d	Intermodulation Distortion	V_s = 24 V R_L = 4 Ω P_o = 10 W f_1 = 250 Hz f_2 = 8 kHz (DIN 45500)		0.2		%
V_i	Input Sensitivity	f = 1 kHz V_s = 18 V R_L = 4 Ω P_o = 7 W V_s = 24 V R_L = 4 Ω P_o = 12 W V_s = 24 V R_L = 8 Ω P_o = 7.5 W		 170 220 245		mV
V_i	Input Saturation Voltage (rms)	V_s = 18 V V_s = 24 V	1.8 2.4			V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
R_i	Input Resistance (pin 5)	f = 1 kHz		60	100		kΩ
I_d	Drain Current	V_s = 24 V R_L = 4 Ω R_L = 8 Ω	f = 1 kHz P_o = 12 W P_o = 7.5 W		820 475		mA
η	Efficiency	V_s = 24 V R_L = 4 Ω R_L = 8 Ω	f = 1 kHz P_o = 12 W P_o = 7.5 W		62 65		%
BW	Small Signal Bandwidth	V_s = 24 V R_L = 4 Ω P_o = 1 W		10 to 120, 000			Hz
BW	Power Bandwidth	V_s = 24 V P_o = 12 W	R_L = 4 Ω d ≤ 0.5 %	40 to 15, 000			Hz
G_v	Voltage Gain (open loop)	f = 1 kHz			75		dB
Gv	Voltage Gain (closed loop)	V_s = 24 V f = 1 kHz	R_L = 4 Ω P_o = 1 W	29.5	30	30.5	dB
e_N	Total Input Noise		R_g = 50 Ω R_g = 1 kΩ (°) R_g = 10 kΩ		1.2 1.3 1.5	3.0 3.2 4.0	µV
			R_g = 50 Ω R_g = 1 kΩ (°°) R_g = 10 kΩ		2.0 2.0 2.2	5.0 5.2 6.0	µV
S/N	Signal to Noise Ratio	V_s = 24 V P_o = 12 W R_L = 4 Ω	R_g = 10 kΩ R_g = 0 (°)	97	103 105		dB
			R_g = 10 kΩ R_g = 0 (°°)	93	100 100		dB
SVR	Supply Voltage Rejection	V_s = 24 V f_{ripple} = 100 Hz	R_L = 4 Ω R_g = 10 kΩ	50	60		dB
T_{sd}	Thermal Shut-down CaseTemperature (*)		P_{tot} = 8 W	110	125		°C

MUTING FUNCTION (refer to muting circuit)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_T	Muting-off Threshold Voltage (pin 11)		1.9		4.7	V
V_T	Muting-on Threshold Voltage (pin 11)		0		1.3	V
			6		V_s	
R_1	Input Resistance (pin 1)	Muting Off	80	200		kΩ
		Muting On		10	30	Ω
R_{11}	Input Resistance (pin 11)		150			kΩ
A_T	Muting Attenuation	R_g + R_1 = 10 kΩ	50	60		dB

Note : (°) Weighting filter = curve A.
(°°) Filter with noise bandwidth : 22 Hz to 22 kHz.
(*) See fig.29 and fig.30.

Figure 1 : Quiescent Output Voltage vs. Supply Voltage.

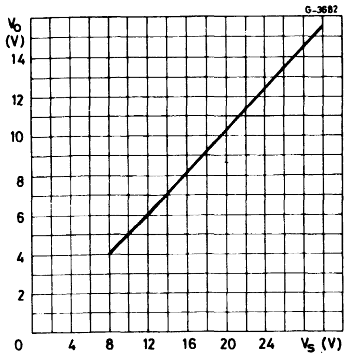


Figure 2 : Quiescent Drain Current vs. Supply Voltage.

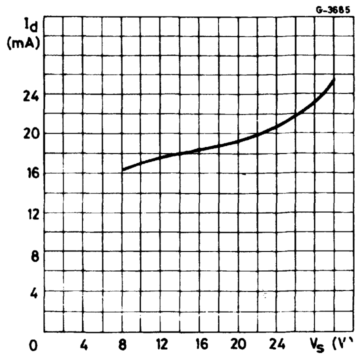


Figure 3 : Open Loop Frequency Response.

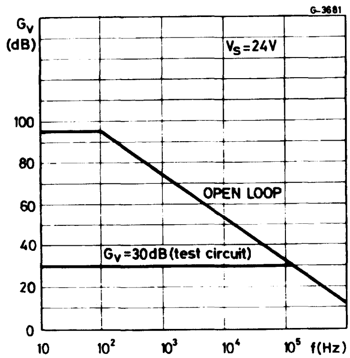


Figure 4 : Output Power vs. Supply Voltage.

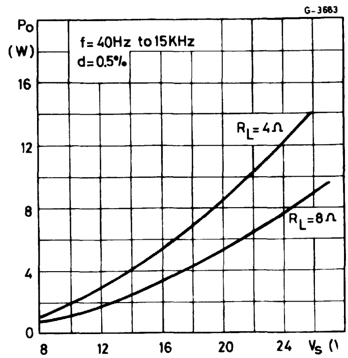


Figure 5 : Output Power vs. Supply Voltage.

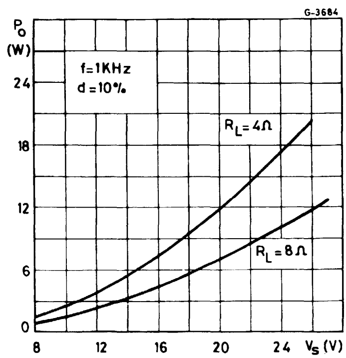


Figure 6 : Distortion vs. Output Power.

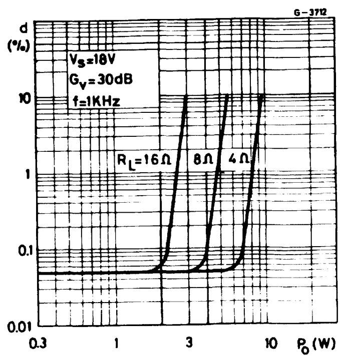


Figure 7 : Distortion vs. Output Power.

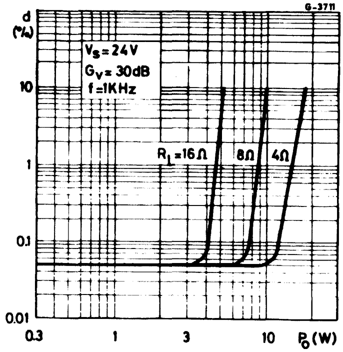


Figure 8 : Output Power vs. Frequency.

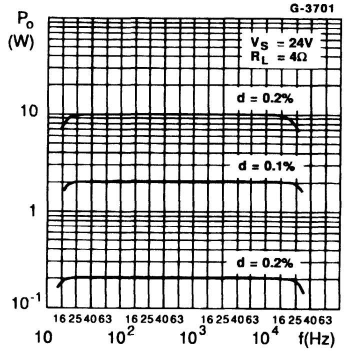


Figure 9 : Output Power vs. Frequency.

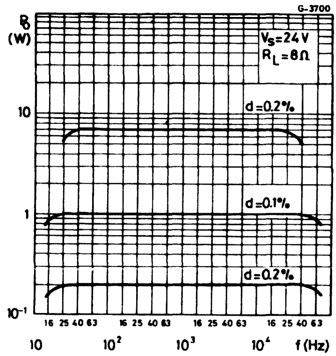


Figure 10 : Output Power vs. Input Voltage.

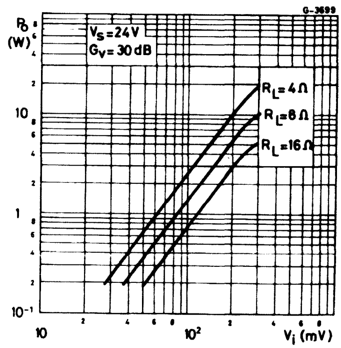


Figure 11 : Output Power vs. Input Voltage.

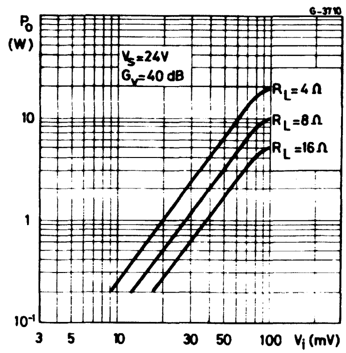


Figure 12 : Total Input Noise vs. Source Resistance.

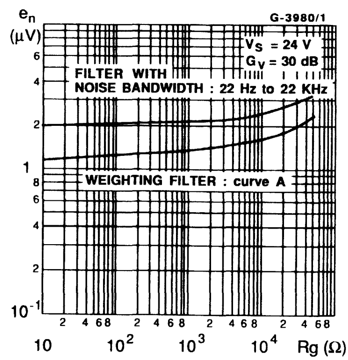


Figure 13 : Values of Capacitor Cx vs. Bandwidth (BW) and Gain (Gv).

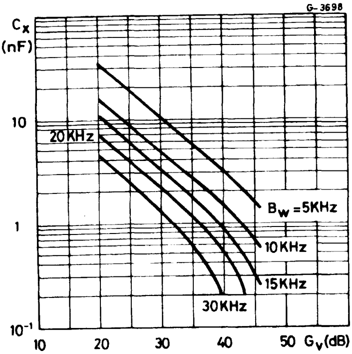


Figure 14 : Supply Voltage Rejection vs. Voltage Gain.

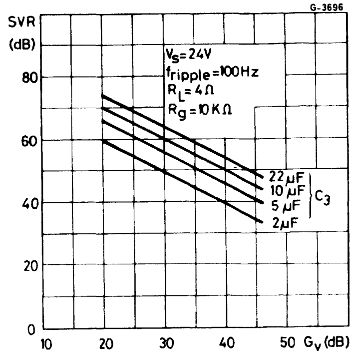


Figure 15 : Supply Voltage Rejection vs. Source Resistance.

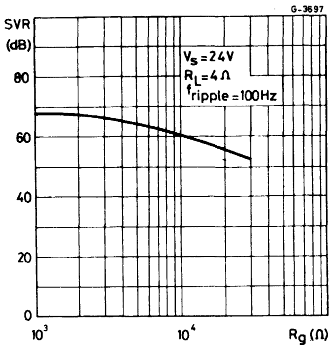


Figure 16 : Power Dissipation and Efficiency vs. Output Power.

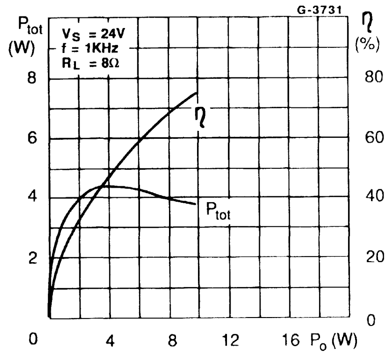


Figure 17 : Power Dissipation and Efficiency vs. Output Power.

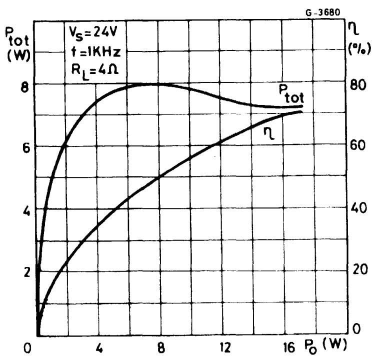
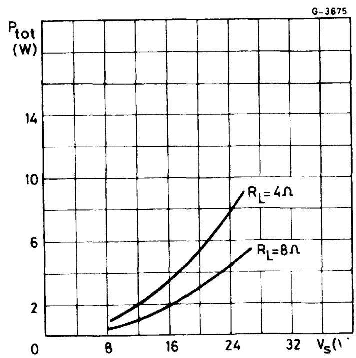


Figure 18 : Max Power Dissipation vs. Supply Voltage.



APPLICATION INFORMATION

Figure 19 : Application Circuit without Muting.

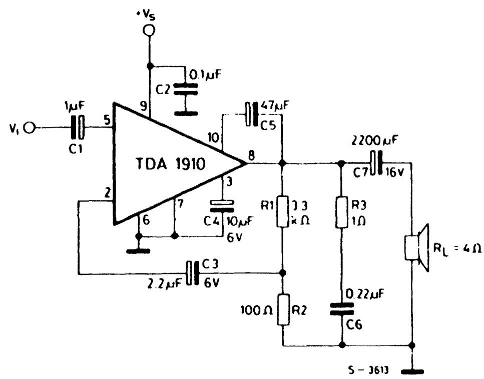


Figure 20 : P.C. Board and Component layout of the Circuit of Fig.19 (1 : 1 scale).

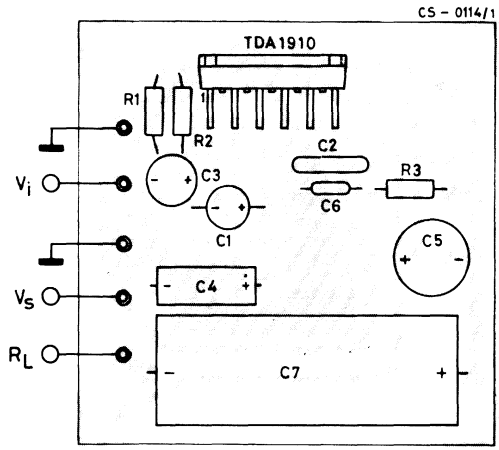
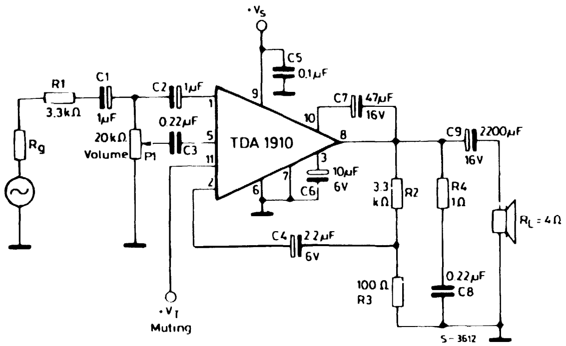


Figure 21 : Application Circuit with Muting.



Performance (circuits of fig.19 and 21)

P_O = 12W (40 to 15000Hz, d ≤0.5%)

V_S = 24V

I_d = 0.82A

G_v = 30dB

Figure 22 : Two Position DC Tone Control (10dB boost 50Hz and 20kHz) using Change of Pin 1 Resistance (muting function).

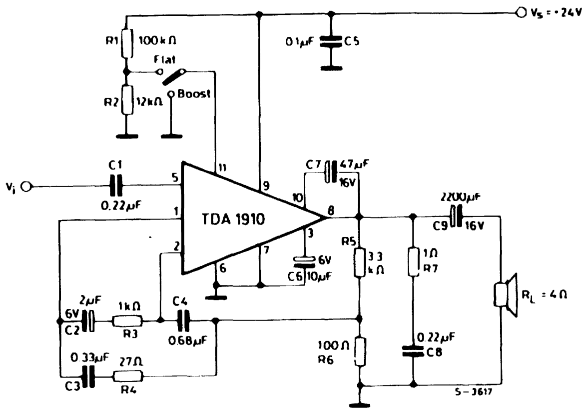


Figure 23 : 10dB 50Hz Boost Tone Control using Change of Pin 1 Resistance (muting function).

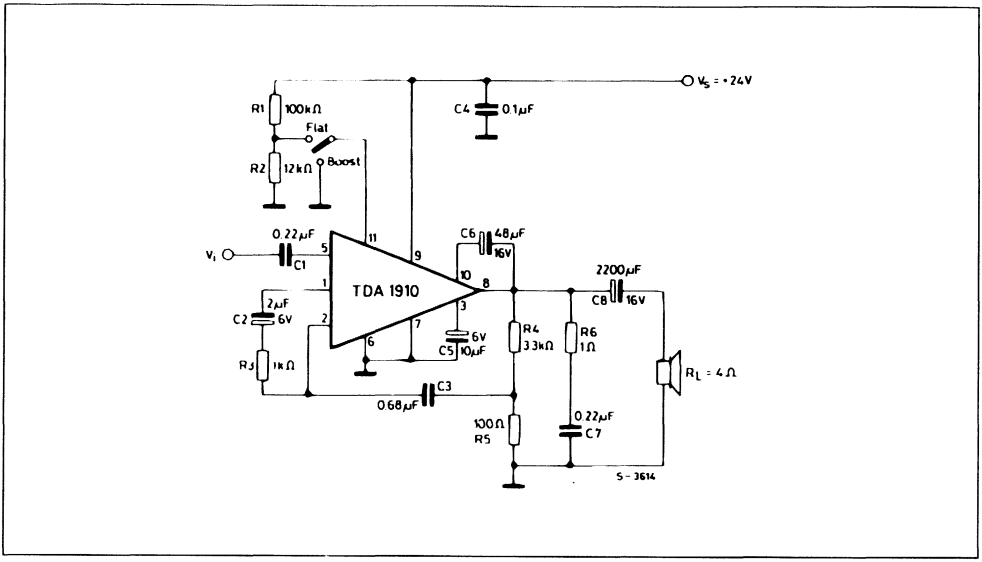


Figure 24 : Frequency Response of the Circuit of fig.22

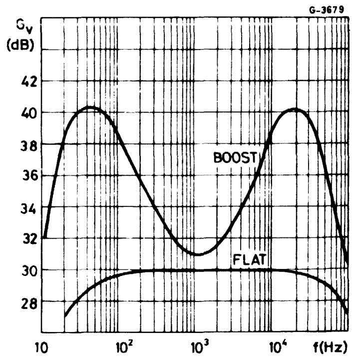


Figure 25 : Frequency Response of the Circuit of fig.23

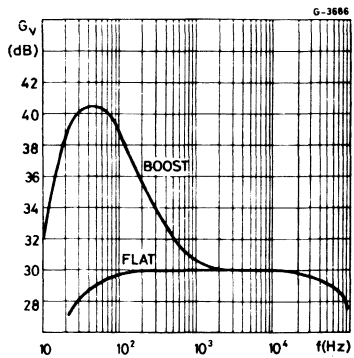


Figure 26 : Squelch Function in TV Applications.

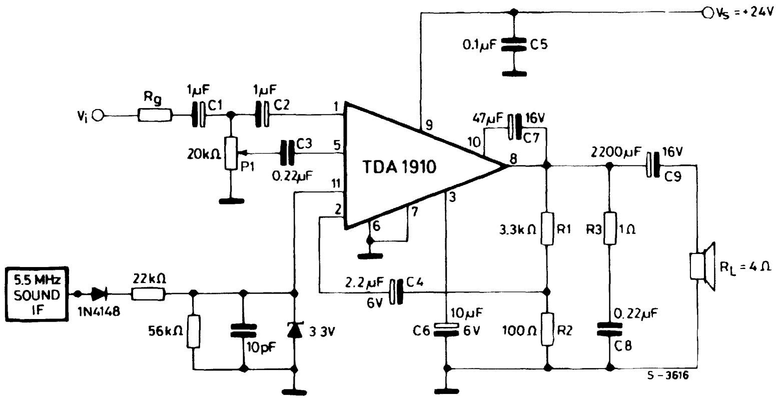
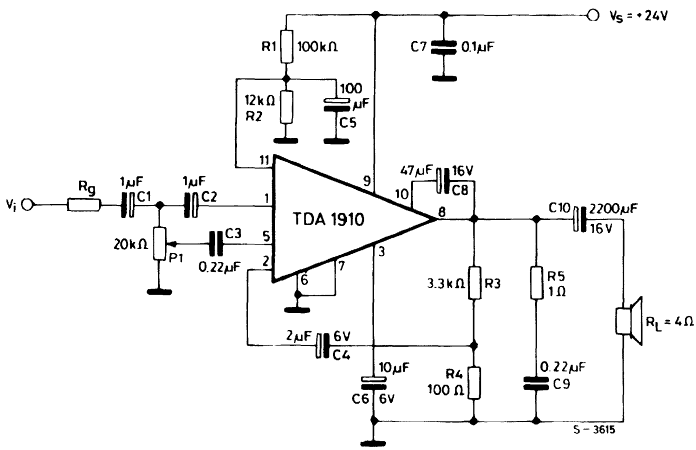


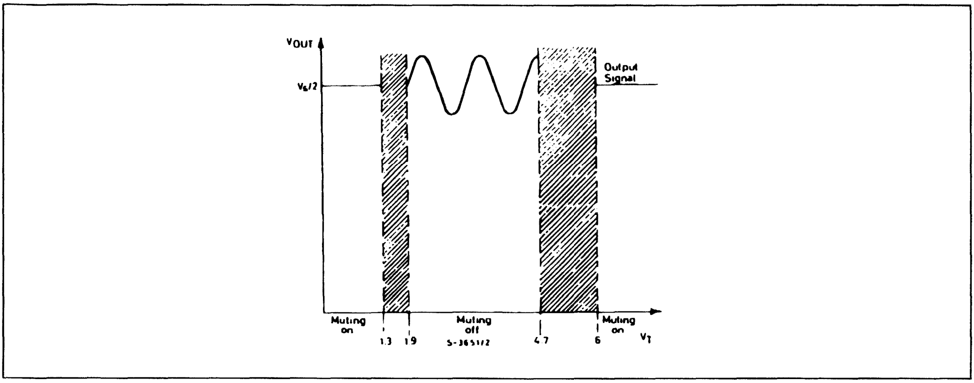
Figure 27 : Delayed Muting Circuit.



MUTING FUNCTION

The output signal can be inhibited applying a DC voltage VT to pin 11, as shown in fig.28.

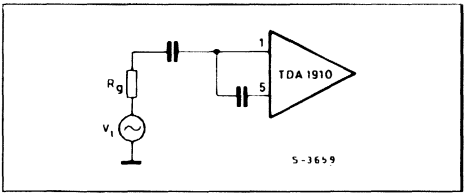
Figure 28.



The input resistance at pin 1 depends on the threshold voltage V_T at pin 11 and is typically.

$R_1 = 200\ k\Omega$	@	$1.9\ V \leq V_T \leq 4.7\ V$	muting-off
$R1 = 10\Omega$	@	$0\ V \leq V_T \leq 1.3\ V$ $6\ V \leq V_T \leq V_S$	muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression.



$$A_T = \frac{V_i}{V_5} = \frac{R_g + R_5//R_1}{R_5//R_1}$$

where R5 = 100kΩ

Considering $R_g = 10\ k\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.

A very low current is necessary to drive the threshold voltage V_T because the input resistance at pin 11 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example :

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 27).
- during commutations at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 1 can be useful in many applications and we have shown 2 examples in fig. 22 and 24, where it has been used to change the feedback network, obtaining 2 different frequency responses.

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 21. Different values can be used.

The following table can help the designer.

Component	Recomm. Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value	Allowed Range	
					Min.	Typ.
$R_g + R_1$	10 kΩ	Input Signal Imped. for Muting Operation	Increase of the Attenuation in Muting-on Condition. Decrease of the Input Sensitivity.	Decrease of the Attenuation in Muting on Condition		
R_2	3.3 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain Increase Quiescent Current	9 R_3	
R_3	100 Ω	Close Loop Gain Setting	Decrease of Gain	Increase of Gain		$R_2/9$
R_4	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads			
P_1	20 kΩ	Volume Potentiometer	Increase of the Switch-on Noise	Decrease of the Input Impedance and The Input Level	10 kΩ	100 kΩ
C_1 C_2 C_3	1 µF 1 µF 0.22 µF	Input DC Decoupling		Higher Low Frequency Cutoff		
C_4	2.2 µF	Inverting Input DC Decoupling	Increase of the Switch-on Noise	Higher Low Frequency Cutoff	0.1 µF	
C_5	0.1 µF	Supply Voltage Bypass		Danger of Oscillations		
C_6	10 µF	Ripple Rejection	Increase of SVR Increase of the Switch-on Time	Degradation of SVR	2.2 µF	100 µF
C_7	47 µF	Boostrap.		Increase of the Distortion at Low Frequency	10 µF	100 µF
C_8	0.22 µF	Frequency Stability		Danger of Oscillation		
C_9	2200 µF (R_L = 4 Ω) 1000 µF (R_L = 8 Ω)	Output DC Decoupling		Higher Low Frequency Cutoff		

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150° C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

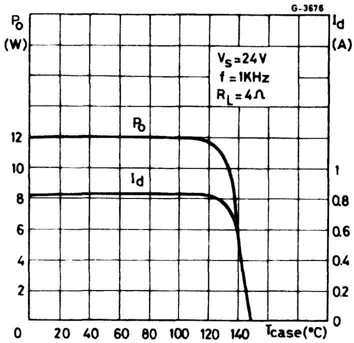


Figure 29 : Output Power and Drain Current vs. Case Temperature.

If for any reason, the junction temperature increases up to 150 ° C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 31 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 30 : Output Power and Drain Current vs. Case Temperature.

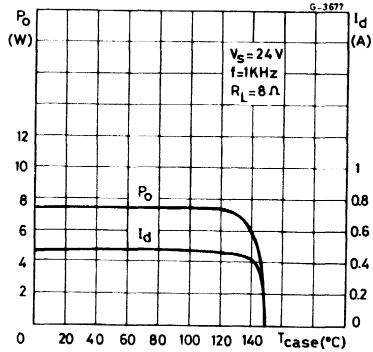
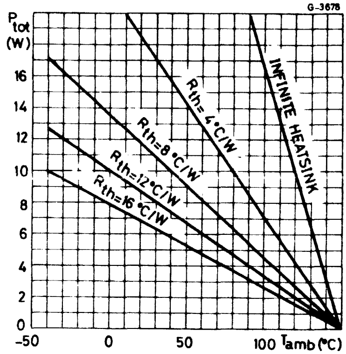


Figure 31 : Maximum allowable Power Dissipation vs . Ambient Temperature.



MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

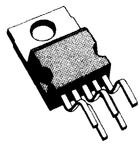
Thanks to the Multiwatt ® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

TDA2006

12W AUDIO AMPLIFIER

DESCRIPTION

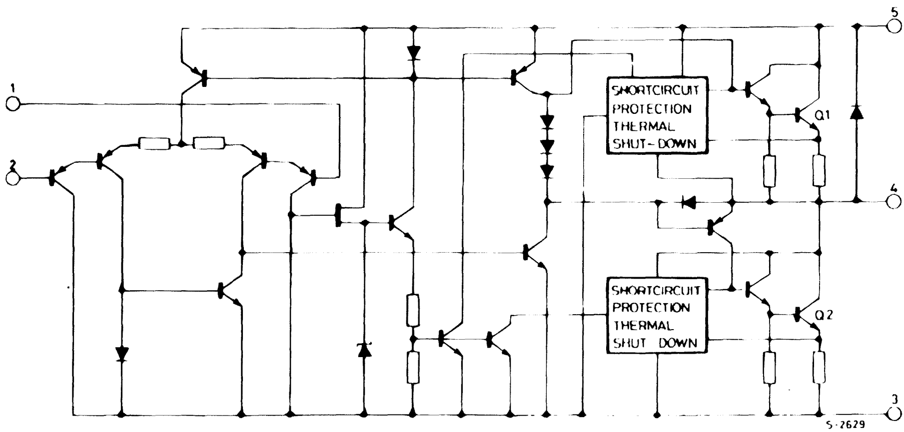
The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ±12V, d = 10 % typically it provides 12W output power on a 4Ω load and 8W on a 8Ω . The TDA2006 provides high output current and has very low harmonic and crossover distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.



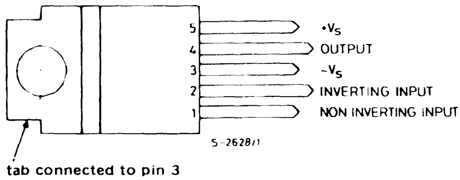
Pentawatt

ORDER CODES : TDA2006H
TDA2006V

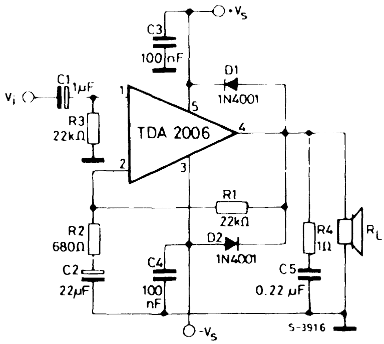
SCHEMATIC DIAGRAM



PIN CONNECTION



TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 12	V
I_o	Output Peak Current (internaly limited)	3	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit ; V_s = ± 12 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 15	V
I_d	Quiescent Drain Current	V_s = ± 15 V		40	80	mA
I_b	Input Bias Current			0.2	3	µA
V_{OS}	Input Offset Voltage			± 8		mV
I_{OS}	Input Offset Current			± 80		nA
V_{OS}	Output Offset Voltage			± 10	± 100	mV
P_o	Output Power	d = 10 % f = 1 kHz R_L = 4 Ω R_L = 8 Ω	 6	 12 8		 W W
d	Distortion	P_o = 0.1 to 8 W R_L = 4 Ω f = 1 kHz		0.2		%
		P_o = 0.1 to 4 W R_L = 8 Ω f = 1 kHz		0.1	1	%
V_i	Input Sensitivity	f = 1 kHz P_o = 10 W R_L = 4 Ω P_o = 6 W R_L = 8 Ω		 200 220		 mV mV
B	Frequency Response (– 3 dB)	P_o = 8 W R_L = 4 Ω	20 Hz to 100 kHz			
R_i	Input Resistance (pin 1)	f = 1 kHz	0.5	5		MΩ
G_v	Voltage Gain (open loop)			75		dB
G_v	Voltage Gain (closed loop)		29.5	30	30.5	dB
e_N	Input Noise Voltage	B (– 3 dB) = 22 Hz to 22 kHz R_L = 4 Ω		3	10	µV
i_N	Input Noise Current			80	200	pA
SVR	Supply Voltage Rejection	R_L = 4 Ω R_g = 22 kΩ f_{ripple} = 100 Hz (*)	40	50		dB
I_d	Drain Current	P_o = 12 W R_L = 4 Ω P_o = 8 W R_L = 8 Ω		850 500		mA mA
T_j	Thermal Shutdown Junction Temperature				145	°C

(*) Referring to Fig. 15, single supply.

Figure 1 : Output Power vs. Supply Voltage.

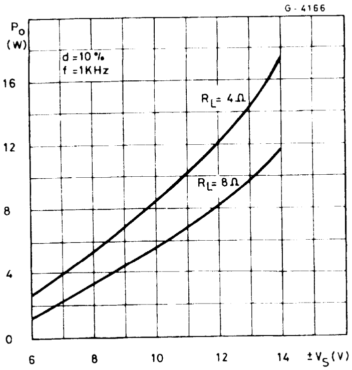


Figure 2 : Distortion vs. Output Power.

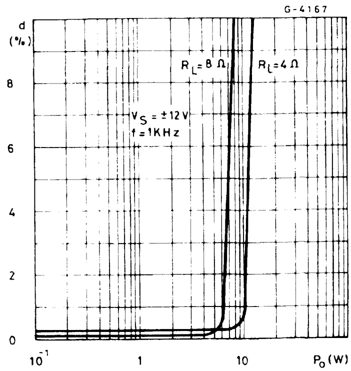


Figure 3 : Distortion vs. Frequency.

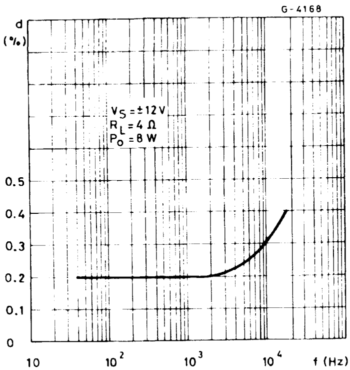


Figure 4 : Distortion vs. Frequency.

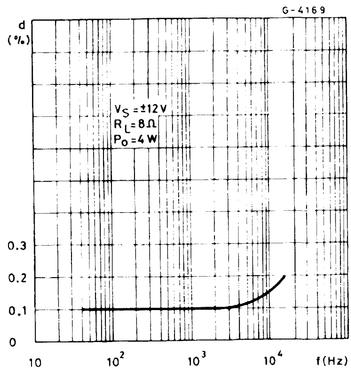


Figure 5 : Sensivity vs. Output Power.

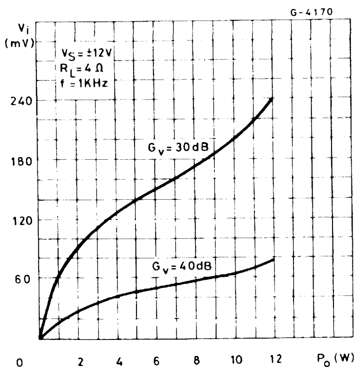


Figure 6 : Sensivity vs. Output Power.

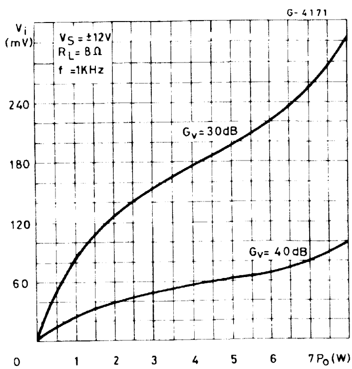


Figure 7 : Frequency Response with different values of the rolloff Capacitor C8 (see fig.13).

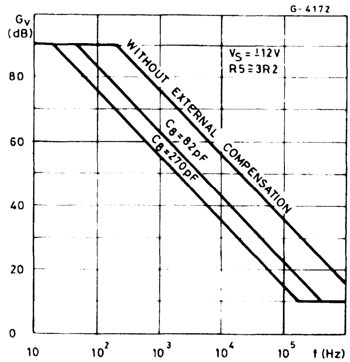


Figure 8 : Value of C8 vs. Voltage Gain for different Bandwidths (see fig.13).

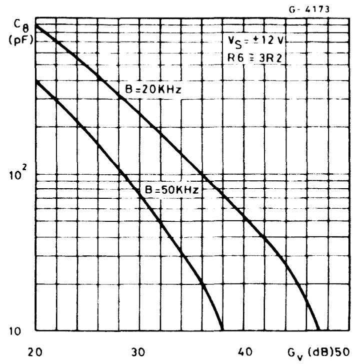


Figure 9 : Quiescent Current vs. Supply Voltage.

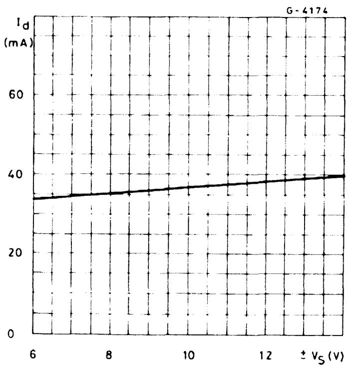


Figure 10 : Supply Voltage Rejection vs. Voltage Gain

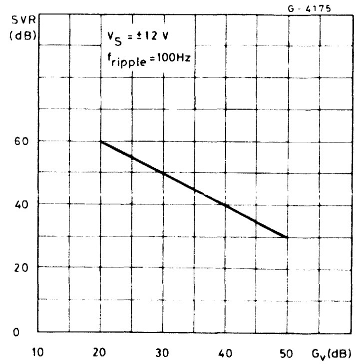


Figure 11 : Power Dissipation and efficiency vs. Output Power.

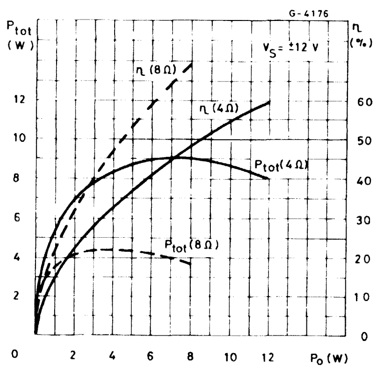


Figure 12 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).

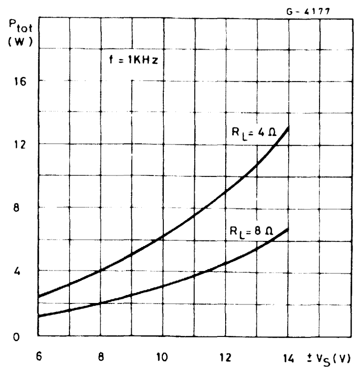


Figure 13 : Application Circuit with Split Power Supply.

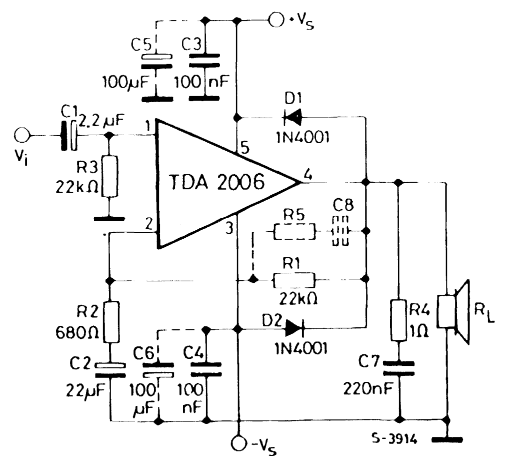


Figure 14 : P.C. Board and Components layout of the Circuit of Fig.13 (1:1 scale).

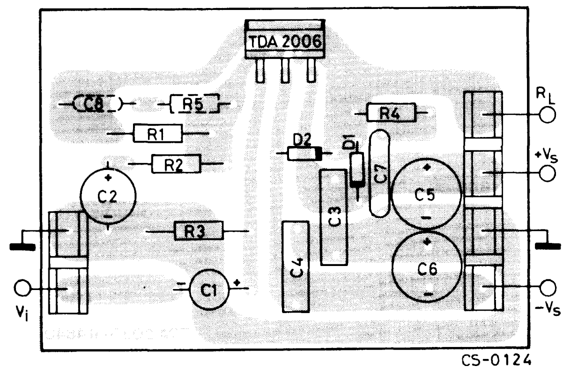


Figure 15 : Application Circuit with Single Power Supply.

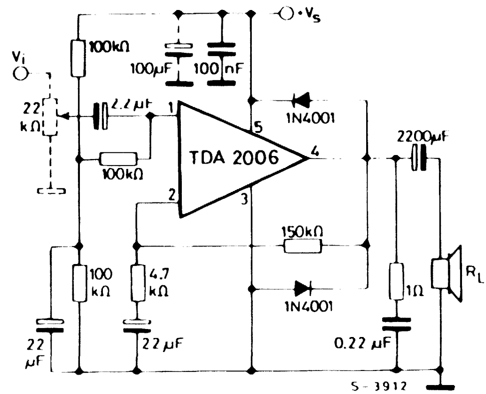


Figure 16 : P.C. Board and Component layout of the Circuit of Fig.15 (1:1 scale)

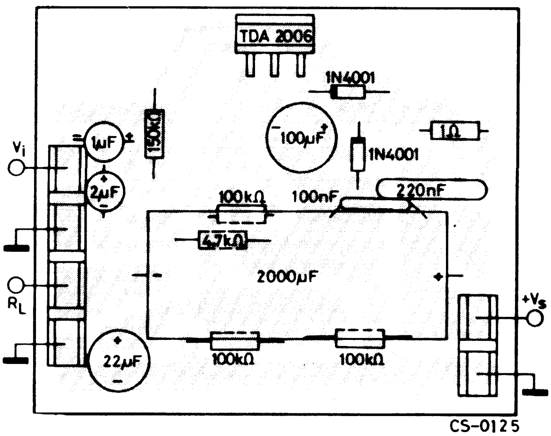
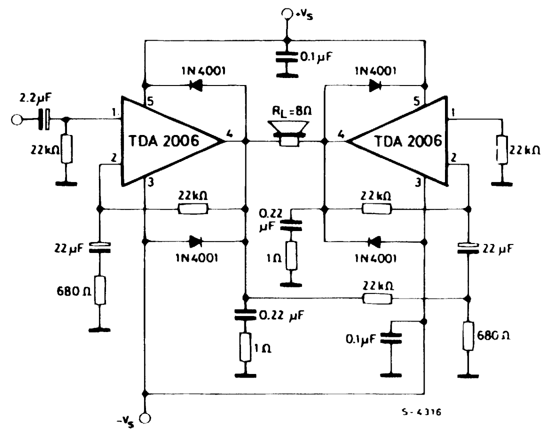


Figure 17 : Bridge Amplifier Configuration with Split Power Supply (P_O = 24W, V_S = ± 12V).



PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout shown in Fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

ASSEMBLY SUGGESTION

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

APPLICATION SUGGESTION

The recommended values of the components are the ones shown on application circuits of Fig. 13. Different values can be used. The following table can help the designers.

Component	Recommanded Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value
R_1	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)
R_2	680 Ω	Closed Loop Gain Setting	Decrease of Gain (*)	Increase pf Gain
R_3	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance
R_4	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads	
R_5	3 R_2	Upper Frequency Cutoff	Poor High Frequencies Attenuation	Danger of Oscillation
C_1	2.2 μF	Input DC Decoupling		Increase of Low Frequencies Cut Off
C_2	22 μF	Inverting Input DC Decoupling		Increase of Low Frequencies Cutoff
C_3C_4	0.1 μF	Supply Voltage by Pass		Danger of Oscillation
C_5C_6	100 μF	Supply Voltage by Pass		Danger of Oscillation
C_7	0.22 μF	Frequency Stability		Danger of Oscillation
C_8	$\frac{1}{2\pi BR_1}$	Upper Frequency Cutoff	Lower Bandwidth	Larger Bandwidth
D_1D_2	1N4001	To Protect the Device Against Output Voltage Spikes.		

(*) Closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage ; hence the output transistors work within their safe operating area (fig. 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

Figure 18 : Maximum Output Current vs. Voltage $V_{CE\,(sat)}$ across each Output Transistor.

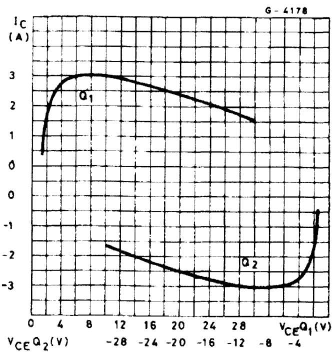
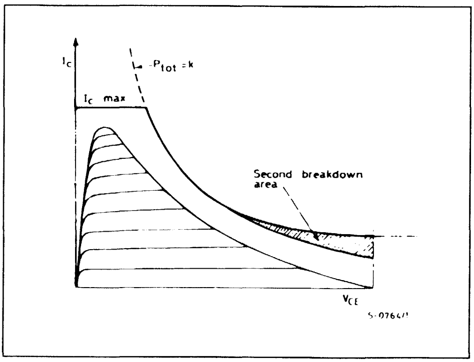


Figure 19 : Safe operating area and Collector Characteristics of the protected Power Transistor.



THERMAL SHUT DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) an overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150 °C.

2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Figure 20 : Output Power and Drain Current vs Case Temperature (R_L = 4Ω)

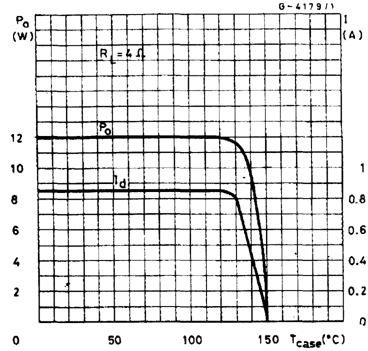
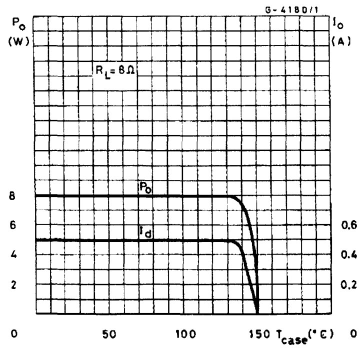


Figure 21 : Output Power and Drain Current vs Case Temperature (R_L = 8Ω)



The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 22 shows the dissipable power as a function of ambient temperature for different thermal resistances.

Figure 22 : Maximum allowable Power Dissipation vs. Ambient Temperature.

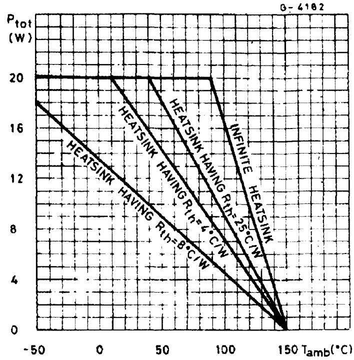
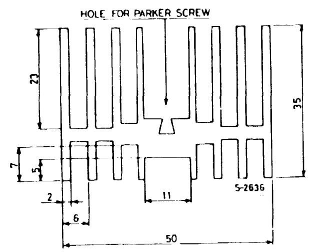


Figure 23 : Exemple of Heatsink.



DIMENSION SUGGESTION

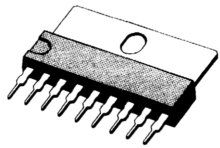
The following table shows the length of the heatsink in fig. 23 for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Lenght of Heatsink (mm)	60	40	30
R_{th} of Heatsink (°C/W)	4.2	6.2	8.3

TDA2007

6 + 6W STEREO AMPLIFIER

- HIGH OUTPUT POWER
- HIGH CURRENT CAPABILITY
- THERMAL OVERLOAD PROTECTION
- SPACE AND COST SAVING : VERY LOW NUMBER OF EXTERNAL COMPONENTS AND SIMPLE MOUNTING THANKS TO THE SIP. 9 PACKAGE



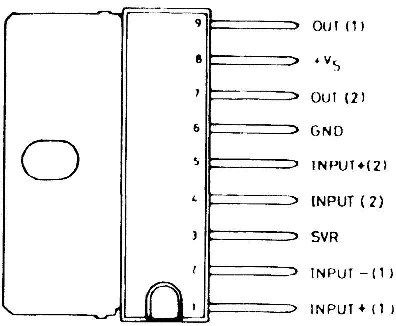
SIP. 9

ORDER CODE : TDA2007

DESCRIPTION

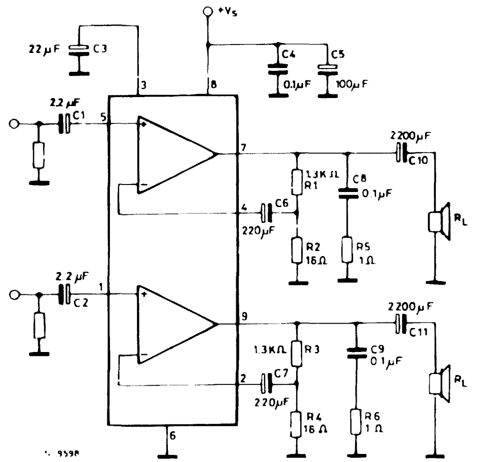
The TDA2007 is a class AB dual Audio power amplifier assembled in single in line 9 pins package, specially designed for stereo application in music centers TV receivers and portable radios.

PIN CONNECTION (top view)

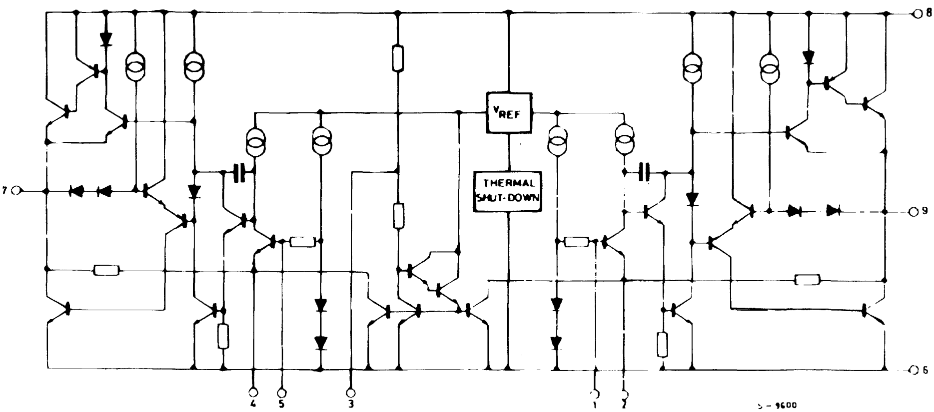


S-9599

STEREO TEST CIRCUIT



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
I_o	Output Peak Current (repetitive f ≥ 20 Hz)	3	A
I_o	Output Peak Current (non repetitive t = 100 μs)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 70 °C	10	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	8	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (refer to the stereo application circuit, T_{amb} = 25 °C, V_s = 18 V, G_v = 36 dB, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			8		26	V
V_o	Quiescent Output Volt.				8.5		V
I_d	Total Quiescent Drain Current				48		mA
P_o	Output Power (each channel)	f = 100 Hz to 16 kHz d = 0.5 % V_s = 18 V R_L = 4 Ω V_s = 22 V R_L = 8 Ω		 5.5 5.5	 6 6		 W W
d	Distortion (each channel)	f = 1 kHz, V_s = 18 V, R_L = 4 Ω P_o = 100 mW to 3 W			0.1		%
		f = 1 kHz, V_s = 22 V, R_L = 8 Ω P_o = 100 mW to 3 W			0.05		%
CT	Cross Talk (°°°)	R_L = ∞	f = 1 kHz	50	60		dB
		R_g = 10 kΩ	f = 10 kHz	40	50		dB
V_i	Input Sat. Volt. (rms)			300			mV
R_i	Input Resistance	f = 1 kHz		70	200		kΩ
f_L	Low Frequency Roll Off (– 3 dB)	R_L = 4 Ω, C10 = C11 = 2200 μF)			40		Hz
f_H	High Frequency Roll Off (– 3 dB)				80		kHz
G_v	Voltage Gain (closed loop)	f = 1 kHz		35.5	36	36.5	dB
Δ G_v	Closed Loop Gain Matching				0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 kΩ (°)			1.5		μV
		R_g = 10 kΩ (°°)			2.5	8	μV
SVR	Supply Voltage Rejection (each channel)	R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V			55		dB
T_j	Thermal Shut-down Junction Temperature				145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized Test Box.

Figure 1 : Stereo Test Circuit (G_V = 36 dB).

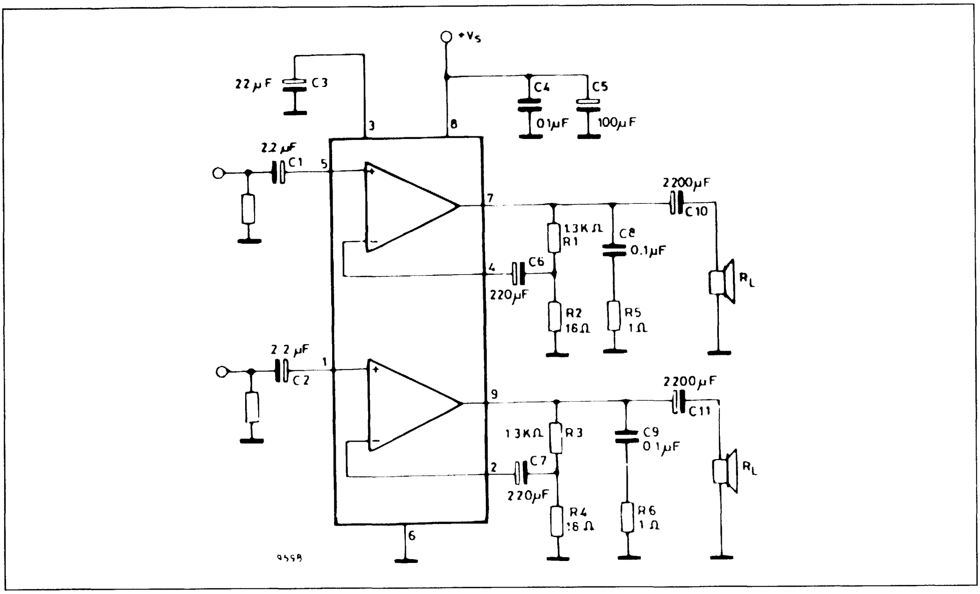


Figure 2 : P.C. Board and Components layout of the Circuit of Fig.1 (1 : 1 scale).

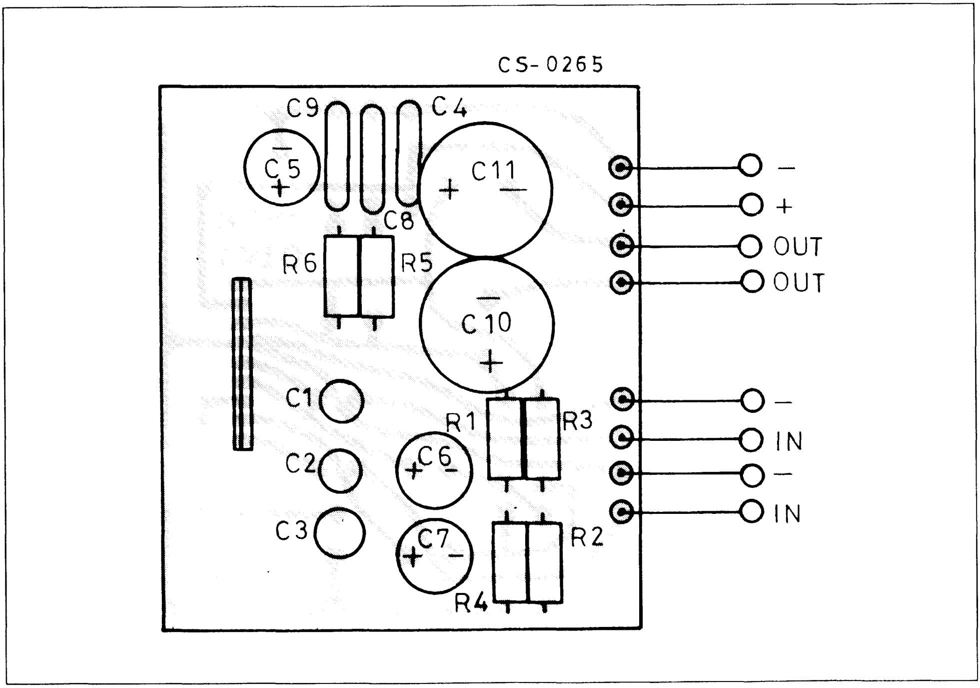


Figure 3 : Output Power vs. Supply Voltage (d = 0.5%).

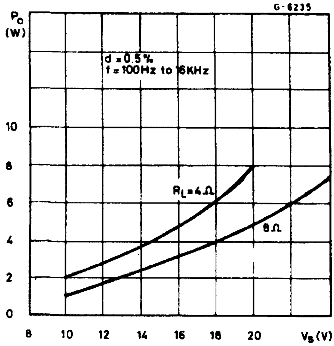


Figure 4 : Output Power vs. Supply Voltage (d = 10%).

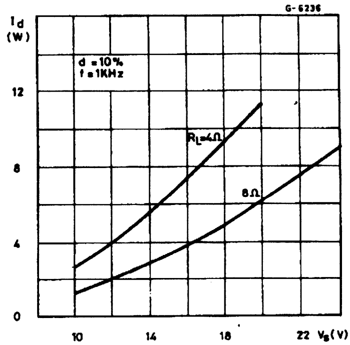


Figure 5 : Quiescent current vs. Supply Voltage.

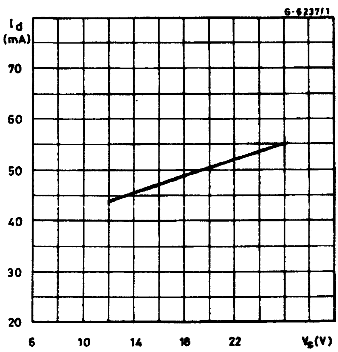


Figure 6 : Supply Voltage Rejection vs. Value of Capacitance C3.

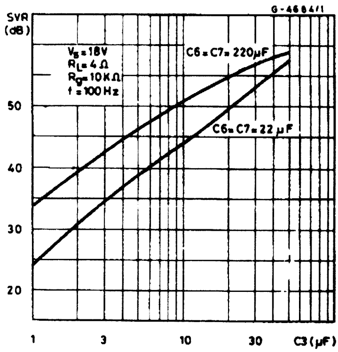


Figure 7 : Supply Voltage Rejection vs. Frequency.

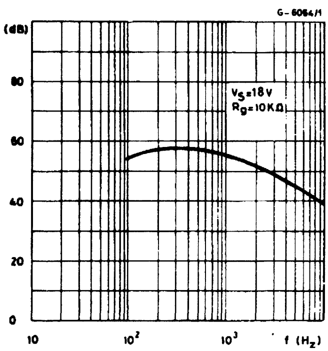


Figure 8 : Total Power Dissipation vs. Output Power.

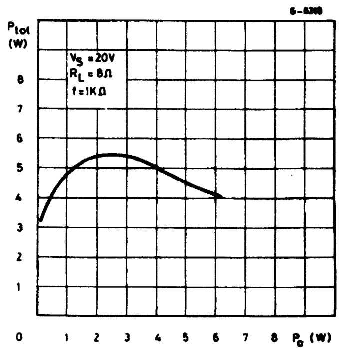


Figure 9 : Cross–talk vs. Frequency.

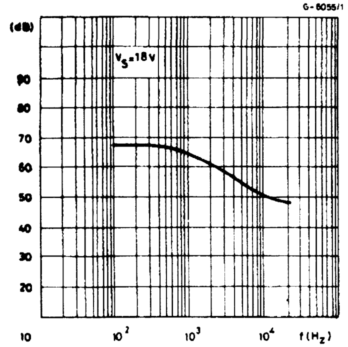


Figure 10 : Simple Short–circuit Protection.

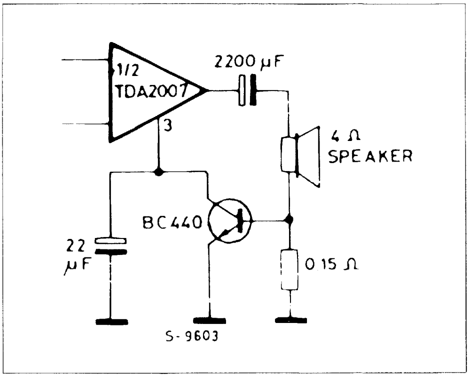
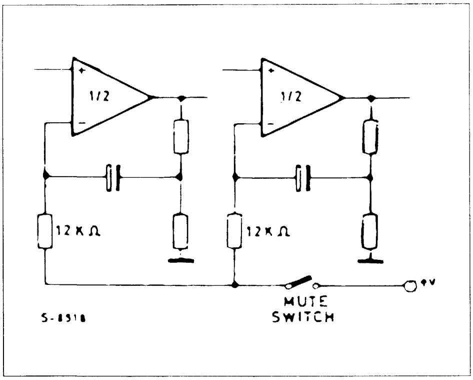
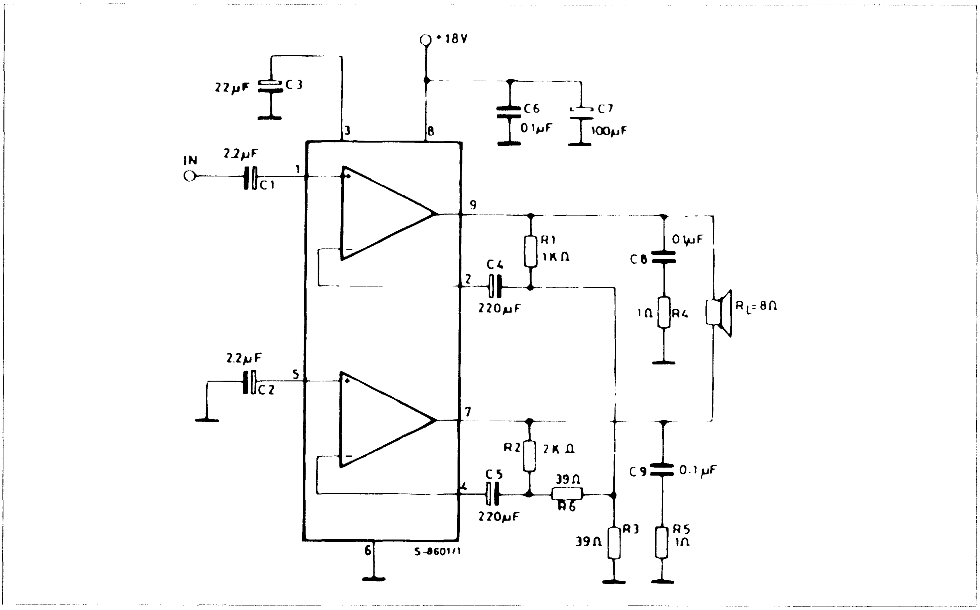


Figure 11 : Example of Muting Circuit.



APPLICATION INFORMATION

Figure 12 : 12 W Bridge Amplifier (d = 0.5%, Gv = 40 dB).



APPLICATION SUGGESTION

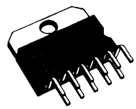
The recommended values of the components are those shown on application circuit of fig.1. Different values can be used ; the following table can help the designer.

Component	Recommanded Value	Purpose	Larger Than	Smaller Than
R1, R3	1.3 kΩ	Close Loop Gain Setting (*)	Increase of Gain	Decrease of Gain
R2 and R4	18 Ω		Decrease of Gain	Increase of Gain
R5 and R6	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Load	
C1 and C2	2.2 µF	Input DC Decoupling	High Turn-on Delay	High Turn-on Pop Higher Low Frequency Cutoff. Increase of Noise
C3	22 µF	Ripple Rejection	Better SVR Increase of the Switch-on Time	Degradation of SVR
C6 and C7	220 µF	Feedback Input DC Decoupling		
C8 and C9	0.1 µF	Frequency Stability		Danger of Oscillation
C10 and C11	1000 µF to 2200 µF	Output DC Decoupling		Higher Low-frequency Cut-off

(*) The closed loop gain must be higher than 26 dB.

10 + 10 W HIGH QUALITY STEREO AMPLIFIER

- HIGH OUTPUT POWER (10 + 10 W min. @ d = 0.5 %)
- HIGH CURRENT CAPABILITY (up to 3.5 A)
- THERMAL OVERLOAD PROTECTION
- SPACE AND COST SAVING : VERY LOW NUMBER OF EXTERNAL COMPONENTS AND SIMPLE MOUNTING THANKS TO THE MULTIWATT ® PACKAGE.



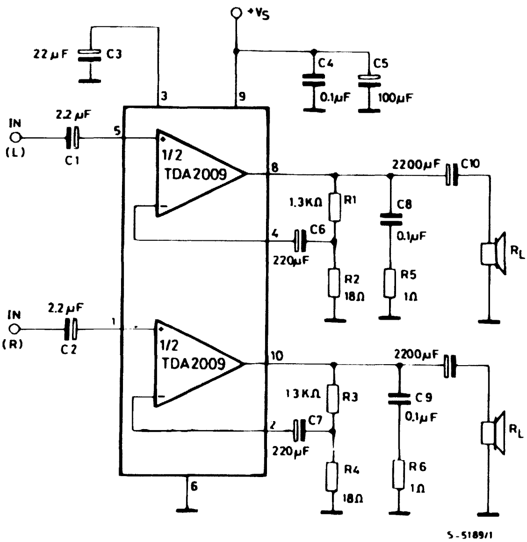
MULTIWATT-11

ORDER CODE : TDA2009

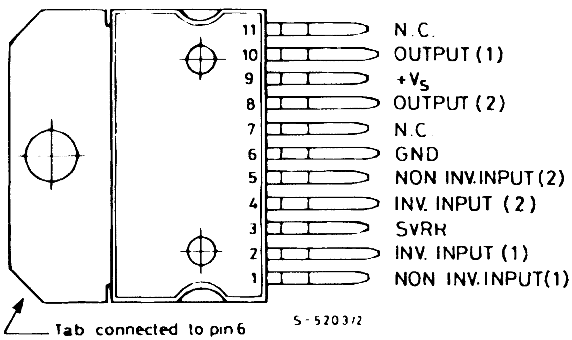
DESCRIPTION

The TDA2009 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt ® package, specially designed for high quality stereo application as Hi-Fi and music centers.

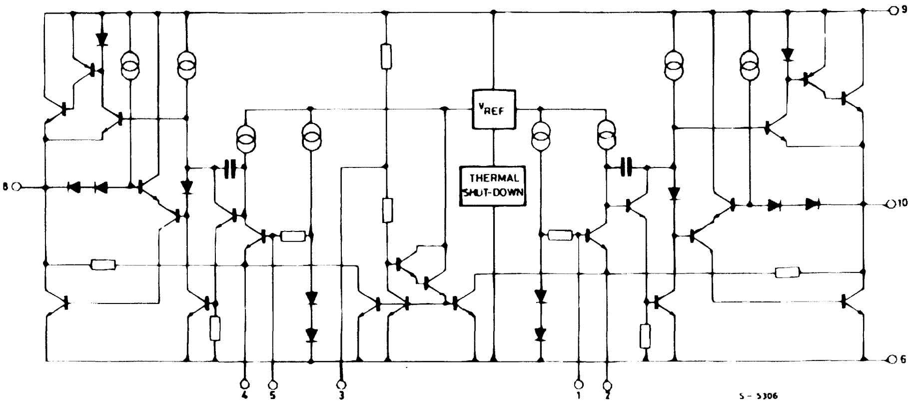
TEST CIRCUIT



PIN CONNECTION (top view)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
I_o	Output Peak Current (repetitive f ≥ 20 Hz)	3.5	A
I_o	Output Peak Current (non repetitive, t = 100 µs)	4.5	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the stereo application circuit, T_{amb} = 25 °C, V_s = 23 V, G_v = 36 dB, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		28	V
V_o	Quiescent Output Voltage	V_s = 23 V		11		V
I_d	Total Quiescent Drain Current	V_s = 23 V		55	120	mA
P_o	Output Power (each channel)	f = 50 Hz to 16 KHz d = 0.5 % V_s = 23 V R_L = 4 Ω R_L = 8 Ω V_s = 18 V R_L = 4 Ω R_L = 8 Ω	 10 5.5 	 11 6.5 6.5 4		 W W W W
d	Distortion (each channel)	f = 1 KHz V_s = 23 V R_L = 4 Ω P_o = 100 mW to 8 W V_s = 23 V R_L = 8 Ω P_o = 100 mW to 3 W		 0.05 0.05		%
CT	Cross Talk (°°°)	R_L = ∞, R_g = 10 KΩ; f = 1 KHz	50	65		dB
		R_L = ∞, R_g = 10 KΩ; f = 10 KHz	40	50		dB
V_i	Input Saturation Voltage (rms)		300			mV
R_i	Input Resistance	f = 1 KHz Non Inverting Input	70	200		KΩ
f_L	Low Frequency Roll off (– 3 dB)	R_L = 4 Ω		20		Hz
f_H	High Frenquency Roll off (– 3dB)	R_L = 4 Ω		80		KHz
G_v	Voltage Gain (closed loop)	f = 1 KHz	35.5	36	36.5	dB
ΔG_v	Closed Loop Gain Matching			0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 KΩ (°)		1.5		µV
		R_g = 10 KΩ (°°)		2.5	8	µV
SVR	Supply Voltage Rejection (each channel)	R_g = 10 KΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V	43	55		dB
T_J	Thermal Shut-down Junction Temperature			145		°C

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Figure 1 : Test and Application Circuit (Gv = 36 dB).

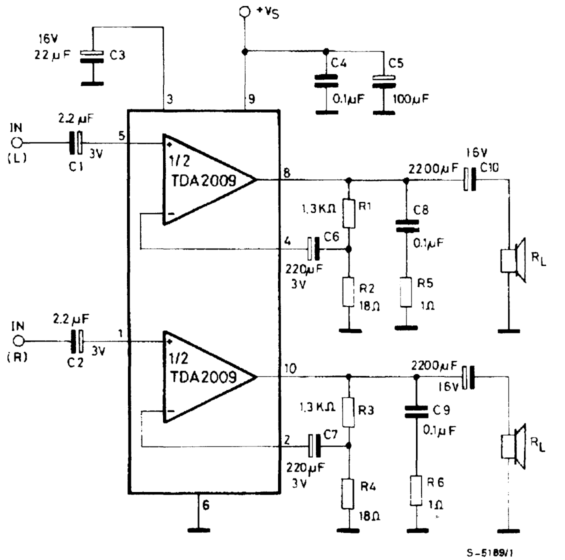


Figure 2 : P.C. Board and Components Layout of the Circuit of Fig. 1 (1 : 1 scale).

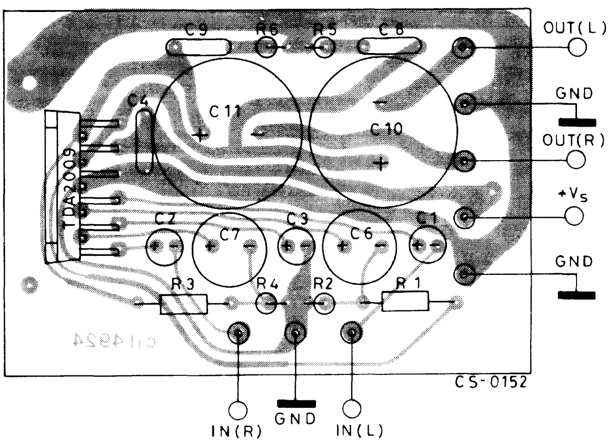


Figure 3 : Output Power vs. Supply Voltage.

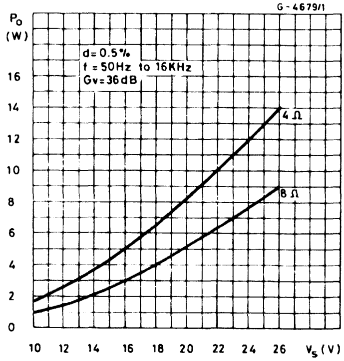


Figure 4 : Output Power vs. Supply Voltage.

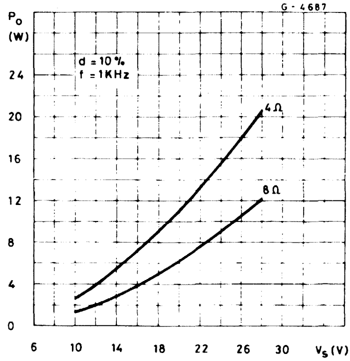


Figure 5 : Distortion vs. Output Power.

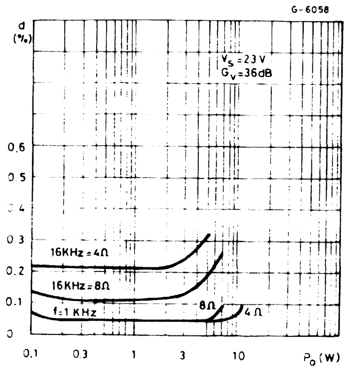


Figure 6 : Distortion vs. Frequency.

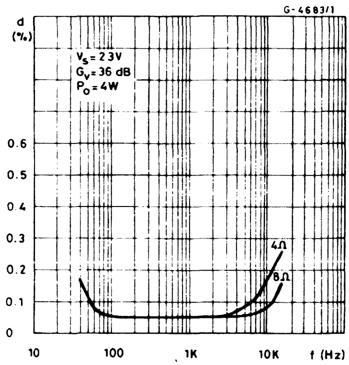


Figure 7 : Quiescent Current vs. Supply Voltage.

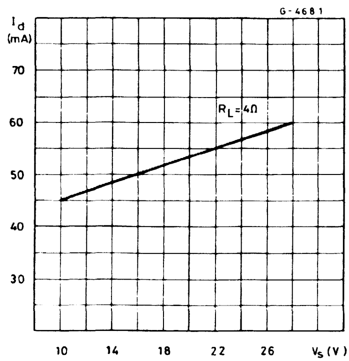


Figure 8 : Supply Voltage Rejection vs. Value of Capacitor C3.

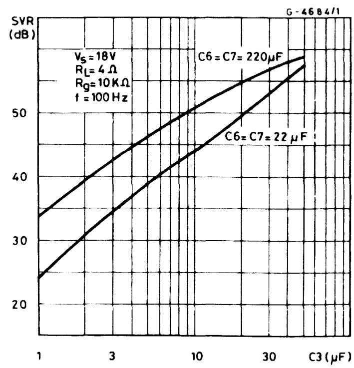


Figure 9 : Supply Voltage Rejection vs. Frequency.

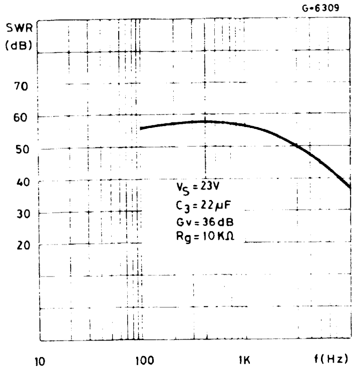


Figure 10 : Total Power Dissipation and Efficiency vs. Output Power.

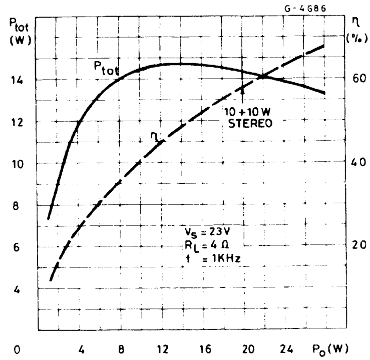


Figure 11 : Total Power Dissipation and Efficiency vs. Output Power.

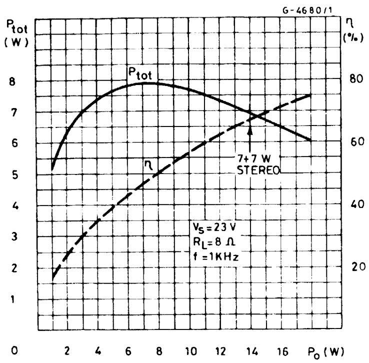


Figure 12 : Cross-talk vs. Frequency.

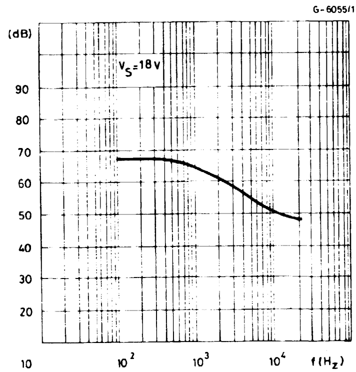


Figure 13 : Output Power vs. Closed Loop Gain.

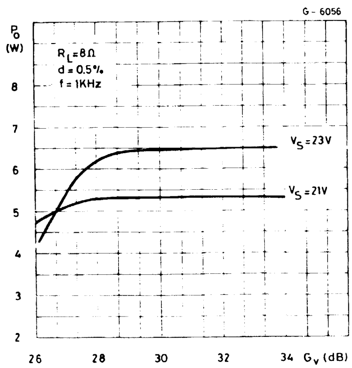
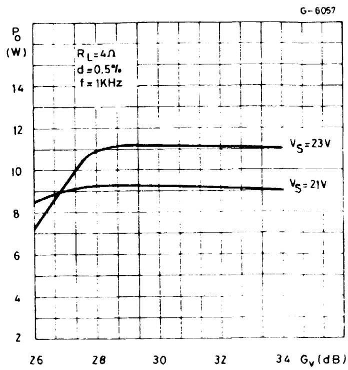


Figure 14 : Output Power vs. Closed Loop Gain.



APPLICATION INFORMATION

Figure 15 : Simple Short-circuit Protection.

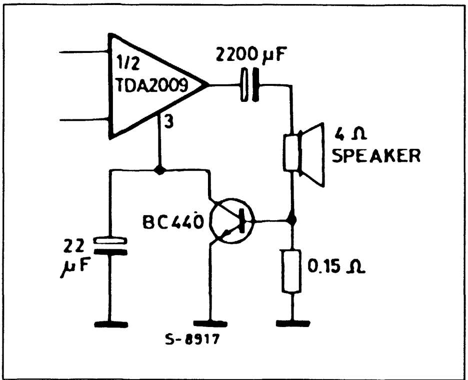


Figure 16 : Example of Muting Circuit.

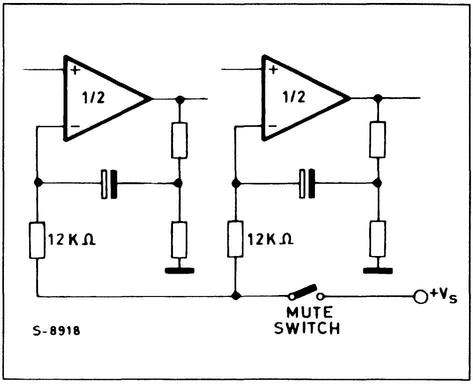
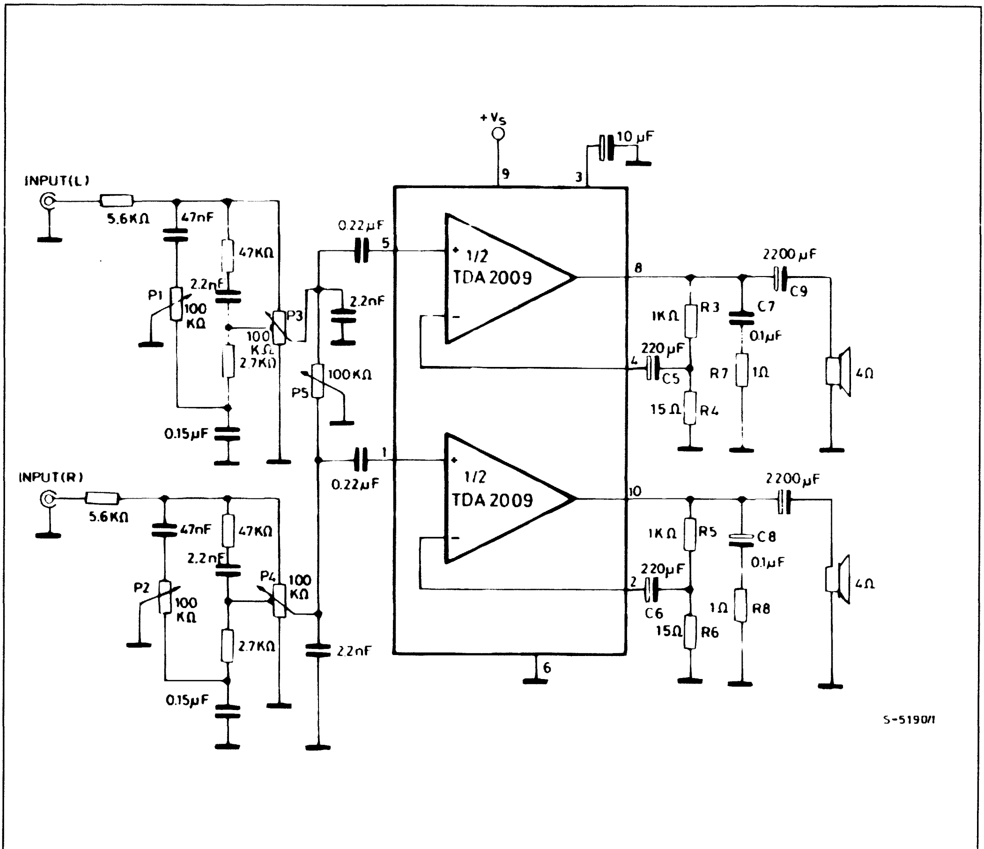


Figure 17 : 10 + 10 W Stereo Amplifier with Tone Balance and Loudness Control.



APPLICATION INFORMATION

Figure 18 : Tone Control Response (circuit of fig. 17).

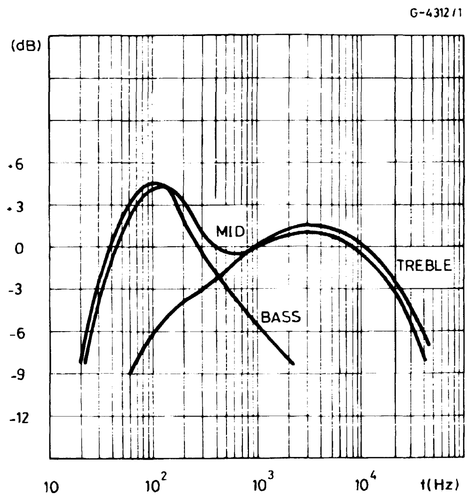
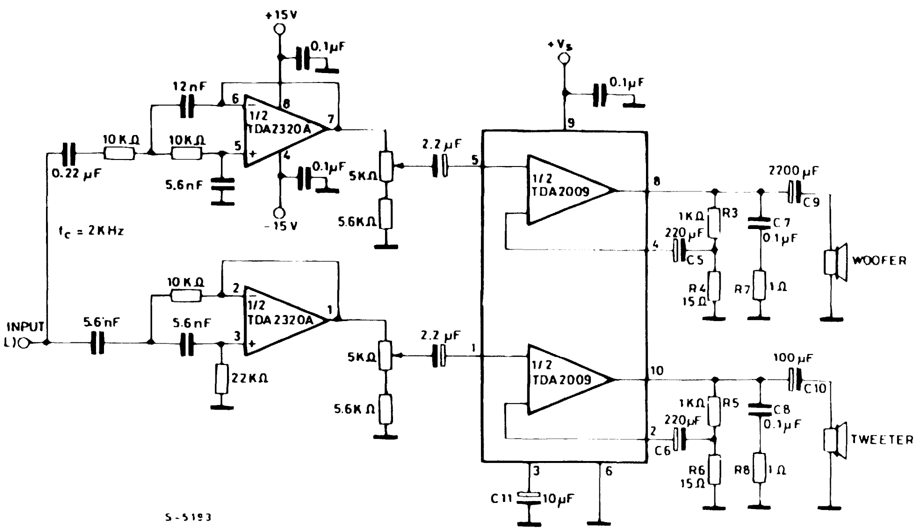


Figure 19 : High Quality 10 + 20 W Two Way Amplifier for Stereo Music Center (one channel only).



APPLICATION INFORMATION (continued)

Figure 20 : 18 W Bridge Amplifier (d = 0.5 %, G_v = 40 dB).

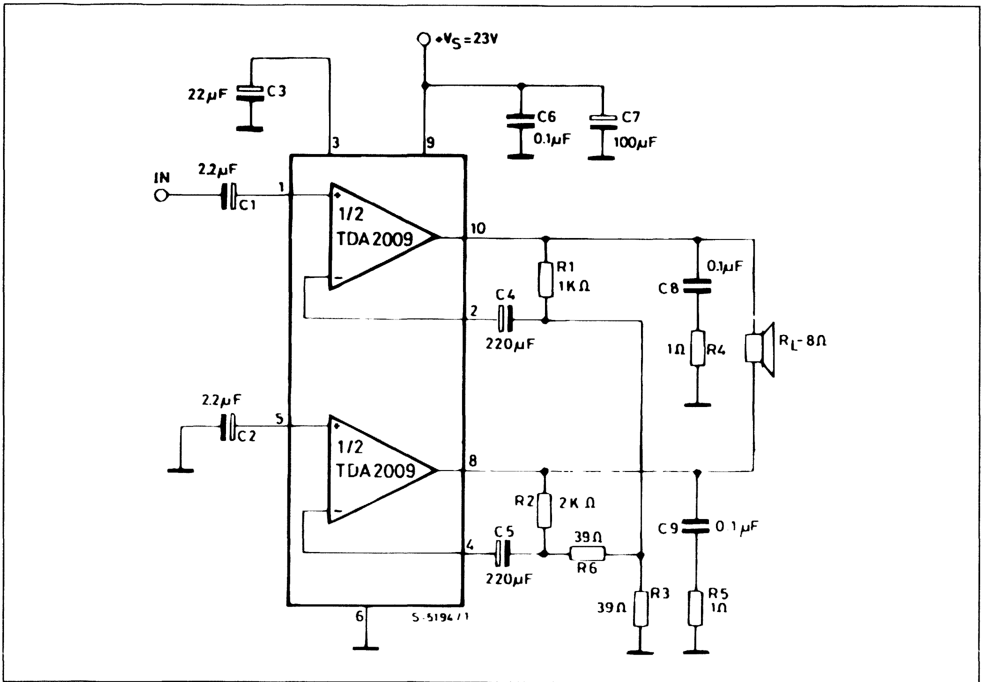
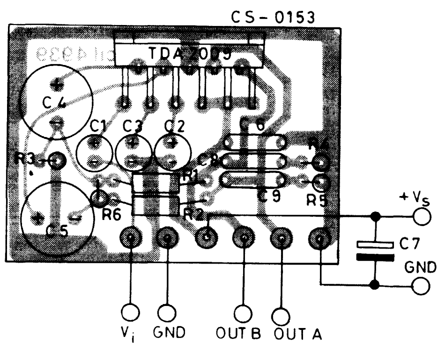


Figure 21 : P.C. Board and Components Layout of the Circuit of Fig. 20 (1 : 1 scale).



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used ; the following table can help the designer.

Component	Recomm. Value	Purpose	Larger Than	Smaller Than
R1 and R3	1.2 KΩ	Close Loop Gain Setting (*)	Increase of Gain	Decrease of Gain
R2 and R4	18 Ω		Decrease of Gain	Increase of Gain
R5 and R6	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Load	
C1 and C2	2.2 µF	Input DC Decoupling	High Turn-on Delay	High Turn-on Pop Higher Low Frequency Cutoff. Increase of Noise
C3	22 µF	Ripple Rejection	Better SVR. Increase of the Switch-on Time	Degradation of SVR
C6 and C7	220 µF	Feedback Input DC Decoupling		
C8 and C9	0.1 µF	Frenquency Stability		Danger of Oscillation
C10 and C11	1000 µF to 2200 µF	Output DC Decoupling		Higher Low-frequency Cut-off

(*) The closed loop gain must be higher than 26 dB

BUILT-IN PROTECTION SYSTEMS

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1)an overload on the output (even it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuits.

There is no device damage in the case of excessive junction temperature : all that happens is that P_o (and therefore P_{tot}) and I_d are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 22 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

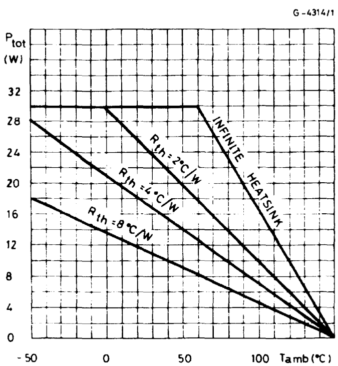
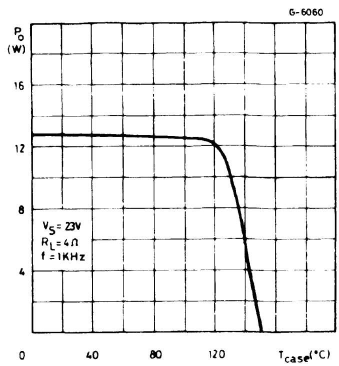


Figure 23 : Output Power vs. Case Temperature.



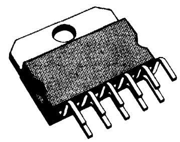
MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the MULTIWATT ® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

10 + 10 W SHORT CIRCUIT PROTECTED STEREO AMPLIFIER

- HIGH OUTPUT POWER (10 + 10 W MIN. @ D = 1 %)
- HIGH CURRENT CAPABILITY (UP TO 3.5 A)
- AC SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION
- SPACE AND COST SAVING : VERY LOW NUMBER OF EXTERNAL COMPONENTS AND SIMPLE MOUNTING THANKS TO THE MULTIWATT ® PACKAGE



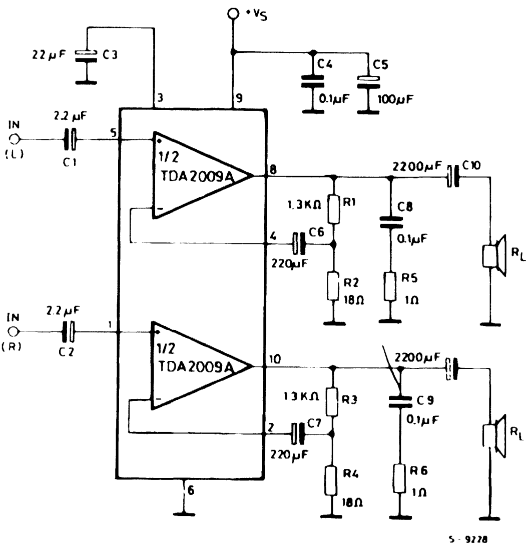
MULTIWATT-11

ORDER CODE : TDA2009A

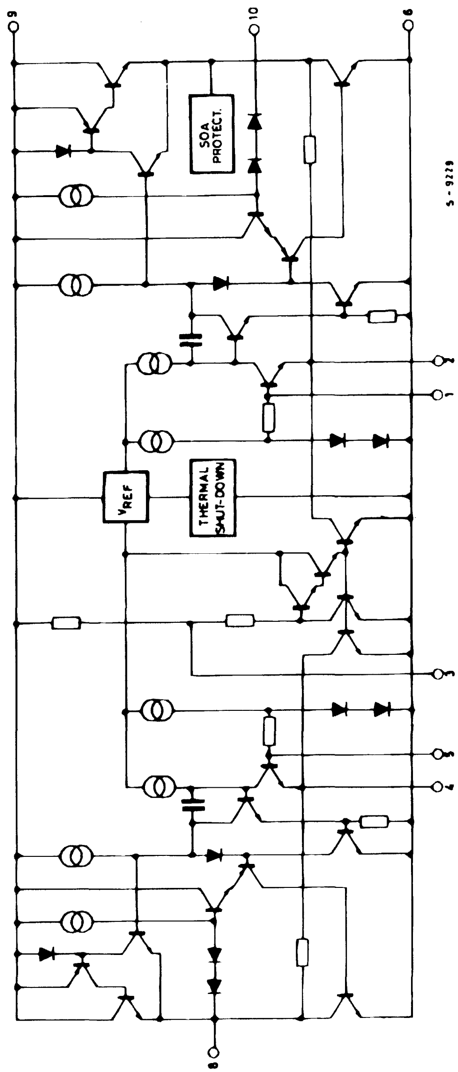
DESCRIPTION

The TDA2009A is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt ® package, specially designed for high quality stereo application as Hi-Fi and music centers. Its main features are :

TEST CIRCUIT



SCHEMATIC DIAGRAM



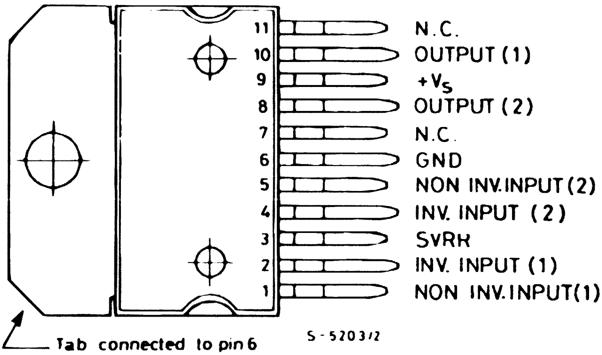
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
I_o	Output Peak Current (repetitive f ≥ 20 Hz)	3.5	A
I_o	Output Peak Current (non repetitive, t = 100 μs)	4.5	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	3	°C/W

PIN CONNECTION (top view)



ELECTRICAL CHARACTERISTICS (refer to the stereo application circuit, T_{amb} = 25 °C, V_s = 24 V, G_v = 36 dB, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		8		28	V
V_o	Quiescent Output Voltage	V_s = 24 V		11.5		V
I_d	Total Quiescent Drain Current	V_s = 24 V		60	120	mA
P_o	Output Power (each channel)	d = 1 % V_s = 24 V f = 1 KHz R_L = 4 Ω R_L = 8 Ω		12.5 7		W W
		f = 40 Hz to 12.5 KHz R_L = 4 Ω R_L = 8 Ω	10 5			W W
		V_s = 18 V f = 1 KHz R_L = 4 Ω R_L = 8 Ω		7 4		W W
d	Distortion (each channel)	f = 1 KHz V_s = 24 V P_o = 0.1 to 7 W R_L = 4 Ω P_o = 0.1 to 3.5 W R_L = 8 Ω		0.2 0.1		% %
		V_s = 18 V P_o = 0.1 to 5 W R_L = 4 Ω P_o = 0.1 to 2.5 W R_L = 8 Ω		0.2 0.1		% %
CT	Cross Talk (°°°)	R_L = ∞, R_g = 10 KΩ; f = 1 KHz		60		dB
		R_L = ∞, R_g = 10 KΩ; f = 10 KHz		50		dB
V_i	Input Saturation Voltage (rms)		300			mV
R_i	Input Resistance	f = 1 KHz Non Inverting Input	70	200		KΩ
f_L	Low Frequency Roll off (– 3 dB)	R_L = 4 Ω		20		Hz
f_H	High Frequency Roll off (– 3dB)	R_L = 4 Ω		80		KHz
G_v	Voltage Gain (closed loop)	f = 1 KHz	35.5	36	36.5	dB
ΔG_v	Closed Loop Gain Matching			0.5		dB
e_N	Total Input Noise Voltage	R_g = 10 KΩ (°)		1.5		µV
		R_g = 10 KΩ (°°)		2.5	8	µV
SVR	Supply Voltage Rejection (each channel)	R_g = 10 KΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V		55		dB
T_J	Thermal Shut-down Junction Temperature			145		°C

(°) Curve A (°°) 22 Hz to 22 KHz (°°°)Optimized test box.

Figure 1 : Test and Application Circuit (Gv = 36 dB).

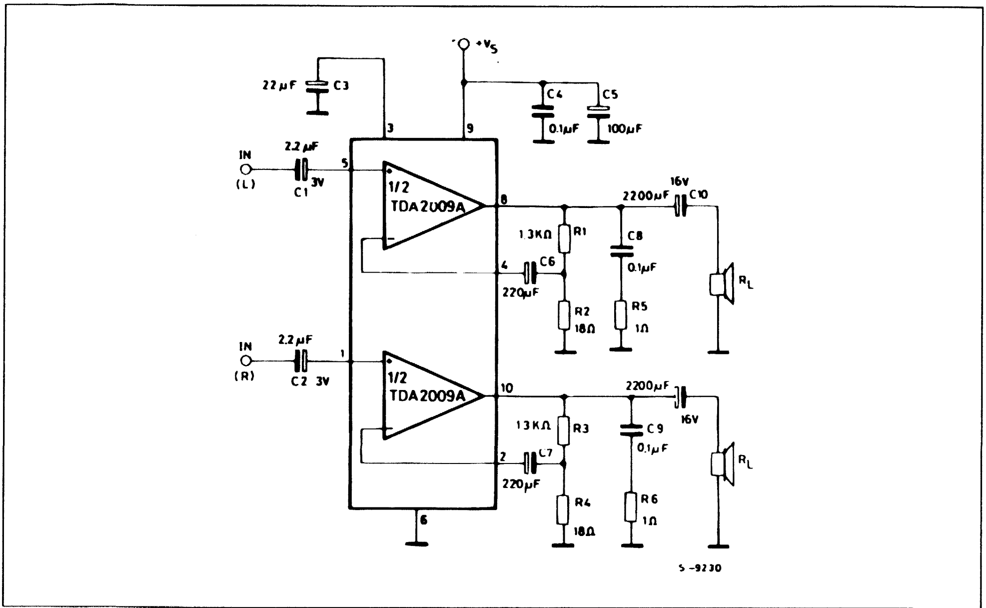


Figure 2 : P.C. Board and Components Layout of the circuit of Fig. 1 (1 : 1 scale).

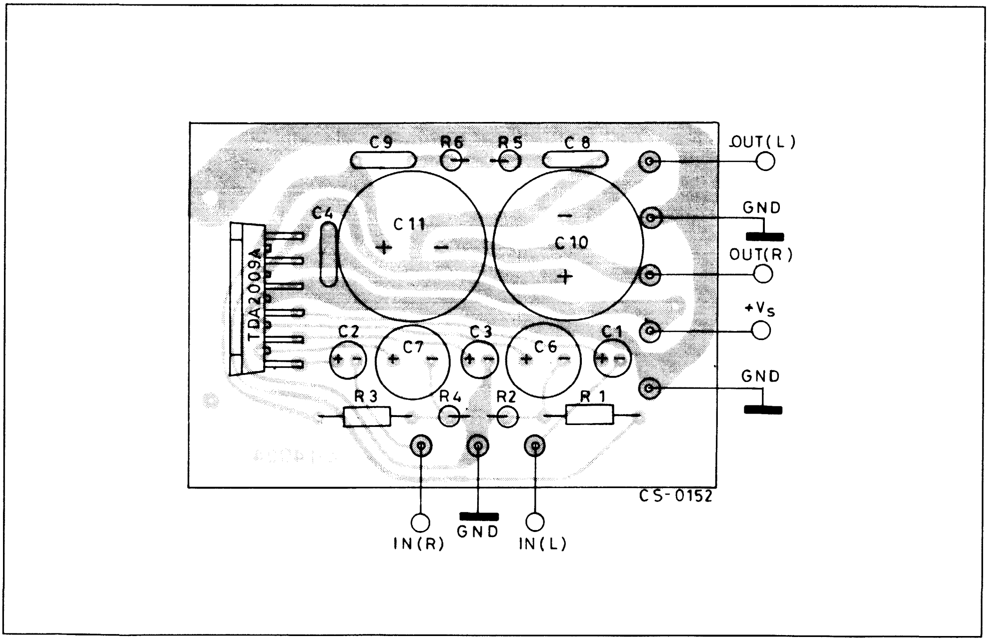


Figure 3 : Output Power vs. Supply Voltage.

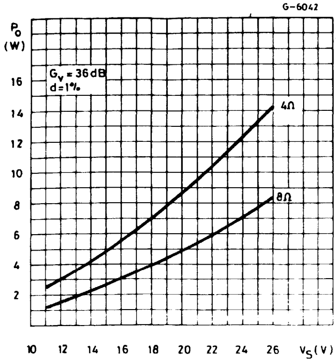


Figure 4 : Output Power vs. Supply Voltage.

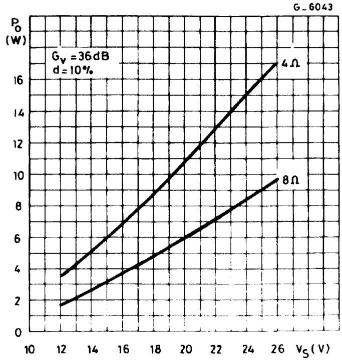


Figure 5 : Distortion vs. Output Power.

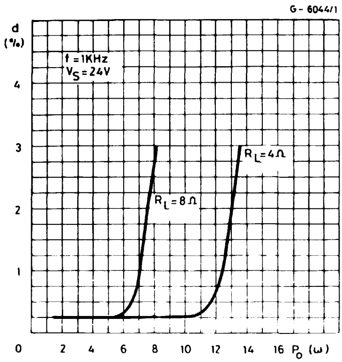


Figure 6 : Distortion vs. Frequency.

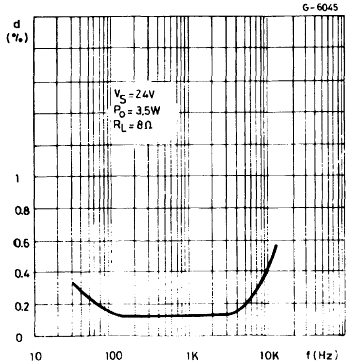


Figure 7 : Distortion vs. Frequency.

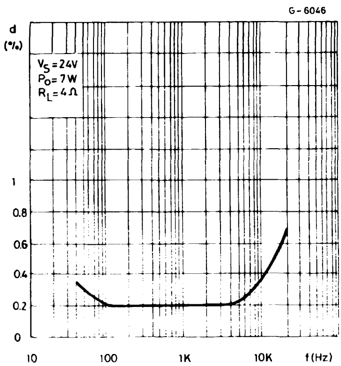


Figure 8 : Quiescent Current vs. Supply Voltage.

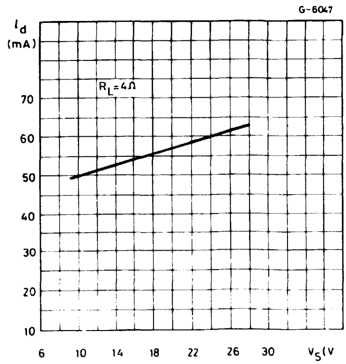


Figure 9 : Supply Voltage Rejection vs. Frequency.

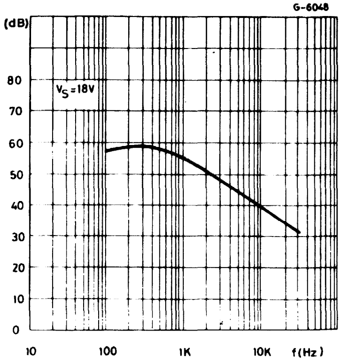


Figure 10 : Total Power Dissipation and Efficiency vs. Output Power.

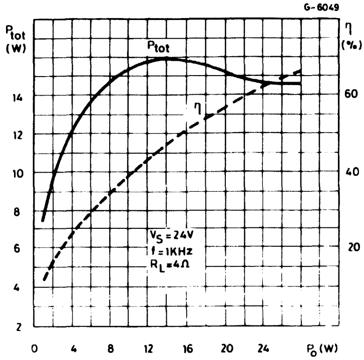
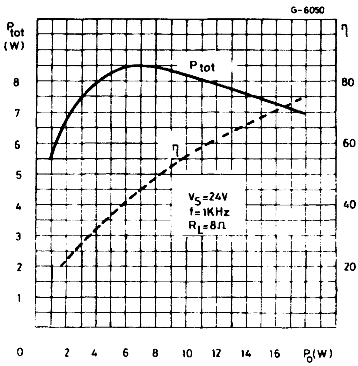
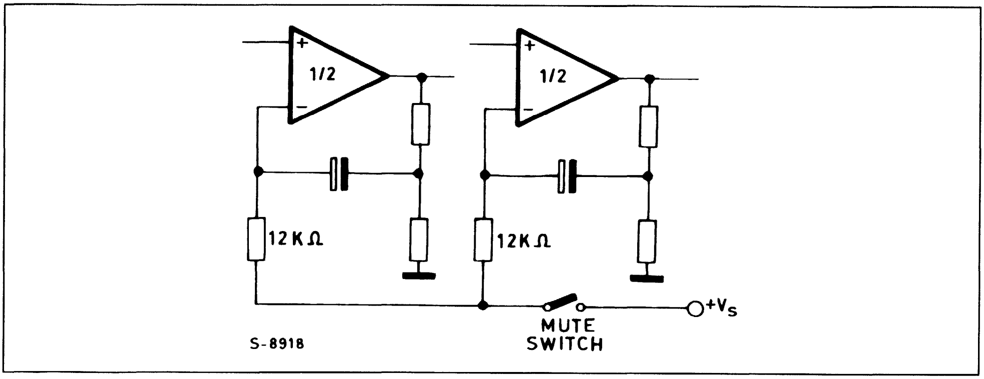


Figure 11 : Total Power Dissipation and Efficiency vs. Output Power .



APPLICATION INFORMATION

Figure 12 : Example of Muting Circuit.



APPLICATION INFORMATION (continued)

Figure 13 : 10 W + 10 W Stereo Amplifier with Tone Balance and Loudness Control.

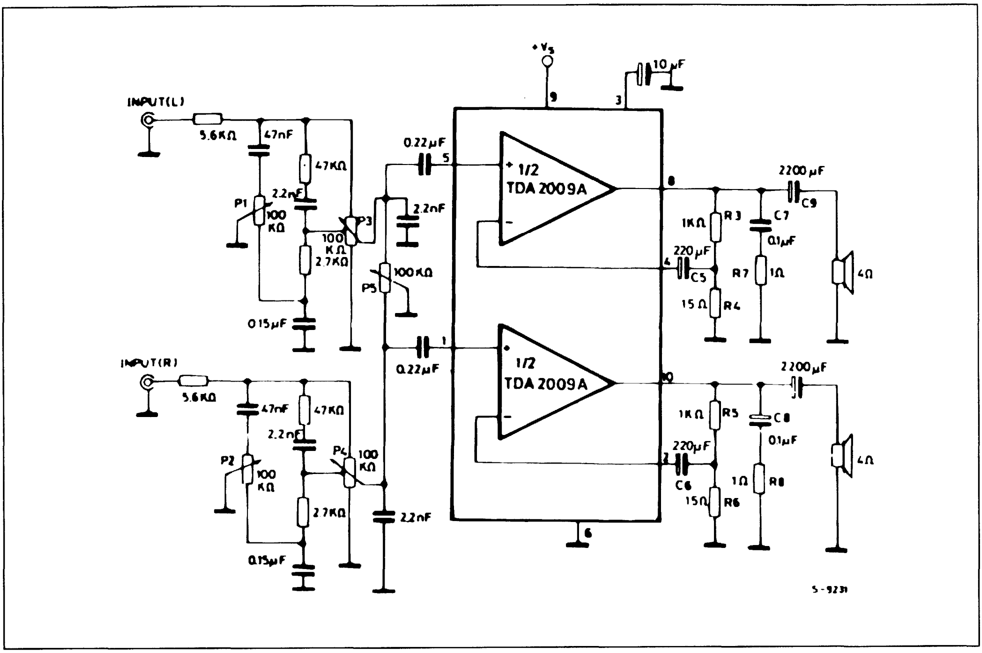
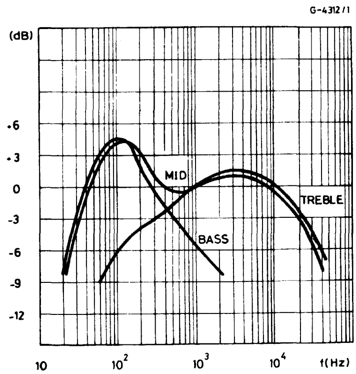


Figure 14 : Tone Control Response (circuit of fig. 13).



APPLICATION INFORMATION (continued)

Figure 15 : High Quality 20 + 20 W Two Way Amplifier for Stereo Music Center (one channel only).

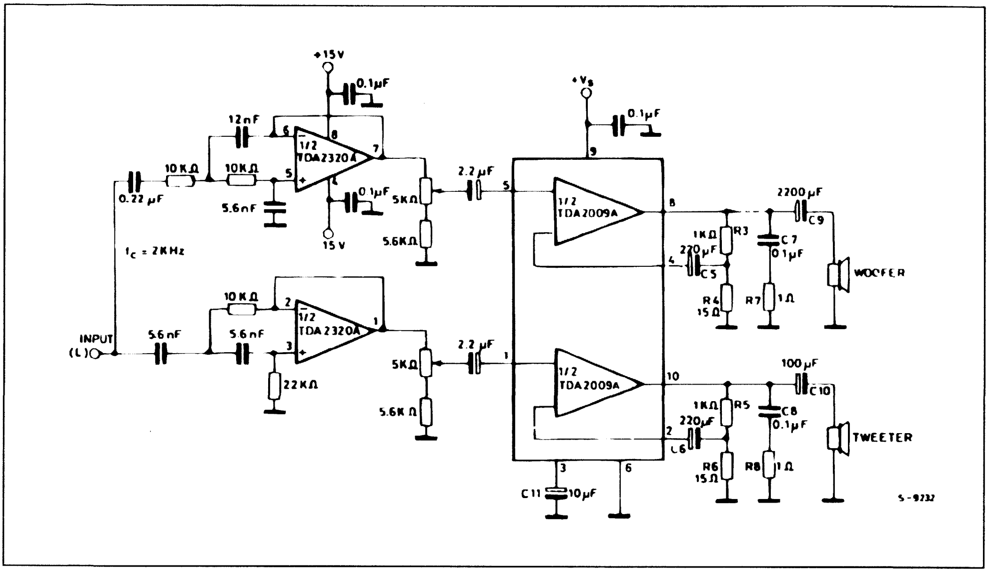


Figure 16 : 18 W Bridge Amplifier (d = 1 %, G_v = 40 dB).

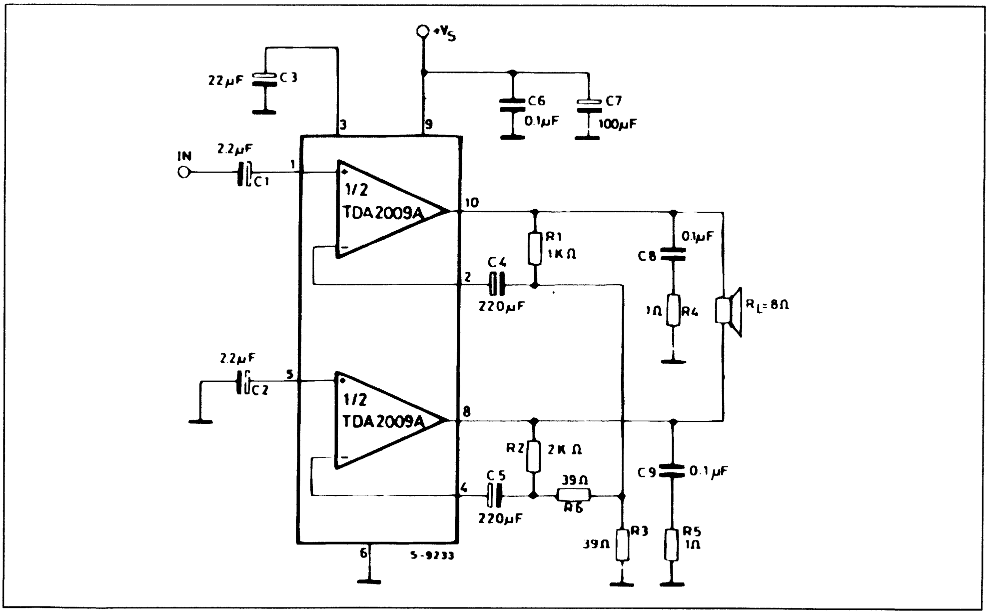
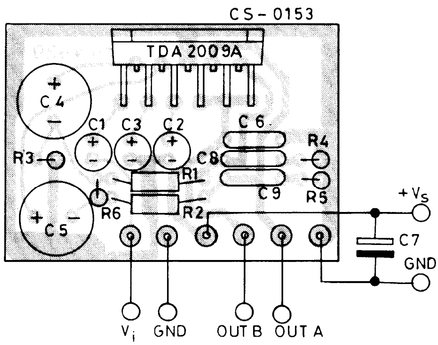


Figure 17 : P.C. Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used ; the following table can help the designer.

Component	Recomm. Value	Purpose	Larger than	Smaller than
R1 and R3	1.2 KΩ	Close Loop Gain Setting (*)	Increase of Gain	Decrease of Gain
R2 and R4	18 KΩ		Decrease of Gain	Increase of Gain
R5 and R6	1 Ω	Frequency Stability	Danger of Oscillation at High Frequency with Inductive Load	
C1 and C2	2.2 µF	Input DC Decoupling	High Turn-on Delay	High Turn-on Pop Higher Low Frequency Cutoff. Increase of Noise
C3	22 µF	Ripple Rejection	Better SVR. Increase of the Switch-on Time	Degradation of SVR
C6 and C7	220 µF	Feedback Input DC Decoupling		
C8 and C9	0.1 µF	Frenquency Stability		Danger of Oscillation
C10 and C11	1000 µF to 2200 µF	Output DC Decoupling		Higher Low-frequency Cut-off

(*) The closed loop gain must be higher than 26 dB

BUILD-IN PROTECTION SYSTEMS

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1)an averload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.

2)the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature : all that happens is that P_o (and therefore P_{tot}) and I_o are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 18 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Short circuit (AC Conditions). The TDA2009A can withstand an accidental short circuit from the output and ground made by a wrong connection during normal play operation.

Figure 18 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

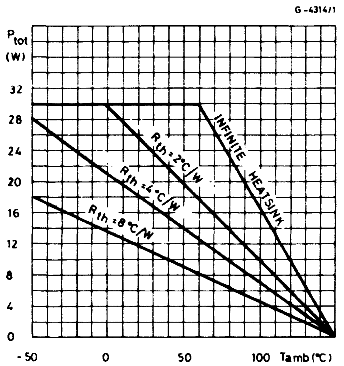


Figure 19 : Output Power vs. Case Temperature.

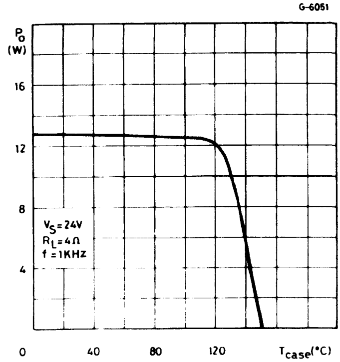
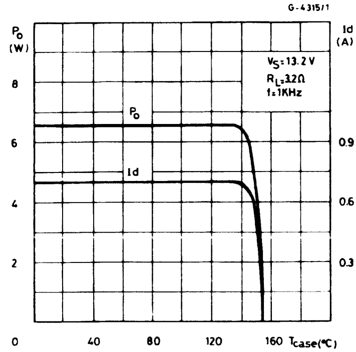


Figure 20 : Output Power and Drain Current vs. Case Temperature.



MOUNTING INSTRUCTIONS

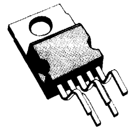
The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the MULTIWATT ® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

14W HI-FI AUDIO AMPLIFIER

DESCRIPTION

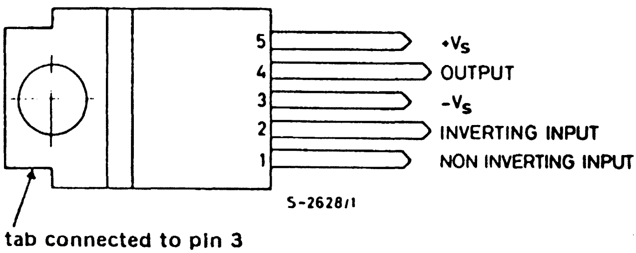
The TDA2030 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at 14V/4Ω ; at ± 14V the guaranteed output power is 12W on a 4 load and 8W on a 8Ω (DIN45500). The TDA2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included.



PENTAWATT

ORDER CODES : TDA2030H
TDA2030V

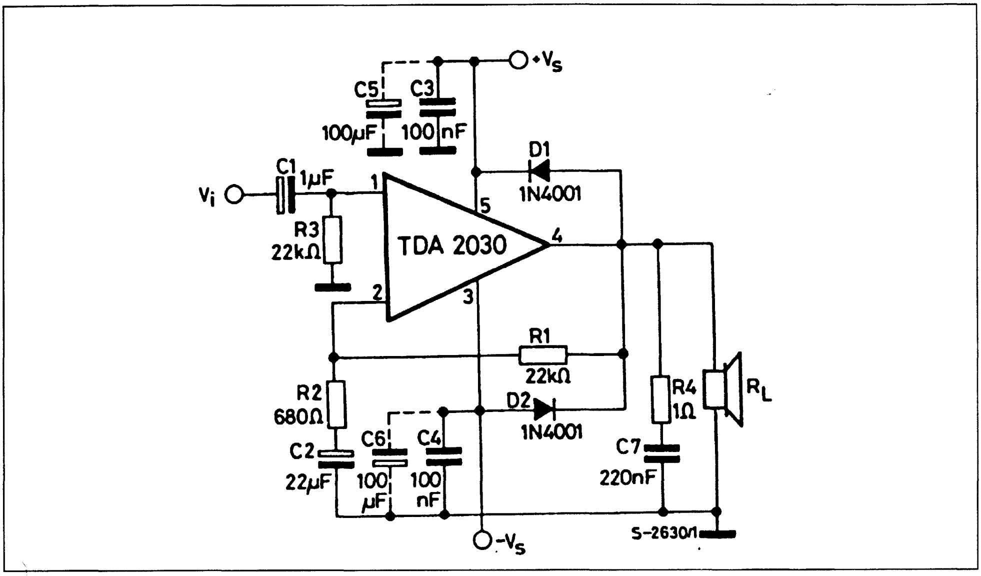
CONNECTION DIAGRAM (top view)



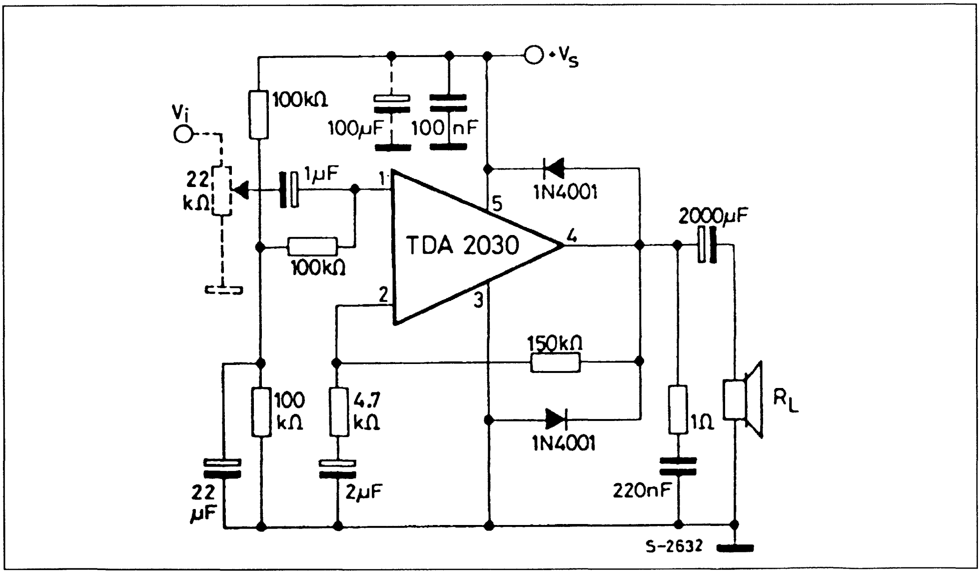
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 18	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 15	V
I_o	Output Peak Current (internally limited)	3.5	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TEST CIRCUIT



TYPICAL APPLICATION



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = ± 14V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 18	V
I_d	Quiescent Drain Current	V_s = ± 18 V		40	60	mA
I_b	Input Bias Current			0.2	2	μA
V_{os}	Input Offset Voltage			± 2	± 20	mV
I_{os}	Input Offset Current			± 20	± 200	nA
P_o	Output Power	d = 0.5 % Gv = 30 dB f = 40 to 15 000 Hz R_L = 4 Ω R_L = 8 Ω	 12 8	 14 9		 W W
		d = 10 % G_v = 30 dB f = 1 kHz R_L = 4 Ω R_L = 8 Ω		 18 11		 W W
d	Distortion	P_o = 0.1 to 12 W R_L = 4 Ω G_v = 30 dB f = 40 to 15 000 Hz		 0.2	 0.5	 %
		P_o = 0.1 to 8 W R_L = 8 Ω G_v = 30 dB f = 40 to 15 000 Hz		 0.1	 0.5	 %
B	Power Bandwidth (– 3 dB)	G_v = 30 dB P_o = 12 W R_L = 4 Ω	10 to 140 000			Hz
R_i	Input Resistance (pin 1)		0.5	5		MΩ
G_v	Voltage Gain (open loop)			90		dB
G_v	Voltage Gain (closed loop)	f = 1 kHz	29.5	30	30.5	dB
e_N	Input Noise Voltage	B = 22 Hz to 22 kHz		3	10	μV
i_N	Input Noise Current			80	200	pA
SVR	Supply Voltage Rejection	R_L = 4 Ω G_v = 30 dB R_g = 22 Ω V_{ripple} = 0.5 V_{eff} f_{ripple} = 100 Hz	40	50		dB
I_d	Drain Current	P_o = 14 W R_L = 4 Ω P_o = 9 W R_L = 8 Ω		900 500		mA mA
T_j	Thermal Shut-down Junction Temperature			145		°C

Figure 1 : Output Power vs. Supply Voltage.

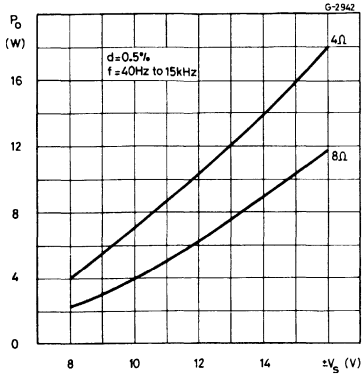


Figure 2 : Output Power vs. Supply Voltage.

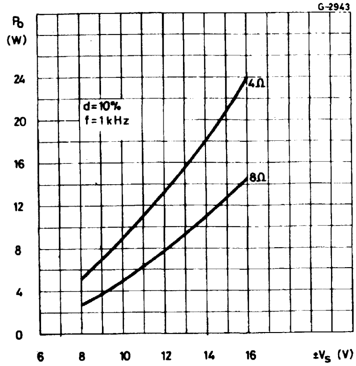


Figure 3 : Distorsion vs. Output Power.

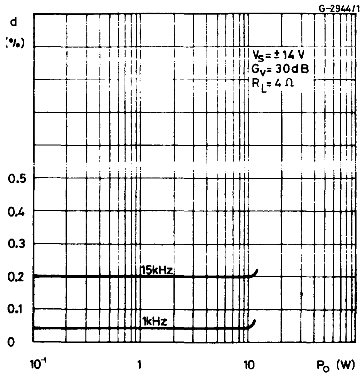


Figure 4 : Distorsion vs. Output Power.

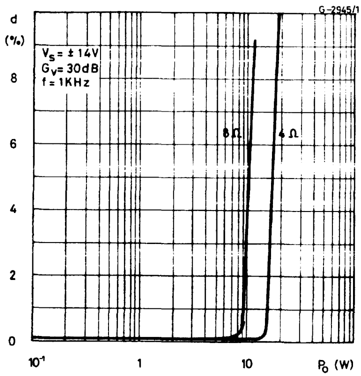


Figure 5 : Distorsion vs. Output Power.

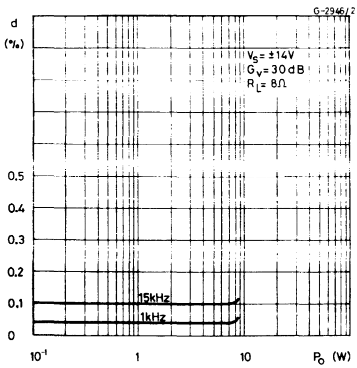


Figure 6 : Distorsion vs. Frequency.

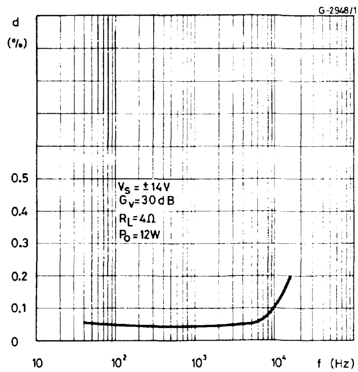


Figure 7 : Distorsion vs. Frequency.

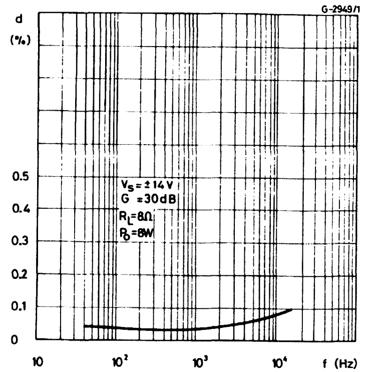


Figure 8 : Frequency Response with Different Values of the Rollof Capacitor C8 (see fig. 13).

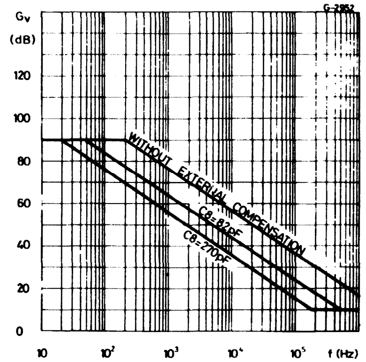


Figure 9 : Quiescent Current vs. Supply Voltage.

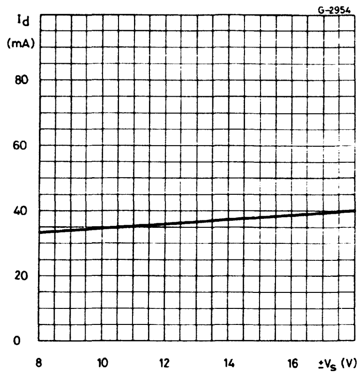


Figure 10 : Supply Voltage Rejection vs. Voltage Gain.

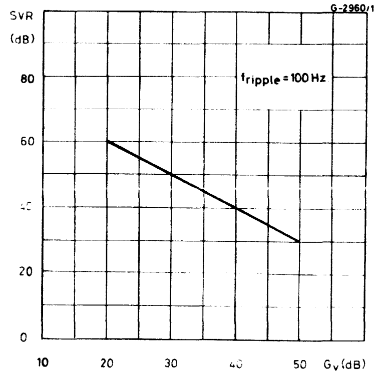


Figure 11 : Power Dissipation and Efficiency vs. Output Power.

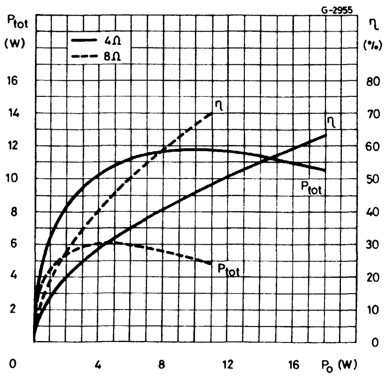
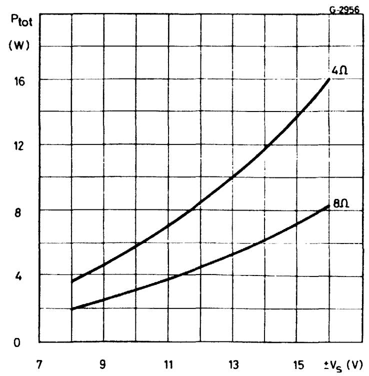


Figure 12 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).



APPLICATION INFORMATION

Figure 13 : Typical Amplifier with Split Power Supply.

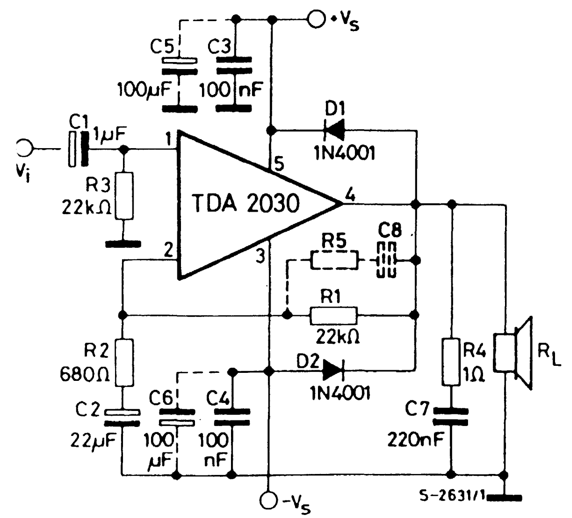


Figure 14 : P.C. Board and Component Layout for the Circuit of Fig. 13 (1 : 1 scale).

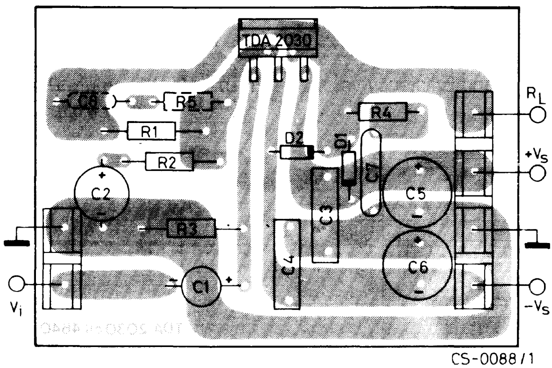


Figure 15 : Typical Amplifier with Single Power Supply.

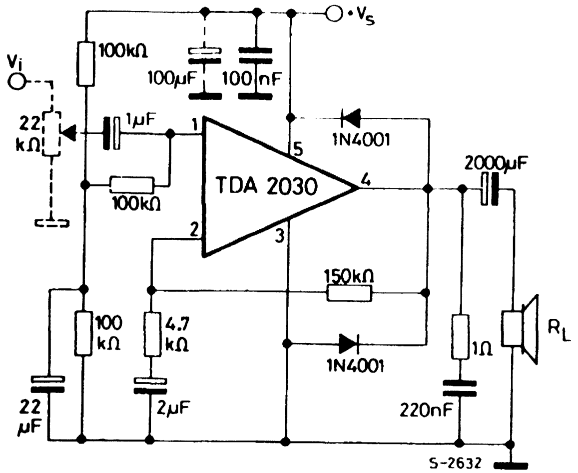


Figure 16 : P.C. Board and Component Layout for the Circuit of Fig. 15 (1 : 1 scale).

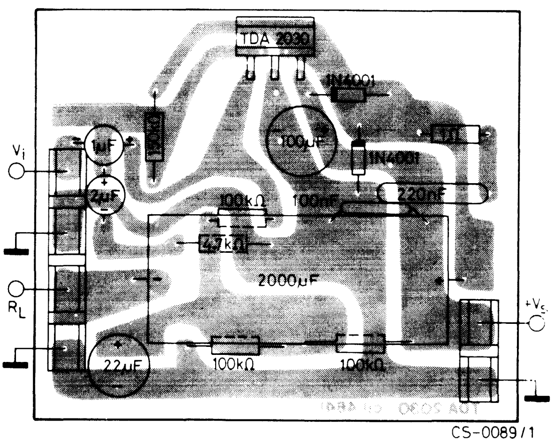
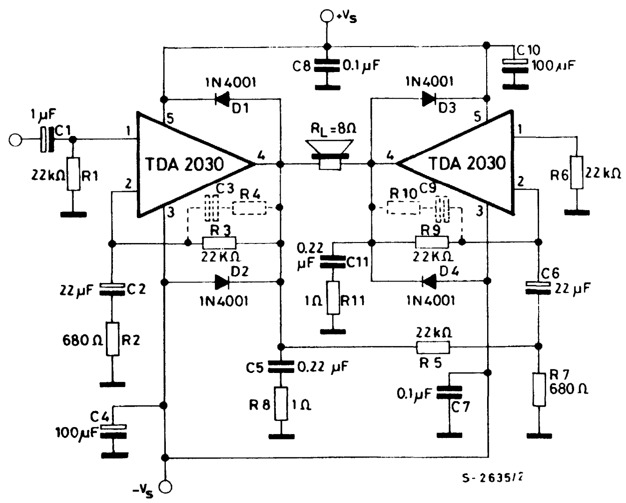


Figure 17 : Bridge Amplifier Configuration with Split Power Supply (P_o = 28W, V_S = ± 14V).



PRACTICAL CONSIDERATIONS

PRINTED CIRCUIT BOARD

The layout showw in fig. 16 should be adopted by the designers. If different layouts ar used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

ASSEMBLY SUGGESTION

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

APPLICATION SUGGESTIONS

The recommended values of the components are those shown on application circuit of fig. 16. Different values can be used. The following table can help the designer.

SHORT CIRCUIT PROTECTION

The TDA2030 as an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage ; hence the output transistors work within their safe operating area (fig. 2). This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possbility that the device gets damaged during an accidental short circuit from AC output to ground.

Component	Recommanded Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value
R1	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)
R2	680 Ω	Closed Loop Gain Setting	Decrease of Gain (*)	Increase of Gain
R3	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance
R4	1 Ω	Frequency Stability	Danger of Oscillat. at High Frequencies with Induct. Loads	
R5	≅ 3 R2	Upper Frequency Cutoff	Poor High Frequencies Attenuation	Danger of Oscillation
C1	1 µF	Input DC Decoupling		Increase of Low Frequencies Cutoff
C2	22 µF	Inverting DC Decoupling		Increase of Low Frequencies Cutoff
C3, C4	0.1 µF	Supply Voltage Bypass		Danger of Oscillation
C5, C6	100 µF	Supply Voltage Bypass		Danger of Oscillation
C7	0.22 µF	Frequency Stability		Danger of Oscillation
C8	$\approx \frac{1}{2\pi B R1}$	Upper Frequency Cutoff	Smaller Bandwidth	Larger Bandwidth
D1, D2	1N4001	To Protect the Device Against Output Voltage Spikes		

* Closed loop gain must be higher than 24dB.

Figure 18 : Maximum Output Current vs. Voltage [V_{CEsat}] Across Each Output Transistor.

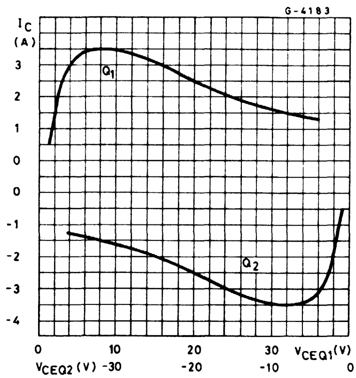
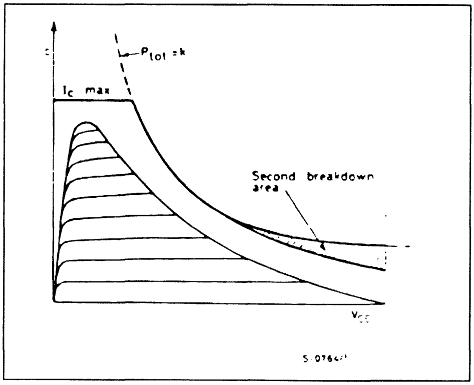


Figure 19 : Safe Operating Area and Collector Characteristics of the Protected Power Transistor.



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

- 1. An overload on the output (evenif it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
- 2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation at the current consumption.

The maximum allowable power dissipation depends upon te size of the external heatsink (i.e. its thermal resistance) ; fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Figure 20 : Output Power and Drain Current vs. Case Temperature (R_L = 4Ω).

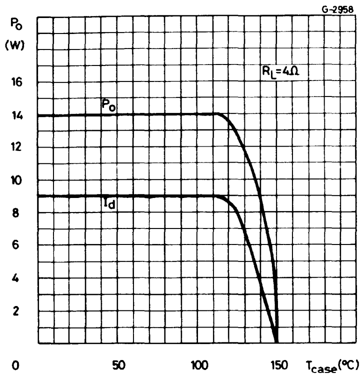


Figure 21 : Output Power and Drain Current vs. Case Temperature (R_L = 8Ω).

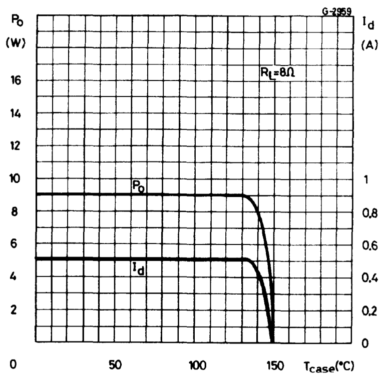


Figure 22 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

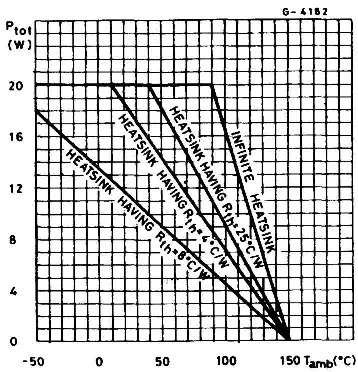
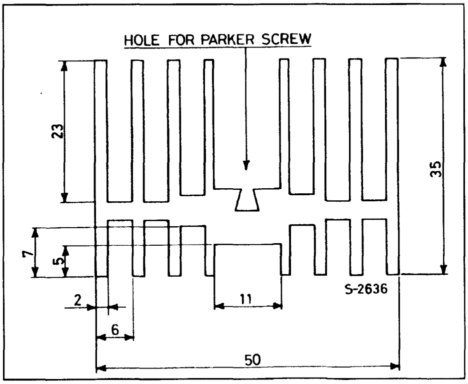


Figure 23 : Example of Heat-sink.



Dimension : suggestion.

The following table shows the length that the heatsink in fig. 23 must have for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Length of Heatsink (mm)	60	40	30
R_{th} of Heatsink (°C/W)	4.2	6.2	8.3

18 W Hi–Fi AMPLIFIER AND 35 W DRIVER

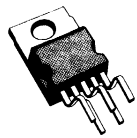
DESCRIPTION

The TDA2030A is a monolithic IC in Pentawatt package intended for use as low frequency class AB amplifier.

With $V_{s\,max}$ = 44V it is particularly suited for more reliable applications without regulated supply and for 35W driver circuits using low-cost complementary pairs.

The TDA2030A provides high output current and has very low harmonic and cross-over distortion.

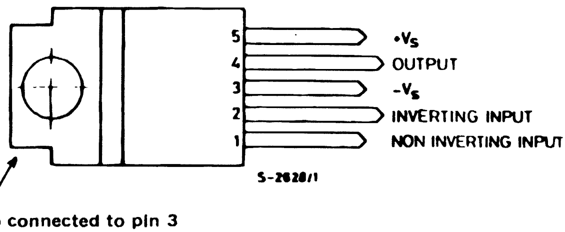
Further the device incorporates a short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included.



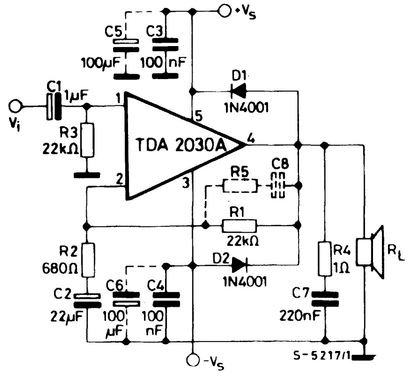
Pentawatt

ORDER CODES : TDA2030A
TDA2030AH

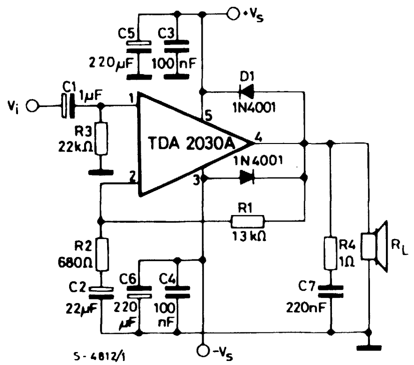
PIN CONNECTION (top view)



TYPICAL APPLICATION



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 22	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 15	V
I_o	Peak Output Current (internally limited)	3.5	A
P_{tot}	Total Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, $V_s = \pm 16$ V, $T_{amb} = 25$ °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 22	V
I_d	Quiescent Drain Current			50	80	mA
I_b	Input Bias Current	$V_S = \pm 22$ V		0.2	2	µA
V_{os}	Input Offset Voltage	$V_S = \pm 22$ V		± 2	± 20	mV
I_{os}	Input Offset Current			± 20	± 200	nA
P_o	Output Power	d = 0.5 % $G_v = 26$ dB f = 40 to 15 000 Hz $R_L = 4\ \Omega$ $R_L = 8\ \Omega$	 15 10	 18 12		W
		$V_S = \pm 19$ V $R_L = 8\ \Omega$	13	16		W
BW	Power Bandwidth	$P_o = 15$ W $R_L = 4\ \Omega$		100		kHz
SR	Slew Rate			8		V/µsec
G_v	Open Loop Voltage Gain	f = 1 KHz		80		dB
G_v	Closed Loop Voltage Gain	f = 1 KHz	25.5	26	26.5	dB
d	Total Harmonic Distortion	$P_o = 0.1$ to 14 W $R_L = 4\ \Omega$ f = 40 to 15 000 Hz f = 1 kHz		 0.08 0.03		%
		$P_o = 0.1$ to 9 W $R_L = 8\ \Omega$ f = 40 to 15 000 Hz		0.5		%
d_2	Second Order CCIF Intermodulation Distortion	$P_O = 4$ W $R_L = 4$ W $f_2 - f_1 = 1$ kHZ		0.03		%
d_3	Third Order CCIF Intermodulation Distortion	$f_1 = 14$ kHz $f_2 = 15$ kHz $2f_1 - f_2 = 13$ kHz		0.08		%
e_N	Input Noise Voltage	B = Curve A		2		µV
		B = 22 Hz to 22 kHz		3	10	µV
i_N	Input Noise Current	B = Curve A		50		pA
		B = 22 Hz to 22 kHz		80	200	pA
S/N	Signal to Noise Ratio	$R_L = 4\ \Omega$ $R_g = 10$ kΩ B = Curve A $P_O = 15$ W		106		dB
		$R_L = 4\ \Omega$ $R_g = 10$ kΩ B = Curve A $P_O = 1$ W		94		dB
R_i	Input Resistance (pin 1)	(open loop) f = 1 KHz	0.5	5		MΩ
SVR	Supply Voltage Rejection	$R_L = 4\ \Omega$ $G_v = 26$ dB $R_g = 22$ KΩ f = 100 Hz		54		dB
T_j	Thermal Shut-down Junction Temperature			145		°C

Figure 1 : Single Supply Amplifier.

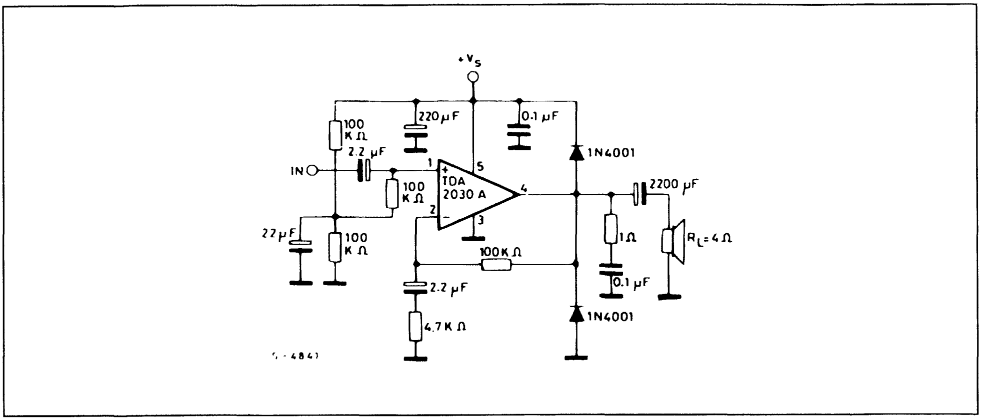


Figure 2 : Open Loop-frequency Response.

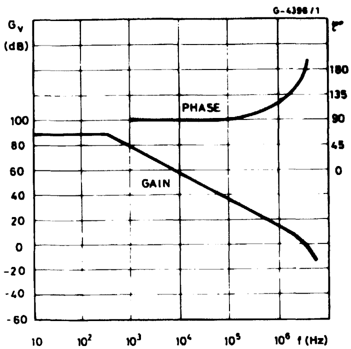


Figure 3 : Output Power vs. Supply Voltage.

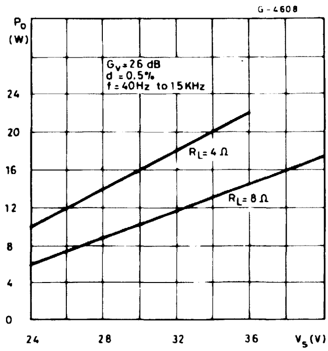


Figure 4 : Total Harmonic Distortion vs. Output Power (*).

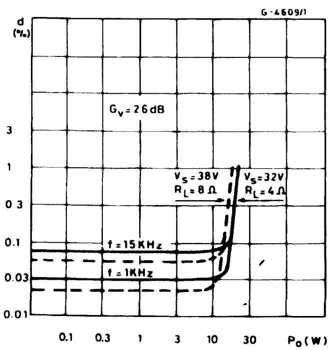
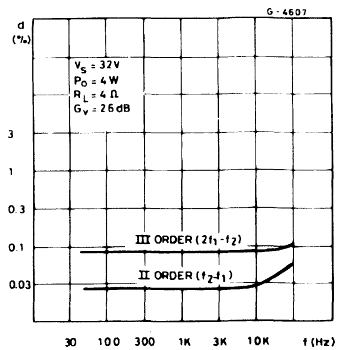


Figure 5 : Two Tone CCIF Intremodulation Distortion.



* Tel using rise filters.

Figure 6 : Large Signal Frequency Response.

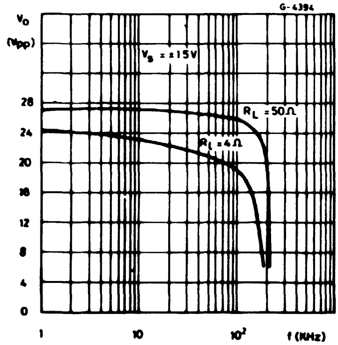


Figure 7 : Maximum Allowable Power Dissipation vs. Ambient Temperature

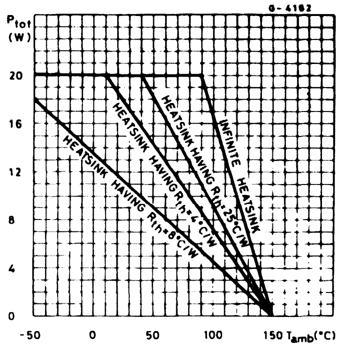


Figure 8 : Single Supply High Power Amplifier (TDA2030A + BD907/BD908).

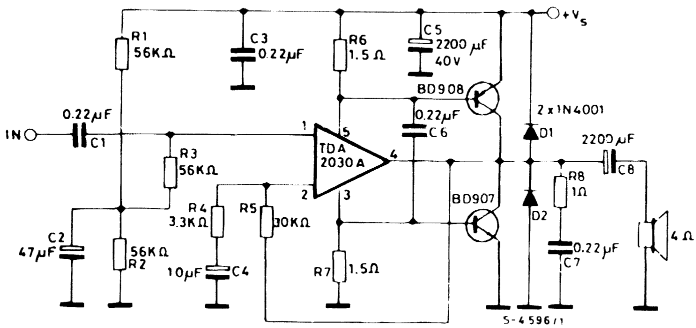
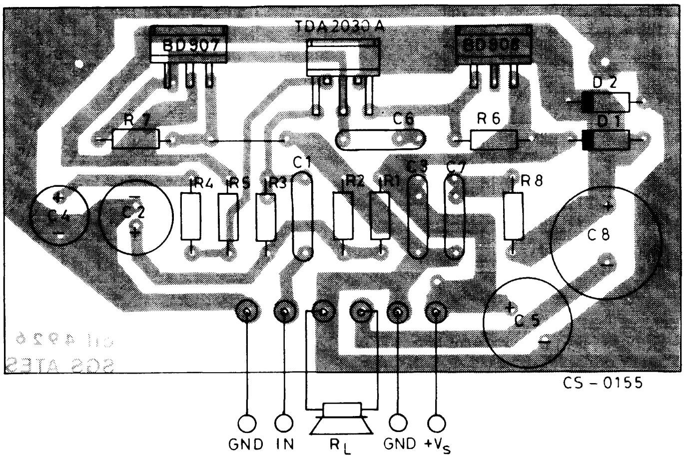


Figure 9 : P. C. Board and Component Layout for the Circuit of fig. 8 (1 : 1 scale).



TYPICAL PERFORMANCE OF THE CIRCUIT OF FIG. 8

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage				36	44	V
I_d	Quiescent Drain Current	V_s = 36 V			50		mA
P_o	Output Power	d = 0.5 %, R_L = 4 Ω, f = 40 Hz to 15 kHz	V_s = 39 V		35		W
			V_s = 36 V		28		
		d = 10 % ; f = 1 kHz, R_L = 4 Ω	V_s = 39 V		44		W
			V_s = 36 V		35		
G_v	Voltage Gain	f = 1 kHz		19.5	20	20.5	dB
SR	Slew Rate				8		V/µsec
d	Total Harmonic Distortion	P_o = 20 W	f = 1 kHz		0.02		%
			f = 40 Hz to 15 kHz		0.05		
V_i	Input Sensitivity	G_v = 20 dB, P_o = 20 W	f = 1 kHz, R_L = 4 Ω		890		mV
S/N	Signal to Noise Ratio	R_L = 4 Ω, R_g = 10 kΩ, B = Curve A	P_o = 25 W		108		dB
			P_o = 4 W		100		

Figure 10 : Output Power vs. Supply Voltage.

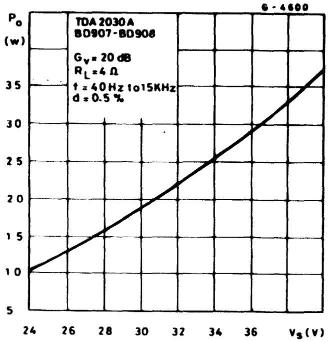


Figure 11 : Total Harmonic Distortion vs. Output Power

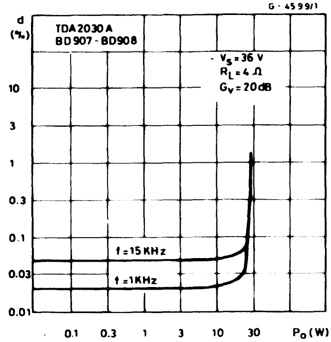


Figure 12 : Output Power vs. Input Level.

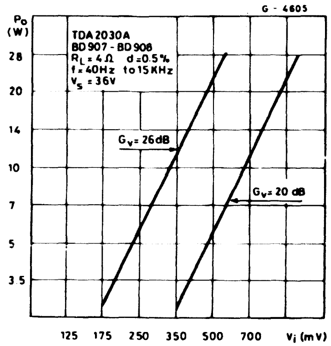


Figure 13 : Power Dissipation vs. Output Power

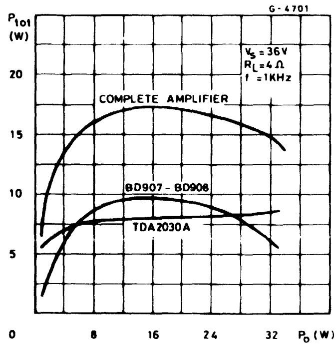


Figure 14 : Typical Amplifier with Split Power Supply.

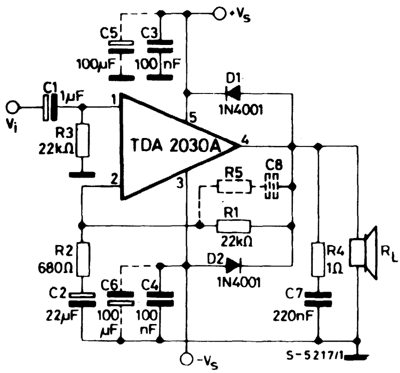


Figure 15 : P. C. Board and Component Layout for the Circuit of fig. 14 (1 : 1 scale).

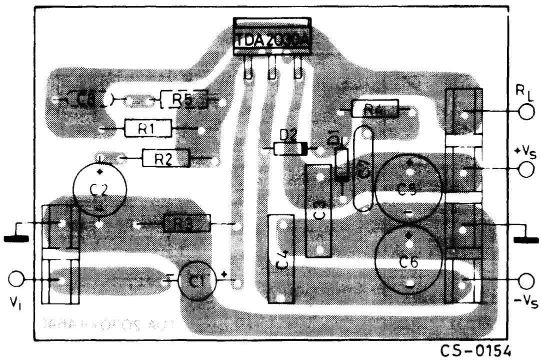


Figure 16 : Bridge Amplifier with Split Power Supply (PO = 34 W, Vs = ± 16 V).

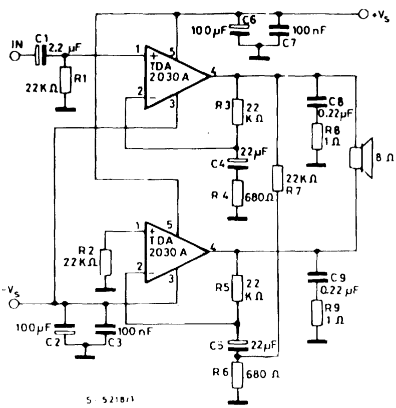
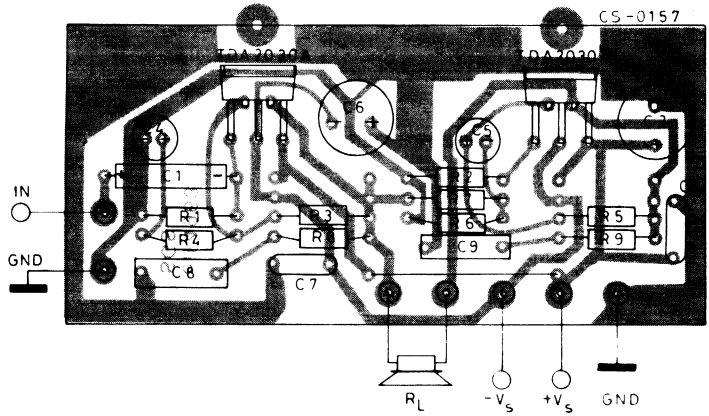


Figure 17 : P. C. Board and Component Layout for the Circuit of fig. 16 (1 : 1 scale).



MULTIWAY SPEAKER SYSTEMS AND ACTIVE BOXES

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two or three bands.

To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segmento of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see Fig. 18). As an example a 100W three-way system with crossover frequencies of 400Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.

Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power less ;
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance.

Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers.

In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6dB/octave) can be recommended.

The result obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.

The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.

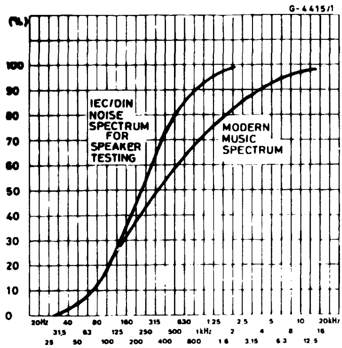
A more effective solution, named "Active Power Filter" is shown in Fig. 19.

The proposed circuit can realize combined power amplifiers and 12dB/octave or 18dB/octave high-pass or low-pass filters.

In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.

The impedance at the pin (-) is of the order of 100 Ω, while that of the pin (+) is very high, which is also what was wanted.

Figure 18 : Power Distribution vs. Frequency.



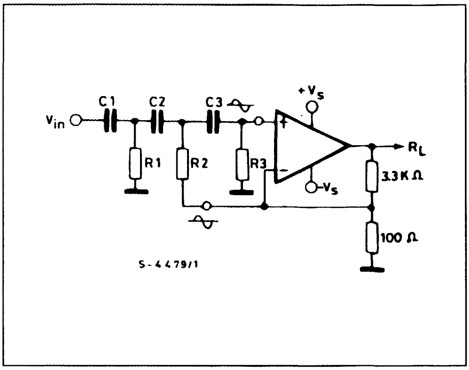
The component values calculated for f_C = 900Hz using a Bessel 3rd order Sallen and Key structure are:

$C_1 = C_2 = C_3$	R_1	R_2	R_3
22 nF	8.2 kΩ	5.6 kΩ	33 kΩ

Using this type of crossover filter, a complete 3-way 60W active loudspeaker system is shown in Fig. 20.

It employs 2nd order Buttherworth filters with the crossover frequencies equal to 300Hz and 3KHz.

Figure 19 : Active Power Filter.

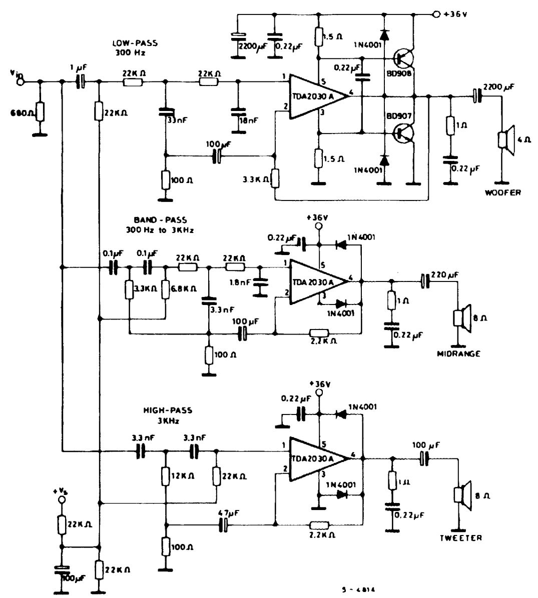


The midrange section consists of two filters, a high pass circuit followed by a low pass network. With V_S = 36V the output power delivered to the woofer is 25W at d = 0.06% (30W at d = 0.5%).

The power delivered to the midrange and the tweeter can be optimized in the design phase taking in account the loudspeaker efficiency and impedance (R_L = 4 Ω to 8 Ω).

It is quite common that midrange and tweeter speakers have an efficiency 3dB higher than woofers.

Figure 20 : 3 Way 60 W Active Loudspeaker System (V_S = 36 V).



MUSICAL INSTRUMENTS AMPLIFIERS

Another important field of application for active systems is music.

In this area the use of several medium power amplifiers is more convenient than a single high power amplifier, and it is also more realiable.

A typical example (see Fig. 21) consist of four amplifiers each driving a low-cost, 12 inch loudspeaker. This application can supply 80 to 160W rms.

TRANSIENT INTERMODULATION DISTORTION (TIM)

Transient intermodulation distortion is an unfortunate phenomen associated with negative-feedback amplifiers. When a feedback amplifier receives an input signal which rises very steeply, i.e. contains high-frequency components, the feedback can arrive too late so that the amplifiers overloads and a burst of intermodulation distortion will be produced as in Fig. 22. Since transients occur frequently in music this obviously a problem for the designer of audio amplifiers. Unfortunately, heavy negative feedback is frequency used to reduce the total harmonic distortion of an amplifier, which tends to aggravate the transient intermodulation (TIM situation. The best known method for the measurement of TIM consists of feeding sine waves superimposed onto square waves, into the amplifier under test. The output spectrum is then examined using a spectrum analyser and compared to the input. This method suffers from serious disadvantages : the accuracy is limited, the measurement is a rather delicate operation and an expensive spectrum analyser is essential. A new approach applied to monolithic amplifiers measurement is fast cheap-it requires nothing more sophisticated than an oscilloscope - and sensitive - and it can be used down to the values as low as 0.002% in high power amplifiers.

The "inverting-sawtooh" method of measurement is based on the response of an amplifier to a 20KHz sawtooth waveform. The amplifier has no difficulty following the slow ramp but it cannot follow the fast edge. The output will follow the upper line in Fig. 23 cutting of the shaded area and thus increasing the mean level. If this output signal is filtered to remove the sawtooth, direct voltage remains which indicates the amount of TIM distortion, although it is difficult to measure because it is indistinguishable from the DC offset of the amplifier. This problem is neatly avoided in the IS-TIM method by periodically inverting the sawtooth waveform at a low audio frequency as shown in Fig. 24.

Figure 21 : High Power Active Box for Musical Instrument.

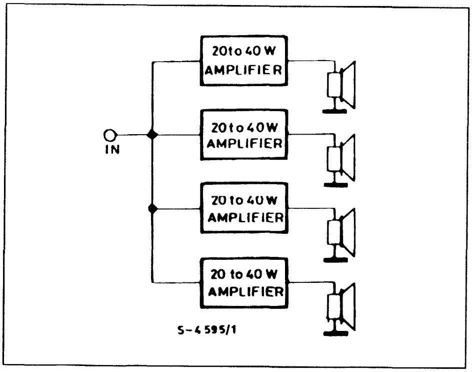


Figure 22 : Overshoot Phenomenon in Feedback Amplifiers.

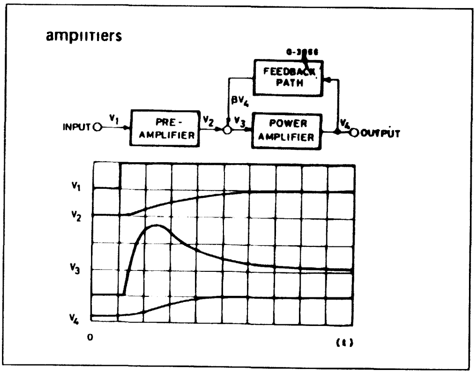


Figure 23 : 20 KHz Sawtooth Waveform.

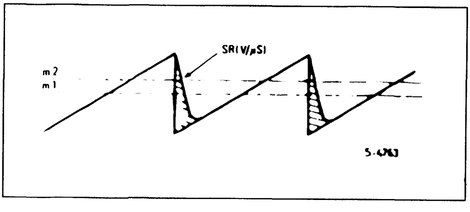
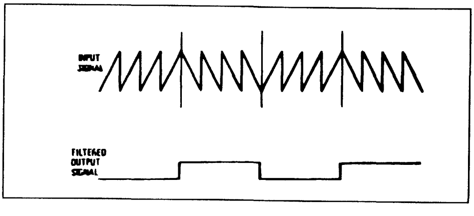


Figure 24 : Inverting Sawtooth Waveform.



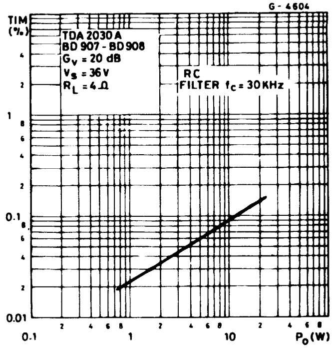
In the case of the sawtooth in Fig. 25 the mean level was increased by the TIM distortion, for a sawtooth in the other direction the opposite is true.

The result is an AC signal at the output whole peak-to-peak value is the TIM voltage, which can be measured easily with an oscilloscope. If the peak-to-peak value of the signal and the peak-to-peak of the inverting sawtooth are measured, the TIM can be found very simply from:

$$TIM = \frac{V_{out}}{V_{sawtooth}} \cdot 100$$

In Fig. 25 the experimental results are shown for the 30W amplifier using the TDA2030A as a driver and a low-cost complementary pair. A simple RC filter on the input of the amplifier to limit the maximum signal slope (SS) is an effective way to reduce TIM.

Figure 25 : TIM Distortion vs. Output Power.



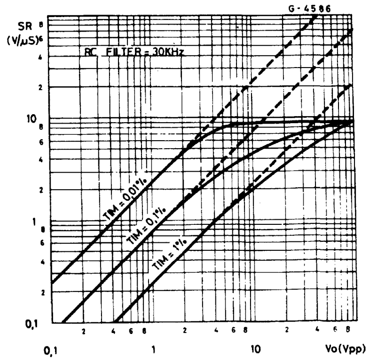
The diagram of Fig. 26 can be used to find the Slew-Rate (SR) required for a given output power or voltage and a TIM design target.

For example if an anti-TIM filter with a cutoff at 30KHz is used and the max. peak-to-peak output voltage is 20V then, referring to the diagram, a Slew-Rate of 6V/µs is necessary for 0.1% TIM.

As shown Slew-Rates of above 10V/µs do not contribute to a further reduction in TIM.

Slew-Rates of 100/µs are not only useless but also a disadvantage in Hi-Fi audio amplifiers because they tend to turn the amplifier into a radio receiver.

Figure 26 : TIM Design Diagram (f_C = 30 KHz).



POWER SUPPLY

Using monolithic audio amplifier with non-regulated supply voltage it is important to design the power supply correctly. In any working case it must provide a supply voltage less than the maximum value fixed by the IC break-down voltage.

It is essential to take into account all the working conditions, in particular mains fluctuations and supply voltage variations with and without load. The TDA2030A ($V_{s\,max}$ = 44V) is particularly suitable for substitution of the standard IC power amplifiers (with $V_{s\,max}$ = 36V) for more reliable applications.

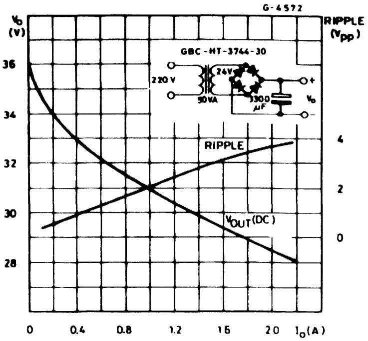
An example, using a simple full-wave rectifier followed by a capacitor filter, is shown in the table and in the diagram of Fig. 27.

A regulated supply is not usually used for the power output stages because of its dimensioning must be done taking into account the power to supply in the signal peaks. They are only a small percentage of the total music signal, with consequently large over-dimensioning of the circuit.

Even if with a regulated supply higher output power can be obtained (V_s is constant in all working conditions), the additional cost and power dissipation do not usually justify its use. Using non-regulated supplies, there are fewer designe restriction. In fact, when signal peaks are present, the capacitor filter acts as a flywheel supplying the required energy.

In average conditions, the continuous power supplied is lower. The music power/continuous power ratio is greater in this case than for the case of regulated supplied, with space saving and cost reduction.

Figure 27 : DC Characteristics of 50 W Non-regulated Supply.



Mains (220 V)	Secondary Voltage	DC Output Voltage (V_o)		
		$I_o = 0$	$I_o = 0.1$ A	$I_o = 1$ A
+ 20 %	28.8 V	43.2 V	42 V	37.5 V
+ 15 %	27.6 V	41.4 V	40.3 V	35.8 V
+ 10 %	26.4 V	39.6 V	38.5 V	34.2 V
–	24 V	36.2 V	35 V	31 V
– 10 %	21.6 V	32.4 V	31.5 V	27.8 V
– 15 %	20.4 V	30.6 V	29.8 V	26 V
– 20 %	19.2 V	28.8 V	28 V	24.3 V

APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of Fig. 14. Different values can be used. The following table can help the designer.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1	22 KΩ	Closed loop gain setting.	Increase of gain.	Decrease of gain.*
R2	680 Ω	Closed loop gain setting.	Decrease of gain.*	Increase of gain.
R3	22 KΩ	Non inverting input biasing.	Increase of input impedance.	Decrease of input impedance.
R4	1 Ω	Frequency Stability	Danger of oscillation at high frequencies with inductive loads.	
R5	≅ 3 R2	Upper Frequency Cutoff	Poor High Frequencies Attenuation	Danger of Oscillation
C1	1 µF	Input DC Decoupling		Increase of low frequencies cutoff.
C2	22 µF	Inverting DC Decoupling		Increase of low frequencies cutoff.
C3, C4	0.1 µF	Supply Voltage Bypass		Danger of Oscillation
C5, C6	100 µF	Supply Voltage Bypass		Danger of Oscillation
C7	0.22 µF	Frequency Stability		Larger Bandwidth
C8	$\cong \frac{1}{2\pi B R1}$	Upper Frequency Cutoff	Smaller Bandwidth	Larger Bandwidth
D1, D2	1N4001	To protect the device against output voltage spikes.		

* The value of closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2030A has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply reduces the power dissipation and the current consumption.

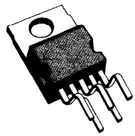
SGS-THOMSON MICROELECTRONICS

TDA2040

20 W Hi–Fi AUDIO POWER AMPLIFIER

DESCRIPTION

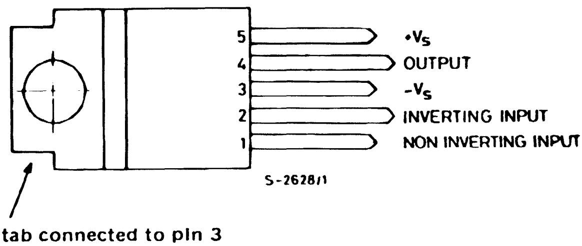
The TDA2040 is a monolithic integrated circuit in Pentawatt package, intended for use as an audio class AB amplifier. Typically it provides 22 W output power (d = 0.5 %) at V_s = 32 V/4Ω . The TDA2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.



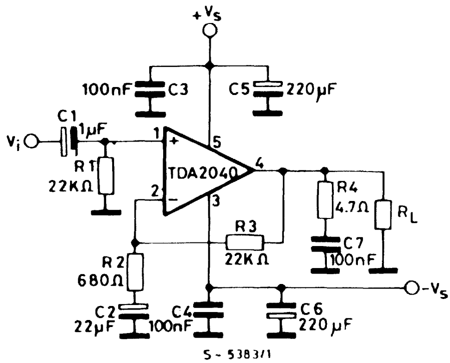
Pentawatt

ORDER CODES : TDA2040V
TDA2040H

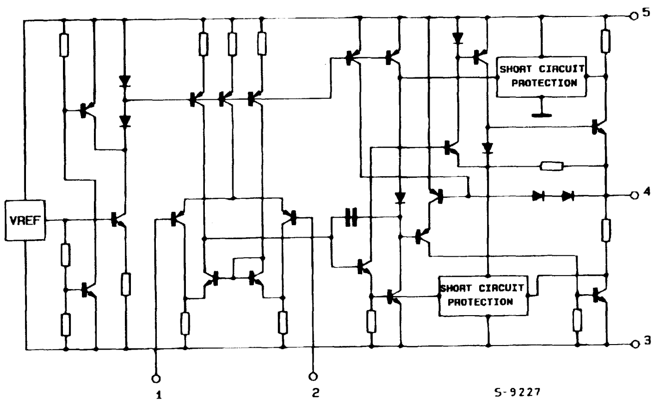
PIN CONNECTION (top view)



TEST CIRCUIT



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 20	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 15	V
I_o	Output Peak Current (internally limited)	4	A
P_{tot}	Power Dissipation at T_{case} = 75 °C	25	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = ± 16 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 2.5		± 20	V
I_d	Quiescent Drain Current	V_s = ± 4.5 V			30	mA
		V_s = ± 20 V		45	100	mA
I_b	Input Bias Current	V_s = ± 20 V		0.3	1	μA
V_{os}	Input Offset Voltage	V_s = ± 20 V		± 2	± 20	mV
I_{os}	Input Offset Current				± 200	nA
P_o	Output Power	d = 0.5 % T_{case} = 60 °C f = 1 kHz R_L = 4 Ω R_L = 8 Ω	20	22 12		W
		f = 15 kHz R_L = 4 Ω	15	18		W
BW	Power Bandwidth	P_o = 1 W R_L = 4 Ω		100		kHz
G_v	Open Loop Voltage Gain	f = 1 kHz		80		dB
G_v	Closed Loop Voltage Gain	f = 1 kHz	29.5	30	30.5	dB
d	Total Harmonic Distortion	P_o = 0.1 to 10 W R_L = 4 Ω f = 40 to 15000Hz f = 1 kHz		0.08 0.03		%
e_N	Input Noise Voltage	B = Curve A		2		μV
		B = 22 Hz to 22 kHz		3	10	μV
i_N	Input Noise Current	B = Curve A		50		pA
		B = 22 Hz to 22 kHz		80	200	pA
R_i	Input Resistance (pin 1)		0.5	5		MΩ
SVR	Supply Voltage Rejection	R_L = 4 Ω G_v = 30 dB R_g = 22 kΩ f = 100 Hz V_{ripple} = 0.5 V_{rms}	40	50		dB
η	Efficiency	f = 1 kHz P_o = 12 W R_L = 8 Ω P_o = 22 W R_L = 4 Ω		66 63		%
T_j	Thermal Shut-down Junction Temperature			145		°C

Figure 1 : Output Power vs. Supply Voltage.

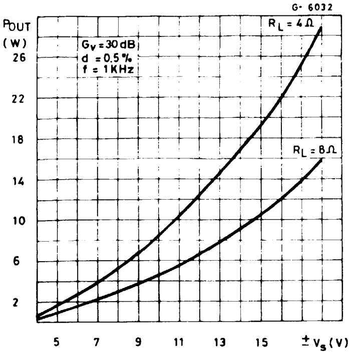


Figure 2 : Output Power vs. Supply Voltage.

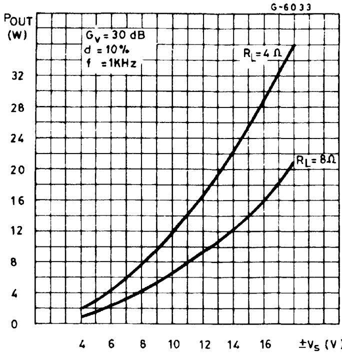


Figure 3 : Output Power vs. Supply Voltage.

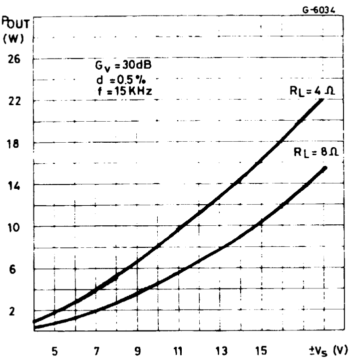


Figure 4 : Distortion vs. Frequency.

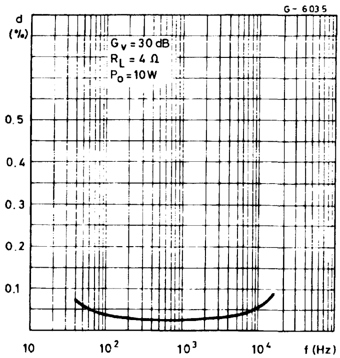


Figure 5 : Supply Voltage Rejection vs. Frequency.

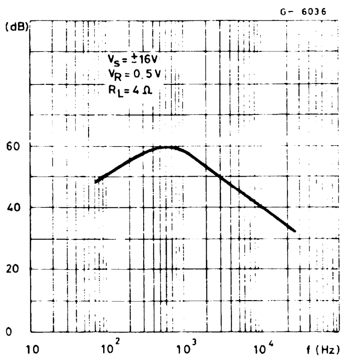


Figure 6 : Supply Voltage Rejection vs. Voltage Gain.

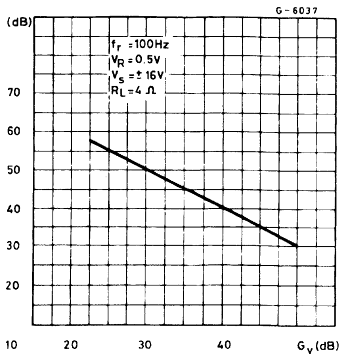


Figure 7 : Quiescent Drain Current vs. Supply Voltage.

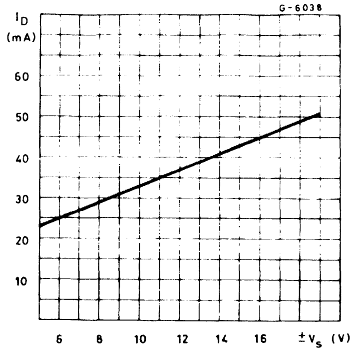


Figure 8 : Open Loop Gain vs. Frequency.

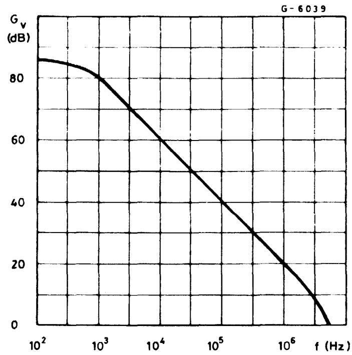
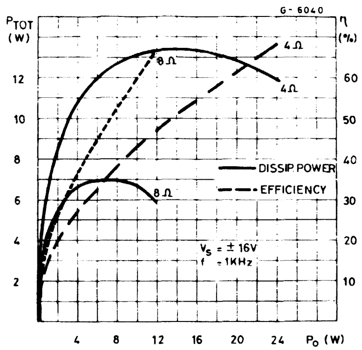
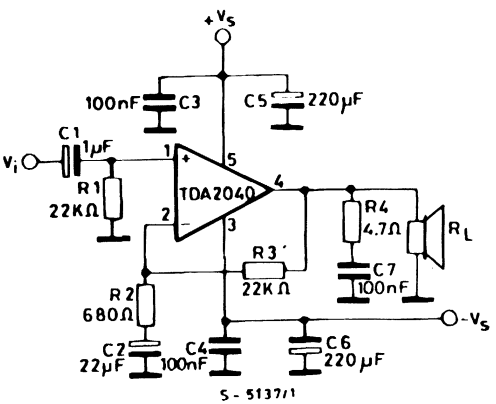


Figure 9 : Power Dissipation vs. Output Power



APPLICATION INFORMATION

Figure 10 : Amplifier with Split Power Supply (*).



$V_S = \pm 16$ V
$R_L = 4\ \Omega$
$P_O \geq 15\ \Omega$ (d = 0.5 %)

APPLICATION INFORMATION (continued)

Figure 11 : P. C. Board and Components Layout for the Circuit of fig. 10 (1 : 1 scale).

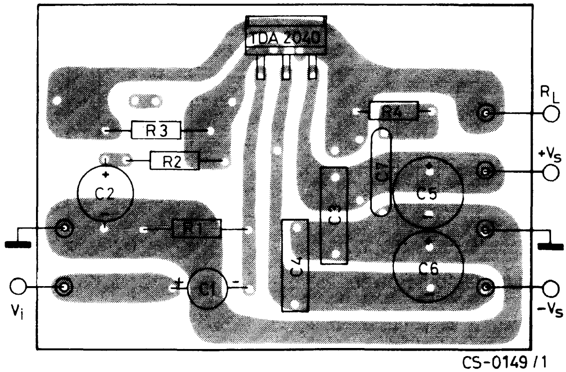
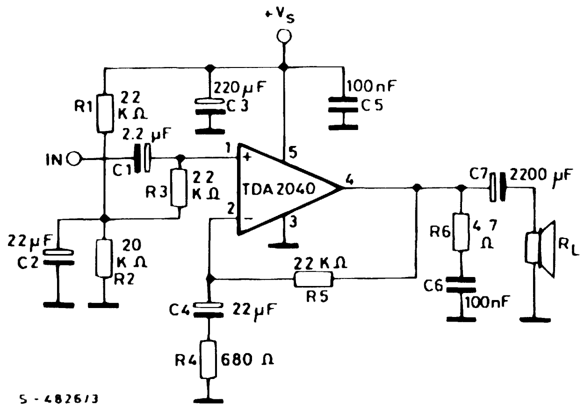


Figure 12 : Amplifier with Single Supply (*).



* In this case of highly inductive loads protection diodes may be necessary.

APPLICATION INFORMATION (continued)

Figure 13 : P. C. Board and Components Layout for the Circuit of fig. 12 (1 : 1 scale).

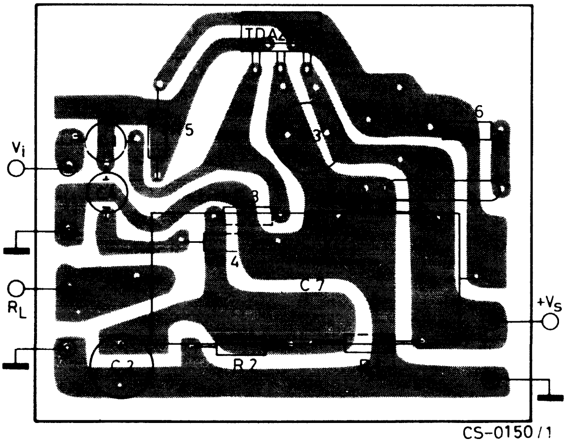
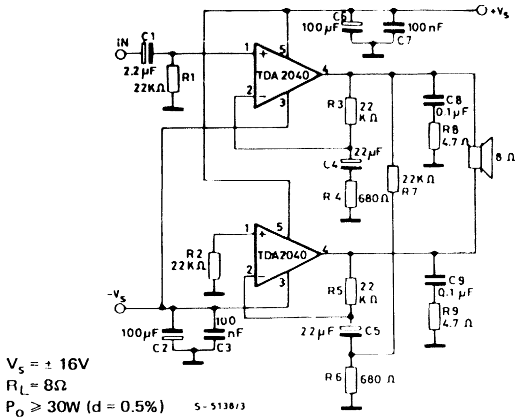


Figure 14 : 30 W Bridge Amplifier with Split Power Supply.



APPLICATION INFORMATION (continued)

Figure 15 : P. C. Board and Components Layout for the Circuit of fig. 14 (1 : 1 scale).

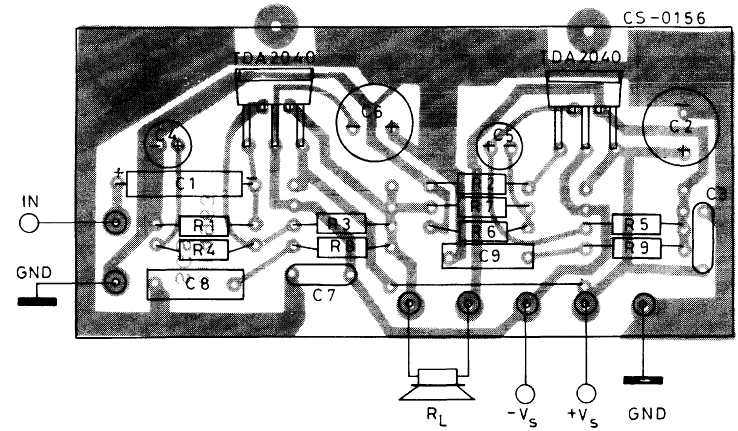
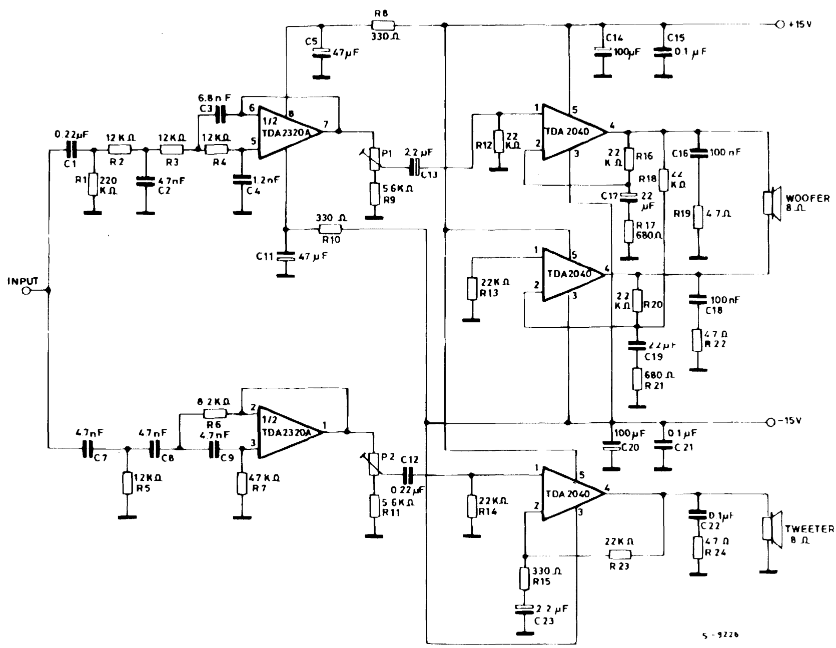


Figure 16 : Two Way Hi-Fi System with Active Crossver.



APPLICATION INFORMATION (continued)

Figure 17 : P. C. Board and Components Layout for the Circuit of fig. 16 (1 : 1 scale).

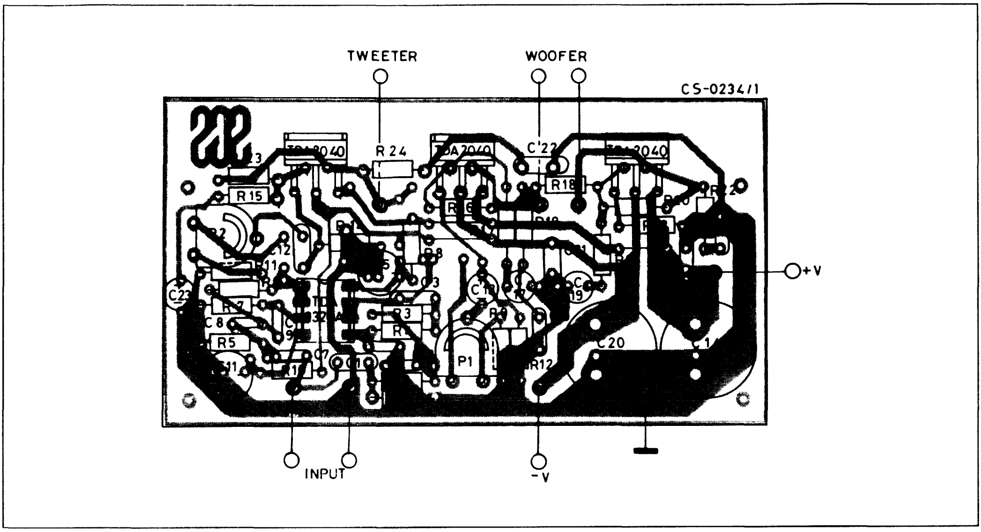


Figure 18 : Frequency Response.

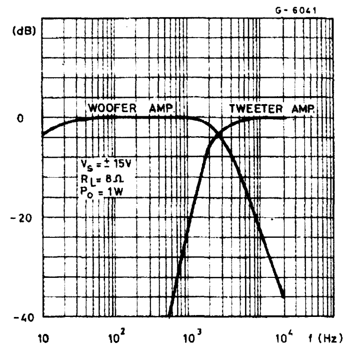
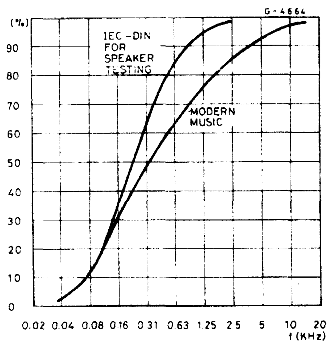


Figure 19 : Power Distribution vs. Frequency.



Multiway Speaker Systems And Active Boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.

To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum determine the cutoff frequencies of the crossover filters (see fig. 19). As an example, a 100 W three-way system with crossover frequencies of 400 Hz and 3 KHz would require 50 W for the woofer, 35 W for the midrange unit and 15 W for the tweeter.

Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters :

- power loss

- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

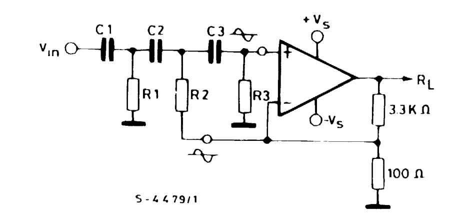
Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit. This makes it particularly interesting and economically sound to use monolithic power amplifiers. In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6 dB/octave) can be recommended.

The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.

The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.

A more effective solution, named "Active Power Filter" is shown in Fig. 20.

Figure 20 : Active Power Filter.



The proposed circuit can realize combined power amplifiers and 12 dB/octave or 18 dB/octave high-pass or low-pass filters.

In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.

The impedance at the pin (-) is of the order of 100 Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for f_C = 900 Hz using a Bessel 3rd order Sallen and Key structure are :

C1 = C2 = C3	R1	R2	R3
22 nF	8.2 kΩ	5.6 kΩ	33 kΩ

In the block diagram of Fig. 21 is represented an active loudspeaker system completely realized using power integrated circuit, rather than the traditional discrete transistors on hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA2320A) and a separate amplifier and loudspeakers for each band.

A modern subwoofer/midrange/tweeter solution is used.

SHORT CIRCUIT PROTECTION

The TDA2040 has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. The TDA2030A is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time the thermal shut down protection keeps the junction temperature within safe limits.

THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the Tj cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increase up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

PRATICAL CONSIDERATION

PRINTED CIRCUIT BOARD

The layout shown in Fig. 11 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the gorund return of the output in which a high current flows.

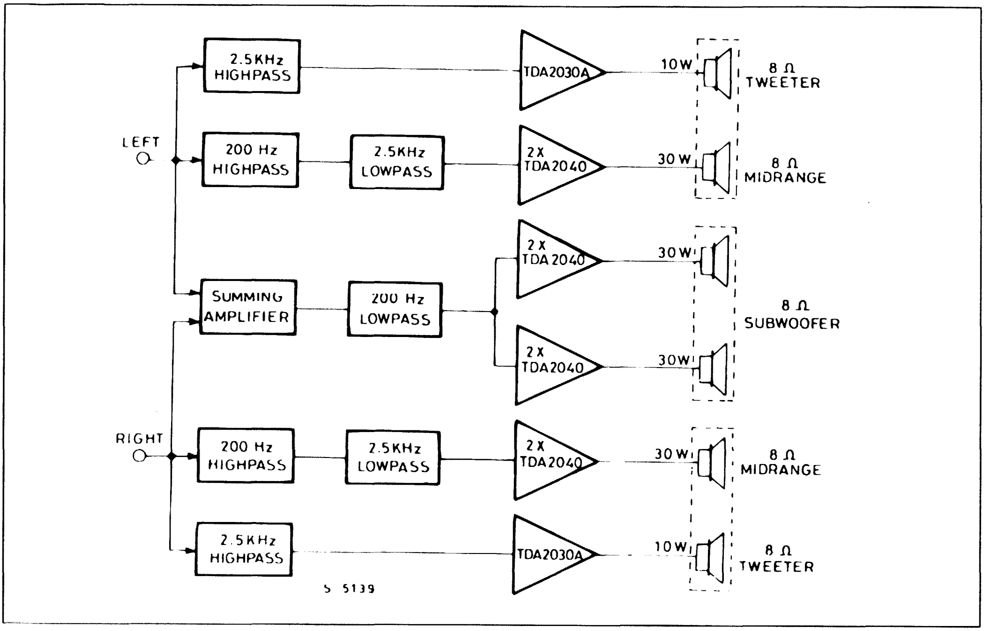
ASSEMBLY SUGGESTION

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

APPLICATION SUGGESTIONS

The recommended values of the components are those shown on application circuit of Fig. 10. Different values can be used. The following table can help the designer.

Figure 21 : High Power Active Loudspeaker System Using TDA 2030A and TDA2040.



Component	Recom. Value	Purpose	Larger Than Recommended Value	Smaller Than Recommended Value
R1	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance
R2	680 Ω	Closed Loop Gain Setting	Decrease of gain (*)	Increase of Gain
R3	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)
R4	4.7 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads	
C1	1 µF	Input DC Decoupling		Increase of Low Frequencies Cutoff
C2	22 µF	Inverting DC Decoupling		Increase of Low Frequencies Cutoff
C3, C4	0.1 µF	Supply Voltage Bypass		Danger of Oscillation
C5, C6	220 µF	Supply Voltage Bypass		Danger of Oscillation
C7	0.1 µF	Frequency Stability		Danger of Oscillation

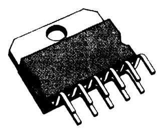
(*) The value of closed loop gain must be higher than 24 dB.

SGS-THOMSON
MICROELECTRONICS

TDA2170

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The functions incorporated are :
- POWER AMPLIFIER
- FLYBACK GENERATOR
- REFERENCE VOLTAGE
- THERMAL PROTECTION



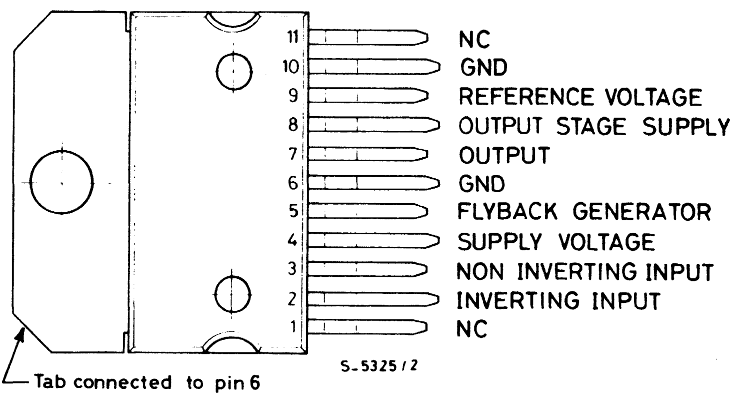
MULTIWATT 11

ORDER CODE : TDA2170

DESCRIPTION

The TDA 2170 is a monolithic integrated circuit in 11-lead Multiwatt® package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour are B & W television receivers as well as in monitors and displays.

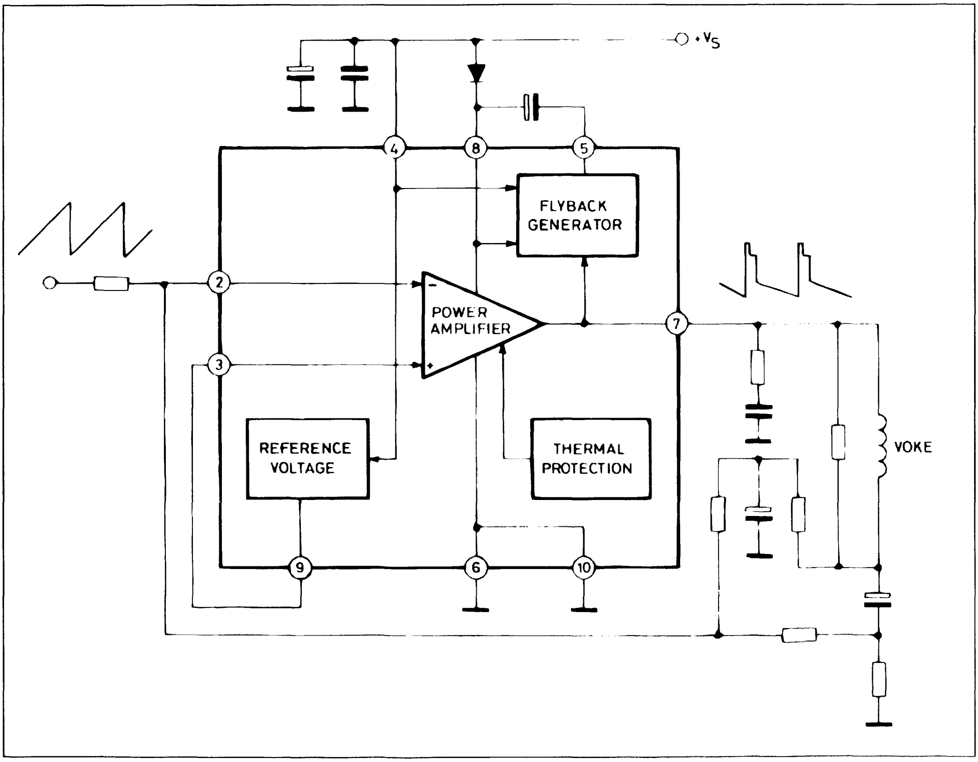
CONNECTION DIAGRAM (top view)



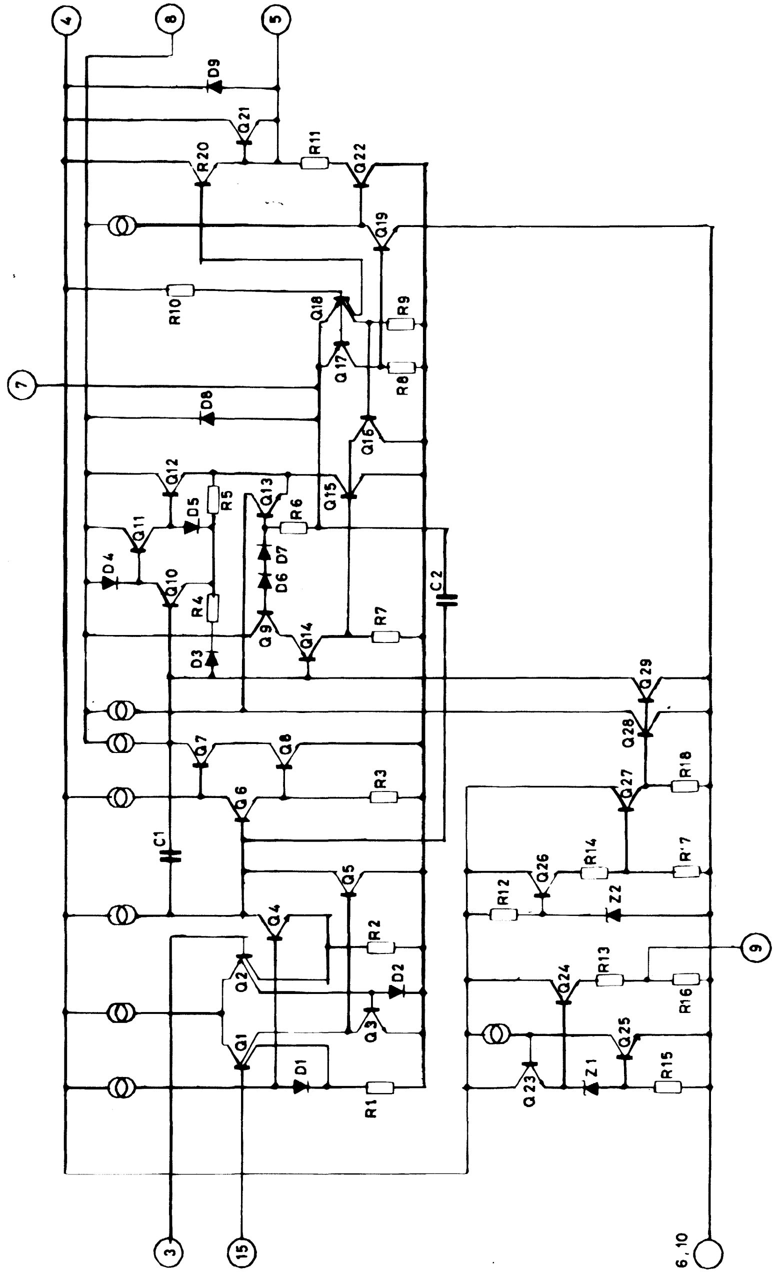
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 4)	35	V
V_7, V_8	Flyback Peak Voltage	60	V
V_5	Voltage at Pin 5	+ V_s	
V_2, V_3	Amplifier Input Voltage	+ V_s – 0.5	V
I_o	Output Peak Current (non repetitive, t = 2 msec)	2.5	A
I_o	Output Peak Current at f = 50 Hz, t ≤ 10 µsec	3	A
I_o	Output Peak Current at f = 50 Hz, t > 10 µsec	2	A
I_5	Pin 5 DC Current at $V_7 < V_4$	100	mA
I_5	Pin 5 Peak to Peak Flyback Current at f = 50 Hz, t_{fly} ≤ 1.5 msec	3	A
P_{tot}	Total Power Dissipation at T_{case} = 60 °C	30	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



THERMAL DATA

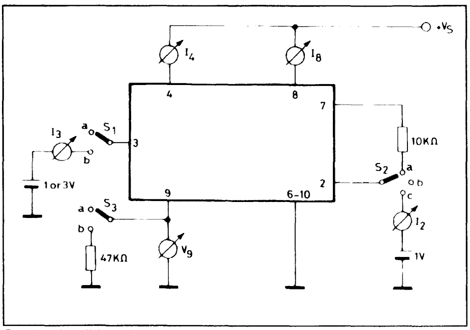
$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction–ambient	Max	40	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_4	Pin 4 Quiescent Current	$I_5 = 0$; $I_7 = 0$; $V_3 = 3$ V		8	16	mA	1a
I_8	Pin 8 Quiescent Current	$I_5 = 0$; $I_7 = 0$; $V_3 = 3$ V		16	36	mA	1a
I_3	Amplifier Input Bias Current	$V_3 = 1$ V		– 0.1	– 1	µA	1a
I_2	Amplifier Input Bias Current	$V_2 = 1$ V		– 0.1	– 1	µA	1a
V_9	Reference Voltage	$I_9 = 0$		2.2		V	1a
$\frac{\Delta V_9}{\Delta V_s}$	Reference Voltage Drift vs. Supply Voltage	Vs = 15 to 30 V		1	2	mV/V	1a
V_{5L}	Pin 5 Saturation Voltage to GND	I_5 = 20 mA		1		V	1c
V_7	Quiescent Output Voltage	V_s = 35 V ; R_a = 13 KΩ		18		V	1d
		Vs = 15 V ; R_a = 13 KΩ		7.5		V	1d
V_{7L}	Output Saturation Voltage to GND	I_7 = 1.2 A		1	1.4	V	1c
		I_7 = 0.7 A		0.7	1	V	1c
V_{7H}	Output Saturation Voltage to Supply	$- I_7$ = 1.2 A		1.6	2.2	V	1b
		$- I_7$ = 0.7 A		1.3	1.8	V	1b
R_9	Reference Voltage Output Resistance			2.1		KΩ	
T_j	Junction Temperature for Thermal Shut Down			140		°C	

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_2 ; I_3 ; I_4 ; I_8 ; I_9 ; $\Delta V_9/\Delta V_S$; R9.



S_1 : (a) I_2 ; (b) I_3, I_4 and I_8.
S_2 : (a) I_4 and I_8 ; (b) I_3 ; (c) I_2.
S_3 : (a) I_2, I_3, I_4, I_8, I_9 and V_9 ; (b) R9.

Figure 1b : Measurement of $V7_H$.

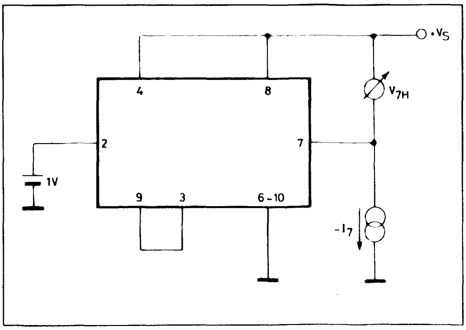
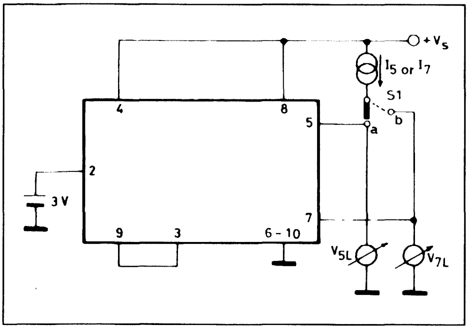


Figure 1c : Measurement of V_{5L}, V_{7L}.



S1 : (a) V_{5L} ; (b) V_{7L}.

Figure 1d : Measurement of V_7.

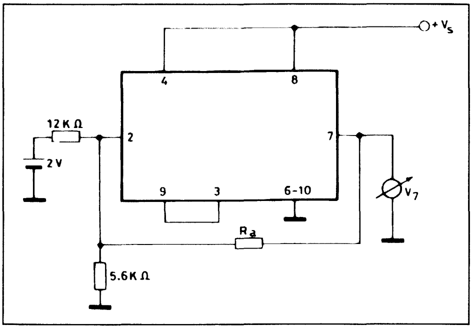


Figure 2 : Application Circuit.

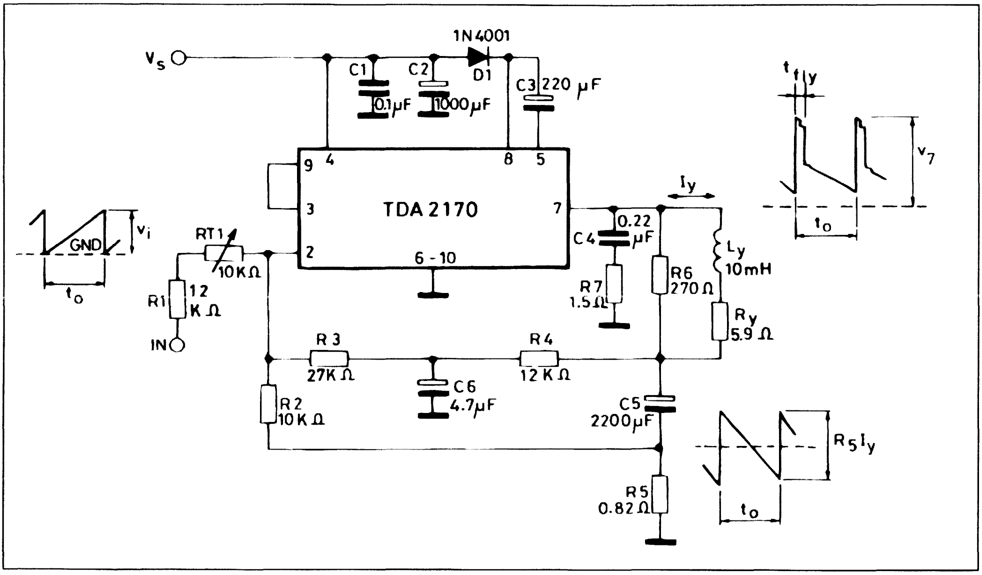
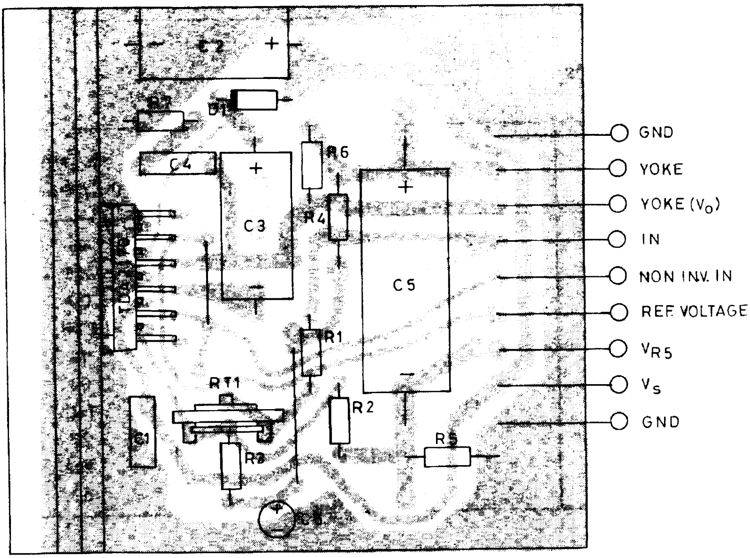


Figure 3 : PC Board and Component Layout (1:1 scale).



COMPONENTS LIST FOR TYPICAL APPLICATIONS

Component	110° TVC 5.9 Ω / 10 mH 1.95 App	110° TVC 9.6 Ω / 24.6 mH 1.2 App	90° TVC 15 Ω / 30 mH 0.82 App	Unit
RT1	10	4.7	10	KΩ
R1	12	10	12	KΩ
R2	10	5.6	5.6	KΩ
R3	27	12	18	KΩ
R4	12	8.2	5.6	KΩ
R5	0.82	1	1	Ω
R6	270	330	330	Ω
R7	1.5	1.5	1.5	Ω
D1	1N 4001	1N 4001	1N 4001	–
C1	0.1	0.1	0.1	µF
C2 el.	1000/25 V	470/25 V	470/25 V	µF
C3 el.	220/25 V	220/25 V	220/25 V	µF
C4	0.22	0.22	0.22	µF
C5 el.	2200/25 V	2200/25 V	1000/16 V	µF
C6 el.	4.7/16 V	4.7/16 V	10/16 V	µF

TYPICAL PERFORMANCES

Parameter	110° TVC 5.9 Ω / 10 mH	110° TVC 9.6 Ω / 27 mH	90° TVC 15 Ω / 30 mH	Unit
V_s – Supply Voltage	24	22.5	25	V
I_s – Current	280	175	125	mA
t_{fly} – Flyback Time	0.6	1	0.7	ms
* P_{tot} – Power Dissipation	4.2	2.5	2.05	W
* $R_{th\ c-a}$ – Heatsink	7	13	16	°C/W
T_{amb}	60	60	60	°C
$T_{j\ max}$	110	110	110	°C
t_o	20	20	20	ms
V_i	2.5	2.5	2.5	Vpp
V_7	50	47	52	Vp

* Worst case condition.

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 4 : Mounting Examples.

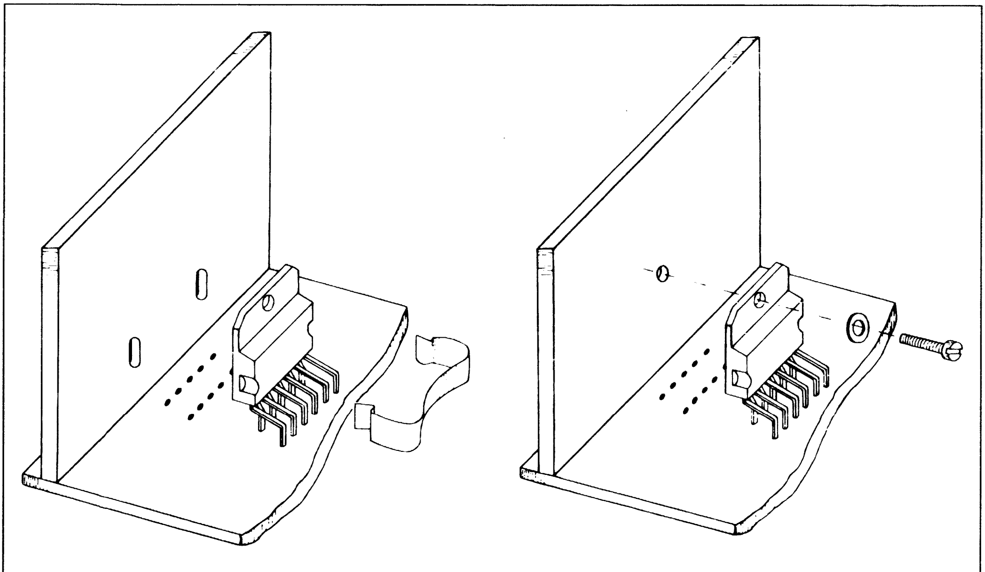
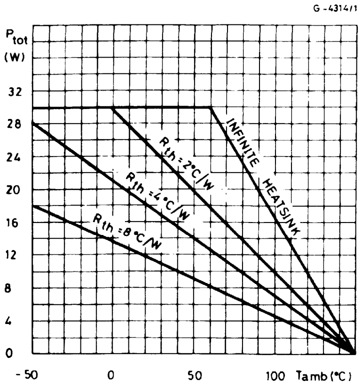
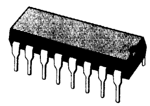


Figure 5 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- DRIVES VERTICAL DEFLECTION WINDINGS DIRECTLY
- HIGH EFFICIENCY
- INTERNAL FLYBACK GENERATOR
- THERMAL PROTECTION
- ON-CHIP VOLTAGE REFERENCE
- HIGH OUTPUT CURRENT (2.2 A peak)
- 16-LEAD POWERDIP PLASTIC PACKAGE



DIP16

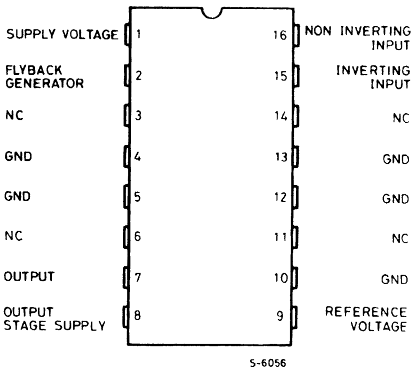
ORDER CODE : TDA2270

DESCRIPTION

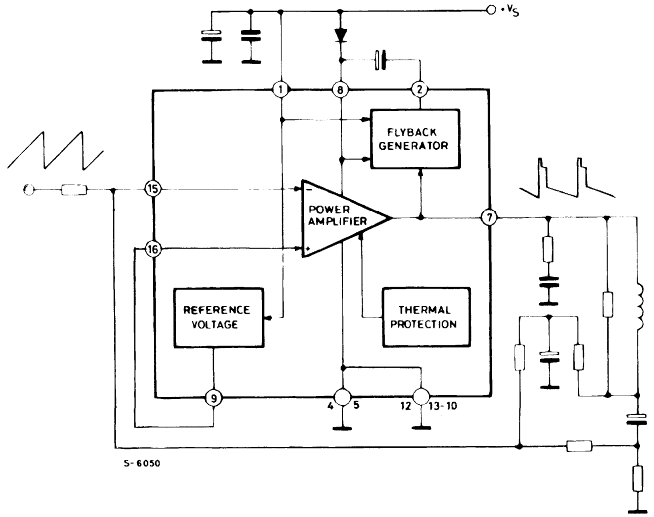
The TDA 2270 is a high efficiency monolithic output stage for vertical deflection circuits in TVs and monitors. Driving the vertical windings directly, the device contains a power amplifier, flyback generator, voltage reference and thermal protection circuit.

The TDA 2270 is supplied in a 16-pin DIP with the four center pins connected together and used for heatsinking.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	35	V
V_7, V_8	Flyback Peak Voltage	60	V
V_2	Voltage at Pin 2	$+ V_s$	
V_{15}, V_{16}	Amplifier Input Voltage	$+ V_s$ $- 0.5$	V
I_o	Output Peak Current (non repetitive, t = 2 ms)	2	A
I_o	Output Peak Current at f = 50 Hz, t ≤ 10 μs	2.2	A
I_o	Output Peak Current at f = 50 Hz, t > 10 μs	1.2	A
I_2	Pin 2 DC Current at $V_7 < V_1$	50	mA
I_2	Pin 2 Peak to Peak Flyback Current at f = 50 Hz, t_{fly} ≤ 1.5 ms	2	A
P_{tot}	Total Power Dissipation at T_{pins} ≤ 90 °C T_{amb} = 70 °C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	14	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction–ambient	Max	80	°C/W

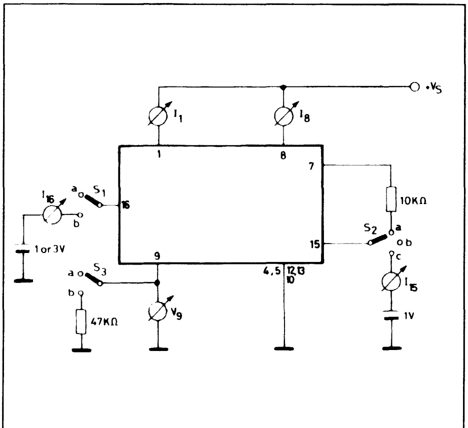
* Obtained with the GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS
(refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_1	Pin 1 Quiescent Current	I_2 = o ; I_7 = 0 ; V_{16} = 3 V		8	16	mA	1a
I_8	Pin 8 Quiescent Current	I_2 = 0 ; I_7 = 0 ; V_{16} = 3 V		16	36	mA	1a
I_{15}	Amplifier Input Bias Current	V_{15} = 1 V		– 0.1	– 1	µA	1a
I_{16}	Amplifier Input Bias Current	V_{16} = 1 V		– 0.1	– 1	µA	1a
V_{2L}	Pin 2 Saturation Voltage to GND	I_2 = 20 mA		1		V	1c
V_7	Quiescent Output Voltage	V_s = 35 V ; R_a = 39 KΩ		18		V	1d
		V_s = 15 V ; R_a = 13 KΩ		7.5		V	1d
V_{7L}	Output Saturation Voltage to GND	I_7 = 0.7 A		0.7	1	V	1c
V_{7H}	Output Saturation Voltage to Supply	– I_7 = 0.7 A		1.3	1.8	V	1b
V_9	Reference Voltage	I_9 = 0		2.2		V	1a
$\frac{\Delta V_9}{\Delta V_s}$	Reference Voltage Drift vs. Supply Voltage	V_s = 15 to 30 V		1	2	mV/V	1a
R_9	Reference Voltage Output Resistance			2.1		KΩ	
T_j	Junction Temperature for Thermal Shut Down			140		°C	

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_1 ; I_8 ; I_{15} ; I_{16} ; V_9 ; $\Delta V_9/\Delta V_S$; R_9 .



S1 : (a) I_{15} ; (b) I_{16}, I_7 and I_8.
S2 : (a) I_7 and I_8 ; (b) I_{16}, (c) I_{15}.
S3 : (a) I_{15}, I_{16}, I_7, I_8, I_9 and V_9 ; (b) R_9.

Figure 1b : Measurement of V_{7H}.

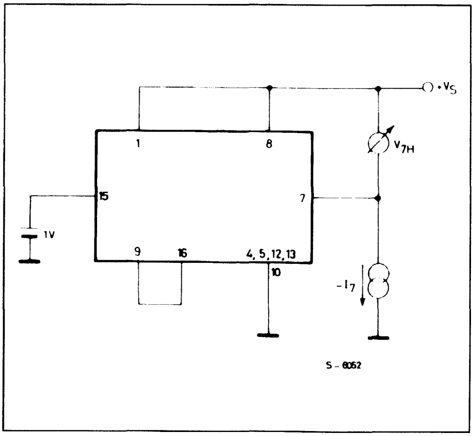


Figure 1c : Measurement of V_{2L} ; V_{7L}.

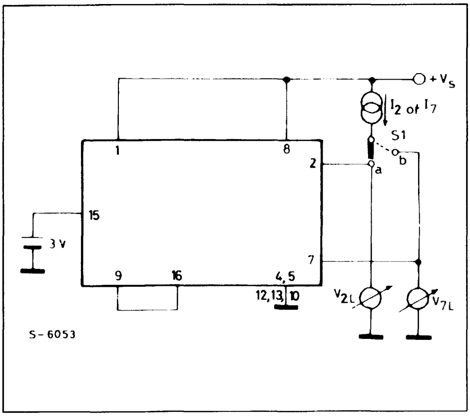
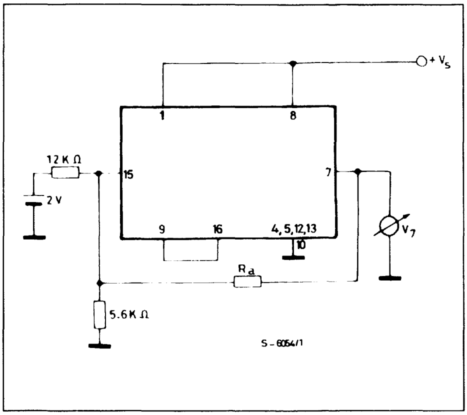


Figure 1d : Measurement of V7.



S1 : (a) V_{2L} ; (b) V_{7L}.

Figure 2 : Application Circuit.

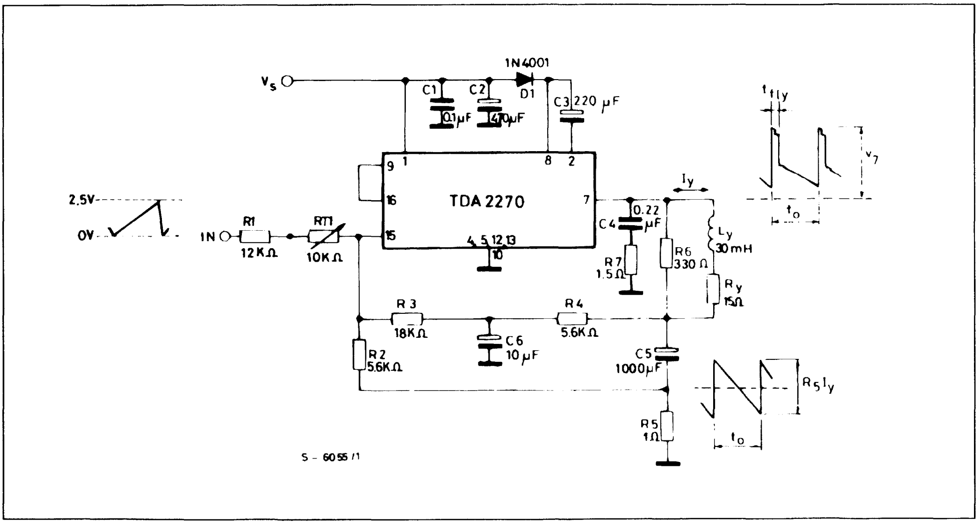
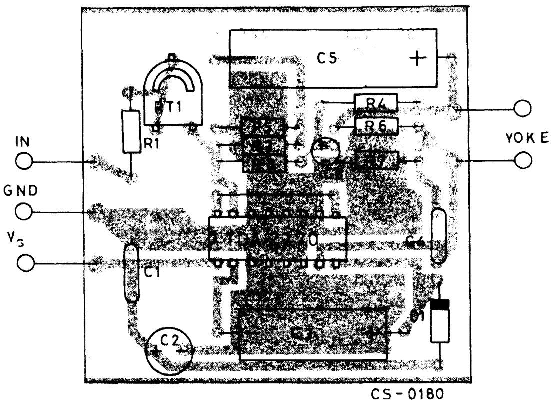


Figure 3 : PC Board and Component Layout (1 : 1 scale).



COMPONENTS LIST FOR TYPICAL APPLICATIONS (refer to the fig. 2)

Component	B/W TV 10 Ω / 20 mH / 1 App	90° TVC 15 Ω / 30 mH 0.82 App	Unit
RT1	10	10	KΩ
R1	10	12	KΩ
R2	5.6	5.6	KΩ
R3	15	18	KΩ
R4	6.8	5.6	KΩ
R5	1	1	Ω
R6	330	330	Ω
R7	1.5	1.5	Ω
D1	1N 4001	1N 4001	–
C1	0.1	0.1	μF
C2 el.	470/25 V	470/25 V	μF
C3 el.	220/25 V	220/25 V	μF
C4	0.22	0.22	μF
C5 el.	1000/25 V	1000/16 V	μF
C6 el.	10/16 V	10/16 V	μF

TYPICAL PERFORMANCE

Parameter	B/W TV 10 Ω / 20 mH / 1 App	90° TVC 15 Ω / 30 mH	Unit
V_s – Supply Voltage	20	25	V
I_s – Current	145	125	mA
t_{fly} – Flyback Time	0.75	0.7	ms
* P_{tot} – Power Dissipation	1.8	2.05	W
* $R_{th\ c-a}$ – Heatsink	14	12	°C/W
T_{amb}	60	60	°C
$T_{j\ max}$	130	130	°C
t_o	20	20	ms
V_i	2.5	2.5	Vpp
V_7 – Flyback Voltage	42	52	Vp

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 2270 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 4) or to an external heatsink (fig. 5).

The diagram of figure 6 shows the maximum dissipable power P_{tot} and the $R_{th\ j\text{-}amb}$ as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 4 : Example of P.C. Board Copper Area which is Used as Heatsink.

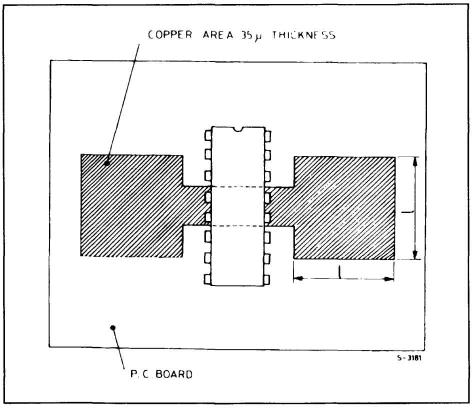


Figure 5 : External Heatsink Mounting Example.

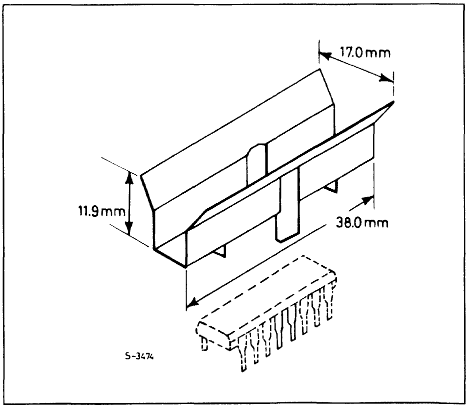


Figure 6 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l" .

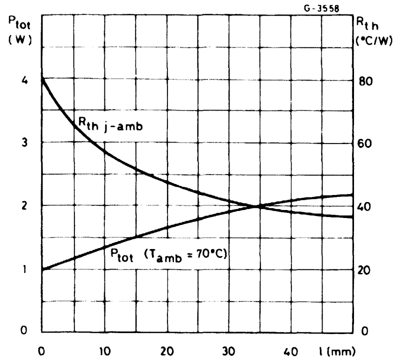
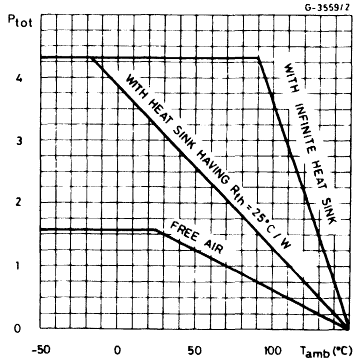


Figure 7 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



SGS-THOMSON MICROELECTRONICS

TDA2320

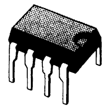
PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

DESCRIPTION

The TDA2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.

The TDA 2320 incorporates a two-stage amplifier with excellent sensitivity and high noise immunity. It can work with a single 5 V supply voltage and flash or carrier transmission modes as provided for example by the M709A/M710A/MOS transmitters.

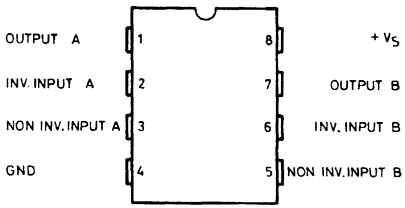
The TDA 2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.

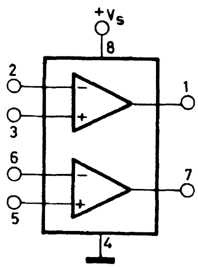


MINIDIP
(Plastic)

ORDER CODE : TDA2320

CONNECTION AND BLOCK DIAGRAM (top view)

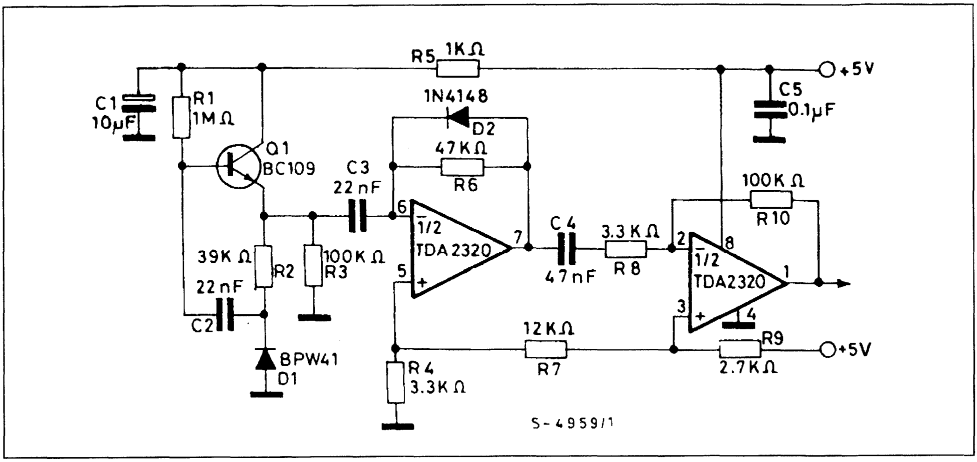




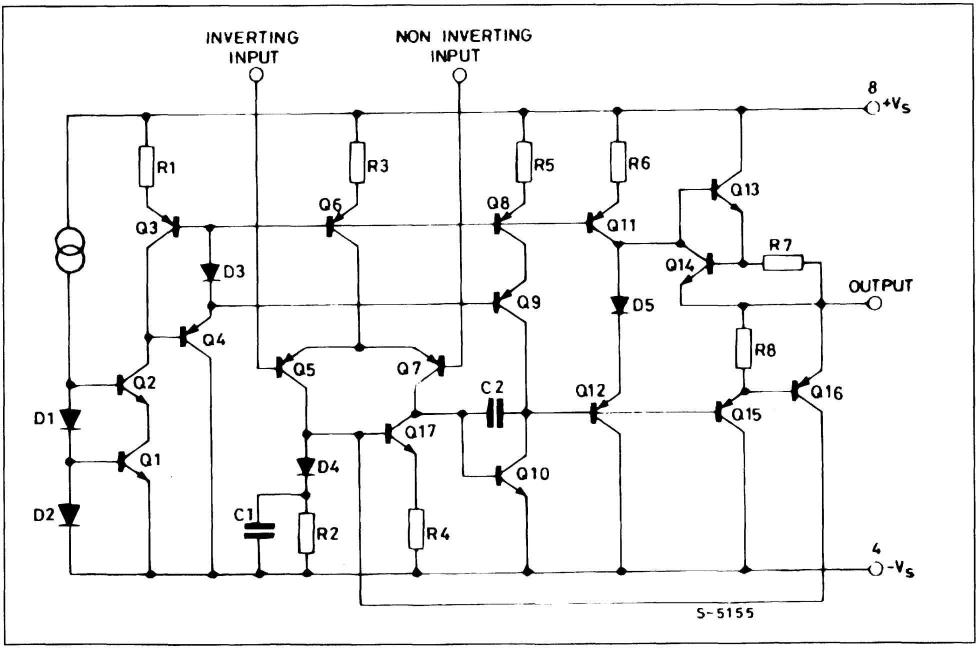
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	20	V
$T_{stg,j}$	Storage and Junction Temperature	– 40 to 150	°C
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	400	mW

APPLICATION CIRCUIT (Flash Mode Preamplifier)



SCHEMATIC DIAGRAM (One Section)



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max 200	°C/W

ELECTRICAL CHARACTERISTICS (V_S = 5 V, T_{amb} = 25 °C, single amplifier, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		20	V
I_S	Total Suppply Current	V_S = 20 V		0.8	2	mA
I_b	Input Bias Current			100	500	nA
V_{OS}	Input Offset Voltage	R_g < 10 KΩ		0.5		mV
I_{OS}	Input Offset Current			15		nA
G_V	Open Loop Voltage Gain	f = 1 KHz	64	70		dB
		f = 100 KHz		30		dB
B	Gain Bandwidth Product	f = 40 KHz	1.5	3		MHz
SR	Slew Rate	R_L = 2 KΩ		1.5		V/µs
e_N	Total Input Noise Voltage	f = 40 KHz R_g = 10 KΩ		20		nV/√Hz
V_o	DC Output Voltage Swing			2.5		Vpp
SVR	Supply Voltage Rejection	f = 100 Hz		80		dB

APPLICATION INFORMATION

Figure 1 : Application Circuit for Carrier Transmission Mode.

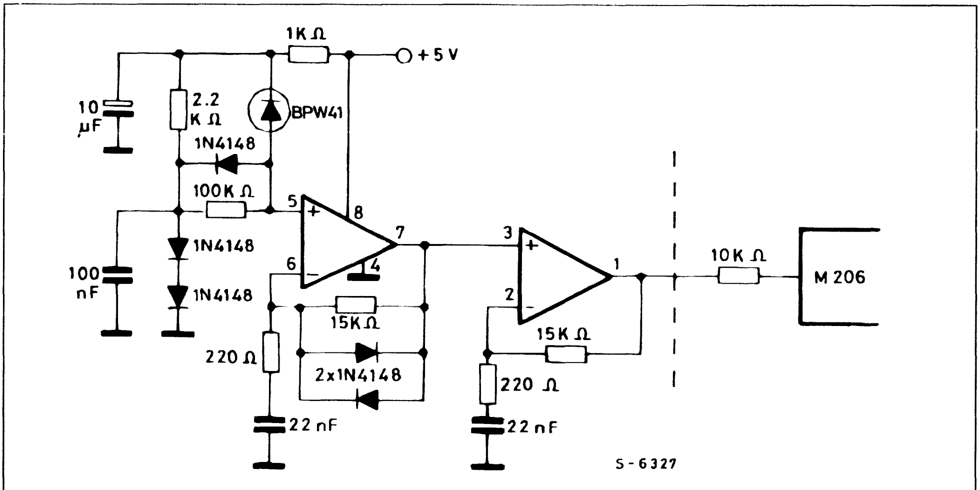


Figure 2 : Flash Mode Preamplifier.

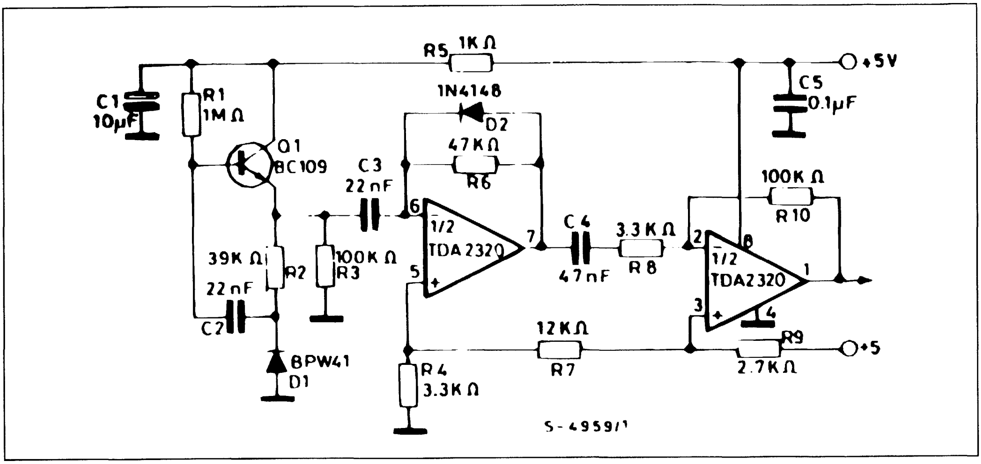


Figure 3 : P.C. and Components Layout of the Circuit of Figure 2 (1:1 scale).

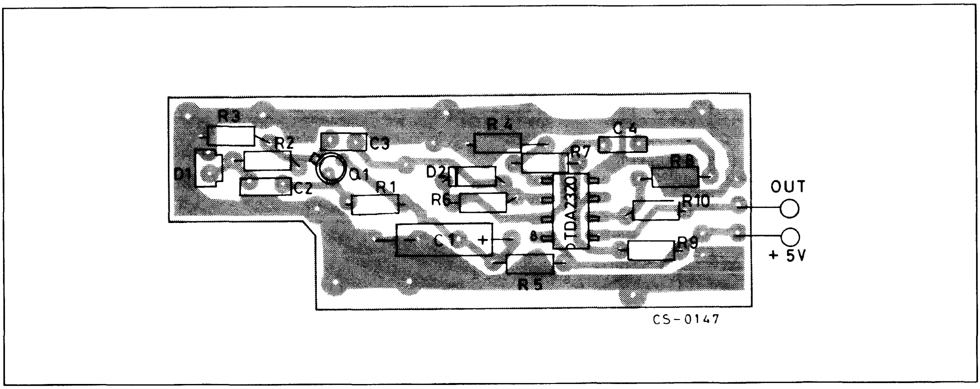


Figure 4 : IR Transmitter Using M709 or M710.

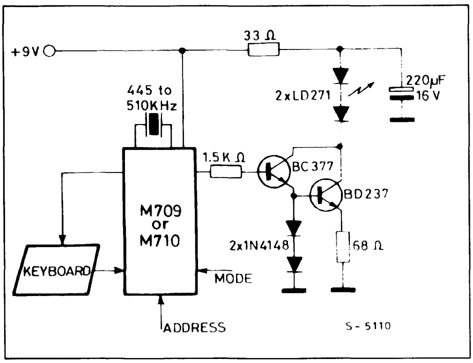


Figure 5 : MMC II - PLL TV Frequency Synthetizer.

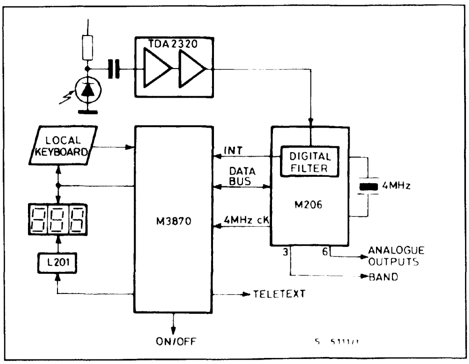
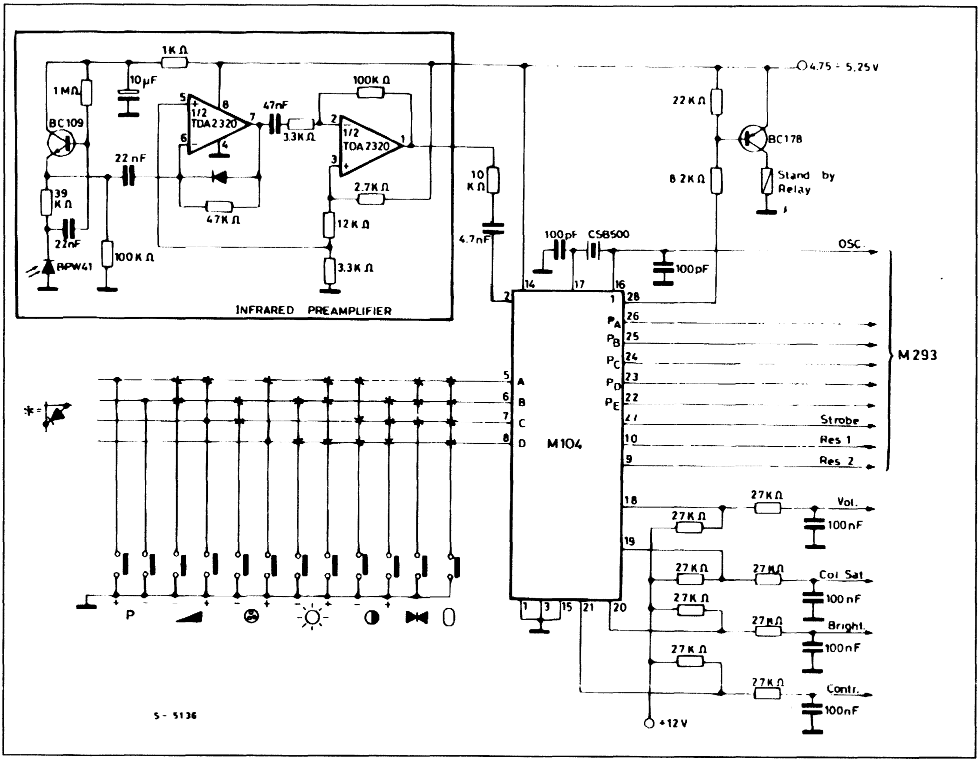


Figure 6 : IR Preamplifier and Remote Control Receiver for 32 Channel Voltage Synthetizer (EPM-M293).

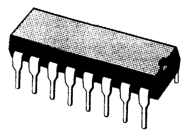


IF AMPLIFIER WITH DEMODULATOR AND AFC

- SUPPLY VOLTAGE : 12 V TYP
- SUPPLY CURRENT : 50 mA TYP
- I.F. INPUT VOLTAGE SENSITIVITY AT F = 38.9 MHz : 85 μV_{RMS} TYP
- VIDEO OUTPUT VOLTAGE (white at 10 % of top synchro) : 2.7 V_{pp} TYP
- I.F. VOLTAGE GAIN CONTROL RANGE : 64 dB TYP
- SIGNAL TO NOISE RATIO AT V_I = 10 mV : 58 dB TYP
- A.F.C. OUTPUT VOLTAGE SWING FOR Δf = 100 kHz : 10 V TYP

They incorporate the following functions :

- Gain controlled amplifier
- Synchronous demodulator
- White spot inverter
- Video preamplifier with noise protection
- Switchable AFC
- AGC with noise gating
- Tuner AGC output (NPN tuner for 2540)-(PNP tuner for 2541)
- VCR switch for video output inhibition (VCR play back)

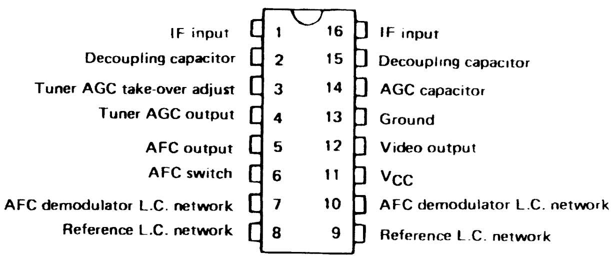


TDA2540-TDA2541
DIP16
(Plastic Package)

DESCRIPTION

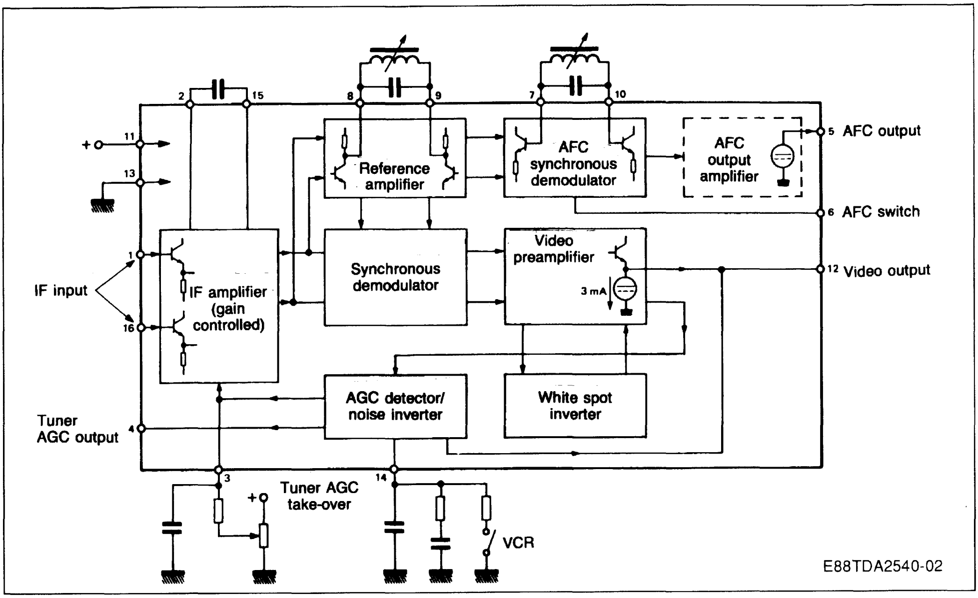
The TDA2540 and 2541 are IF amplifier and A.M. demodulator circuits for colour and black and white television receivers using PNP or NPN tuners. They are intended for reception of negative or positive modulation CCIR standard.

PIN CONNECTIONS



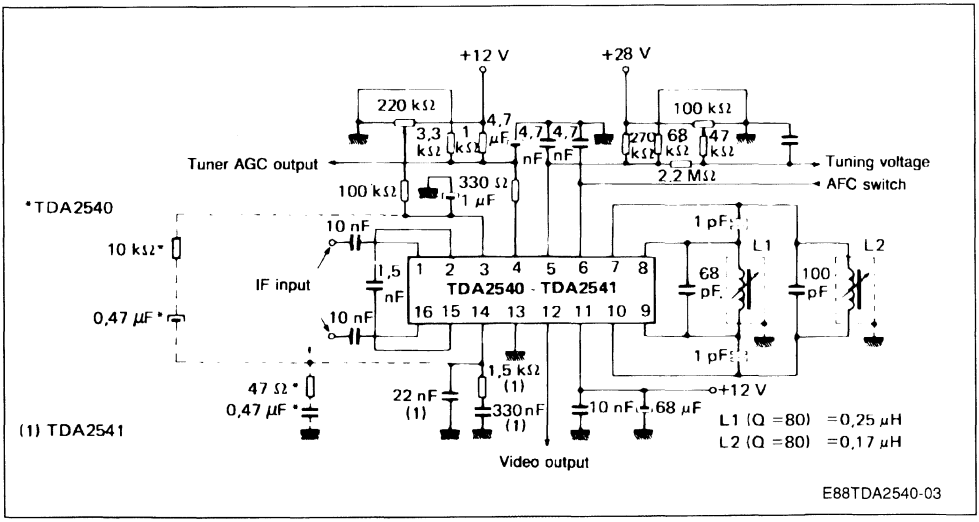
E88TDA2540-01

BLOCK DIAGRAM



E88TDA2540-02

APPLICATION CIRCUIT



E88TDA2540-03

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V (11–13)	Supply Voltage	13.8	V
V (4–13)	Tuner A.G.C. Voltage	12	V
P_{tot}	Power Dissipation	900	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_{amb}	Operating Ambient Temperature	0 to + 70	°C

THERMAL DATA

R_{th}(j-a)	Junction - ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V (11 – 13) = 12 V; f = 38.9 MHz (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V (11-13)	Supply Voltage Range	10.2	12	13.8	V
I_{11}	Supply Current		50	60	mA
V (1-16)	IF Input Voltage Sensitivity	60	85	180	µVRMS
	Max Input Voltage (pins 1-16)		140		mV
V (12-13)	Video Output Voltage		2.7		V_{pp}
Z (1-16)	Differential Input Impedance (in parallel with 2 pF)		2		kΩ
V (12-13)	Zero Signal Output Level	5.7	6	6.3	V
V (12-13)	Top Synchro Output Level	2.9	3.07	3.2	V
ΔG_V	IF Voltage Gain Control Range	52	64		dB
S/N	Signal to Noise Ratio (V_I = 10 mV) (see note 1)	50	58		dB
B	Bandwidth of Video Amplifier (– 3 dB)		6		MHz
dG	Differential Gain		4	10	%
dφ	Differential Phase		2	10	%
V (12-13)	Carrier Signal at Video Output (V_I = 10 mV)		4	30	mVRMS
V (12-13)	2nd Harmonic of Carrier at Video Output (V_I = 10 mV)		20	30	mVRMS
	Intermodulation at 1.1 MHz (blue) (see figures 2 and 3)	46	60		dB
	Intermodulation at 1.1 MHz (yellow) (see figures 2 and 3)	46	50		dB
	Intermodulation at 3.3 MHz (blue) (see figures 2 and 3)	46	54		dB

Note : 1. $S/N = \frac{V_O \text{ (black to white)}}{V_N \text{ . (RMS at B = 5 MHz)}}$ (dB)

ELECTRICAL OPERATING CHARACTERISTICS(continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V (14-13)	VCR Switches Off Output at : (VCR = low Level)			1.1	V
	White Spot Inverter Threshold Level (see figure 1)		6.6		V
	White Spot Insertion Level (see figure 1)		4.7		V
	Noise Inverter Threshold Level (see figure 1)		1.8		V
	Noise Insertion Level (see figure 1)		3.8		V
I 4	Tuner AGC output Current Range		0 to 10		mA
V (14-13)	Tuner AGC Output Voltage			0.3	V
I 4	Tuner AGC Output Leakage Current TDA2541 V 14-13 = 11 V V 4-13 = 12 V TDA2540 V 14-13 = 5 V V 4-13 = 12 V			15	µA
ΔV (5-13)	AFC Output Voltage Swing (Δf = 100 kHz)	10	11		V
Δf	Change of Frequency at AFC Output (voltage swing of 10 V)		100	200	kHz
V (6-13)	AFC Switches OFF (AFC = low level) at :			2.5	V
V (6-13)	AFC Switches LOW (AFC = High level) at :	3.2			V
V (5-13)	AFC Zero = Signal Output Voltage (minimum gain)	4	6	8	V

Note : 1. $S/N = \frac{V_O \text{ (black to white)}}{V_N \text{ . (RMS at B = 5 MHz)}}$ (dB)

Figure 1 : Video Output Waveform Showing White Spot and Noise Inverter Threshold Levels.

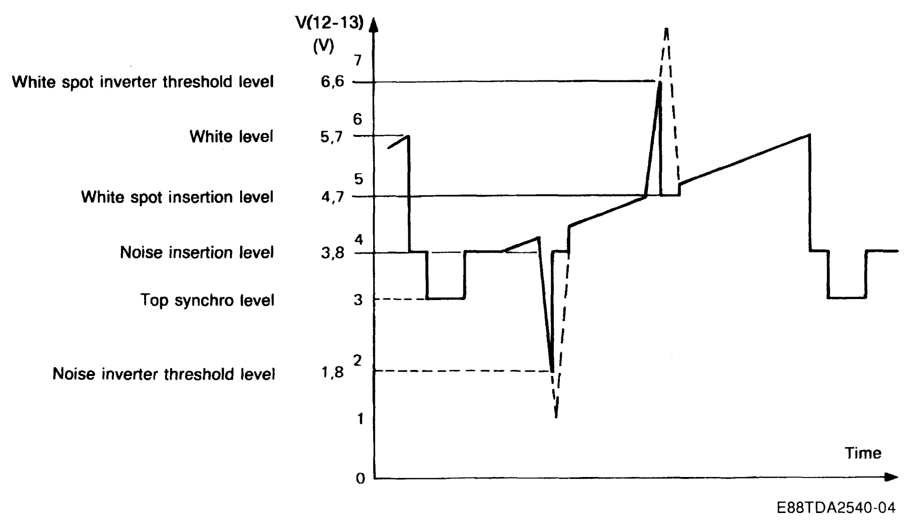


Figure 2 : Input Conditions for Intermodulation Measurements.

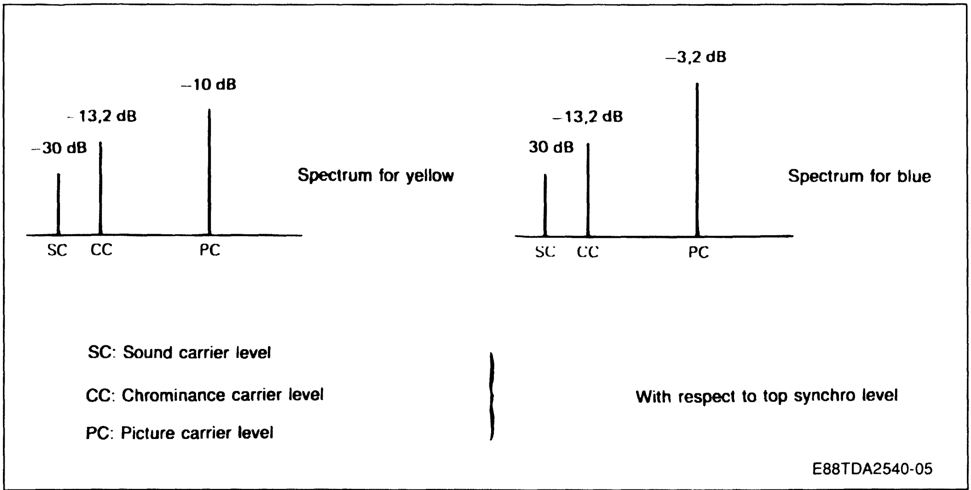
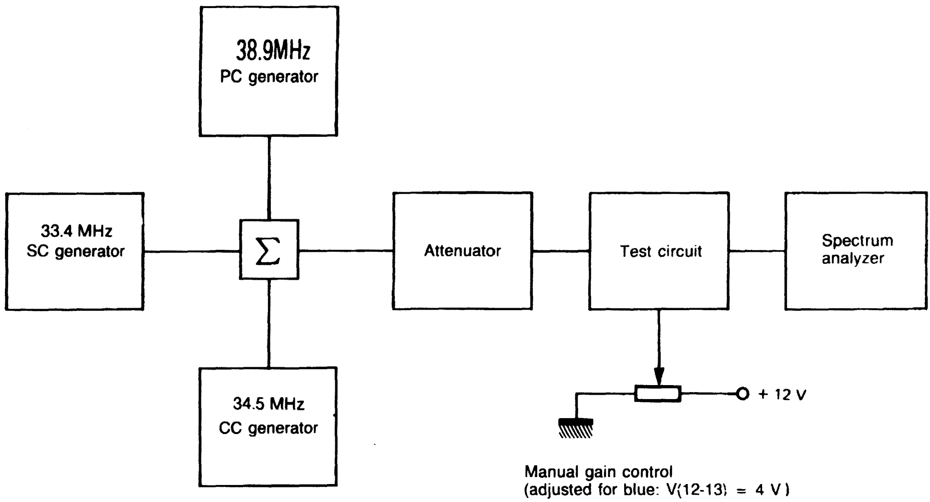


Figure 3 : Test Set-up for Intermodulation.



$$\text{Intermodulation 1.1 MHz} = 20 \log \left(\frac{V_O \text{ at 4.4 MHz}}{V_O \text{ at 1.1 MHz}} \right) + 3.6 \text{ dB}$$

$$\text{Intermodulation 3.3 MHz} = 20 \log \left(\frac{V_O \text{ at 4.4 MHz}}{V_O \text{ at 3.3 MHz}} \right)$$

E88TDA2540-06

Figure 4 : AFC Voltage Versus Frequency V(5-13).

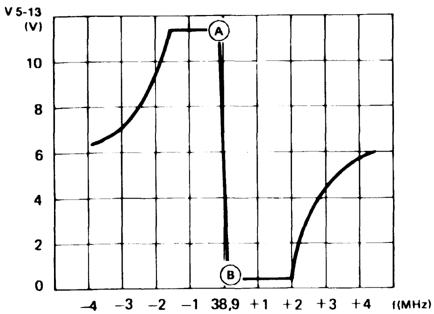


Fig. 4 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

E88TDA2540-07

Figure 5 : AFC Voltage Versus Frequency V(5-13).

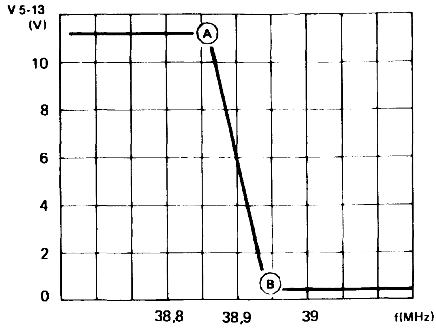


Fig. 5 — AFC VOLTAGE VERSUS FREQUENCY V 5-13

E88TDA2540-08

Figure 6 : Signal/Noise Ratio Versus Input Voltage V(1-16).

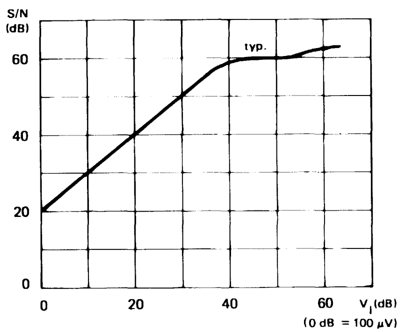
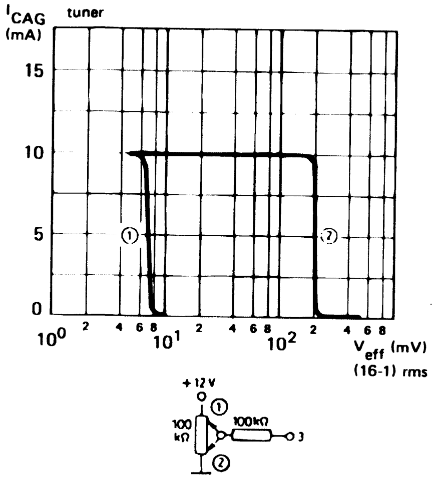


Fig. 6 — SIGNAL/NOISE RATIO VERSUS INPUT VOLTAGE V 1-16

E88TDA2540-09

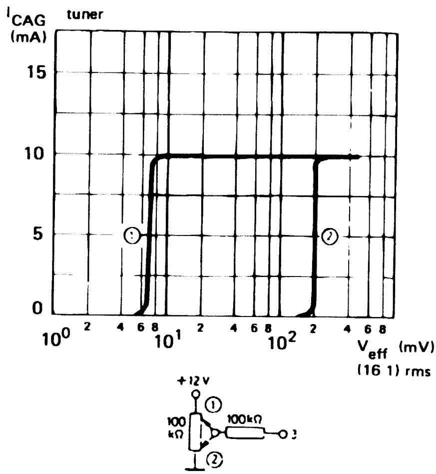
Figure 7 : AGC Tuner Current Curve.

TDA2540



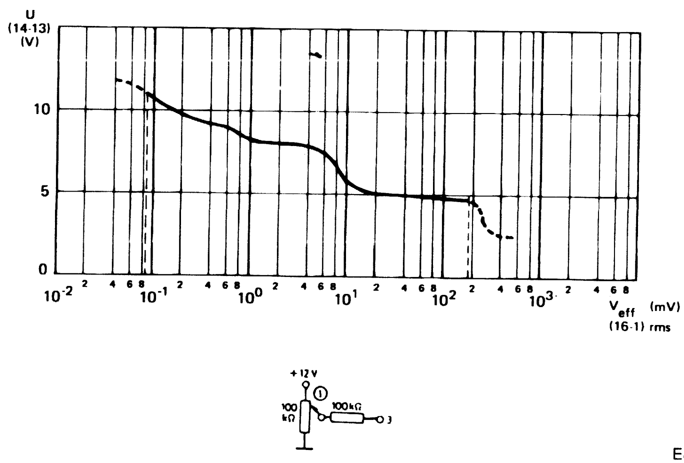
E88TDA2540-10

TDA2541



E88TDA2540-11

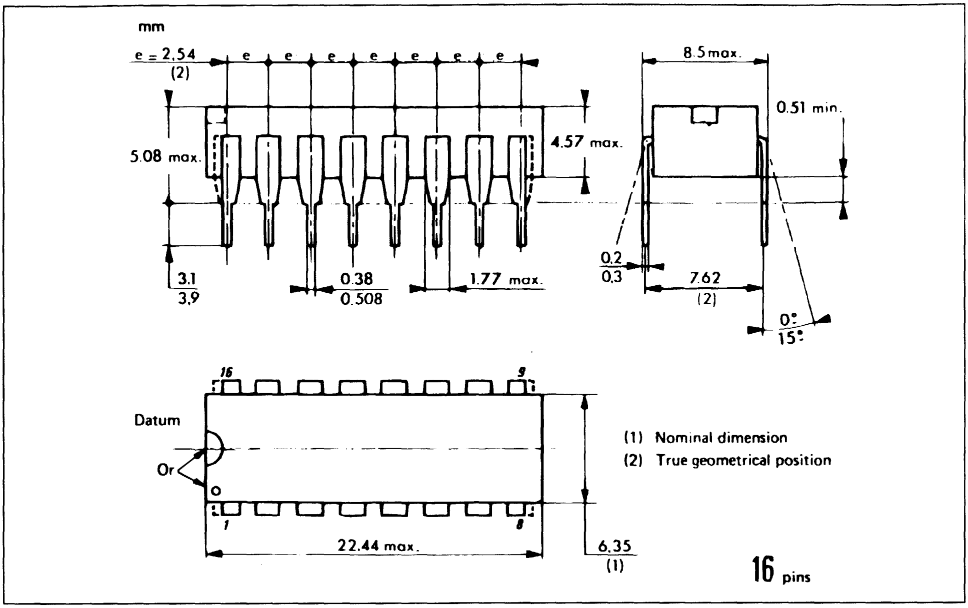
TDA2540-TDA2541



E88TDA2540-12

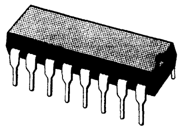
PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



IF AMPLIFIER WITH DEMODULATOR AND AFC FOR POSITIVE MODULATION STANDARD

- SUPPLY VOLTAGE : 12 V TYP
- SUPPLY CURRENT : 50 mA TYP
- IF INPUT VOLTAGE SENSITIVITY AT f = 32.7 MHz : 85 μV_{RMS} TYP
- VIDEO OUTPUT VOLTAGE : 2.5 V_{pp} TYP
- IF VOLTAGE GAIN CONTROL RANGE : 64 dB TYP
- SIGNAL TO NOISE RATIO AT V_I = 10 mV : 58 dB TYP
- A.F.C. OUTPUT VOLTAGE SWING FOR Δf = 100 kHz : 10 V TYP



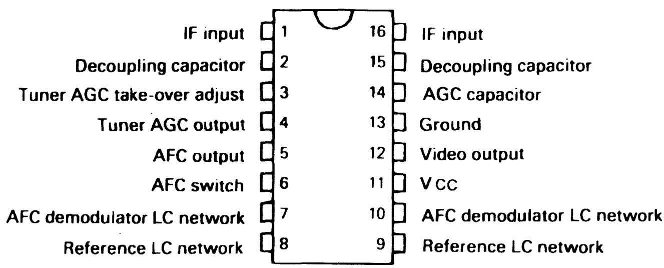
TDA2542
DIP16
(Plastic Package)

DESCRIPTION

The TDA2542 is an IF amplifier and AM demodulator circuit for colour and black and white television receivers using PNP tuners. It is intended to reception positive modulation for french standard.

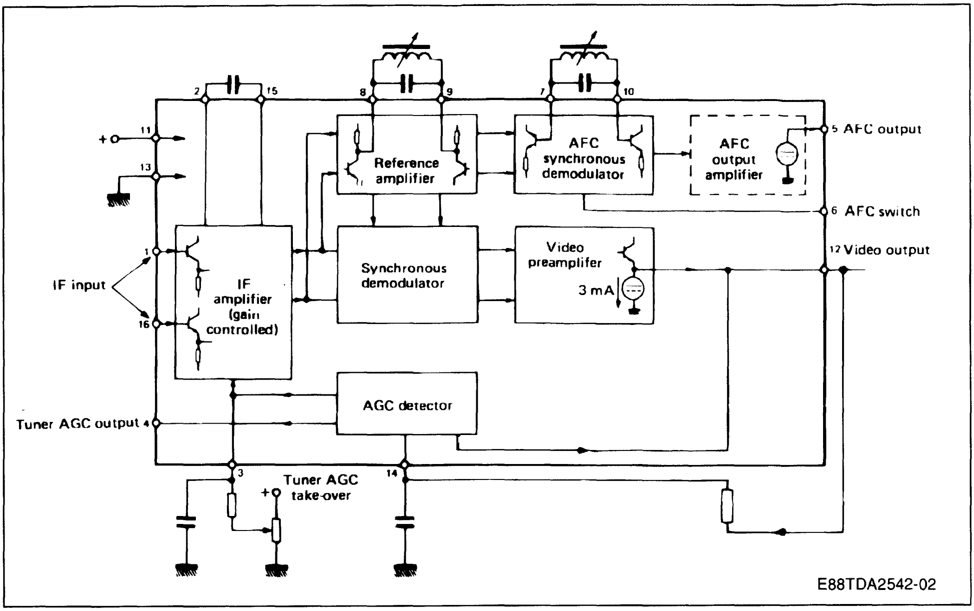
It incorporates the following functions
- Gain controlled amplifier
- Synchronous demodulator
- Video preamplifier
- Switchable AFC
- AGC
- Tuner AGC output (PNP tuner)

PIN CONNECTIONS

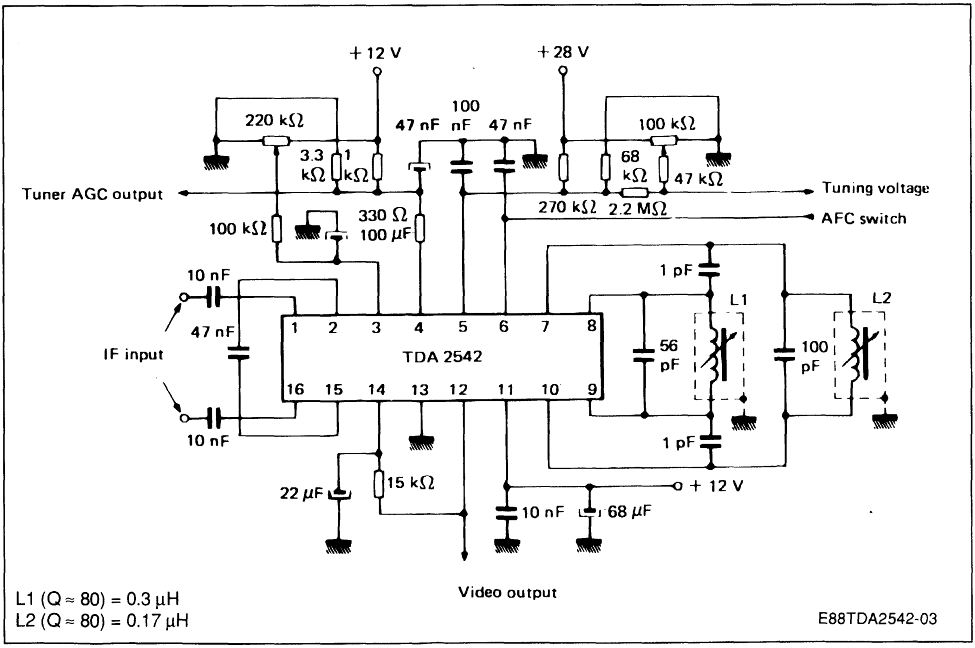


E88TDA2542-01

BLOCK DIAGRAM



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V (11-13)	Supply Voltage	13.8	V
V (4-13)	Tuner A.G.C. Voltage	12	V
P_{tot}	Power Dissipation	900	mW
T_{stg}	Storage Temperature	– 55 to + 125	°C
T_{amb}	Operating Ambient Temperature	0 to + 70	°C

THERMAL DATA

R_{th}(j-a)	Junction - ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C; V(11 – 13) = 12 V; f = 32. 7 MHz (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V(11-13)	Supply Voltage Range	10.2	12	13.8	V
I11	Supply Current	40	50	58	mA
V(1-16)	IF Input Voltage Sensitivity		85	160	µVRMS
	Max Input Voltage (pins 1-16)		140		mV
V(12-13)	Video Output Voltage		2.5		V_{pp}
Z 1-16	Differential input Impedance (in parallel with 2 pF)		2		kΩ
V(12-13)	Zero Signal Output Level		2.9		V
ΔG_V	IF Voltage Gain Control Range		64		dB
S/N	Signal to Noise (see note 1) (V_I = 10 mV)		58		dB
B	Bandwidth of Video Amplifier (– 3 dB)		6		MHz
dG	Differential Gain		4	10	%
dϕ	Differential Phase		2	10	%
V(12-13)	Carrier Signal at Video Output		4	30	mVRMS
V(12-13)	2nd Harmonic of Carrier at Video Output		20	30	mVRMS
V 14	Reference Voltage of AGC Detector		3.9		V
I 4	Tuner AGC Output Current Range		0 → 10		mA
V(4-13)	Tuner AGC Output Voltage (I 4 = 10 mA)			0.3	V
I 4	Tuner AGC Output Leakage Current (V(14-13) = 11 V ; V(4-13) = 12 V)			15	µA
V(5-13)	AFC Output Voltage Swing (Δf = 100 kHz)	10	11		V
Δf	Change of Frequency at AFC Output (voltage swing of 10 V)		100	200	kHz
V(6-13)	AFC Switches ON (AFC = high level) at	3.2			V
V(6-13)	AFC Switches OFF (AFC = low level)at			1.5	V

Note : 1. $S/N = \frac{V_O \text{ (black to white)}}{V_n \text{ . (RMS at B = 5 MHz)}}$ (dB)

Figure 1 : AFC Voltage versus Frequency V(5-13).

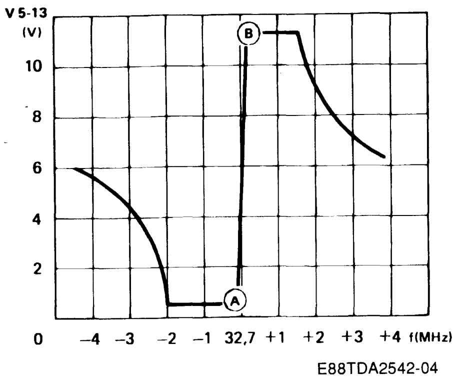


Figure 2 : AFC Voltage versus Frequency V(5-13).

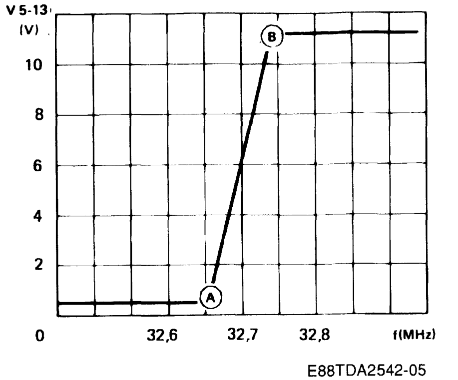


Figure 3 : Signal/Noise Ratio versus Input Voltage V(1-16).

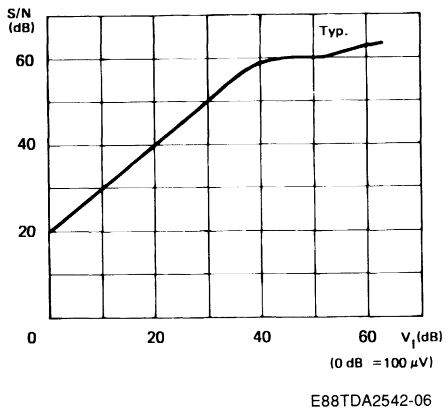
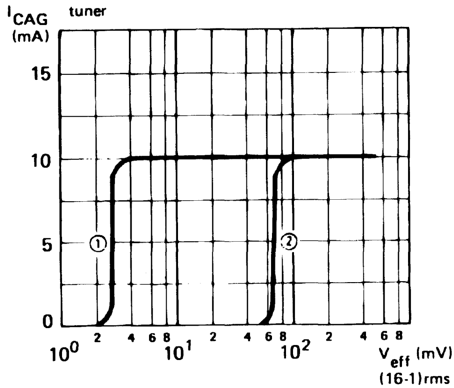
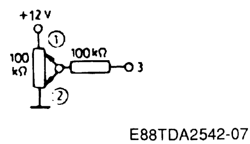


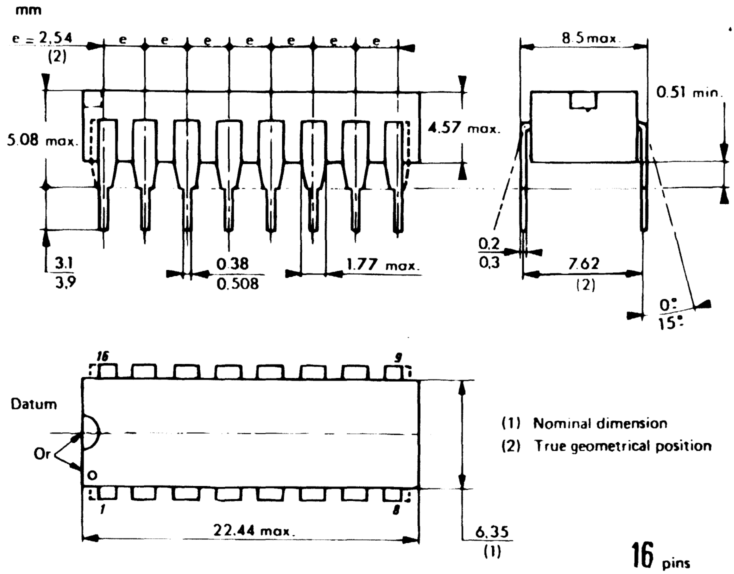
Figure 4 : AGC Tuner Current Curve.





PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

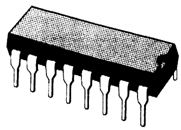
TDA2593

SYNCHRO AND HORIZONTAL DEFLECTION CONTROL FOR COLOR TV SET

- LINE OSCILLATOR (two levels switching)
- PHASE COMPARISON BETWEEN SYNCHRO-PULSE AND OSCILLATOR VOLTAGE Ø 1, ENABLED BY AN INTERNAL PULSE, (better parasitic immunity)
- PHASE COMPARISON BETWEEN THE FLY-BACK PULSES AND THE OSCILLATOR VOLTAGE Ø 2
- COINCIDENCE DETECTOR PROVIDING A LARGE HOLD-IN-RANGE
- FILTER CHARACTERISTICS AND GATE SWITCHING FOR VIDEO RECORDER APPLICATION
- NOISE GATED SYNCHRO SEPARATOR
- FRAME PULSE SEPARATOR
- BLANKING AND SAND CASTLE OUTPUT PULSES
- HORIZONTAL POWER STAGE PHASE LAGGING CIRCUIT
- SWITCHING OF CONTROL OUTPUT PULSE WIDTH
- SEPARATED SUPPLY VOLTAGE OUTPUT STAGE ALLOWING DIRECT DRIVE OF SCR'S CIRCUIT
- SECURITY CIRCUIT MAKES THE OUTPUT PULSE SUPPRESSED WHEN LOW SUPPLY VOLTAGE

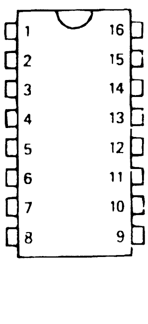
DESCRIPTION

The TDA2593 is a circuit intended for the horizontal deflection of color TV sets, supplied with transistors or SCR'S.



TDA2593
DIP16
(Plastic Package)

PIN CONNECTIONS



1 - Supply Voltage
2 - Output stage supply voltage
3 - Output pulse
4 - Selection of output pulse duration
5 - Decoupling
6 - Reference pulse (fly-back) for The 2nd phase comparator
7 - Sand castle pulse
8 - Vertical synchro output
9 - Synchro separator output
10 - Noise separator input
11 - V.C.R. switching
12 - Time constant switching
13 - First phase comparator output
14 - Ramp oscillator capacitance
15 - Adjustment of the charge current
16 - Ground

E88TDA2593-01

MAIN CHARACTERISTICS

Symbol	Parameter	Typ.	Unit
V(1–16)	Supply Voltage	12	V
I(1)	Supply Current	30	mA
	Input Signals		
V(9–16) (pp)	Synchro Separator Input Voltage	3 to 4	V
V(10-16) (pp)	Noise Separators Input Voltage	3 to 4	V
	Control Voltage of the Output Pulse Switching Circuit		
V(4–16)	t = 7 µs (thyristor)	9.4 to V(1–16)	V
V(4–16)	t = 14 µs + t_d (transistor)	0 to 3.5	V
V(4–16)	t = 0 (V(3–16) = 0)	5.4 to 5.6	V
	Output Signals		
V(8–16) (pp)	Frame Synchro Pulse	11	V
V(7–16) (pp)	Sandcastle Pulse	11	V
V(3–16) (pp)	Horizontal Driver Stage Control Pulse	10.5	V

ABSOLUTE MAXIMUM RATINGS

Maximum Ratings According to CEI 134 Data Sheet

Symbol	Parameter	Value	Unit
V(1–16)	Supply Voltage to Pin 1	13.2	V
V(2–16)	Supply Voltage to Pin 2	18	V
V(4–16)	Voltage to Pin 4	13.2	V
V(9–16)	Voltage to Pin 9	± 6	V
V(10–16)	Voltage to Pin 10	± 6	V
V(11–16)	Voltage to Pin 11	13.2	V
$I_{2M} = - I_{3M}$	Current at Pins 2 and 3 (with thyristor)	650	mA
$I_{2M} = I_{3M}$	Current at Pins 2 and 3 (with transistor)	400	mA
I(4)	Current to Pin 4	1	mA
I(6)	Current to Pin 6	± 10	mA
I(7)	Current to Pin 7	– 10	mA
I(11)	Current to Pin 11	2	mA
P_{tot}	Power Dissipation	800	mW
T_{amb}	Operating Ambient Temperature	– 20 to + 70	°C
T_{stg}	Storage Temperature	– 25 to + 125	°C

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V1–V16 = 12 V (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit
V(9–16)	Input Signals Synchro Separator (pin 9) Input Threshold Voltage		0.8		V
I(9)	Input Threshold Current			5	µA
I(9)	On-state Input Current		5 to 100		µA
I(9)	Disconnect Input Current	100	150		µA
I(9)	Off-state Input Current (V(9–16) = – 5 V)			– 1	µA
V(9)	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		Vpp
V(10–16)	Noise Separator (pin 10) Input Threshold Voltage		1.4		V
I(10)	Input Threshold Current	100	150		µA
I(10)	Input Current		5 to 100		µA
I(10)	Off-state Input Current (V(10–16) = – 5 V)			– 1	µA
V(10)	Video Input Signal (positive synchro pulses) (note 1)		3 to 4		Vpp
V(10)	Allowed superimposed parasitic signal			7	V
V(6–16)	Fly-back Pulse (pin 6) Input Threshold Voltage		1.4		V
V(6)	Input Limitation Level		– 0.7 and + 1.4		V
I(6)	Input Current	0.01	1	2	mA
V(4–16) V(4–16) V(4–16)	Output Pulse Width Control Switch (pin 4) Input Voltage t = 7 µs (thyristor) t = 14 µs + t_d (transistor) t = 0 (V3–16 = 0) (note 2)		 9.4 to V(1–16) 0 to 3.5 5.4 to 6.6		 V V V
I(4) I(4) I(4)	Input Current t = 7 µs (thyristor) t = 14 µs + t_j (transistor) t = 0 (V3–16 = 0)	200 200	 0		µA µA
V(11–16)	Video Recorder Switch (pin 11) Input Voltage (pin 11 low level) (pin 11 to + V_{CC})		 0 to 2.5 9 to V(1–16)		 V V
I(11) I(11)	Input Current (pin 11 low level) (pin 11 to + V_{CC})			200 2	µA mA
V(8–16)	Output Signals Frame Synchro Pulses (positive) (pin 8) Output Voltage (peak value)	10	11		V
R(8)	Output Impedance		2		kΩ
t_{on}	Delay Between Leading Edge of Input Signal and Leading Edge of Output Signal		15		µs
t_{off}	Delay Between Trailing Edge of Input Signal and Trailing Edge of Output Signal		15		µs

Notes : 1. Allowed range 1 to 7 V.
2. Or pin 4 not connected.

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = 25 °C, V_1–V_{16} = 12 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V(7–16)	Sandcastle Pulse (positive) (pin7) Output Voltage (peak valve)	10	11		V
R(7)	Output Impedance		70		Ω
I(7)	Output Current During Trailing Edge		2		mA
t_7	Sandcastle Pulse Width (V7 = 7 V)	3.7		4.3	µs
Δ_t	Phase Between Middle Input Synchro Pulse and Leading Edge of Sandcastle Pulse (V7 = 7 V)	2.15		3.15	µs
V(7–16)	Fly-back Blanking Pulse (pin 7) Output Voltage (peak value)	4		5	V
R(7)	Output Impedance		70		Ω
I(7)	Output Current During Trailing Edge		2		mA
V(3–16)	Control Pulse for Horizontal Driver (positive) (pin 3) Output Voltage (peak value)		10.5		V
R(3) R(3)	Output Impedance (leading edge) (trailing edge)		2.5 20		Ω Ω
t_3 t_3	Control Pulse Width V4 = 9.4 to V(1–16) V4 = 0 to 4 V (note 3)	5.5	 14 + t_c	8.5	µs µs
V(1–16)	Control pulse is disabled for		4		V
t_z	Overall Phase Relation Ship Phrase Between Middle Synchro Pulse and Middle Fly-back Pulse t_r = 12 µs (note 4)	1.9		3.3	µs
ΔI/Δt	Sensitivity to Current Adjust		30		µA/µs
V(14–16) V(14–16)	Oscillator (pins 14 and 15) Threshold Voltage (low level) (high level)		 4.4 7.6		 V V
I(14)	Current Generator		± 0.47		mA
f	Free Running Frequency (C_{osc} = 4700 pF R_{osc} = 12 kΩ)		15625		Hz
Δf	Tolerance on Frequency (note 5)			± 5	%
Δf/15	Frequence Control Sensitivity		31		Hz/µA
Δf	Spread of Frequency		± 10		%
$\frac{\Delta f/f}{\Delta V/V\ nom.}$	Influence of Supply Voltage on Frequency (note 5)			± 0.05	%
Δf	Frequency change when decreasing the supply down to 5 V V(1–16) = 5V (note 5)			± 10	%
T	Frequency Temperature Coefficient (note 5)			$\pm 10^{-4}$	Hz/°C
V(13–16)	Phase Comparator ø 1 (pin 13) Control Voltage Range		3.8 to 8.2		V
I(13) I(13)	Control Current (peak value) Off-state Current (V (13–16) = 4 to 8 V)		± 1.9 to ± 2.3	 – 1	mA µA

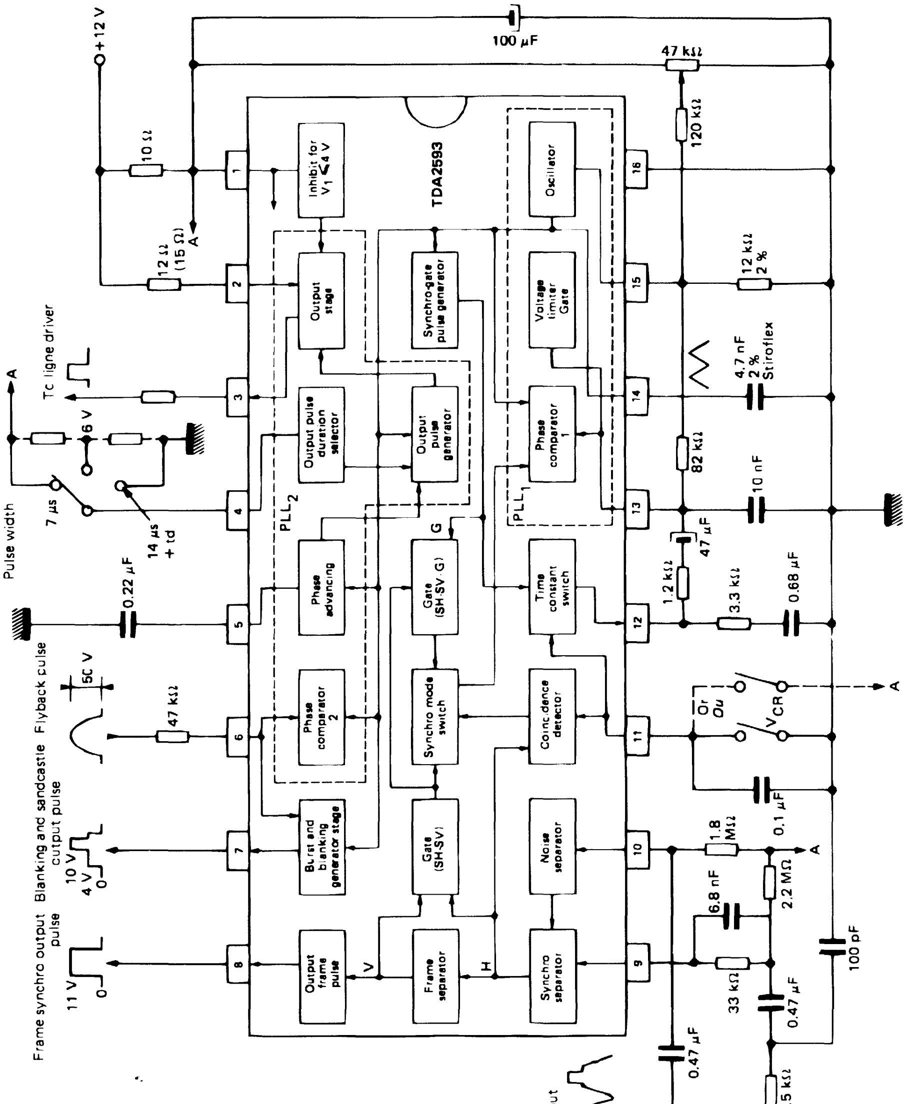
Notes : 3. With t_r = 12 µs.
4. The adjustement of overall phase relation (and output pulse leading edge position) is automatically performed by phase comparator Ø 2. If additional adjustement is needed, a current have to be imposed at pin 5.
5. Tolerance of peripheral components not included.

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = 25 °C, V_1–V_{16} = 12 V (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit
R(13) R(13)	Output Impedance (V(13–16) = 4 to 8 V (note 6)) (V(13–16) < 3.8 V cr > 8.2 V (note 7))		High Low		
	Control Sensibility		2		kHz/µs
Δf	Catching and Holding Range		± 780		Hz
Δf/f	Catching and Holding Range Tolerance (note 5)		± 10		%
V(5–16)	Phase Comparator φ 2 and Phase-shift (pin 5) Control Voltage Range		5.4 to 7.6		V
I(5)	Control Current (peak value)		± 1		mA
I(5)	Off-state Output Current (V (5–16) = 5.4 to 7.6 V)			– 5	µA
R(5) R(5)	Output Impedance (V (5–16) = 5.4 to 7.6 V (note 6)) (V (5–16) < 5.4 V or > 7.6 V)		High 8		kΩ
t_d	Max. delay Between Output Pulse Leading Edge and Fly-back Pulse Trailing Edge (t_r = 12 µs)			15	µs
$\Delta_t/\Delta t_d$	Static Control Error			0.2	%
V(11–16)	Coïncidence Detector (pin 11) Output Voltage		0.5 to 6		V
I(11) I(11)	Output Current (without coïncidence) (with coïncidence)		0.1 – 0.5		mA mA
V(12–16)	Time Constant Switch (pin 12) Output Voltage		6		V
I(12)	Output Current		± 1		mA
R(12) R(12)	Output Impedance (V (11–16) = 2.5 to 7 V) (V (11–16) < 1.5 or > 9 V)		100 60		Ω kΩ
t	Pulse Generator (internal) Pulse Width		7.5		µs

Notes : 6. Current generator.
7. Emitter-follower.

BLOCK DIAGRAM AND TYPICAL APPLICATION

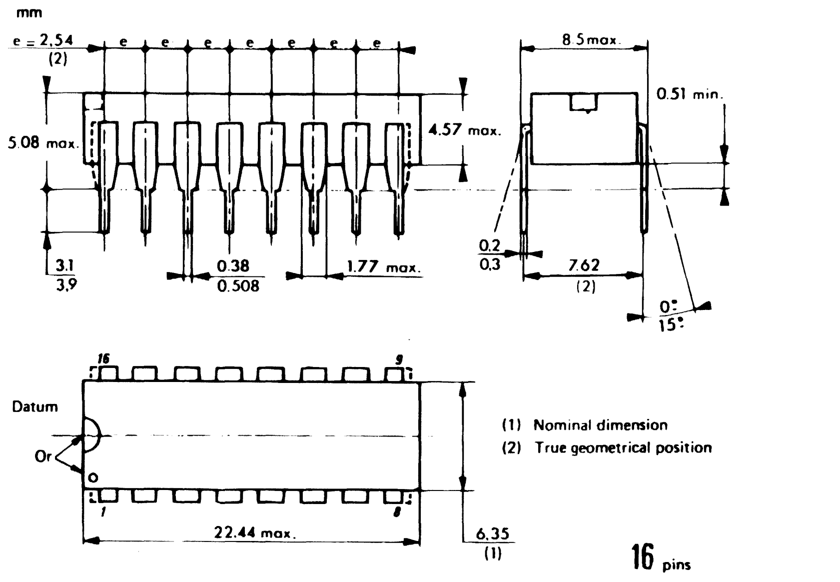


PLL 1 : Phase locked loop 1
PLL 2 : Phase locked loop 2 (with power stage)

E88TDA2593-02

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



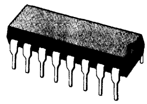
SGS-THOMSON MICROELECTRONICS

TDA3190

COMPLETE TV SOUND CHANNEL

The TDA3190 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It performs all the functions needed for the TV sound channel :

- IF LIMITER AMPLIFIER
- ACTIVE LOW-PASS FILTER
- FM DETECTOR
- DC VOLUME CONTROL
- AF PREAMPLIFIER
- AF OUTPUT STAGE



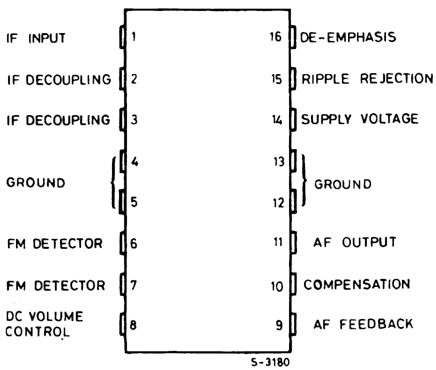
DIP-16

ORDER CODE : TDA3190

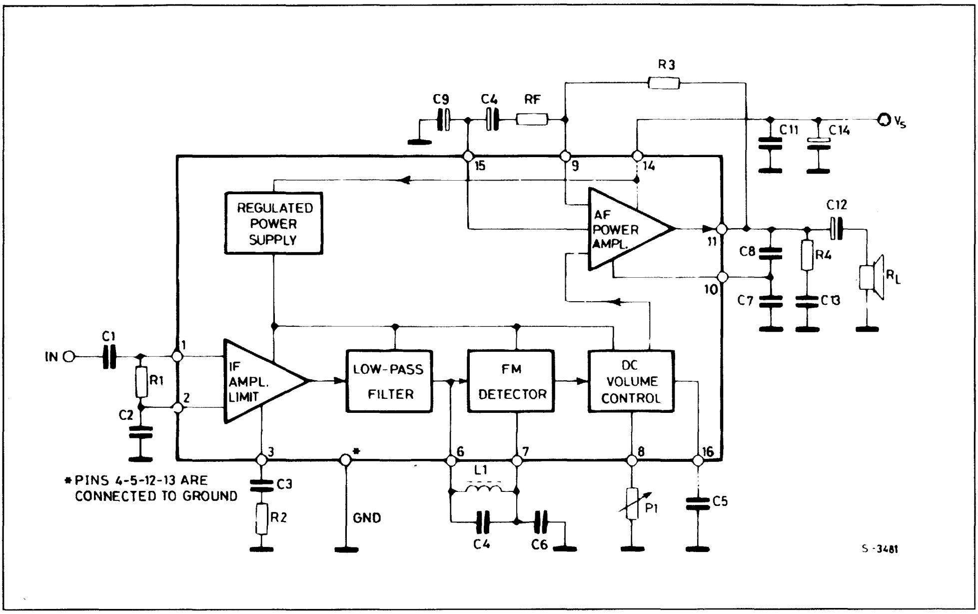
DESCRIPTION

The TDA3190 can give an output power of 4.2 W (d = 10 %) into a 16 Ω load at V_S = 24 V, or 1.5 W (d = 10 %) into an 8 Ω load at V_S = 12 V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.
The TDA3190 is a pin to pin replacement of TDA1190Z.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

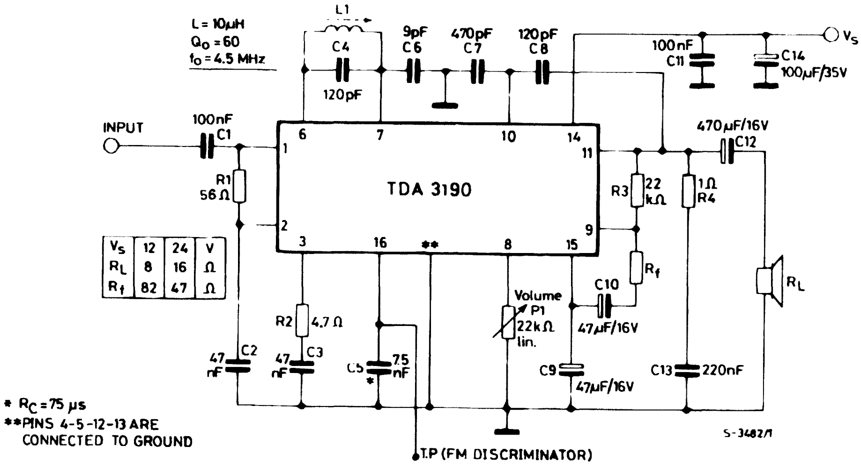
Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 10)	28	V
V_i	Input Signal Voltage (pin 1)	1	V
I_o	Output Peak Current (non-repetitive)	2	A
I_o	Output Peak Current (repetitive)	1.5	A
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C (free air)	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80*	°C/W

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

TEST CIRCUIT



ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = 24 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 14)			9		28	V
V_o	Quiescent Output Voltage (pin 11)	V_s = 24 V		11	12	13	V
		V_s = 12 V		5.1	6	6.9	V
I_d	Quiescent Drain Current	P_1 = 22 KΩ					
		V_s = 24 V		11	22	45	mA
		V_s = 12 V			19	40	mA
Po	Output Power	d = 10 %	f_m = 400 Hz				
		f_o = 4.5 MHz	Δf = ± 25 KHz				
		V_s = 24 V	R_L = 16 Ω		4.2		W
		V_s = 12 V	R_L = 8 Ω		1.5		W
		d = 2 %	f_m = 400 Hz				
		f_o = 4.5 MHz	Δf = ± 25 KHz				
		V_s = 24 V	R_L = 16 Ω		3.5		W
		V_s = 12 V	R_L = 8 Ω		1.4		W

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input Limiting Voltage (– 3 dB) at Pin 1	f_o = 4.5 MHz $\Delta f = \pm$ 7.5 KHz f_m = 400 Hz P_1 = 0		40	100	µV
d	Distortion	P_o = 50 mW f_m = 400 Hz f_o = 4.5 MHz $\Delta f = \pm$ 7.5 KHz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		0.75 1		% %
B	Frequency Response of audio-amplifier (– 3 dB)	R_L = 16 Ω C_8 = 120 pF C_7 = 470 pF P_1 = 22 KΩ R_f = 82 Ω R_f = 47 Ω		70 to 1200 70 to 7000		Hz Hz
V_o	Recovered Audio Voltage (pin 16)	$V_i \geq$ 1 mV f_o = 4.5 MHz f_m = 400 Hz $\Delta f = \pm$ 7.5 KHz P_1 = 0		120		mV
AMR	Ampliture Modulation Rejection	$V_i \geq$ 1 mV f_o = 4.5 MHz f_m = 400 Hz $\Delta_f = \pm$ 25 KHz m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	$V_i \geq$ 1 mV V_o = 4 V f_o = 4.5 MHz f_m = 400 Hz $\Delta f = \pm$ 25 KHz	50	65		dB
R_3	External Feedback Resistance (between pins 9 and 11)				25	KΩ
R_i	Input Resistance (pin 1)	V_i = 1 mV fo = 4.5 MHz		30		KΩ
C_i	Input Capacitance (pin 1)			5		pF
SVR	Supply Voltage Rejection	R_L = 16 Ω f_{ripple} = 120 Hz P_1 = 22 KΩ		46		dB
A_v	DC Volume Control Attenuation	P_1 = 12 KΩ		90		dB

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

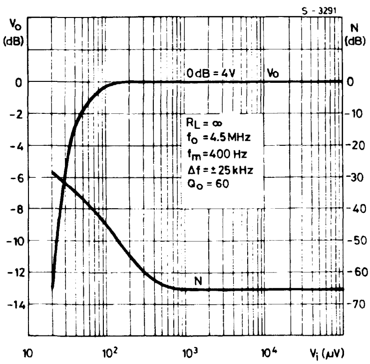


Figure 2 : Output Voltage Attenuation vs. DC Volume Control Resistance.

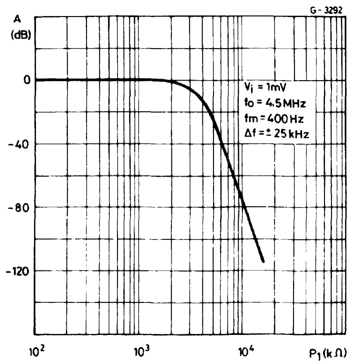


Figure 3 : Amplitude Modulation Rejection vs. Input Signal.

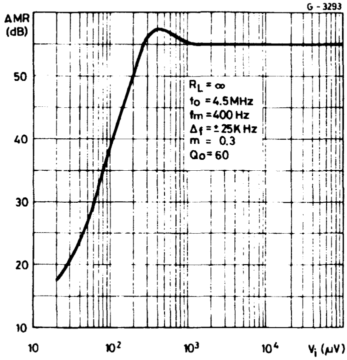


Figure 4 : Δ AMR vs. Tuning Frequency Change.

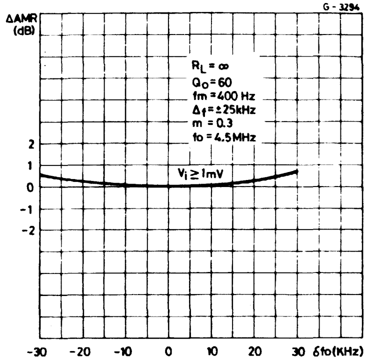


Figure 5 : Recovered Audio Voltage vs. Unloaded Q Factor of the Detector Coil.

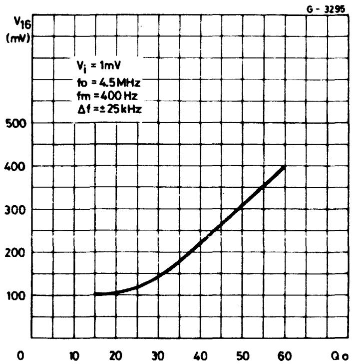


Figure 6 : Distortion vs. Output Power.

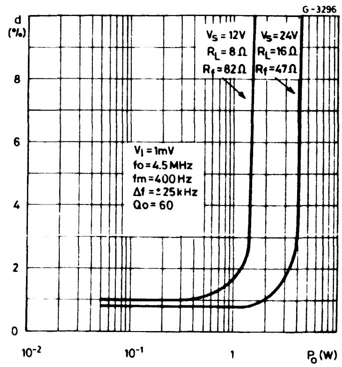


Figure 7 : Distortion vs. Frequency Deviation.

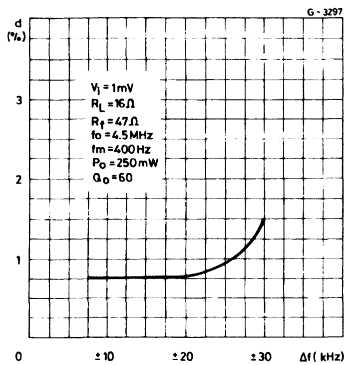


Figure 8 : Distortion vs. Tunning Frequency Change.

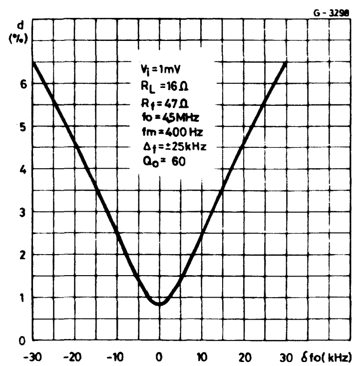


Figure 9 : Audio Amplifier Frequency Response.

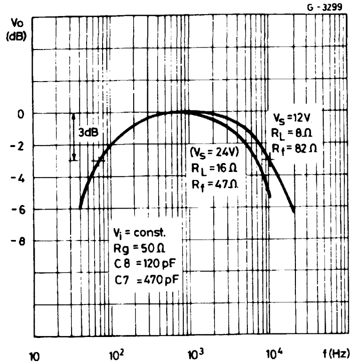


Figure 10 : Supply Voltage Ripple Rejection vs.

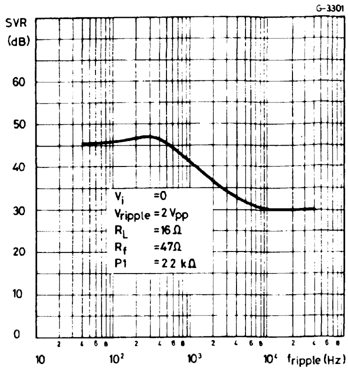


Figure 11 : Supply Voltage Ripple Rejection vs; Volume Control Attenuation.

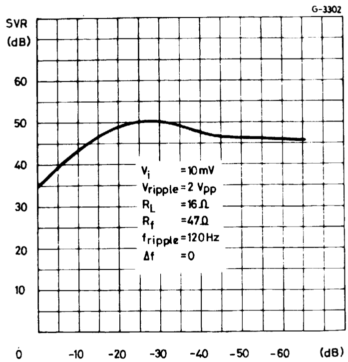


Figure 12 : Output Power vs. Supply Voltage.

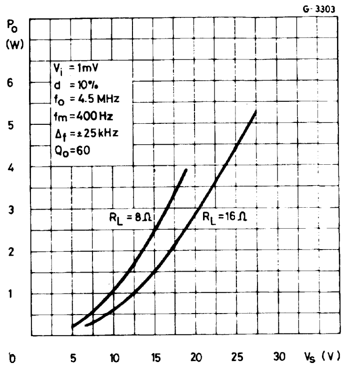


Figure 13 : Maximum Power Dissipation vs. Supply Voltage (sine wave operation).

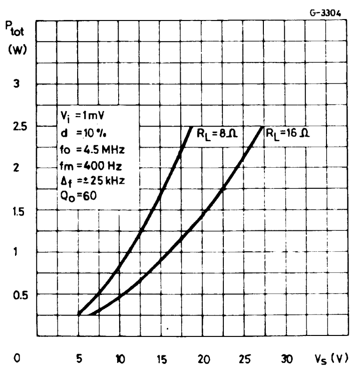


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

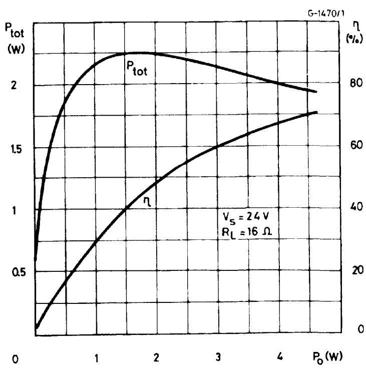
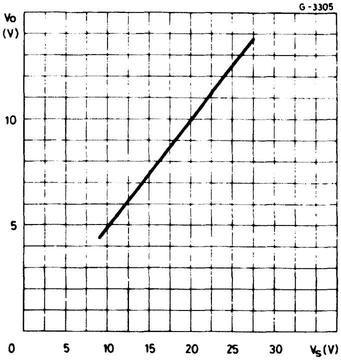


Figure 15 : Quiescent Output Voltage (pin 11) vs. Supply Voltage.



APPLICATION INFORMATION

The electrical characteristics of the TDA3190 remain almost constant over the frequency range 4.5 to 6 MHz, therefore it can be used in all television standards (FM mod.). The TDA3190 has a high input impedance, so it can work with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 9, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier, must enter into clipping.

Capacitor C8, connected between pins 10 and 11, determines the upper cutoff frequency of the audio bandwidth. To increase the bandwidth the values of C8 and C7 must be reduced, keeping the ratio C7/C8 as shown in the table of fig. 16.

The capacitor connected between pin 16 and ground, together with the internal resistor of 10 KΩ forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker.

Figure 16 : Typical Application Circuit.

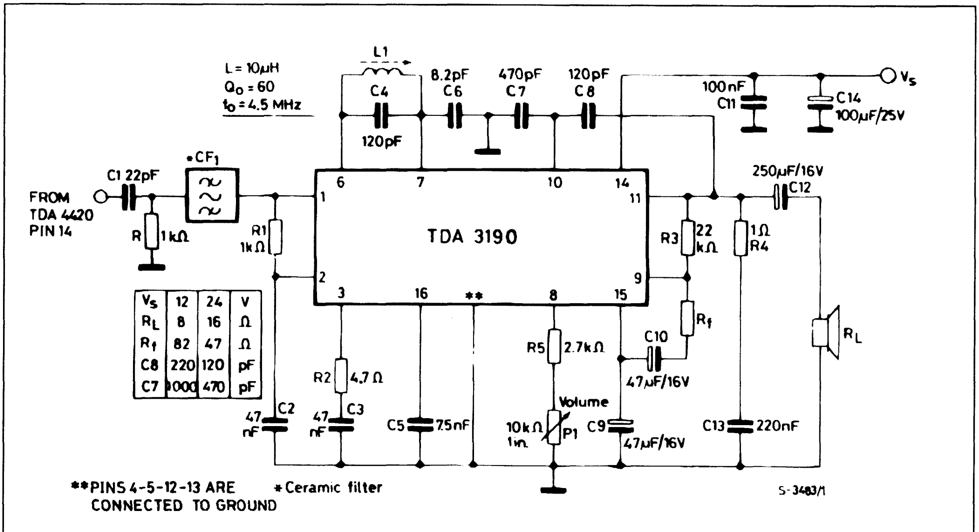
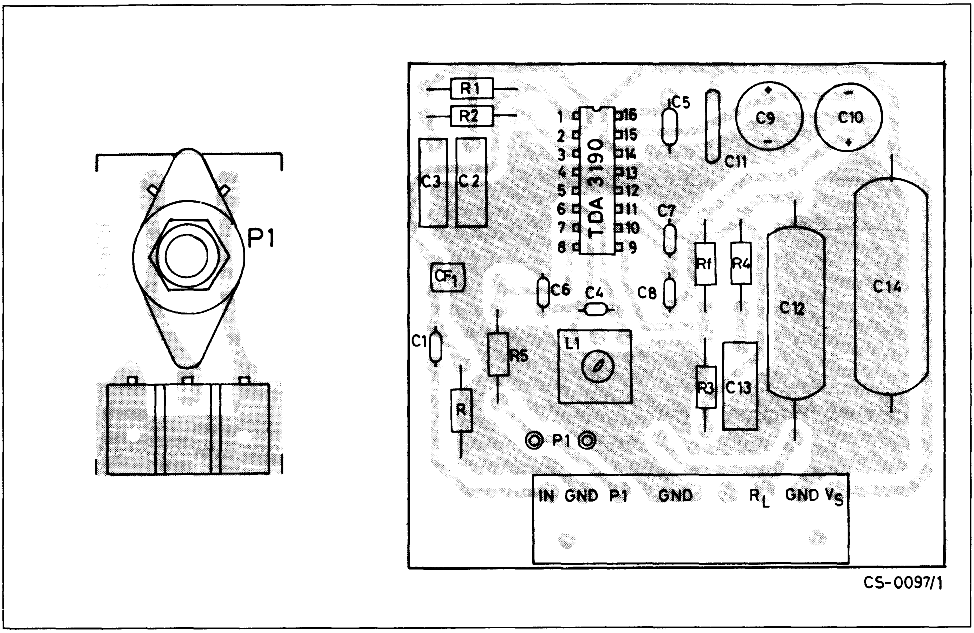


Figure 17 : P.C. Board and Component Layout of the Circuit Shown in Fig. 16 (1 : 1 scale).



MOUNTING INSTRUCTION

The Rth j-amb of the TDA3190 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (fig. 18) or to an external heatsink (fig. 19).

The diagram of figure 20 shows the maximum dissipable power Ptot and the Rth j-amb as a function of the side "l" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 18 : Example of P.C. Board Copper Area which is used as Heatsink.

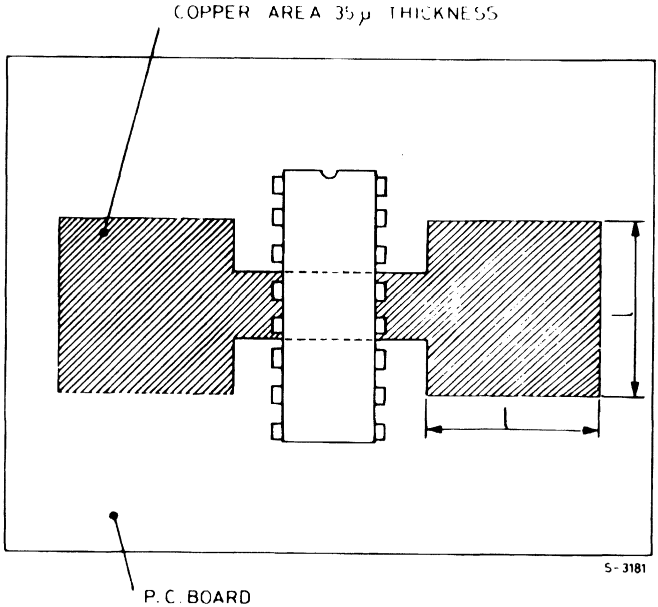


Figure 19 : External Heatsink Mounting Example.

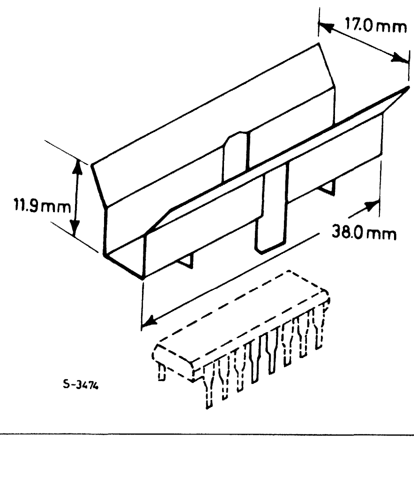


Figure 20 : Maximum Dissipable Power and Junction to Ambient Thermal Resistance vs. Side "l"

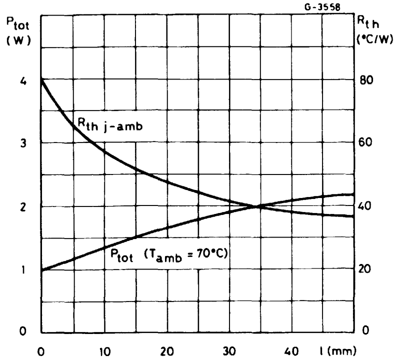
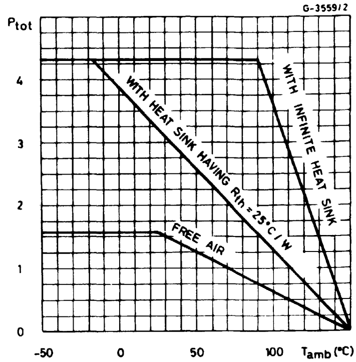
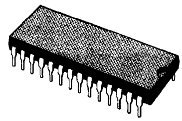


Figure 21 : Maximum Allowable Power Dissipation vs. Ambient Temperature.



PAL/NTSC ONE-CHIP DECODER

- CHROMINANCE SIGNAL PROCESSOR
- LUMINANCE SIGNAL PROCESSING WITH CLAMPING
- HORIZONTAL AND VERTICAL BLANKING
- LINEAR TRANSMISSION OF INSERTED RGB SIGNALS
- LINEAR CONTRAST AND BRIGHTNESS CONTROL ACTING ON INSERTED AND MATRIXED SIGNALS
- AUTOMATIC CUT-OFF CONTROL
- NTSC HUE CONTROL



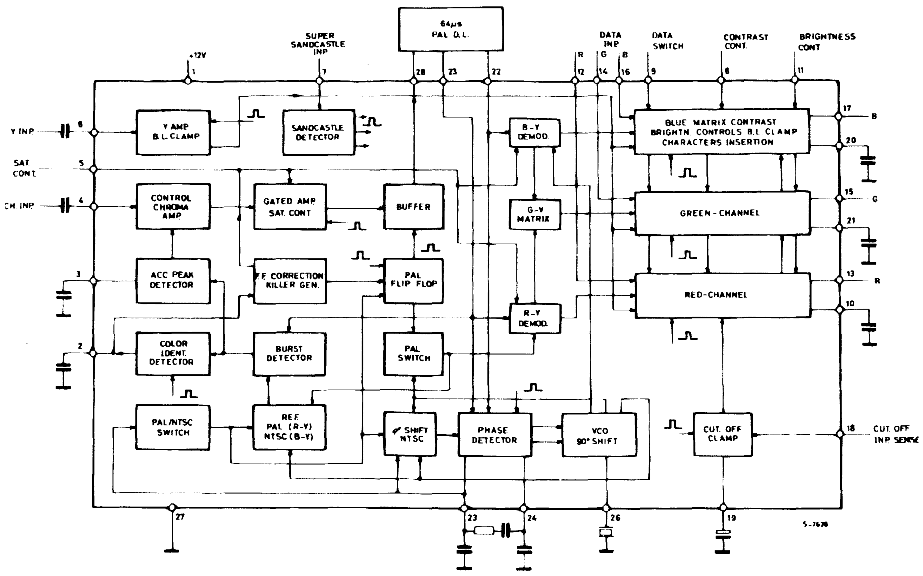
DIP-28

ORDER CODE : TDA3562A

DESCRIPTION

The TDA3562A is a monolithic IC designed as decode PAL and/or NTSC colour television standards and it combines all functions required for the identification and demodulation of PAL and NTSC signals.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	13.2	V
P_{tot}	Power Dissipation at T_{amb} = 65 °C	1.7	W
T_{stg}	Storage Temperature	– 25 to 150	°C
T_j	Junction Temperature	– 25 to 150	°C
T_{amb}	Ambient Temperature Range	0 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	40	°C/W

Figure 1 : Contrast Control Voltage Range.

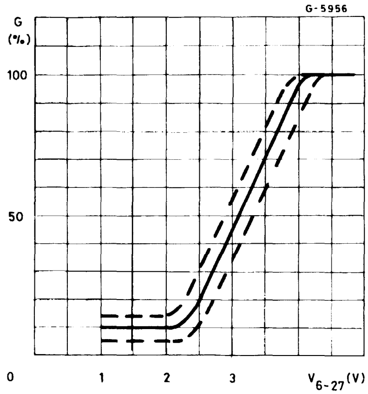


Figure 2 : Saturation Control Voltage Range.

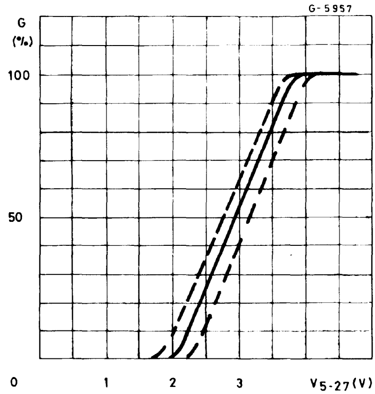


Figure 3 : Difference Between Signal Black Level and Measuring level (3L windows after cut off current stabilization) at the RGB Outputs (ΔV) vs. Control Voltage (V_{11} - V_{12}).

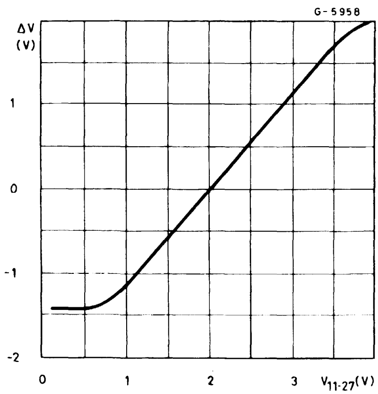
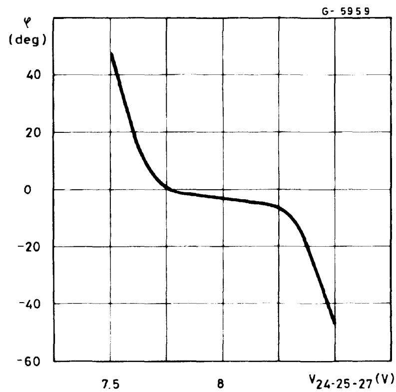


Figure 4 : Hue Control Voltage Range.



ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified :
Supply voltage : Pin 1 at 12 V
T_{amb} = 25 °C

Input signals :

Luminance input signal	V8 = 0.48 Vp/p	(1)
Chrominance input signal	V4 = 0.39 Vpp	(2)
Data input signals	$V_{12, 14, 16}$ = 1.4 Vpp	(3)

Control inputs at nominal value :
Pin 6 Nom. contrast = max. contrast – 5 dB
Pin 5 Nom. saturation = max. saturation – 6 dB
Pin 11 Nom. brightness = 2 V
Pin 9 at 0.4 V

(1) Composite video signal (100 % white)
(2) Colour bar signal with 75 % colour saturation and chrominance to burst ratio = 2.2 : 1.
(3) Including neg.going sync. pulse.

SUPPLY INPUT (pin 1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Supply Voltage Range		10.8		13.2	V
	Supply Current	V_1 = 12 V		80	110	mA

LUMINANCE INPUT (pin 8)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Composite Input Signal				0.8	V_{pp}
	Input Current			0.1	1	µA

CHROMINANCE INPUT (pin 4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Input Signal		40		1100	mVpp
	Input Resistance			10		KΩ
	Input Capacitance				6.5	pF

SUPER SANDCASTLE INPUT (pin 7)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Gating & Clamping Level		7.5			V
	H-pulse Separating Level		4		5	V
	V-pulse Separating Level		2		3	V
	Forbidded Range			1 to 2		V
	Input Current	V_7 = 0 to 1 V			– 460	µA
		V_7 = 1 to 8.5 V		50		µA
		V_7 = 8.5 to 12 V			2	mA
	Delay Between Black Level Clamping Pulse and Gating Pulse			0.6		µs

DATA BLANKING INPUT (pin 9)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Input Voltage for no Data Insertion				0.4	V
	Input Voltage for Data Insertion		0.9		3	V
	Input Resistance		7		13	kΩ

"BLACK CURRENT" STABILIZATION INPUT (pin 18)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	D. C. Bias Voltage		3.5	5	7	V
	Internal Limiting Threshold			9		V
	Switching Threshold for "Black Current" ON			8		V
	Difference between Input Voltage for "Black Current" and Leakage Current			0.5		V
	Input Resistance during Scan			1.5		kΩ
	Input Current during "Black Current" Measurement				2	µA
	Input Current during Scan				10	mA

RGB - OUTPUTS (Pins 13, 15, 17)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Output Resistance			50		Ω
	Current Source		2	3		mA
	Peak Output Level		10.7		11.3	V
	Residual 4.4 MHz at RGB Outputs				100	mVpp
	Residual 8.8 MHz at RGB Outputs				150	mVpp

LUMINANCE CHANNEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Frequency Resp. of Total Lumin. Amplifiers	f = 0 to 5 MHz		– 1	– 3	dB
	RGB Output Signal (black to white)		3.5	4	4.5	Vpp
	Relative Spread of RGB - Output Signals				1	dB
	Contrast Control Range	(see fig. 1)		– 5 to 10		dB
	Tracking Over 10 dB Contrast Control			0		dB
	Contrast Control Input Current				15	µA
	Blanking Level of RGB - Output Signals			1	1.2	V
	Difference Between Blanking Levels,			0		mV
	Differential Drift of Blanking Levels	ΔT = 40 °C		0		mV
	Brightness Control Input Current				5	µA
	Brightness Control Range	(see fig. 3)		1 to 3		V
	Relation Ship between Black Level Variation and Brightness Control Variation	(see fig. 3)		1.3		V/V
	Black Level of RGB Output Signals	(see note 4)		3		V
	Difference between Black Levels	(see note 4)		0		mV
	Tracking Over Brightness Control				2	%
	Differential Drift of Black Levels	ΔT = 40 °C			20	mV
	Drift of Black Level Versus 10 % Variation of Supply Voltage and Contrast Control				20	mV

"CUT OFF CURRENT" REGULATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	RGB Output Level of the "3L Windows" after Switch-on		7.5			V
	RGB Outputs Level of the "3L Windows" after Cut off Current Stabilization	(see note 4)	1	3	5	V
	RGB Output Range		1		5	V
	Charge/Discharge Current during Measuring Time (3L windows) at Pins 10, 19, 20 and 21			1		mA
	Leakage Currents Flowing into Pins 10, 20 and 21 during Scan				50	nA

RGB DATA INSERTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Data RGB Output Signal	V_9 = 0.9 to 3 V		4		Vpp
	Differential Amplitude Error between RGB Output Signal and Data Output Signal				10	%
	Differential Error between Black Levels of RGB Output Signals and Black Levels of Data Output Signals				200	mV
	Rise Time of Data Output Signal			50	80	ns
	Differential Delay			0	40	ns
	Attenuation of RGB Output Signal	V_9 = 0.9 to 3 V		46		dB
	Frequency Response for f = 0 to 5 MHz			– 1	– 3	dB

CHROMINANCE CHANNEL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Pin 4	Chrominance Input Signal		40		1100	mVpp
Pin 4	Input Resistance			10		kΩ
Pin 4	Input Capacitance				6.5	pF
	ACC Control Range		30			dB
PIn 28	Burst Change Over 30 dB ACC Range				1	dB
	Saturation Control Range	(see fig. 2)		– 44 to 6		dB
Pin 5	Sat. Control Input Current				20	µA
Pin 28	Chrominance Output Voltage	V_5 = 4.2 V	4			Vpp
	Burst Input Signal at Pins 22 and 23			100		mVpp
	Input Resist. Bet. Pins 22, 23 and Ground			1		kΩ
Pin 28	Phase Shift Bet. Burst and Chrom. Signal		– 5	0	5	°
Pin 2	Voltage at Nom. Input Signal			4.7		V
Pin 2	Voltage without Input Signal			2.6		V
Pin 2	Identificaton-on Voltage			2.1		V
Pin 2	Colour-off Voltage			3.4		V
Pin 2	Colour-on Voltage			3.6		V
Pin 3	Voltage at Nom. Input Signal			5.1		V

COLOUR DEMODULATORS AND G-Y MATRIX

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Ratio (B-Y) / (R-Y)		1.60	1.78	1.96	
	Ratio (G-Y) / (R-Y)	(B – Y) = 0	– 0.46	– 0.51	– 0.56	
	Ratio (G-Y) / (B-Y)	(R – Y) = 0	– 0.14	– 0.19	– 0.24	

REFERENCE OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Oscillator Frequency			2 fcs		MHz
	Temp. Coefficient of Oscillator Frequency	(see note 5)		– 2		Hz/k
Pin 26	Input Resistance			400		Ω
Pin 26	Input Capacitance				10	pF
	Pull-in Range	(see note 5)	500	700		Hz
	Phase Shift for ± 400 Hz Deviation				5	°C
	Phase Shift between (R – Y) and (R – Y) Ref. Signal				5	°C
	Phase Shift between (R – Y) and (B – Y) Ref. Signal		85	90	95	°C

NTSC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Pins 24, 25	PAL-on Operating Range		9		11	V
Pins 24, 25	Threshold for NTSC-on			8.8		V
$J_{24} + J_{25}$	Avarage Output Current	Key Pulse = 4 µs		90		µA
	Hue Control		± 30			°C
Pins 24, 25	Hue Control Voltage		7.5		8.5	V

(4) The levels depend on the application circuit and on the spread and drift of picture tube guns.
(5) All frequency variations are referred to 4.4 MHz carrier frequency.

Figure 5 : Application Diagram Showing the TDA3562A for a PAL Decoder.

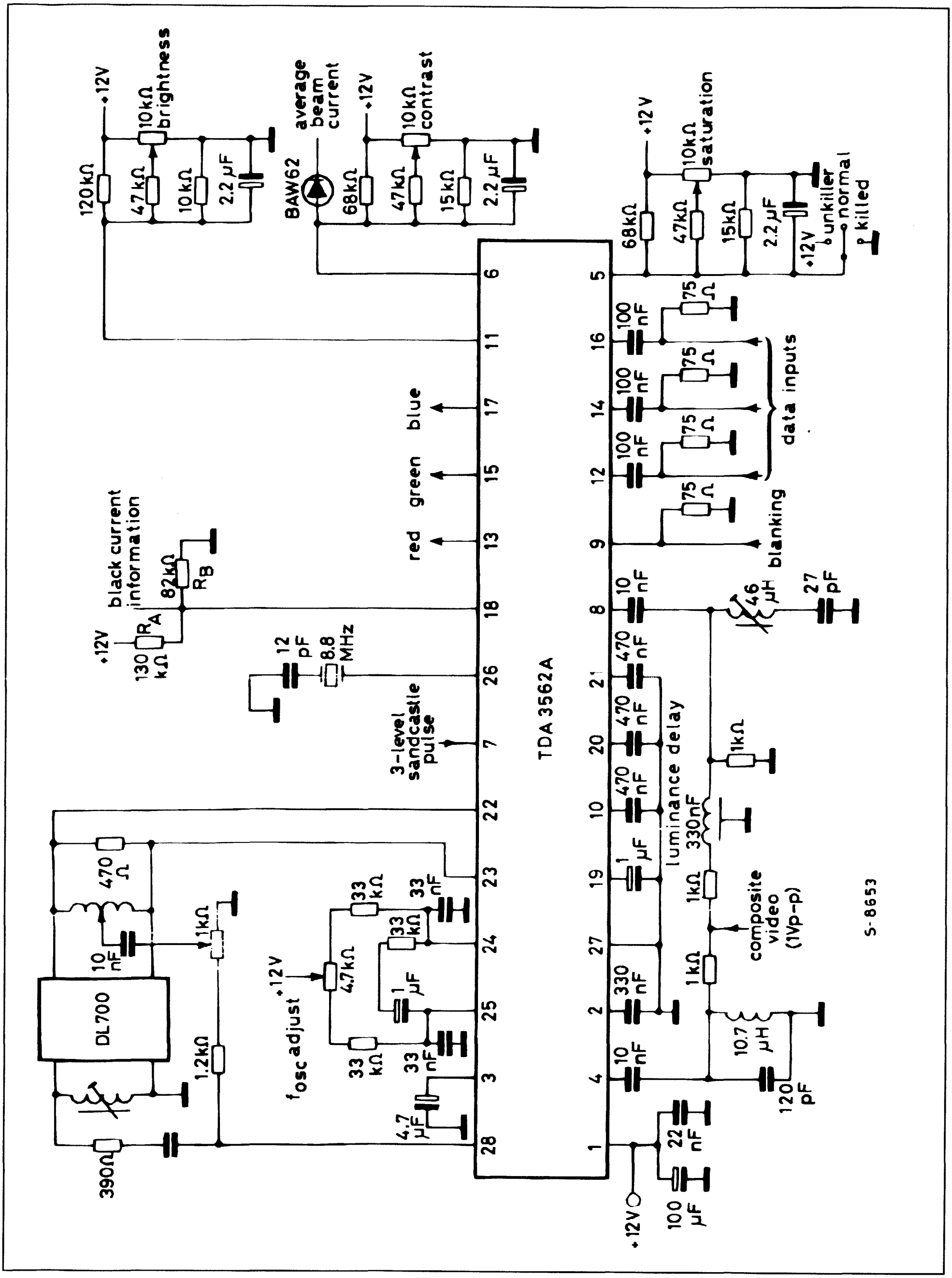
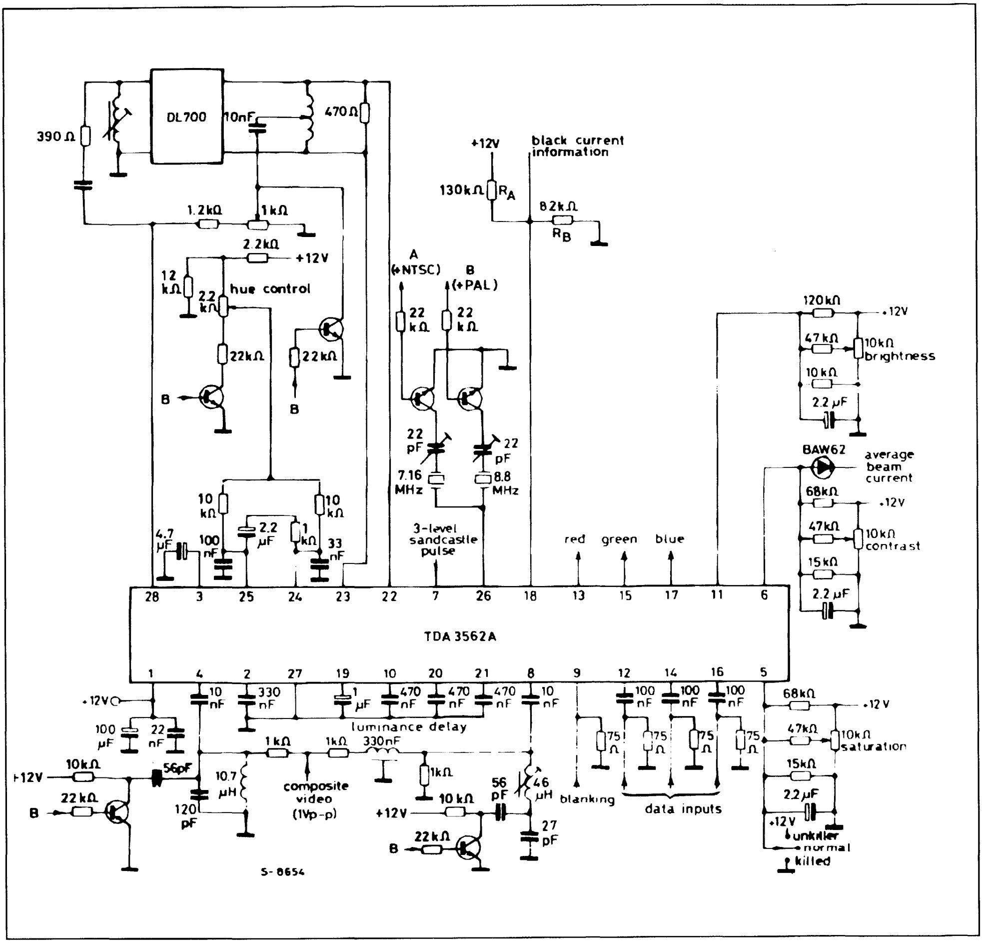


Figure 6 : Application Diagram Showing the TDA3562A for a PAL/NTSC Decoder.



5 BIT BINARY TO 7-SEGMENT DECODER DRIVER

- ROM MASK OPTION
- STANDARD CONFIGURATION FOR 2 DIGIT 7-SEGMENT LED TO PRESENT THE NUMBERS 1 TO 32
- CONSTANT CURRENT OUTPUT STAGES FOR DIRECT DRIVING OF COMMON ANODE LEDs
- OUTPUT PROVIDED TO DISPLAY THE STAND-BY MODE
- $\overline{AV}$ OUTPUT ACTIVATED WHENEVER PROGRAM 32 IS SELECTED
- TTL COMPATIBLE INPUTS
- 5 V SUPPLY VOLTAGE

DESCRIPTION

The TDA4092 is a monolithic integrated circuit designed to display the program number (1 to 32) in TV or Radio sets in conjunction with voltage or frequency synthesizers. The inputs accept a 5 bit binary code with TTL levels and have internal pull-up.

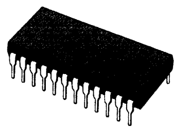
The outputs can directly drive LED display elements with common anode.

One of these outputs is intended to display the stand-by mode of the set.

No external resistors are required if the LEDs are supplied at 5 V.

The LEDs can also be supplied with higher voltage (up to 18 V) but in this case a single resistor in series with the LED elements must be used in order to limit the power dissipation of the IC ; moreover, a suitable R_{ext} must be chosen.

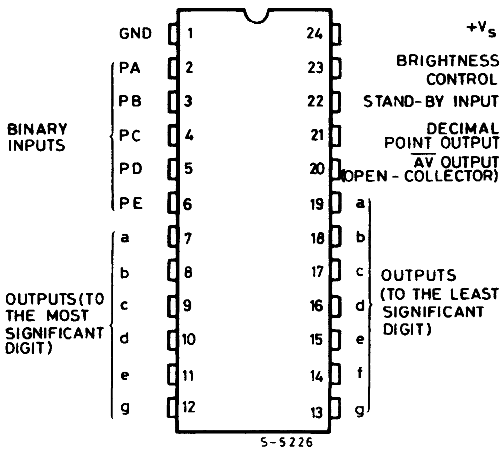
The circuit is produced in I^2L technology and is available in a 24 pin dual in-line plastic package.



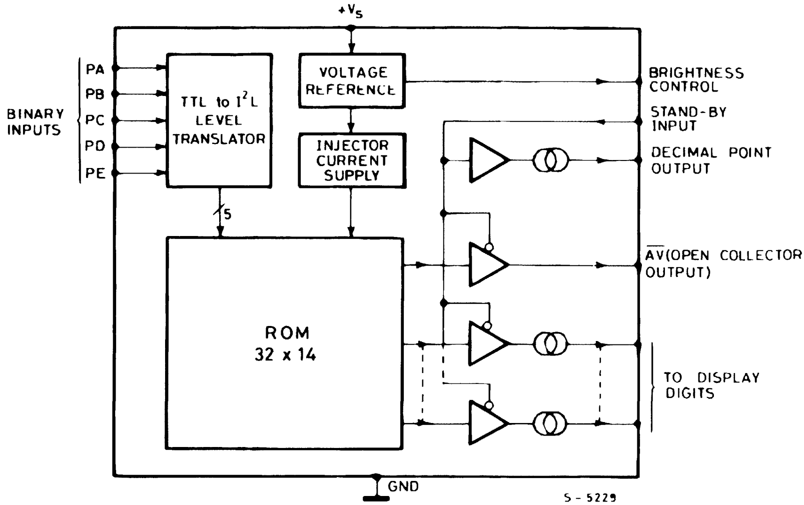
DIP24

ORDER CODE : TDA4092

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



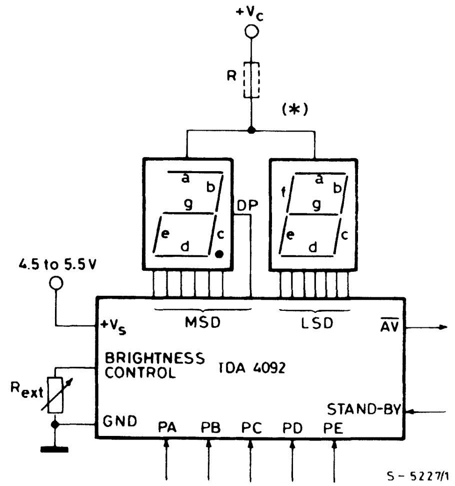
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	10	V
V_I	Input Voltage	10	V
$V_{O\ (off)}$	Off State Output Voltage	20	V
I_{OL}	Output Current	22	mA
P_{tot}	Total Power Dissipation at T_{amb} = 55 °C	0.8	W
T_{stg}, T_j	Storage and Junction Temperature	– 25 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	120	°C/W

APPLICATION CIRCUIT



(*) R is necessary only with Vc greater than 5.5 V.

ELECTRICAL CHARACTERISTICS (V_s = 5 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_S	Supply Voltage			4.5		5.5	V
I_S	Quiescent Supply Current	V_s = 5.5 V			20	28	mA
V_{IH}	High Level Input Voltage	T_{amb} = 0 to 70 °C		2			V
V_{IL}	Low Level Input Voltage	T_{amb} = 0 to 70 °C				0.8	V
I_{IH}	High Level Input Current	T_{amb} = 0 to 70 °C V_S = 5.5 V	V_{IH} = 2 V			– 30	µA
I_{IL}	Low Level Input Current		V_{IL} = 0.8 V		– 50	– 200	µA
V_{out}	Output Voltage	I_o = 15 mA		2			V
V_{AV}	AV Output Voltage (pin 20)	(all the binary inputs high) I_{AV} = 1.6 mA			50	260	mV
I_B	Pin 23 Input Current (brightness control)	R_{ext} = 3.3 KΩ			– 375		µA
		R_{ext} = 5.6 KΩ			– 225		
I_o	Output Current (*)	R_{ext} = 3.3 K		13.5	15	16.5	mA
		R_{ext} = 5.6 K		8	9	10	
I_{DP}	Output Current for Decimal Point (pin 21) (**)				12.5		mA
$\frac{\Delta I_o}{I_o} / \Delta V_S$	Segment Current Stability	I_o = 15 mA V_s = 4.5 to 5.5 V			0.2		%

(*) I_O = 40 I_B.
(**) I_{DP} is fixed and independent of R_{EXT} value.

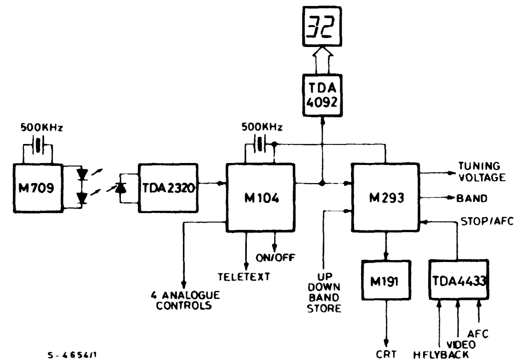
FUNCTION TABLE

Inputs		Number Displayed	Outputs														
			Ten's Digit (MSD)						Unit's Digit (LSD)							DP	$\overline{AV}$*
A B C D E	Standby		a	b	c	d	e	g	a	b	c	d	e	f	g		
L L L L L	L	1								On	On						
H L L L L	L	2							On	On		On	On		On		
L H L L L	L	3							On	On	On	On			On		
H H L L L	L	4								On	On			On	On		
L L H L L	L	5							On		On	On		On	On		
H L H L L	L	6							On		On	On	On	On	On		
L H H L L	L	7							On	On	On						
H H H L L	L	8							On	On	On	On	On	On	On		
L L L H L	L	9							On	On	On	On		On	On		
H L L H L	L	10		On	On				On	On	On	On	On	On			
L H L H L	L	11		On	On					On	On						
H H L H L	L	12		On	On				On	On		On	On		On		
L L H H L	L	13		On	On				On	On	On	On			On		
H L H H L	L	14		On	On					On	On			On	On		
L H H H L	L	15		On	On				On		On	On		On	On		
H H H H L	L	16		On	On				On		On	On	On	On	On		
L L L L H	L	17		On	On				On	On	On						
H L L L H	L	18		On	On				On	On	On	On	On	On	On		
L H L L H	L	19		On	On				On	On	On	On		On	On		
H H L L H	L	20	On	On		On	On	On	On	On	On	On	On	On			
L L H L H	L	21	On	On		On	On	On		On	On						
H L H L H	L	22	On	On		On	On	On	On	On		On	On		On		
L H H L H	L	23	On	On		On	On	On	On	On	On	On			On		
H H H L H	L	24	On	On		On	On	On		On	On			On	On		
L L L H H	L	25	On	On		On	On	On	On		On	On		On	On		
H L L H H	L	26	On	On		On	On	On	On		On	On	On	On	On		
L H L H H	L	27	On	On		On	On	On	On	On	On						
H H L H H	L	28	On	On		On	On	On	On	On	On	On	On	On	On		
L L H H H	L	29	On	On		On	On	On	On	On	On	On		On	On		
H L H H H	L	30	On	On	On	On		On	On	On	On	On	On	On			
L H H H H	L	31	On	On	On	On		On		On	On						
H H H H H	L	32	On	On	On	On		On	On	On		On	On		On		On
X X X X X	H	None														On	**

H = High L = Low X = Don't care.
* $\overline{AV}$: open collector output.
** $\overline{AV}$ output is "on" whenever the input bits are all high, regardless of the standby input.

APPLICATION INFORMATION

Figure 1 : Remote Controlled Voltage Synthesizer (up to 32 stations) for TV and radio.



When operating with a supply voltage higher than 5.5 V for LED elements, it is necessary to limit the IC power dissipation by means of one external resistance connected in series with the common point of the digits (R in fig. 2).

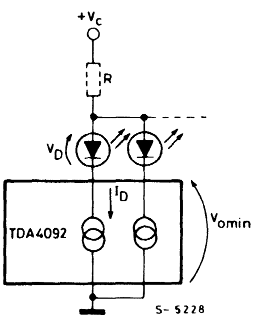
Unused outputs must be connected to V_S taking into account the additional power dissipation.

The value of R must be chosen taking into account the worst working conditions.

The maximum number of ON segments is 12 (number 28 displayed), so,

$$R = \frac{V_C - V_D - V_{out\ min}}{12 \cdot I_D}$$

Figure 2 : Schematic Diagram for LED Driving.



I_D, depending on R_{ext} (see Table of Electrical characteristics), can be fixed to the most suitable value to minimize the power dissipation in the IC. Since the worst condition for the device is with seven outputs active, it follows that :

$P_{d\ out} = 7 \cdot I_D (V_C - V_D - 7R \cdot I_D)$ Power dissipation in the output stage

$P_d = V_S \cdot I_{s\ max}$ Power drained from the supply

$P_{tot} = P_{d\ out} + P_D$ Total power dissipation

P_{tot} must not exceed the Absolute Maximum Ratings of 800 mW, at T_{amb} = 55 °C.

Otherwise the maximum operating ambient temperature can be fixed by :

$$T_{amb\ max} = T_{j\ max} - R_{th\ j\text{-}amb}\ P_{tot}$$

Example :

V_c = 18 V ; I_D = 10 mA (fixed by means of R_{ext} = 5.6 KΩ) ; $V_{out\ min}$ = 2 V ; $I_{s\ max}$ = 28 mA ; $T_{j\ max}$ = 150 °C ; V_D = 2 V ; V_s = 5.5 V.

Applying the previous formulae, it follows that : R ≅ 120 Ω ; $P_{d\ out}$ = 0.532 W ; P_d = 0.154 W P_{tot} = 0.686 W ; $T_{amb\ max}$ ≅ 68 °C.

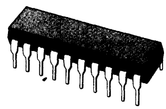
TV SOUND CHANNEL WITH DC CONTROLS

- INTERNAL VCR INPUT/OUTPUT SWITCHING
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

DESCRIPTION

The TDA4190 is a complete TV sound channel with DC tone and volume controls plus an internally switched VCR input/output. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4 W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA4190 are : IF amplifier limiter, active low-pass filter, AF preamplifier and power amplifier, turn-off muting, VCR switch, mute circuit and thermal protection.

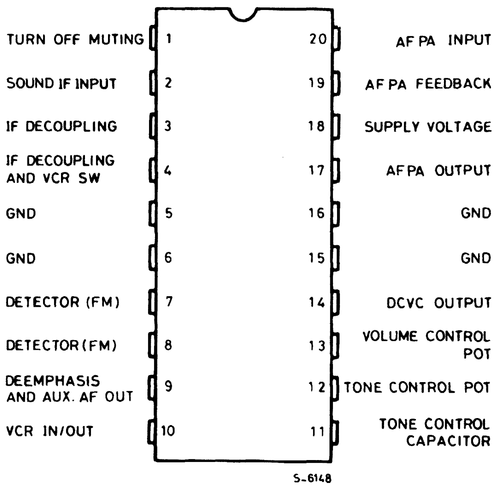
High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.



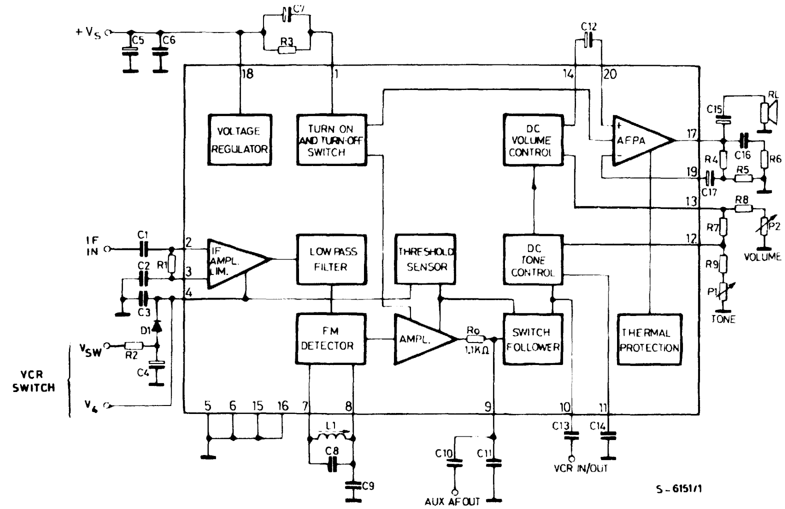
DIP-20
(plastic package)

ORDER CODE : TDA4190A

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 18)	28	V
V_I	Voltage at pin 1	$\pm V_S$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation : at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_s = 24V, V_{sw} = 2V or no V4, Δf = ± 25KHz, R_L = 16Ω, V_i = 1mV, P_1 = 12KΩ, f_o = 4.5MHz, f_m = 400Hz, T_{amb} = 25°C, unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 18)	P_2 = 12 KΩ	10.8		27	V
V_O	Quiescent Output Voltage (pin 18)	P_2 = 12 KΩ	11	12	13	V
V_1	Pin 1 DC Voltage	P_2 = 12 KΩ R_1 = 270 KΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12 KΩ		3.2		V
I_d	Quiescent Drain Current	P_2 = 12 KΩ		32		mA

IF AMPLIFIER AND DETECTOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{i\ (threshold)}$	Input Limiting Voltage at Pin 2 (– 3 dB)	V_o = 4 V_{rms}		50	100	µV
V_9	Recovered Audio Voltage (pin 9)	Δf = ± 7.5 KHz P_2 = 12 KΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3 ; V_I = 1 mV ; V_o = 4 V_{rms}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0 P_2 = 12 KΩ		30		KΩ
C_i	Input Capacitance (pin 2)	Δf = 0 P_2 = 12 KΩ		6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0.75	1.1	1.5	KΩ

DC VOLUME CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Kv	Volume Attenuation (resistance control)	P_2 = 0 KΩ P_2 = 4.3 KΩ P_2 = 12 KΩ	20	0 26 88	32	dB dB dB
Vc	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_v}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} 25 to 85 °C P_2 = 4.3 KΩ		– 0.05		$\frac{dB}{°C}$

DC TONE CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_T	Tone Cut	V_{sw} = 8 V or V_4 = 2 V V_{10} = 200 mV P_1 = 12 KΩ to 100 Ω f = 10 KHz		14		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO FREQUENCY AMPLIFIER

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
P_o	Output Power (d = 10 %)	V_s = 24 V V_s = 12 V	R_L = 16 Ω R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W V_{sw} = 8 V or V_{10} = 200 mV	R_L = 16 Ω V_4 = 2 V V_o = 4 Vrms @ 400 Hz	15	50		KHz
SVR	Supply Voltage Rejection	P_2 = 12 KΩ Δf = 0	f_{ripple} = 120 Hz		26		dB

V.C.R.

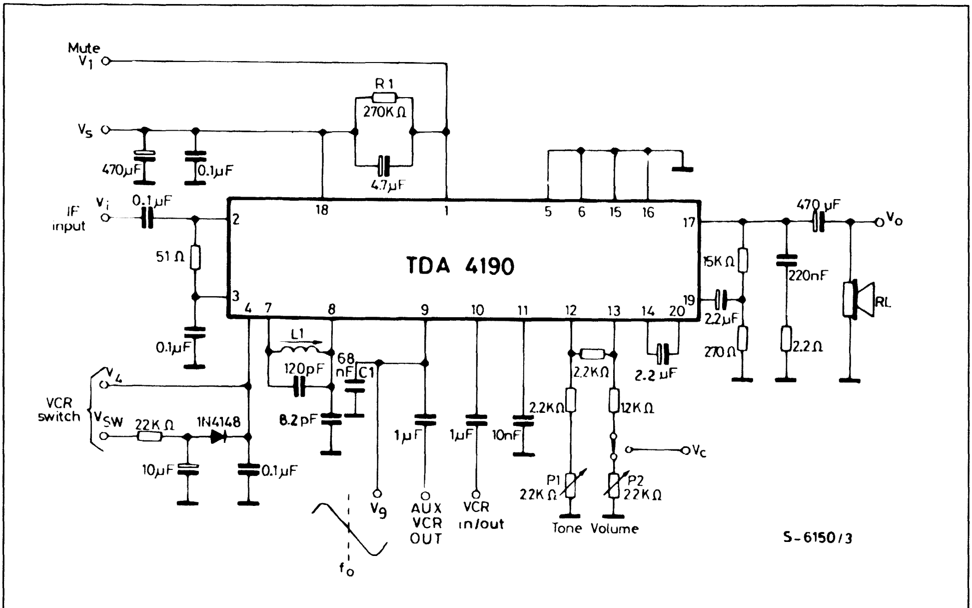
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_4	Input Switching Voltage for Recording for Playback			Floating			
						2	V
V_{sw}	Input Switching voltage for Recording for Playback					2	V
				8			V
V_{10}	Input Voltage (playback)	V_4 = 2 V or V_o = 4 V_{rms}	V_{sw} = 8 V P_2 = 0	50	70	100	mV
V_{10}	Output Voltage (recording)	P_2 = 12 KΩ	Δf = ± 7.5 KHz	140	200	280	mV
R_{10}	Input Resistance (playback)	V_4 = 2 V or	V_{sw} = 8 V	10			KΩ
R_{10}	Output Resistance (recording)	Δf = ± 7.5 KHz, no	V_4 or V_{sw} = 2 V			100	Ω
d	Total harmonic Distortion of Pin 10 Output Signal	Δf = ± 7.5 KHz	V_i = 1 mV		0.5		%
d	Total Harmonic distortion of 20 dB Over Load V_{10}	V_4 = 2 V V_{10} = 1 V_{rms}	V_{sw} = 8 V V_o = 4 V_{rms}		0.5	2	%
SVR	Supply Voltage Rejection at Output Pin 10	Δf = 0 f_{ripple} = 120	Hz P_2 = 12 KΩ		66		dB
$\frac{S+N}{N}$	Signal and Noise Ratio at Output Pin 10	Δf = ± 25 KHz	V_i ≥ 1 mV		70		dB

OVERALL CIRCUIT

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	V_i ≥ 1 mV Δf = 0	V_o = 4 Vrms		70		dB
d	Distortion (*)	P_o = 50 mW V_s = 24 V V_s = 12 V	Δf = ± 7.5 Hz R_L = 16 Ω R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms} @ no	V_1 ; V_1 = 0	100			dB
Δf		P_2 = 0	V_o = 4 Vrms		3	6	KHz

* Test bandwidth = 20 KHz.

TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

V_s = 24V ;	V_{SW} = 2V or no V4 ;	R_L = ∞ ;
V_{in} = 1mV ;	Q_o = 60 ;	f_o = 4.5MHz ;
P_1 = 12KW ;	f_m = 400Hz ;	Δf = ± 25KHz.

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

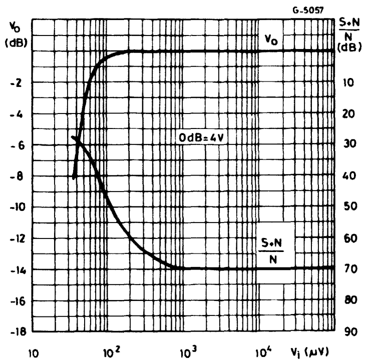


Figure 2 : Output Voltage Alternance vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).

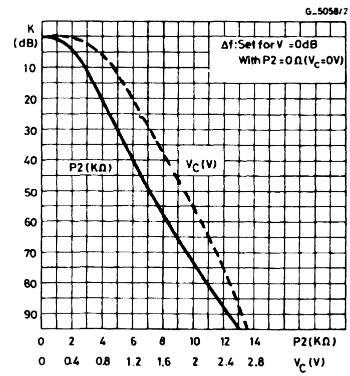


Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance Adjusted by P1.

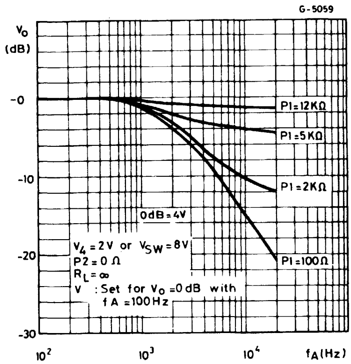


Figure 4 : Amplitude Modulation Rejection vs. Input Signal.

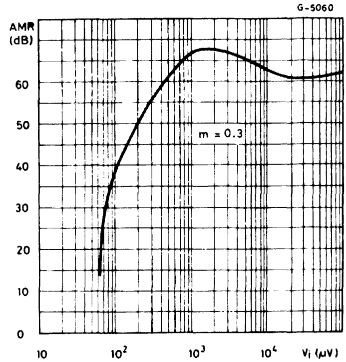


Figure 5 : Δ AMR vs. Timing Frequency Change.

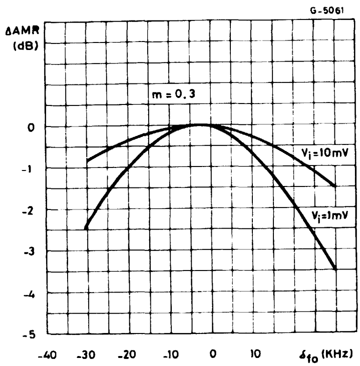


Figure 6 : Recovered Audio Voltage vs. Unloaded Q-factor of the Detector Coil.

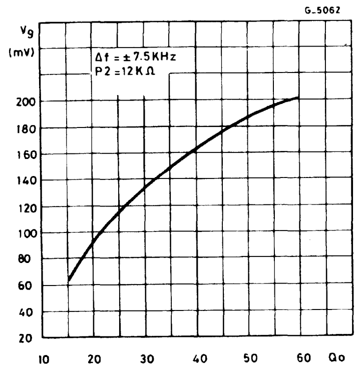


Figure 7 : Distortion vs. Unloaded Q-factor of the Detector Coil.

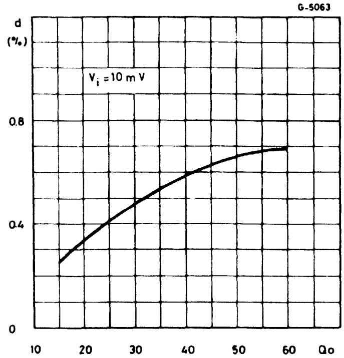


Figure 8 : Distortion vs. Frequency Variation.

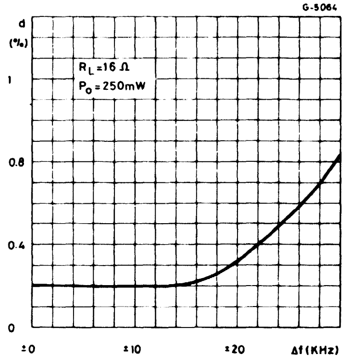


Figure 9 : Distortion vs. Tuning Frequency Change.

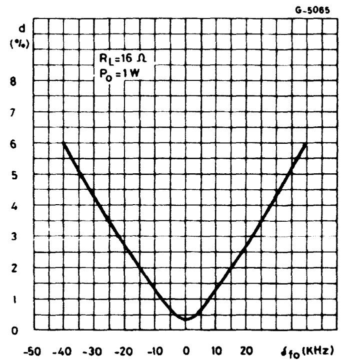


Figure 10 : Distortion vs. Output Power.

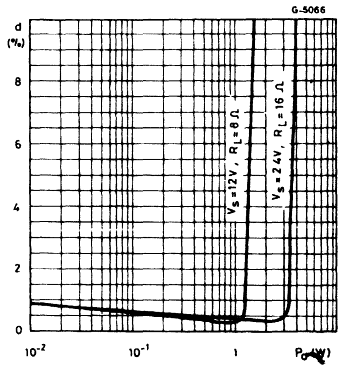


Figure 11 : Audio Amplifier Frequency Response.

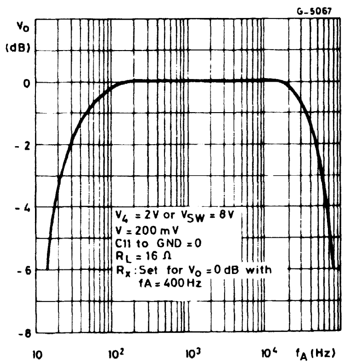


Figure 12 : Output Power vs. Supply Voltage.

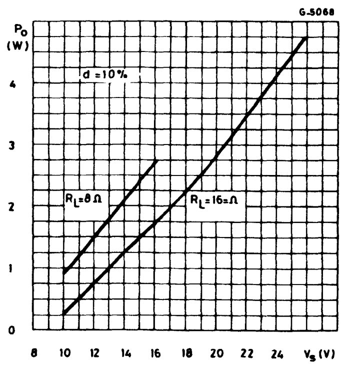


Figure 13 : Power Dissipation vs. Supply Voltage (sine Wave operation).

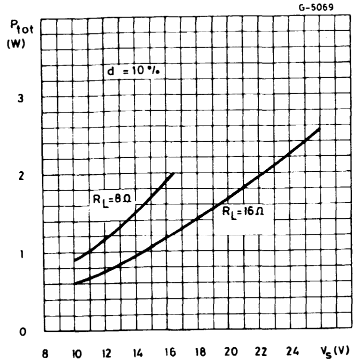


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

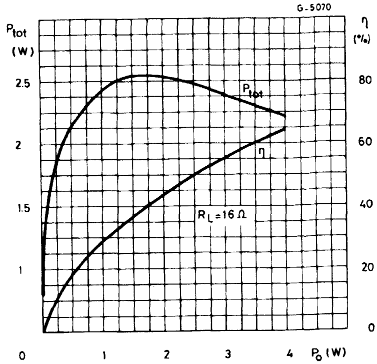
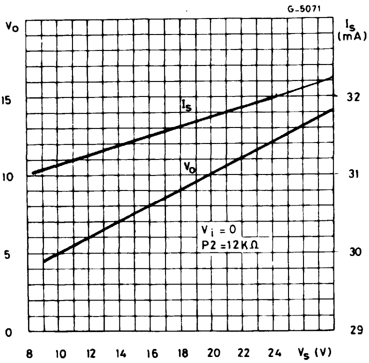


Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90 dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50μV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50μV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f2}{f1} = \sqrt{1 \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1 KΩ, is available the recovered audio signal as auxiliary output.

VCR FACILITY

The deemphathized AF signal reaches the switch follower block can provide to change the impedance of its output depending on the VCR function required.

The switch follower is driven by the threshold sensor block. This one switches both the amplifier and the switch follower by sensing the voltage at pin 4.

When no voltage is forced at pin 4 the function of pin 10 is of VCR output with low impedance ; when the voltage at pin 4 is lower or higher than its quiescent value, the amplifier is muted and the impedance of pin 10 is switched to a high value for a proper VCR input operation.

Since pin 4 reaches also the inverting input of the IF amplifier-limiter, this one can be switched off two for best insulation of the pin 10 with the TV signal path.

So, the VCR facility followed this truth table :

Mode	Vsw	or V_4	Function of Pin 10	Impedance of Pin 10
Recording	≤ 2 V	No One	Output	≤ 100 Ω
Playback	≥ 8 V	≤ 2 V	Input	≥ 10 KΩ

The output signal available when operating during recording is not dependent from both the volume and tone controls while, during playback, the input signal can be regulated by P1 and P2.

Pin 10, as input, can accept until 1 VRMS of overload.

- Pin 4 is the VCR switch driver
- Pin 10 is the VCR input/output pin.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10 KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1

The maximum slope of the RC network is of 20 dB per decade and its pole is defined by :

X_{C11} = 6.8KΩ, typically.
Pin 11 – At this pin is tied the tone capacitor
Pin 12 – is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block, that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out a this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_V = 20 \text{ Log } \frac{R5 + R4}{R5} \text{ (dB)}$$

The amplifier, thermally protected, can supply 4 W of power into a 16 Ω load with 24 V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_S, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turning on, pin 1 follows the supply voltage V_S by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_S reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_S trend, in series to the voltage $VS - V_1$ and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The threshold that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching.

By shorting pin 1 to ground through a 10 KΩ resistor the muting can be obtained.

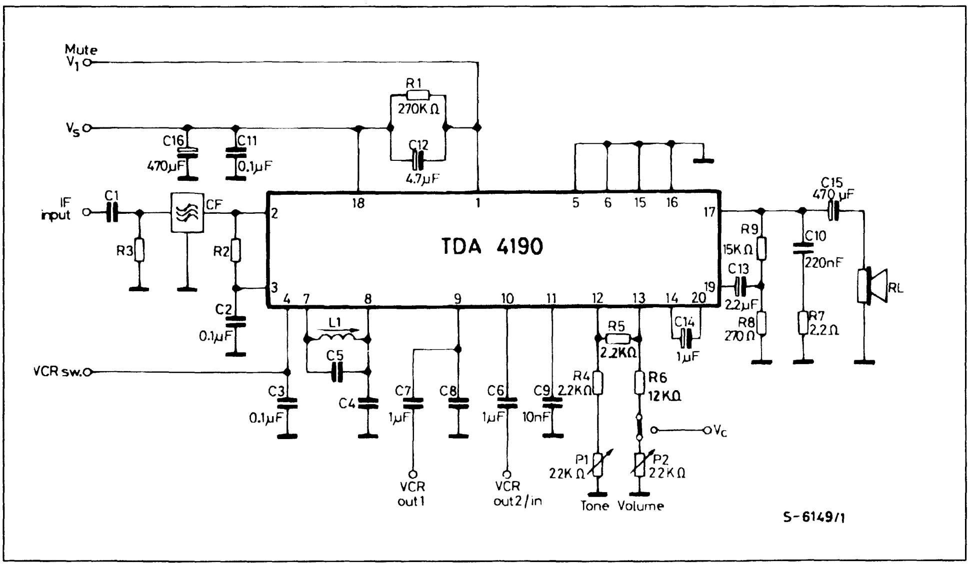
- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

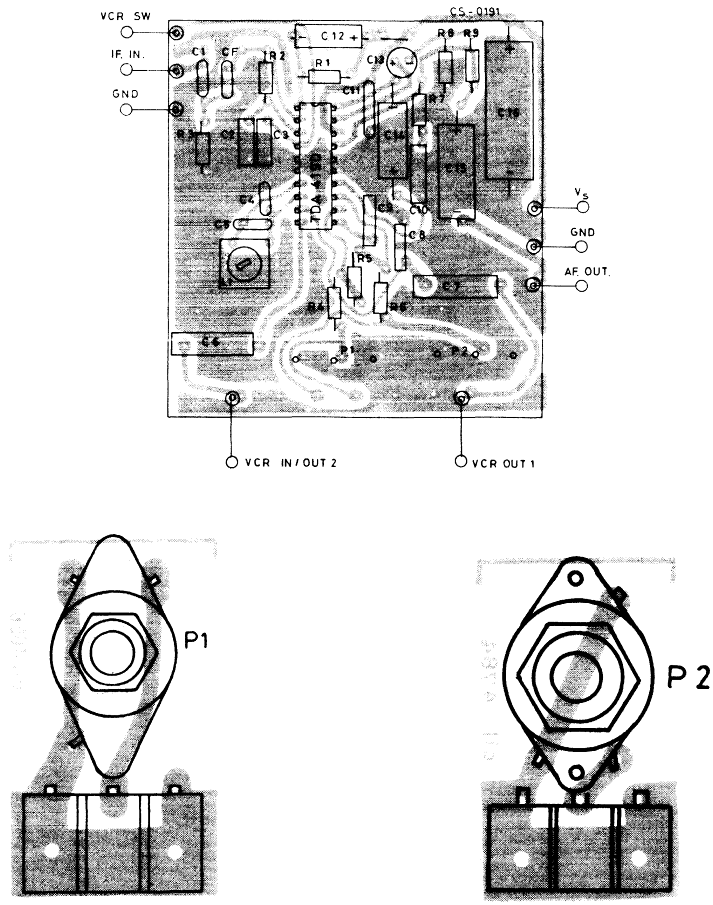
Figure 16 : Application Circuit.



SGS-THOMSON MICROELECTRONICS

Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 $Q_0 = 60$	12 $Q_0 = 80$	10 $Q_0 = 70$
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C.F.	–	Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



SGS-THOMSON
MICROELECTRONICS

TDA4420

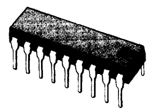
VISION IF SYSTEM WITH AFC

- HIGH GAIN-HIGH STABILITY
- VERY LOW INTERMODULATION PRODUCTS
- MINIMUM DIFFERENTIAL ERROR
- CONSTANT INPUT IMPEDANCE INDEPENDENT OF AGC
- FAST AGC GATING-ACTION, LARGELY INDEPENDENT OF PULSE SHAPE AND AMPLITUDE
- ADJUSTABLE WHITE LEVEL
- LARGE AFC OUTPUT CURRENT SWING (push-pull output)
- SWITCHABLE AFC

DESCRIPTION

The TDA4420 is a monolithic integrated circuit in 18 lead dual in-line plastic package. The functions incorporated are :

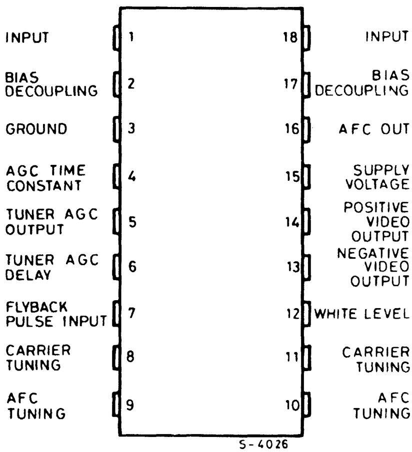
- gain controlled vision IF amplifier
- video demodulator controlled by picture carrier
- AGC detector with gating facility
- AGC amplifier for tuner drive with variable delay
- phase comparator for AFC current generation
- electronic AFC switch, controlled by a DC threshold detector
- thermally compensated push-pull AFC output stage.



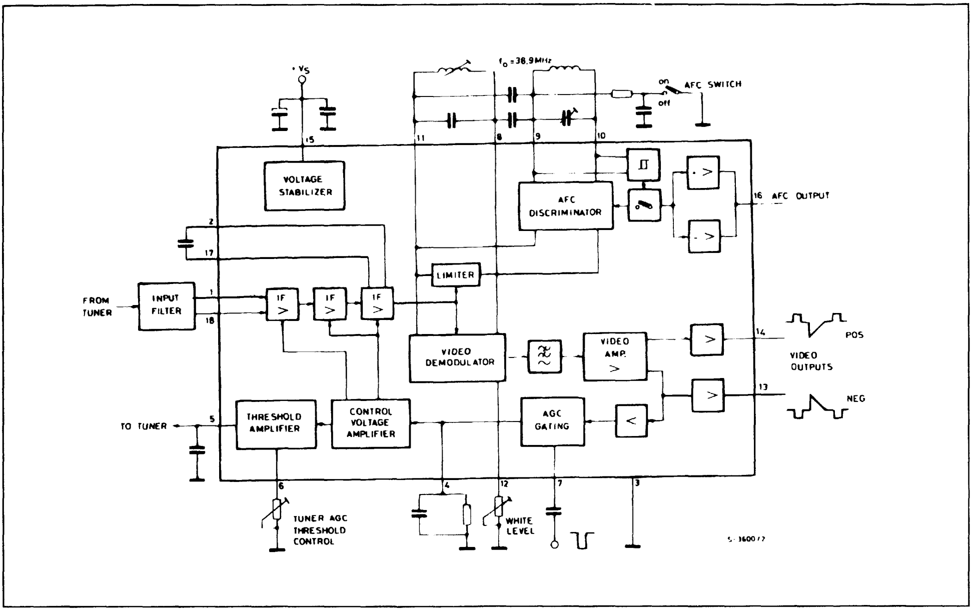
DIP-18

ORDER CODE : TDA4420

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



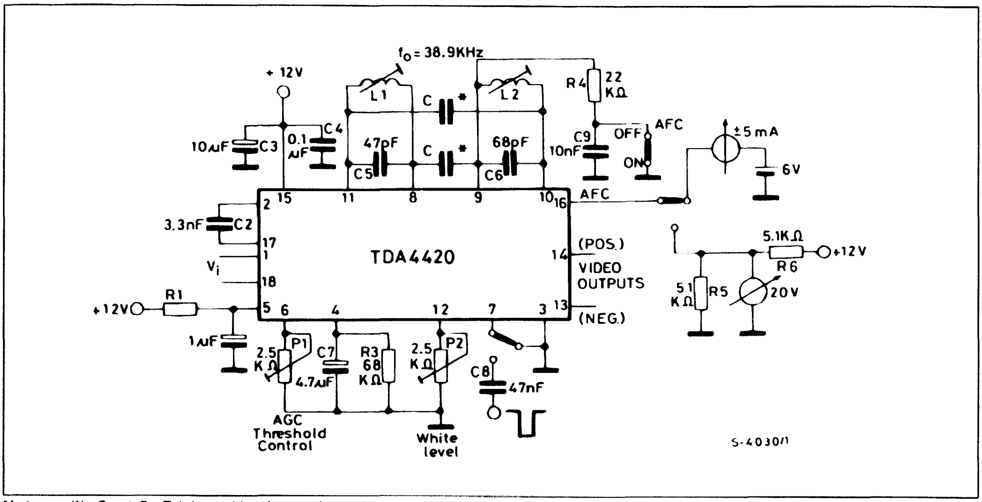
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 15)	15	V
V_5	Voltage at Pin 5	15	V
I_{13}, I_{14}	Video DC Output Current	5	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	- 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

TEST CIRCUIT



Note : (*) C ≅ 1.5 pF (pin and lead capacitance).

ELECTRICAL CHARACTERISTICS (Refer to the test circuit ; V_s = 12 V, f_0 = 38.9 MHz ; P_1 = 2.5 KΩ ; pin 7 connected to GND ; P_2 adjusted for V_{13} = 3.3 Vpp ; AFC off ; T_{amb} = 25 °C unless otherwise specified)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range (pin 15)		10	12	15	V
I_S	Suppply Current (pin 15)			52		mA
V_{14}	Video Output DC Voltage	V_{13} = 5.5 V (1)		5.6		V
V_{13}	Video Output DC Voltage	Pin 12 Open (1)			4.5	V
		Pin 12 Grounded (1)	7			V
V_{13}	Peak Black Clamping Level at Negative Video Output		1.75	1.9	2.15	V
I_{13}	Output DC Current (pin 13)	V_s = 15 V V_{13} = 8 V		1.6		mA
I_9, I_{10}	DC Control Current for AFC off		150	300		µA

Notes :
1. V_{13} and V_{14} are simultaneously adjustable by means of the resistance connected between pin 12 and ground (P_2).
2. ΔV_i = + 60 dB (see note 7) ; f_m = 100 KHz ; m = 0.82.
3. Input at pin 7 through C8.
4. The input voltage V_i can have any value within the AGC range.
5. P_2 adjusted for V_{13} = 5.5 V or V_{13} = 6.4 V ; f_m = 100 KHz ; m = 0.82.
6. ΔV_o = 1 dB ; f_m = 100 KHz ; m = 0.82.
7. The measured amplitude is assumed as 0 dB reference level of V_i that is the rms value of the unmodulated video carrier (modulation down).
8. P_2 is adjusted in order to have V_{13} = 3 Vpp at V_i = 4 mV, then the sensitivity is obtained as the minimum input voltage that maintains this output level. f_m = 100 KHz ; m = 82 %.
9. f_o = 38.9 MHz (video carrier) ; f_a = 33.4 MHz (sound carrier) ; the amplitude of the sound carrier is 30 dB below the amplitude of the video carrier.
10. V_i at f_o = 38.9 MHz (video carrier) ; f_a = 33.4 MHz, 6 dB below V_i (sound carrier) ; f_b = 34.47 MHz, 24 dB below V_i (Chroma subcarrier).
11. V_i = 40 dB ; R_5 = R_6 = 5.1 KΩ ; AFC on ; f_o = 39.9 MHz ; f_o = 37.9 MHz.
12. V_i = 40 dB ; f_o = 39.2 MHz ; AFC on ; V_{16} = 6 V.
13. V_i = 40 dB ; f_o = 38.9 MHz ; f_2 = 39.2 MHz ; AFC on ; V_{16} = 6 V.

ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_5	Available Tuner AGC Current	(2)		10		mA
V_7	AGC Gating Pulse Input Peak Voltage	f pulse = 15625 Hz (3)	– 1.5	– 3	– 5	V
V_0	Peak to Peak Video Output Signal (pin 13)	V_{13} = 5.5 V (4), (5)		3.3		V
		V_{13} = 6.4 V (4), (5)		4.2		V
ΔV_i	AGC Range	(6)	50	60		dB
B	Frequency Response (– 3 dB)	(4)	8	10		MHz
V_i	Input Sensitivity	(7), (8)	100	150	200	µV
V_{13}, V_{14}	Video carrier and video carrier 2nd harmonic leakage at video output.	V_i = 30 dB f_o = 38.9 MHz (4) 2 f_o = 77.8 MHz			30 50	mV mV
V_{14}	Sound IF at Positive Video Output (5.5 MHz)	(4), (9)	30			mV
d	Differential Distortion of Negative Video Output Signal	V_i = 30 dB (standard staircase modulating signal)		3		%
d_{im}	Intermodulation Product at Video Outputs (1.07 MHz)	(4), (10)		– 50		dB
R_i	Input Resistance between Pins 1 and 18	(4)		1.4		KΩ
C_i	Input Capacitance between Pins 1 and 18	(4)		2		pF
V_{16}	AFC Voltage Range	(11)	1		V_s–1.5	V
I_{16}	Maximum Available AFC Current	(12)			± 3	mA
$\frac{\Delta I_{16}}{\Delta f}$	AFC Slope	(13)		± 0.01		$\frac{mA}{KHz}$

Notes :
1. V_{13} and V_{14} are simultaneously adjustable by means of the resistance connected between pin 12 and ground (P_2).
2. ΔV_i = + 60 dB (see note 7) ; f_m = 100 KHz ; m = 0.82.
3. Input at pin 7 through C8.
4. The input voltage V_i can have any value within the AGC range.
5. P_2 adjusted for V_{13} = 5.5 V or V_{13} = 6.4 V ; f_m = 100 KHz ; m = 0.82.
6. ΔV_o = 1 dB ; f_m = 100 KHz ; m = 0.82.
7. The measured amplitude is assumed as 0 dB reference level of V_i that is the rms value of the unmodulated video carrier (modulation down).
8. P_2 is adjusted in order to have V_{13} = 3 Vpp at V_i = 4 mV, then the sensitivity is obtained as the minimum input voltage that maintains this output level. f_m = 100 KHz ; m = 82 %.
9. f_o = 38.9 MHz (video carrier) ; f_a = 33.4 MHz (sound carrier) ; the amplitude of the sound carrier is 30 dB below the amplitude of the video carrier.
10. V_i at f_o = 38.9 MHz (video carrier) ; f_a = 33.4 MHz, 6 dB below V_i (sound carrier) ; f_b = 34.47 MHz, 24 dB below V_i (Chroma subcarrier).
11. V_i = 40 dB ; R_5 = R_6 = 5.1 KΩ ; AFC on ; f_o = 39.9 MHz ; f_o = 37.9 MHz.
12. V_i = 40 dB ; f_o = 39.2 MHz ; AFC on ; V_{16} = 6 V.
13. V_i = 40 dB ; f_o = 38.9 MHz ; f_2 = 39.2 MHz ; AFC on ; V_{16} = 6 V.

Figure 1 : Set-up for Measurement of d_{im}.

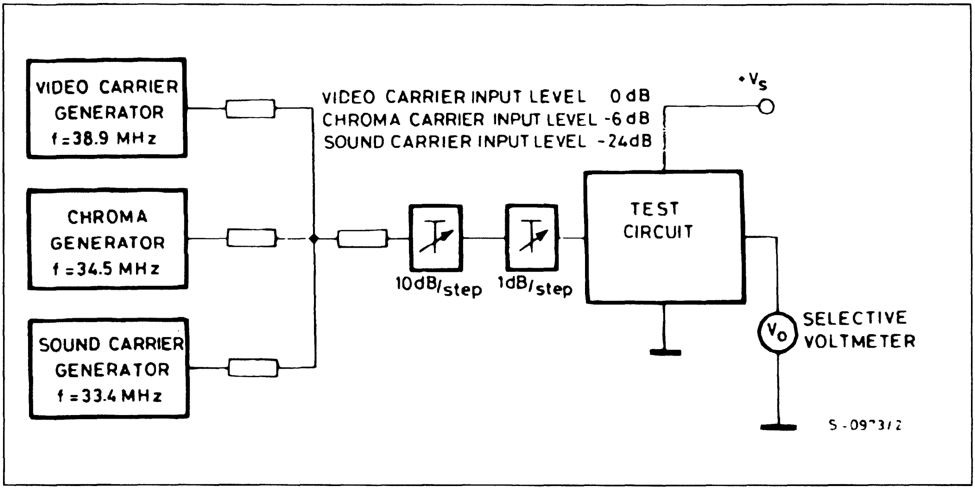
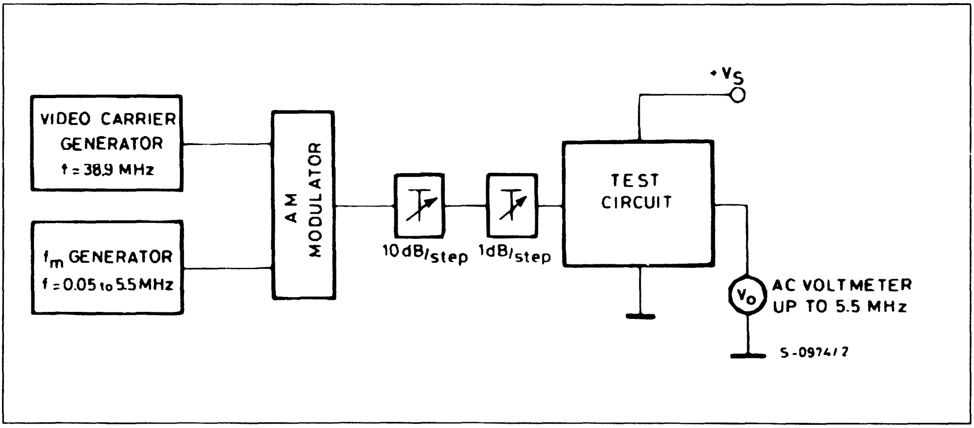


Figure 2 : Set-up for Measurement of ΔV_O.



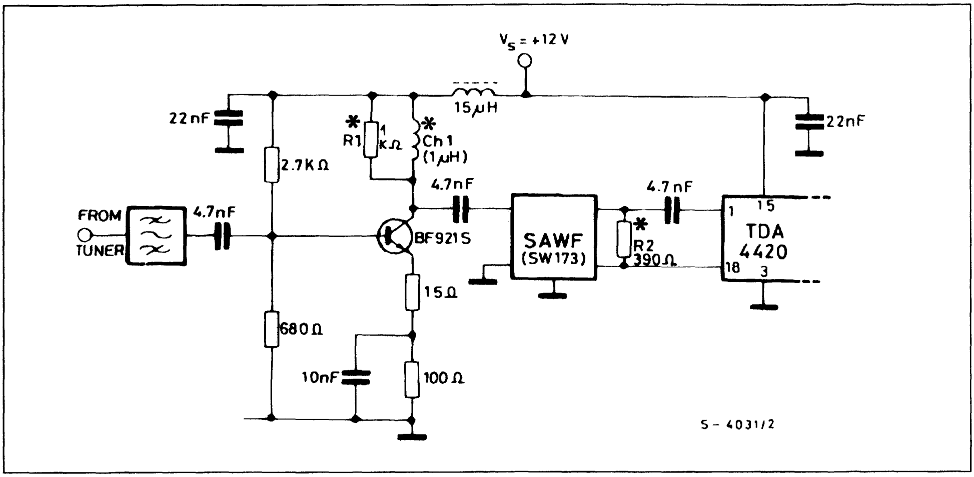


Figure 3 : Application Circuit.

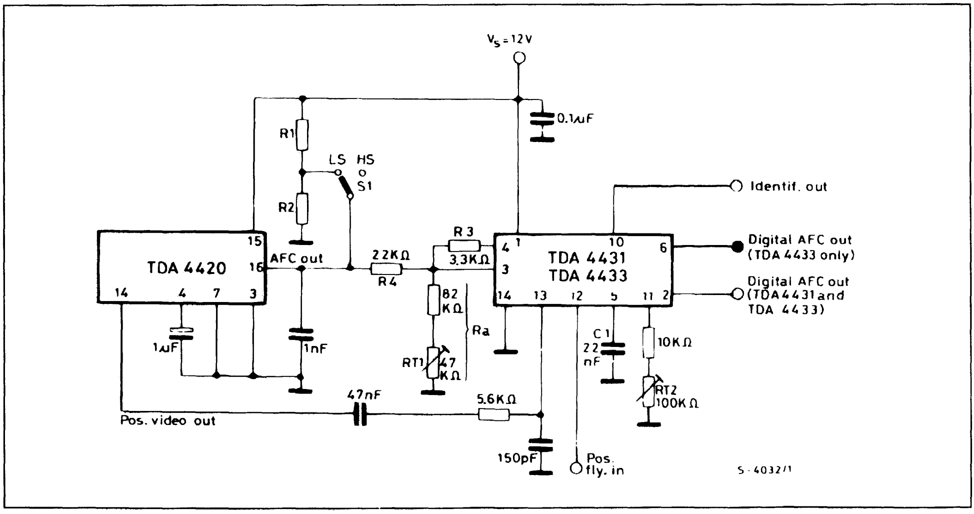


Figure 4 : TV Signal Identification Circuit.

TV signal identification circuit :

The suggested application circuit is shown in fig. 4.

The passive components are chosen as follows :

R_1 and R_2 : these define the AFC response slope. For $R_1 = R_2 = 5.1\ K\Omega$, the typical slope is 750/11 KHz/V (with AFC output unloaded).

S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

R_3 and R_4 : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12$ V, the relation is :

$$\delta f = 0.036\ (2\Delta f)\ \frac{R_3 + R_4}{R_3}$$

R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is :

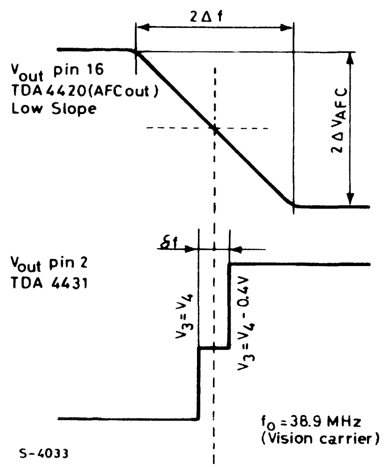
$$R_a = 33\ R_3$$

with R_3 = 3.3 KΩ, R_a can be a fixed resistor of 110 KΩ.

To make better sensitivity adjustment of trimmer R_{T2}, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.

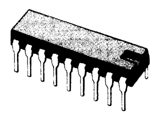
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Figure 5 : Linear and Digital AFC Characteristics (TDA4420 and TDA4431).



VIDEO IF AMPLIFIER WITH DEMODULATOR AND AFC

- SYNCHRONOUS DEMODULATORS
- GAIN CONTROLLED AMPLIFIER
- VERY HIGH INPUT SENSITIVITY
- CONSTANT INPUT IMPEDANCE INDEPENDENT OF AGC
- FIXED VIDEO OUTPUT VOLTAGE WITH SMALL TOLERANCE RANGE
- SWITCHABLE AFC
- POSITIVE OR NEGATIVE AGC GATING PULSE
- VERY FEW EXTERNAL COMPONENTS
- OUTPUT VIDEO SIGNAL NO MUCH AFFECTED BY SUPPLY VOLTAGE VARIATIONS
- THE TDA4426 AND TDA4427 GET DIFFERENT AFC CURVES (inverted AFC for TDA4427)

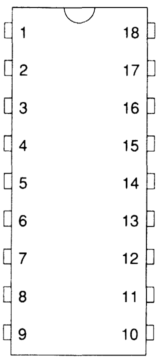


TDA4426/TDA4427
DIP18
(Plastic Package)

DESCRIPTION

The TDA4426 and TDA4427 are IF amplifier and A.M. demodulator circuits for colour or black and white television receiver using PNP tuner. They are intended for reception of negative or positive modulation CCIR standards.

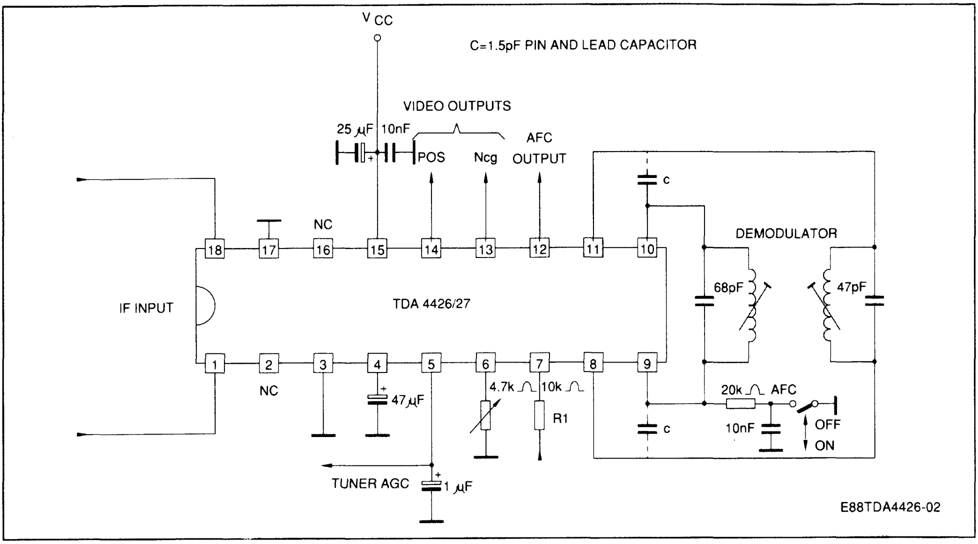
PIN CONNECTION



1 - IF input
2 - Not to be connected
3 - Ground
4 - AGC filter capacitor
5 - Tuner AGC output
6 - Tuner AGC adjustment
7 - Pulse input for AGC gated
8 - Carrier tuned circuit output 1
9 - AFC tuned circuit output 1
10 - AFC tuned circuit output 2
11 - Carrier tuned circuit output 2
12 - AFC output
13 - Negative video output
14 - Positive video output
15 - Supply voltage
16 - Not to be connected
17 - Ground
18 - IF input

E88TDA4426-01

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
V_5	Voltage at pin 5	V_{CC}	V
V_4	Voltage at Pin 4	5	V
$I_{13} - I_{14}$	Output Current to Ground Pins 13, 14. (source Current) Max : 1 s	30	mA
$I_{13} - I_{14}$	Output Current from Positive Supply Pins 13, 14. (sink current) Max : 1 s	5	mA
T_j	Junction Temperature	125	°C
T_{amb}	Operating Ambient Temperature	0 to + 70	°C
T_{stg}	Storage Temperature	– 25 to + 125	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R_{th}(j-a)	Junction - ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

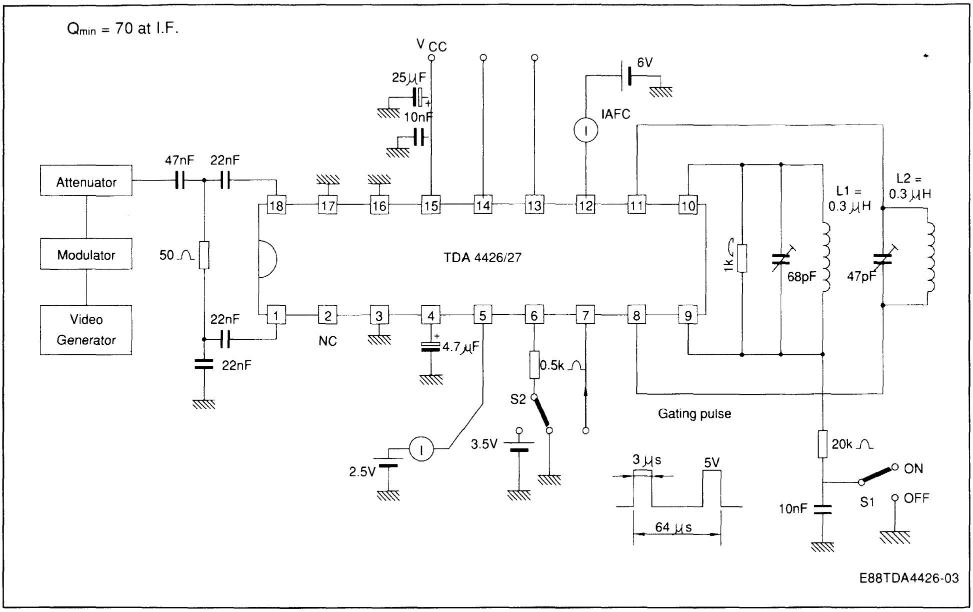
T_{amb} = + 25 °C, V_{CC} = 12 V, F = 38.9 MHz, m = 80 % (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	10	12	15	V
I_{CC}	Supply Current V_4 = 3.5 V	35		70	mA
V_{13} V_{14}	Ultra White Level	4.7	5.2 1.8	5.8	V V
V_{13} V_{14}	Top Synchro DC Output Voltage	1.75	1.9 5.0	2.05	V V
I_{13} - I_{14}	Output DC Current (V_{13} = V_{14} = 7 V)		1.5		mA
V_7	AGC Pulse Input DC Voltage		1.1		V
R_{1-18} C_{1-18}	Input Impedance		1.6 2		kΩ pF
	Input Voltage Sensitivity (output voltage 3 V_{pp})		100	150	µv
V_{13} - V_{14}	IF Residual Carrier at Video Output (F = 38.9 MHz) Pins 13 - 14		20		mVRMS
V_{13} - V_{14}	2^{nd} Harmonic Carrier at Video Output (F = 77.8 MHz) Pins 13 - 14		40		mVRMS
	Differential Distorsion on Compositive Video Signal (pin 13, 14)		3	5	%
	Intermodulation At (input condition) Color Subcarrier (1.07 MHz) PC : Picture Carrier Level = 0 dB CC : Color Subcarrier Level = – 6 dB SC : Sound Carrier Level = – 24 dB		50		dB
V_{13}	Composite Video Output Level V_I = 30 mV m = 80 % Without Load	2.7	3.0	3.3	Vpp
V_{14}		2.7	3.0	3.3	Vpp
$\Delta V_{13}/\Delta V_{CC}$, or $\Delta V_{14}/\Delta V_{CC}$	Ultra Black Level Variation with Supply Voltage (V_{CC})		0.5		%
$\Delta V_{13}/\Delta V_{CC}$, or $\Delta V_{14}/\Delta V_{CC}$	Ultra White Level Variation with Supply Voltage (V_{CC})		3		%
BW	Video Bandwidth (– 3 dB) Pins 13 - 14		6		MHz
	AGC Range	55	60		dB
I_{AGCT}	Available Turner Control Output Current (input level 10 dB higher than level threshold)	7	10		mA
	AGC Tuner Range		60		dB
I_5	Tuner AGC Output Leakage Current (V_5 = 12 V)			20	µA
V_9 - V_{10}	AFC Tank Pin DC Voltage Pins 9 - 10		3		V
V_{AFC}	AFC Output Voltage Range Pin 12 (Δf = 200 kHz)	1.0		V_{CC} – 1.5	V

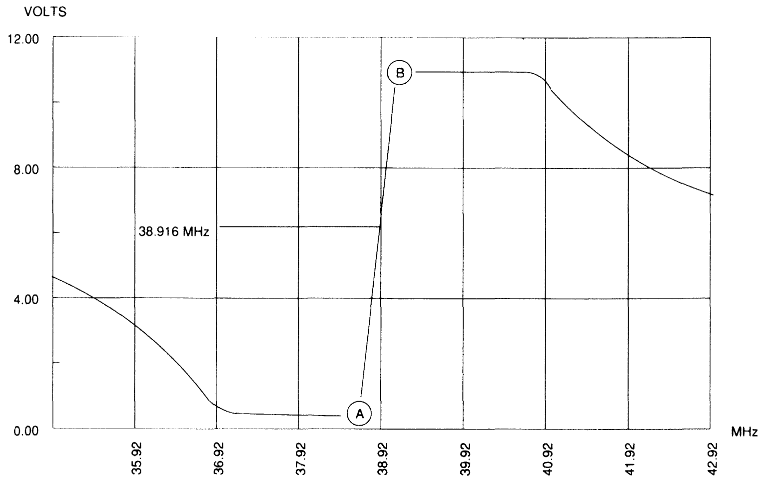
ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$\pm I_{AFC}$	AFC Output Current Pin 12		1.2		mA
$\pm \frac{\Delta I_{AFC}}{\Delta f}$	AFC Slope		0.2		mA/ 100 kHz
	AFC Output Current (AFC switch off) Pin 12			60	µA
	Switching Current for AFC Pins 9 - 10	100	150		µA

TEST CIRCUIT



TDA4426 AFC VOLTAGE VS. INPUT FREQUENCY



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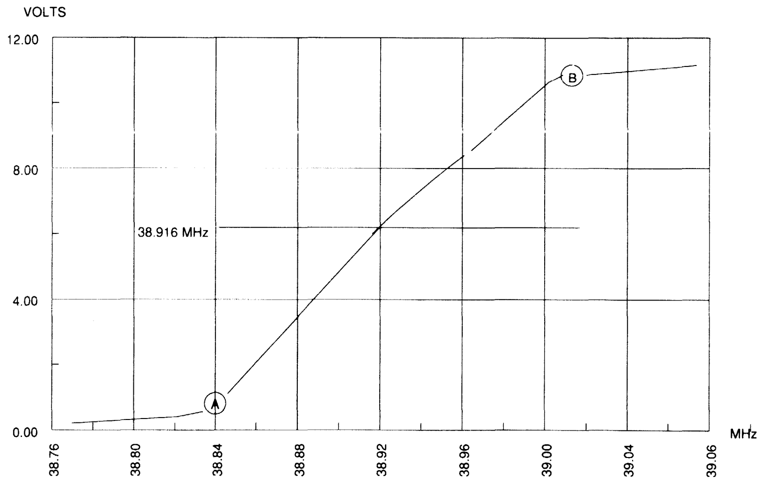
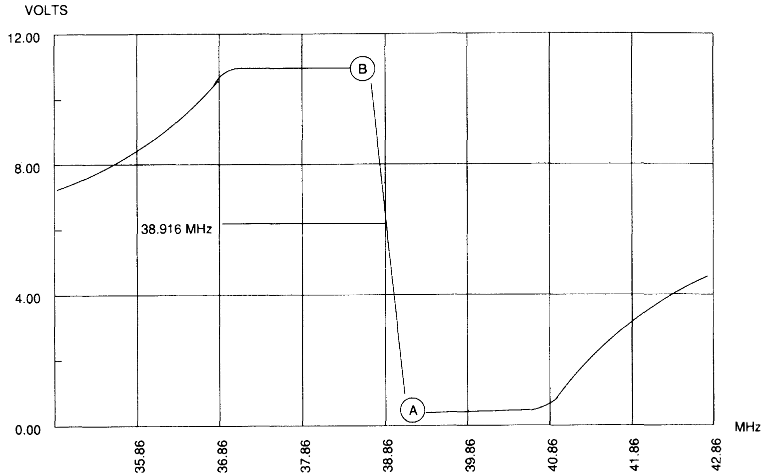


E88TDA4426-05

TDA4427 AFC VOLTAGE VS. INPUT FREQUENCY



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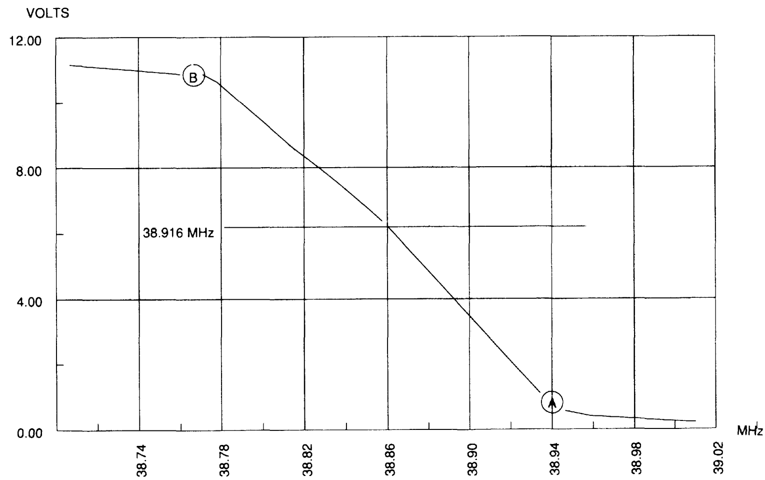
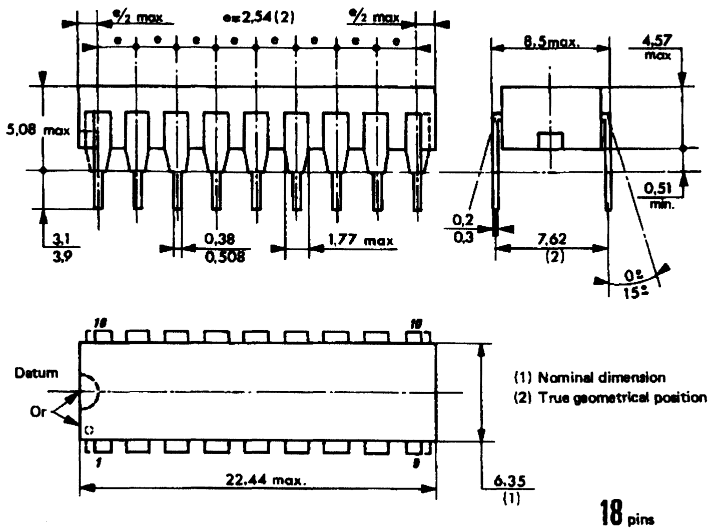


E88TDA4426-07

PACKAGE MECHANICAL DATA

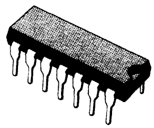
18 PINS – PLASTIC DIP



TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

The circuit features are :

- IDENTIFICATION OF TRUE TV STATIONS ONLY
- LOW IMPEDANCE OUTPUT OF THE IDENTIFICATION SIGNAL
- DIGITAL CONTROL SIGNAL FOR AUTOMATIC SEARCH AND AFC OPERATION
- THERMAL COMPENSATION OF THE VOLTAGE REGULATOR



DIP14

ORDER CODE : TDA4433

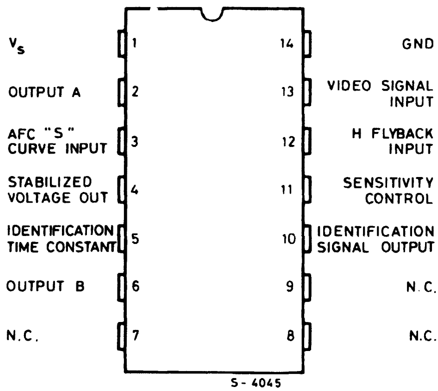
DESCRIPTION

The TDA4433 is a monolithic integrated circuit in a 14 lead dual-in-line plastic package. It integrates the following functions :

- TV signal identificator - Sync. separator - Threshold detector - Digital Interface - Voltage regulator.

It is intended for use in Electronic Program Memory tuning systems, in conjunction with M293B1.

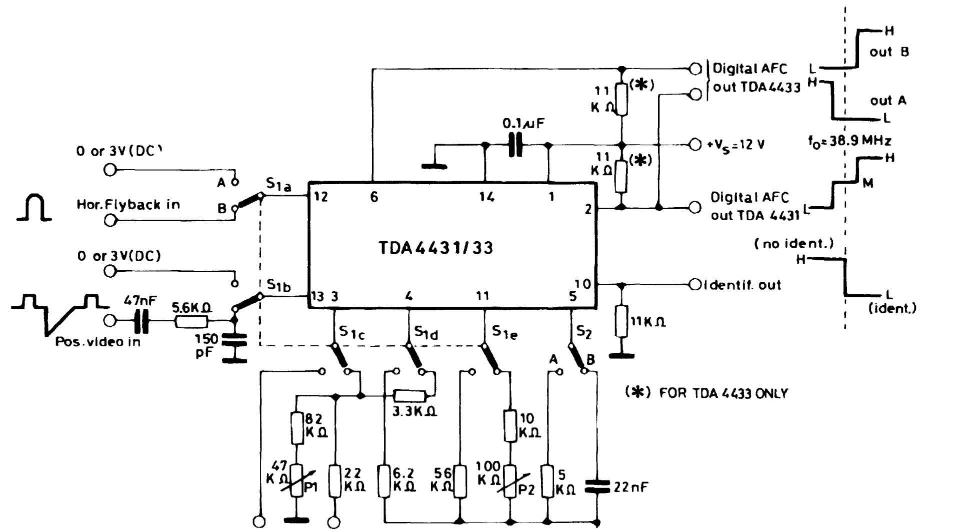
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
V_3	Voltage at Pin 3	16	V
V_{13}	Voltage at Pin 13	– 5 to + 6	V
I_6 ; I_2	Pin 6 and Pin 2 Current	1	mA
I_{10}	Pin 10 Current	2	mA
I_{11}	Pin 11 Current	2	mA
I_{12}	Pin 12 Current	± 2	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	800	mW
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

TEST CIRCUIT

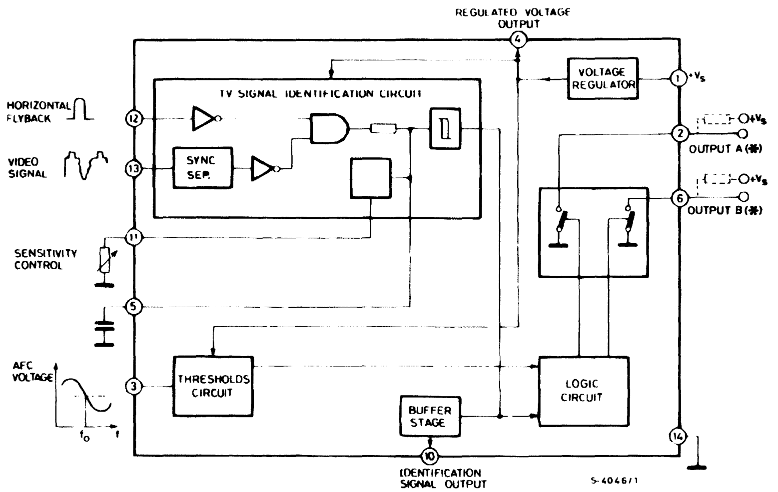


S1 A : Static tests
B : Functional tests

S2 A : DC or pulses width
B : Functional tests

P1 Digital AFC perfect tuning
P2 Sensitivity control

BLOCK DIAGRAM



* Open collector outputs.

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (refer to the test circuit ; V_s = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range (pin 1)		10.8		14.5	V
I_s	Supply Current (pin 1)	V_s = 14.5 V			30	mA
V_2	Output Voltage	f_{tuning} < fo I_2 = 1 mA	V_s – 0.5			V
		$f_{tuning} = f_o$			0.8	V
		$f_{tuning} > f_o$			0.8	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_6	Output Voltage		$f_{tuning} < f_o$ $I_6 = 1$ mA			0.8	V
			$f_{tuning} = f_o$ $I_6 = 1$ mA			0.8	V
			$f_{tuning} > f_o$	$V_s - 0.5$			V
V_3	Input Voltage Range			4		8	V
V_{3U}	Upper Threshold Voltage (see fig. 2)			$V_4 - 25$	V_4	$V_4 + 25$	mV
V_{3L}	Lower Threshold Voltage (see fig. 2)			$V_4 - 425$	$V_4 - 400$	$V_4 - 375$	mV
R_3	Input Resistance		$V_3 = V_4$	1.4			MΩ
V_4	Regulated Voltage		$I_4 = 1$ mA		6.6		V
I_4	Output Current					1	mA
R_4	Output Differential Resistance				60		Ω
$\frac{\Delta V_4}{\Delta T_s}$	Regulated Voltage Thermal Drift					± 2	mV/°C
V_{10}	Identification Output Voltage	No Identification	$I_{10} = 1$ mA	$V_s - 1.3$			V
		Identification				20	mV
R_{10}	Output Resistance				100		Ω
V_{12}	Switch off Threshold Voltage					1	V
I_{12}	Input Flyback Current			0.5		1.5	mA
R_{12}	Input Resistance		$V_{12} = 3$ V		10		KΩ
t_{fly}	Flyback Pulse Duration			10		17	µsec.
t	Time Delay between Leading Edges of Flyback Pulse and Sync. Pulse.			0		3.5	µsec.
V_{13}	Video Input Signal (peak to peak)			2.5		4.5	V
V_{13}	Sync. Pulse Amplitude (above black level)			0.52			V
R_{13}	Input Resistance					1.5	KΩ

Figure 1 : Medium Output Voltage vs. Supply Voltage.

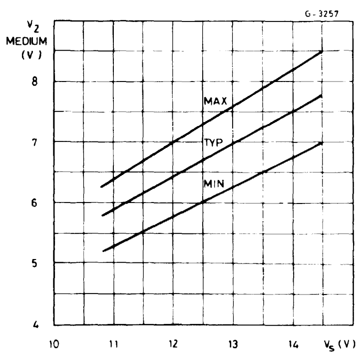
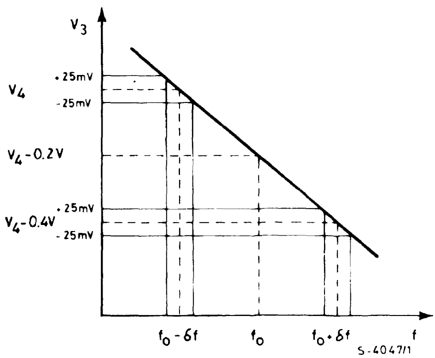


Figure 2 : Digital AFC Threshold Voltage vs. Frequency.



Input Voltage (V_3)	TDA4433	
	Output Voltage (V_2)	Output Voltage (V_6)
$V_3 > V_4$	High level	Low Level
$V_4 - 0.4\ V < V_3 < V_4$	Low Level	Low Level
$V_2 < V_4 - 0.4\ V$	Low Level	High Level

APPLICATION INFORMATION (refer to the block diagram)

TV SIGNAL IDENTIFICATION CIRCUIT :

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.

The signal identification is carried out by charging the capacitor connected to pin 5 ; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.

When the identification has been made, a signal (level L) is available at pin 10.

THRESHOLD CIRCUIT :

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.

With a correct TV signal, the output levels corresponding to the 3 ranges are :

	TDA4433	
	(V_2)	(V_6)
$f_o - \delta f$	H	L
f_o	L	L
$f_o + \delta f$	L	H

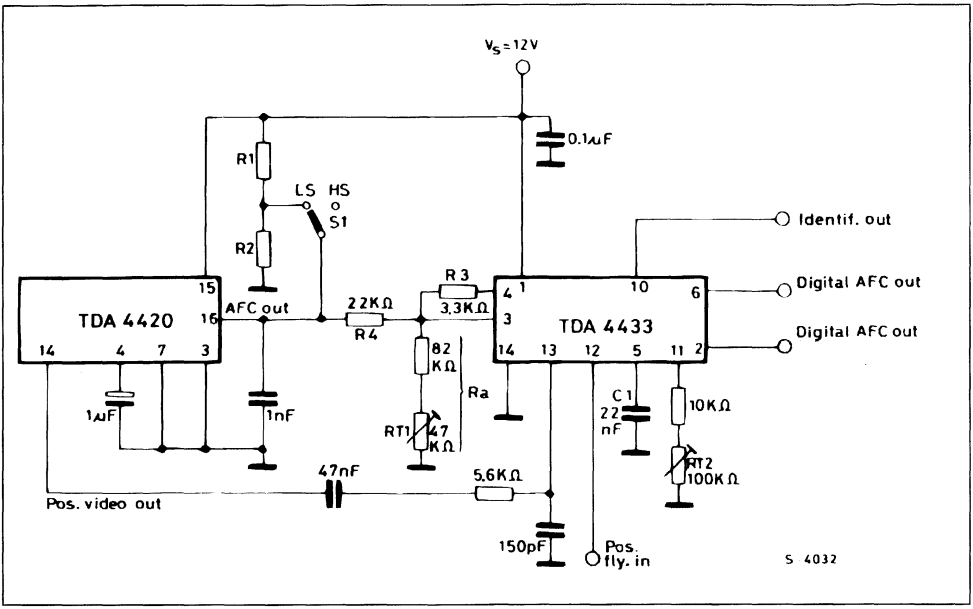
L = Low level.
H = High level.

The TDA4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

VOLTAGE REGULATOR

The circuit can deliver 1 mA and it can be used as D/A converter reference to supply fine tuning voltage.

Figure 3 : Application Circuit.



The passive components should be chosen as follows :

R_1 and R_2 : these define the AFC response slope. For $R_1 = R_2 = 5.1$ KΩ, the typical slope is 750/11 KHz/V (with AFC output unloaded).

S_1 : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

R_3 and R_4 : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width (δf) calculated from the linear AFC width (2Δf). With V_s = 12 V, the relation is :

$$\delta f = 0.036\ (2\Delta f)\ \frac{R_3 + R_4}{R_3}$$

R_{T1} : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is :

$$R_a = 33\ R_3$$

with R_3 = 3.3 KΩ, R_a can be a fixed resistor of 110 KΩ.

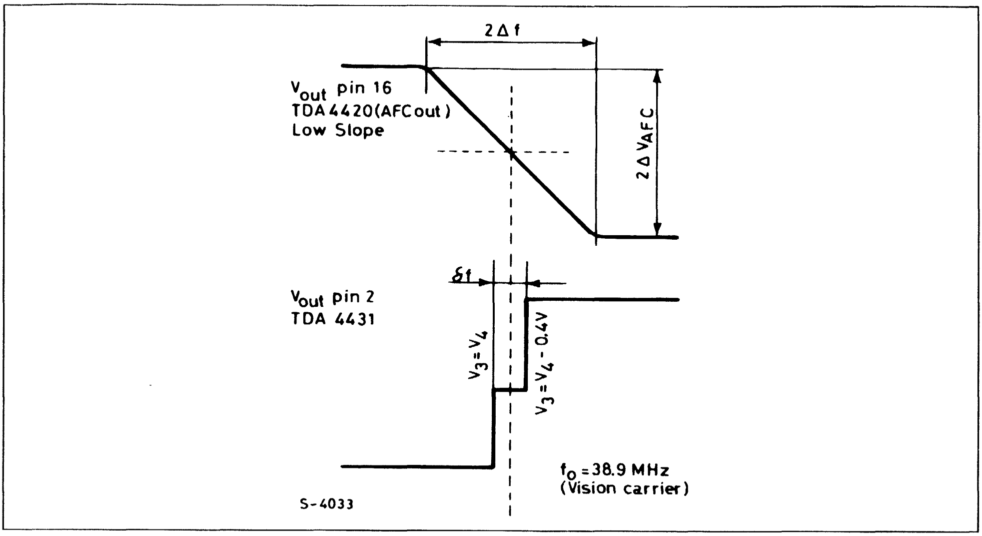
R_{T2} : by means of this trimmer it is possible to choose the better sensitivity. It is possible to put a fixed resistor at pin 11 in the range of 68 KΩ to 100 KΩ.

To make a better sensitivity adjustment of trimmer R_{T2}, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field.

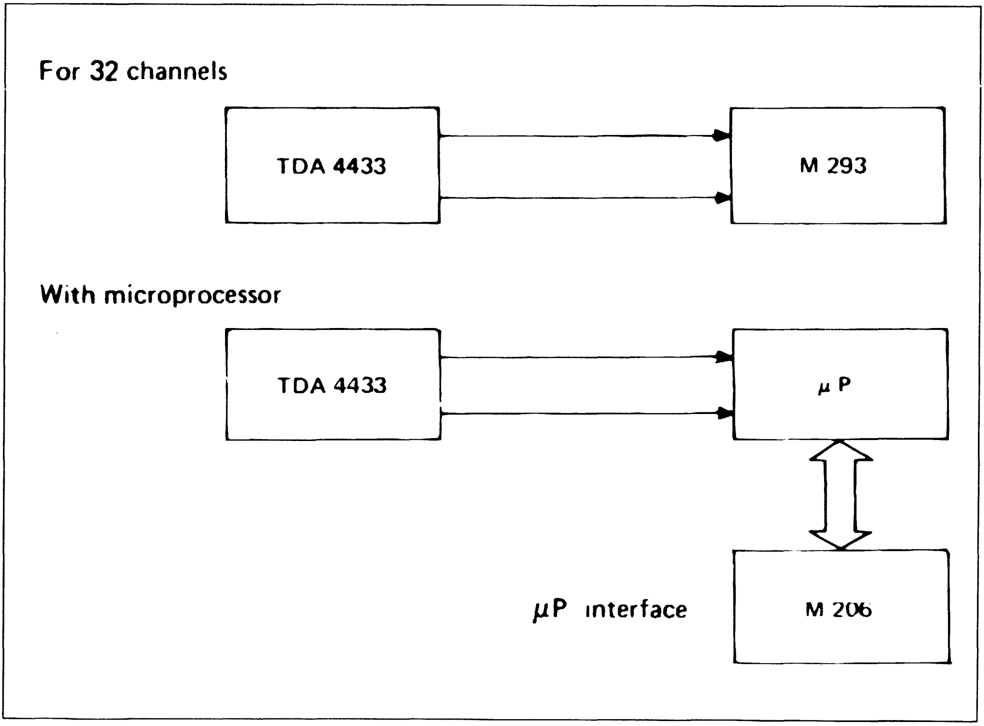
Furthermore, the action of the syncs separator must be as quick as possible.

In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Figure 4 : Linear and Digital AFC.



EPM SYSTEM CONFIGURATIONS

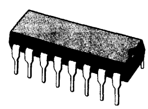


SGS-THOMSON MICROELECTRONICS

TDA4443

VIDEO IF AMPLIFIER FOR MULTISTANDARD APPLIANCES

- SWITCHING OFF THE IF AMP. WHEN OPERATING IN VTR MODE VIA DIN PLUG
- DEMODULATION OF NEGATIVE OR POSITIVE IF SIGNALS. THE OUTPUT REMAINS ON THE SAME POLARITY IN EVERY CASE
- IF AGC AUTOMATICALLY ADJUSTS TO THE ACTUAL STANDARD
- TWO AGC POSSIBILITIES FOR B/G MODE :
  1. GATED AGC
  2. UNGATED AGC ON SYNC. LEVEL AND CONTROLLED DISCHARGE DEPENDENT ON THE AVERAGE SIGNAL LEVEL FOR VTR AND PERI TV APPLICATIONS
  FOR STANDARD L : FAST AGC ON PEAK WHITE BY CONTROLLED DISCHARGE
- POSITIVE OR NEGATIVE GATING PULSE
- EXTREMELY HIGH INPUT SENSITIVITY
- LOW DIFFERENTIAL DISTORTION
- CONSTANT INPUT IMPEDANCE
- VERY HIGH SUPPLY VOLTAGE REJECTION
- FEW EXTERNAL COMPONENTS
- LOW IMPEDANCE VIDEO OUTPUT
- SMALL TOLERANCES OF THE FIXED VIDEO SIGNAL AMPLITUDE
- ADJUSTABLE, DELAYED AGC FOR PNP TUNERS
- PIN COMPATIBLE WITH THE IF IC's TDA4426 AND TDA4427

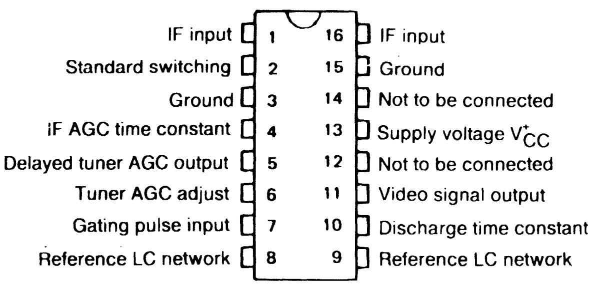


TDA4443
DIP16
(Plastic Package)

DESCRIPTION

The TDA4443 is a Video IF amplifier with standard switch for multistandard colour or monochrome TV sets, and VTR's.

PIN CONNECTIONS



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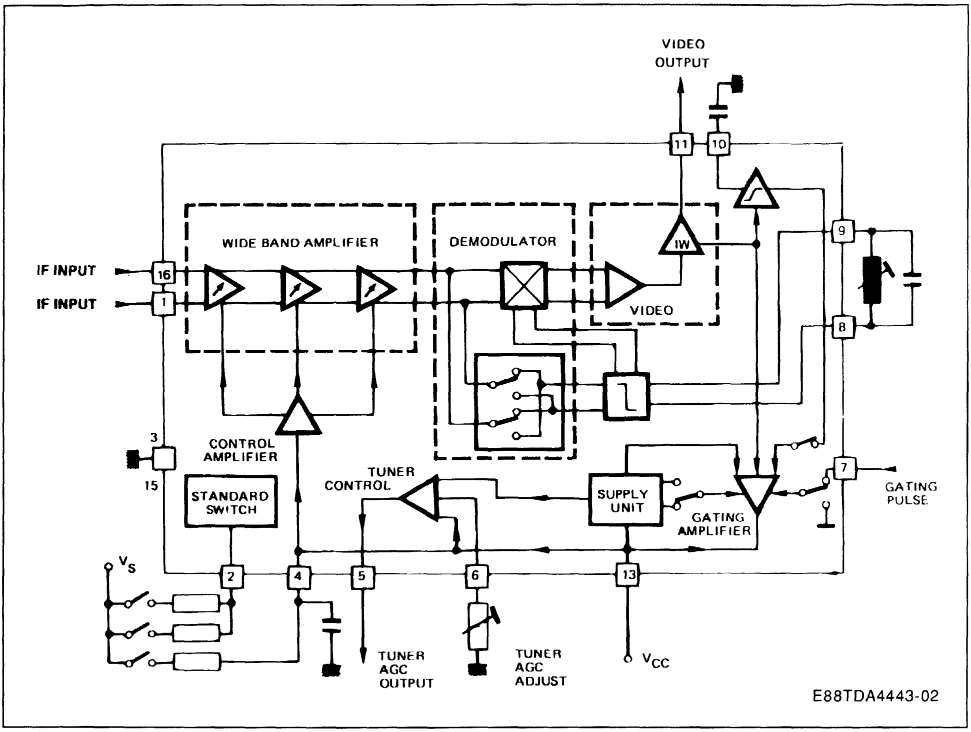
BLOCK DIAGRAM



GENERAL DESCRIPTION

This video IF processing circuit integrates the following functional blocks :

- Three symmetrical, very stable, gain controlled wideband amplifier stages - without feedback by a quasi-galvanic coupling.
- Demodulator controlled by the picture carrier
- Video output amplifier with high supply voltage rejection
- Polarity switch for the video output signal
- AGC on peak white level
- Gated AGC
- Discharge control
- Delayed Tuner AGC
- At VTR reading mode the video output signal is at ultra white level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage Range	Pin 13	15	V
V_0	Open Loop Voltage	Pin 5	max. V_{CC}	V
V_{ext}	External Voltage	Pin 4	12	V
I_4	Control Current for VTR Mode	Pin 4	0.3	mA
I_2	Control Current for Standard Mode	Pin 2	0.5	mA
I_0	Max. Video Output Current	Pin 11	5	mA
I_0	Short Circuit Current ($t \leq$ 1sec)	Pin 11	30	mA
P_{tot}	Power Dissipation		1	W
T_j	Junction Temperature		125	°C
T_{amb}	Ambient Temperature Range		0 to + 70	°C
T_{stg}	Storage Temperature Range		– 25 to + 125	°C

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified. Test Circuits Page 6.

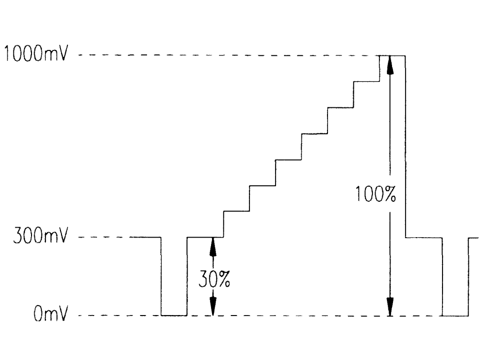
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	Pin 13	10	12	15	V
I_{CC}	Supply Current V_{CC} = 12V V4 = 3.5V Pin 6 Pin 7 Pin 2 open Vin = 0	Pin 13		55	75	mA
V_{11}	Ultra White Level at Standard B/G VCC = 15V V4 = 3.5V	Pin 11	4.8	5.1	5.6	V
V_{AA}	Ultra black clamping level at standard B/G SIGNAL 1	Pin 11	1.70	1.85	2.10	V
V_O	Picture to sync. output voltage of the video signal without load in standard B/G (residual carrier 10%) without load SIGNAL 1	Pin 11	2.6	2.9	3.3	V_{PP}
V_O	Picture to blanking level output voltage of the video signal without load in standard L (blanking level at 28% of carrier amplitude) SIGNAL 2 (residual carrier 5%)	Pin 11	1.80	2.1	2.40	V_{PP}
$\frac{\Delta(V_p - V_{blank})}{V_p - V_{blank}}$	Output voltage change of the picture to blanking level from standard L to standard B/G (mode BG signal 1 mode L signal 2)	Pin 11			10	%
ΔVblack	Supply voltage influence on the ultra black level in standard B/G	Pin 11		0.5		%V
ΔVwhite	Supply voltage influence on the ultra white level in standard B/G	Pin 11		1		%V
ΔVvideo	Video Bandwith Video Signal Attenuation with Vin at 4.43MHZ	Pin 11		1	1.5	dB
Bvideo	Video Bandwidth at – 3dB	Pin 11	6			MHz

ELECTRICAL OPERATING CHARACTERISTICS (continued)
T_{amb} = 25°C, V_{CC} = 12V, unless otherwise specified. Test Circuits Page 6.

Symbol	Parameter		Min.	Typ.	Max.	Unit
ΔVvideo	Video frequency response changes within the AGC range	Pin 11		0.5	2.0	dB
I_O	DC Output Current V_{11} = 10V V_{CC} = 15V	Pin 11		1.5	2	mA
I_7	Gating Pulse Current	Pin 7	0.30		1.0	mA
V_7	DC Voltage at Gating Input	Pin 7		1.3	1.6	V
V_1	Input Voltage Sensitivity Vin with Vout = VO – 3dB Standard B/G SIGNAL 1	Pin 1–16		120		μV_{RMS}
I	Control Current for Status B (see status of mode switching) V2 = 5V	Pin 2		10	40	µA
I	Control Current for Status C (see status of mode switching) V2 = 6.3V	Pin 2		60	400	µA
ΔG_{IF}	IF AGC Range			60		dB
I_{AGC}	Available Tuner AGC Current (10dB above the AGC starting point)	Pin 5	8	12		mA
ΔAGC	Delay Between Tuner AGC and IF AGC (pin 6 not connected)	Pin 5		50		dB
VIF V2IF	IF residual carrier at the video o/p withing the AGC range 38.9MHz 77.8MHz	Pin 11 Pin 11		20 50		mVRMS mVRMS
d	Differential Distortion on Composite Video Signal Amplitude Signal 3	Pin 11			5	%
aM	Attenuation of sound to color carrier intermodulation signal (1.07MHz) referred to the demodulated color carrier Picture Carrier = 0dB Color Carrier = – 6dB Sound Carrier = – 24dB	Pin 11		50		dB
$\frac{\Delta Sync}{Sync}$	Sync. Pulse Compression Within the IF AGC Range			3		%
RI CI	Input Impedance : Resistance Capacitance	Pin 1–16 Pin 1–16		2.5 2		KΩ pF
V	Switch off Control Voltage for VTR Mode	Pin 4	9		10	V
I	Switch off Current for VTR Mode	Pin 4			150	µA

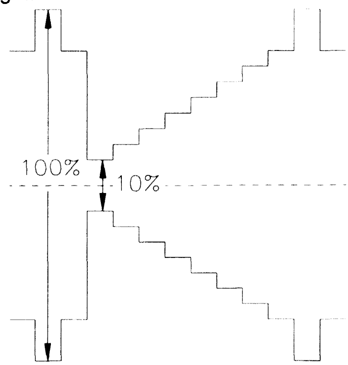
SIGNAL 1

Demodulated Signal.



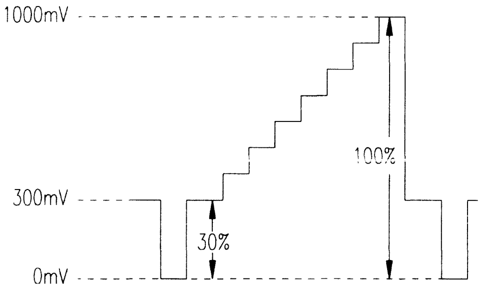
E88TDA4443-03

IF Signal.



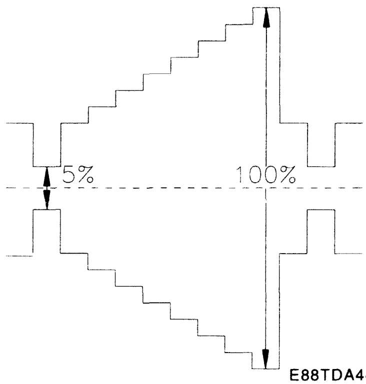
E88TDA4443-04

SIGNAL 2



E88TDA4443-05

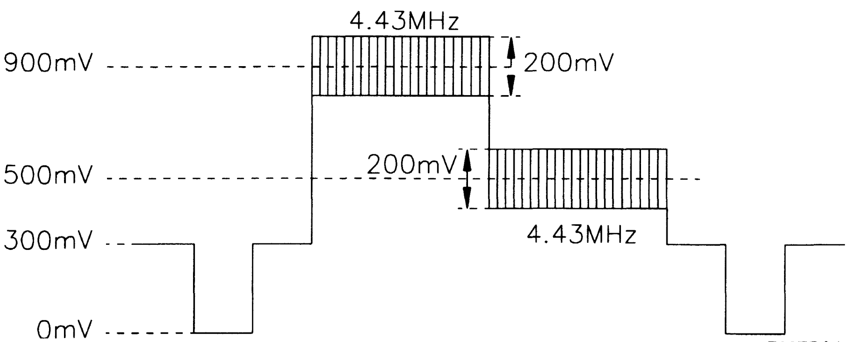
Demodulated Signal.



E88TDA4443-06

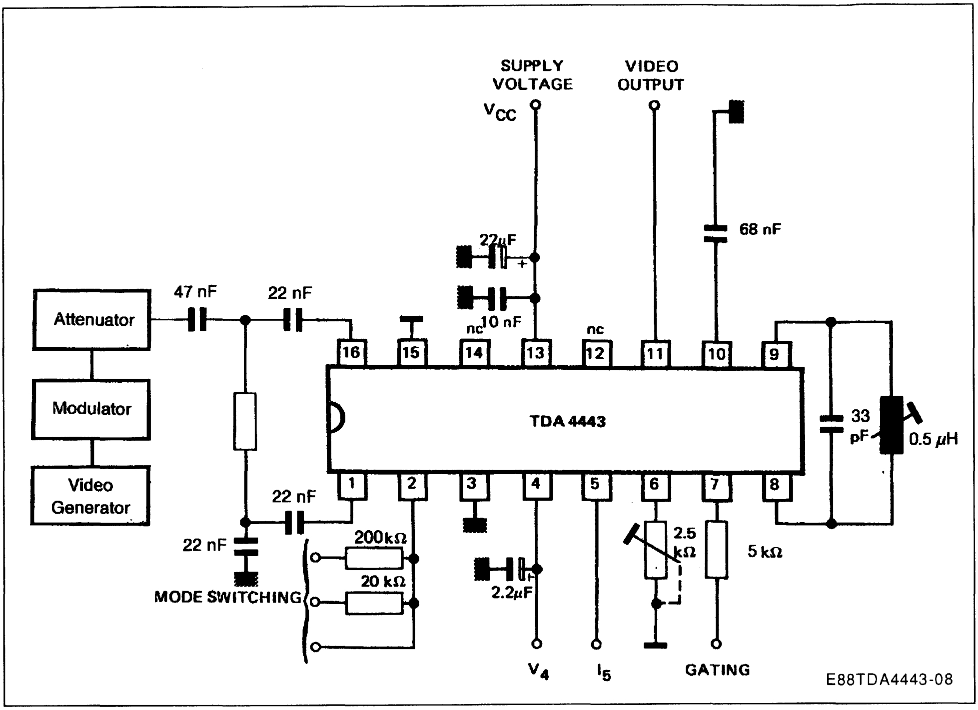
SIGNAL 3

Demodulated Signal.



E88TDA4443-07

TEST CIRCUIT



DEFINITION OF MODE SWITCHING

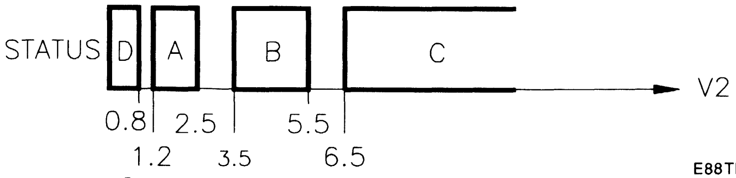
Status	Pin 2	Pin 4	Function
A	Not connected	No External Voltage	Standard B/G mode, gated charge and discharge.
B	12V High Impedance	No External Voltage	Standard B/G, ungated, charging up to sync. level, discharging dependant from average signal (peri operation).
C	12V Low Impedance	No External Voltage	At standard L ungated, charging up to peak white level, discharge dependant from average signal level, inverted polarity of the video output.
D	No Specifications	≥ 7.5V	In VTR reading mode the IF amplifier is blocked, turned gain controlled down : The video output signal is fixed at constant ultra white level for standard B/G mode.

The gating pulse at Pin 7 is internally switched off.

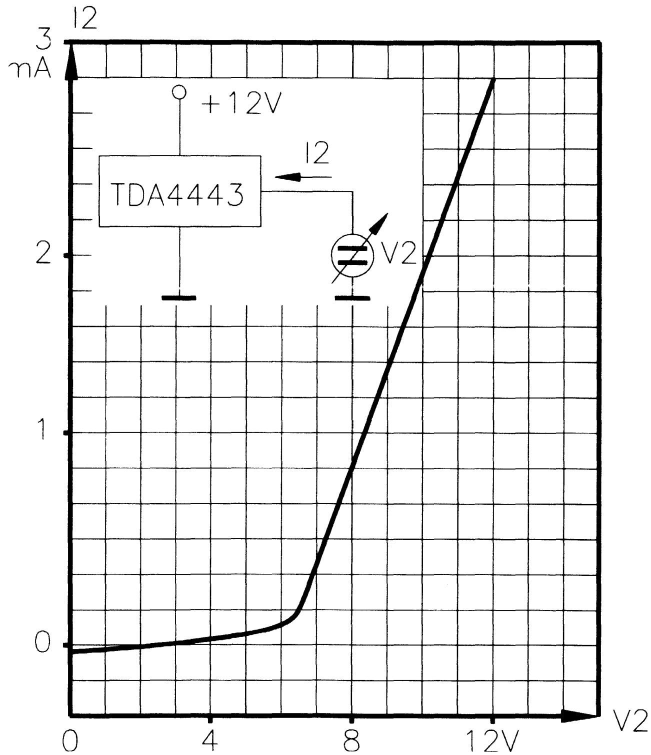
STATUS OF MODE SWITCHING, REFERRING TO CONTROL VOLTAGE PIN 2

Control Voltage Pin 2	Connections of Pin 2	Status	Function
(1.2 to 2.5V*)	Open	A	Standard B/G gated sync. operation.
3.0 to 5.0V	High Impedance	B	Standard B/G, no Sync, Operation
> 6.2V	Low Impedance	C	Standard L
0.0 to 0.8V	Ground	D	Standard L

* Voltage measured on Pin 2.



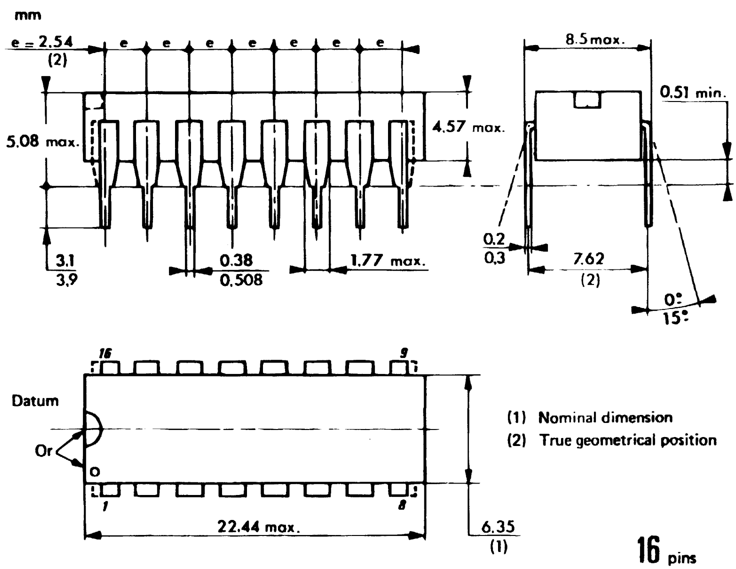
E88TDA4443-09



E88TDA4443-10

PACKAGE MECHANICAL DATA

16 PINS– PLASTIC DIP

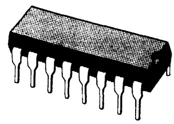


SGS-THOMSON
MICROELECTRONICS

TDA4445A
TDA4445B

SOUND IF AMPLIFIER

- QUADRATURE INTERCARRIER DEMODULATOR
- VERY HIGH INPUT SENSITIVITY
- GOOD SIGNAL TO NOISE RATIO
- FAST AVERAGING AGC
- IF AMPLIFIER CAN BE SWITCHED OFF FOR VTR MODE
- GOOD AM SUPPRESSION
- OUTPUT SIGNAL STABILIZED AGAINST SUPPLY VOLTAGE VARIATIONS
- VERY FEW EXTERNAL COMPONENTS



TDA4445A
TDA4445B
DIL16
(Plastic Package)

DESCRIPTION

TDA4445A :

Sound IF amplifier, with FM processing for quasi parallel sound system.

TDA4445B :

Sound IF amplifier, with FM processing and AM demodulator, for multi-standard sound TV appliances.

TDA4445B additionnal :

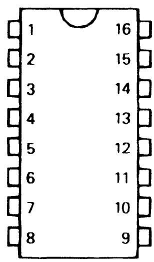
Bistandard applications (B/G and L)

No adjustment of the AM demodulator

Low AM distortion

PIN CONNECTIONS

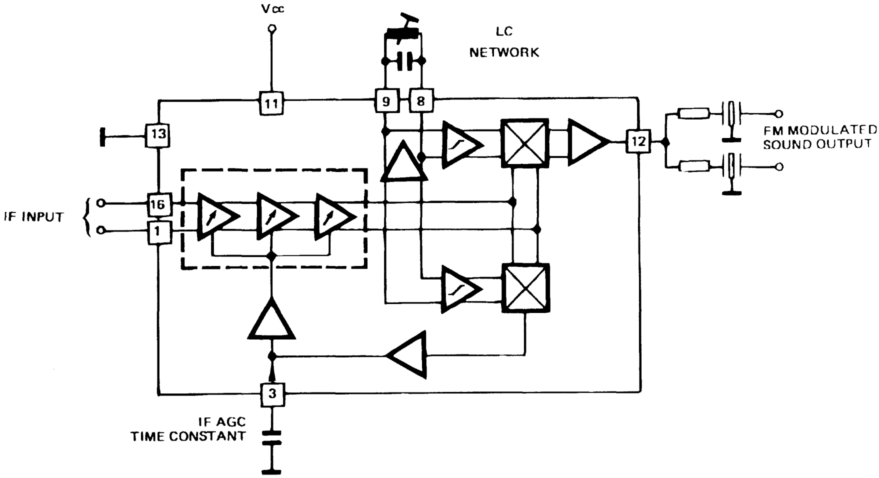
TDA4445A	TDA4445B
1 - IF Input	1 - IF Input
2 - Not to be connected	2 - Not to be connected
3 - IF AGC Time Constant	3 - IF AGC Time Constant
4 - Not to be connected	4 - Not to be connected
5 - Not to be connected	5 - Averaging capacitor
6 - Not to be connected	6 - A.F. Sound Output
7 - Not to be connected	7 - Not to be connected
8 - Reference LC Network	8 - Reference LC Network
9 - Reference LC Network	9 - Reference LC Network
10 - Not to be connected	10 - Not to be connected
11 - Supply Voltage	11 - Supply Voltage
12 - FM modulated sound output	12 - FM modulated sound output
13 - Ground	13 - Ground
14 - Not to be connected	14 - Not to be connected
15 - Not to be connected	15 - Not to be connected
16 - IF Input	16 - IF Input



E88TDA4445A-01

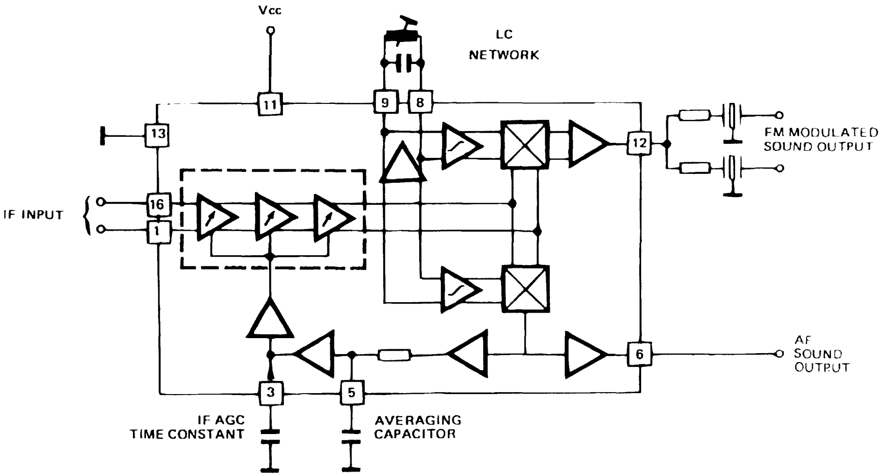
BLOCK DIAGRAMS

TDA4445A



E88TDA4445A-02

TDA4445B



E88TDA4445A-03

GENERAL DESCRIPTION

This circuit includes the following functions :

- Three symmetrical and gain controlled wide band amplifier stages, which are extremely stable by quasi DC coupling without feedback.
- Averaging AGC with discharge control circuit
- AGC voltage generator

Quasi parallel sound operation :

- High phase accuracy of the carrier signal processing, independent from AM
- Linear quadrature demodulator
- Sound-IF-amplifier stage with impedance converter

AM-Demodulation (only TDA4445B) :

- Carrier controlled demodulator
- Audio frequency stage with impedance converter
- Averaging low pass AGC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage Range	Pin 11	15	V
I_{CC}	Supply Current	Pin 11	70	mA
V_{ext} V_{ext}	External Voltages TDA4445A/TDA4445B	Pin 3 Pin 12	12 8	V V
V_{ext} V_{ext}	External Voltages only TDA4445B	Pin 5 Pin 6	8 8	V V
P_{tot}	Power Dissipation		1	W
T_j	Junction Temperature		125	°C
T_{amb}	Ambient Temperature Range		0 to + 70	°C
T_{stg}	Storage Temperature Range		– 25 to + 125	°C

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 12V (unless otherwise specified)

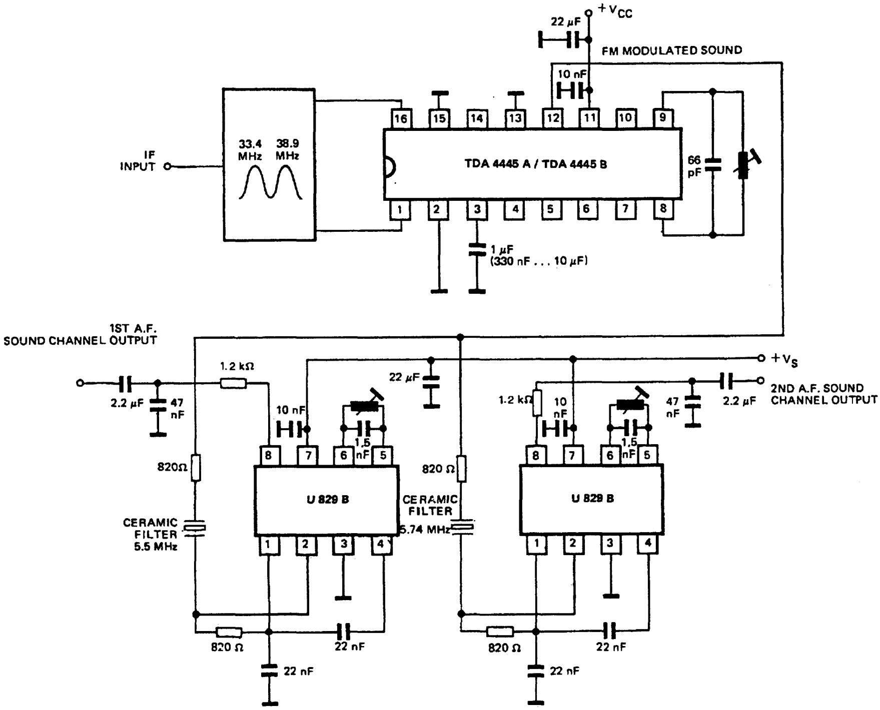
Symbol	Parameter		Min.	Typ.	Max.	Unit
	DC CHARACTERISTICS					
V_{CC}	Supply Voltage	Pin 13	10	12	15	V
I_{CC}	Supply Current V_3 = 3.5V	Pin 11		45	60	mA
V_O	DC Output Voltage V_3 = 3.5V	Pin 12	4.25	5	5.75	V
I	Output DC Current V_3 = 3.5V V_{11} = 12V	Pin 12	1		2	mA
R	Input Impedance	Pins 1-16		2		KΩ
C		Pins 1-16		2		pF
V	Switch off Control Voltage for VTR Mode	Pin 3	9		10	V
I	Switch off Control Current for VTR Mode	Pin 3			150	µA
Δ_{GIF}	AGC CHARACTERISTICS IF AGC Range			62		dB
	QUASI PARALLEL SOUND OPERATION (TDA4445A and TDA4445B) f_{PC} = 38.9MHz, f_{SC1} = 33.4MHz, f_{SC2} = 33.16MHz, PC/SC_1 = 13dB, PC/SC2 = 20dB, PC unmodulated					
V_I	Min. Input Voltage 5.5MHz - Output Signal - 3dB	Pins 1-16		70		μV_{eff}
V_I	Max. Input Voltage 5.5MHz - Output Signal + 1dB	Pins 1-16		90		mV_{eff}
	Sound-IF-output Voltage V_{1-16} = 20mV_{eff} SC unmodulated					
V_O	5.5MHz Output Voltage	Pin 12	200		400	mV_{eff}
V_O	5.74MHz Output Voltage	Pin 12	100		300	mV_{eff}
	Signal to noise ratio measured according to CCIR 468-2 Picture Modulation Ratio 90% Reference signal : V_{1-16} = 10mV, FM-frequency deviation 30kHz → Out 1 350mV_{RMS} f_{mod} = 1kHz, measured at audio-output Out 2 350mV_{RMS}					
$\frac{S+N}{N}$	Black Screen 1. Channel/2. Channel	Pin 12		55/50		dB
$\frac{S+N}{N}$	Grid Screen 1. Channel/2. Channel	Pin 12		45/40		dB

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)
T_{amb} = + 25°C, V_{CC} = 12V (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_I	AM DEMODULATION (TDA4445B only) f_{SC} = 39.2MHz, m = 80%, f_{mod} = 1kHz Min. Input Voltage Audio Output Signal - 3dB	Pins 1-16		70		μV_{eff}
V_O	Output DC Voltage V_{1-16} = 10mV_{eff} unmodulated	Pin 6	3.3		4.5	V
I	Output DC Current V_6 = 7.5V, V_3 = 3.5V	Pin 6	0.3		1.2	mA
d	Distortion V_{1-16} = 10mV f_{mod} = 1kHz , m = 80%	Pin 6		2.5	4	%
V_O	AF Output Voltage V_{1-16} = 100mV_{eff} m = 50% , f_{mod} = 10KHz	Pin 6	500	700	900	mV_{eff}

TYPICAL APPLICATION

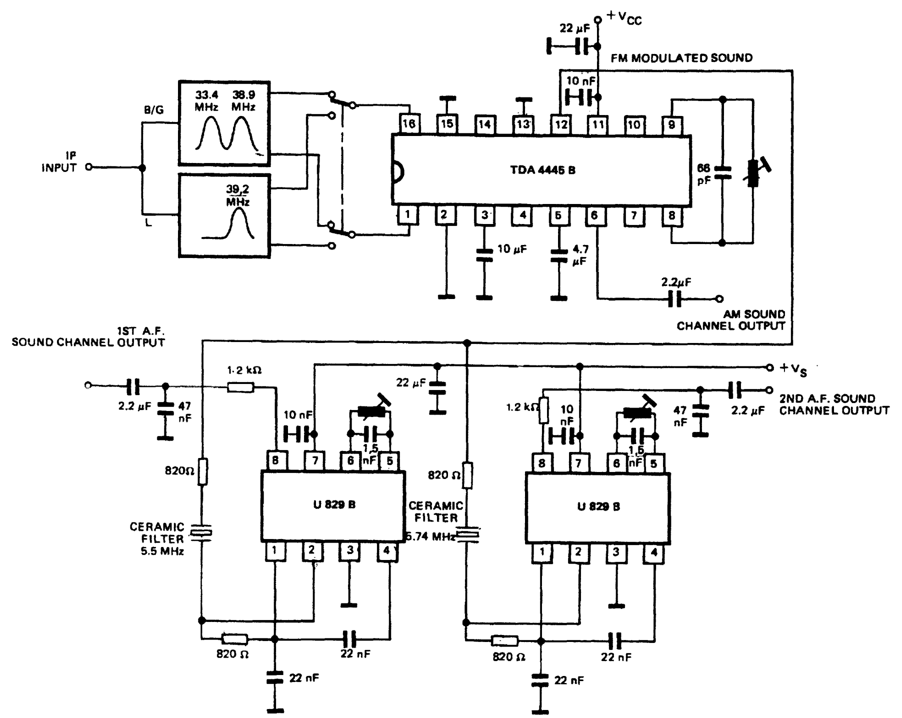
Figure 1 : Quasi Parallel Sound Operation.



E88TDA4445A–04

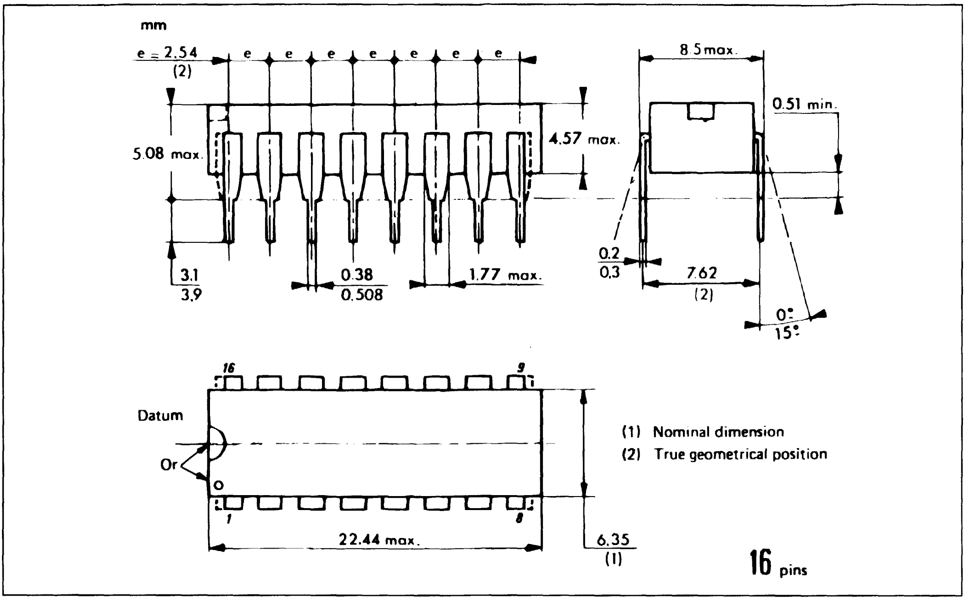
TYPICAL APPLICATION

Figure 2 : Bistandard Operation (FM stereo sound + AM sound).



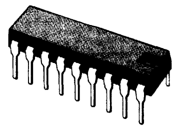
PACKAGE MECHANICAL DATA

16 PINS–PLASTIC DIP

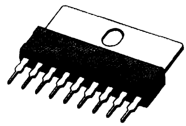


SWITCH-MODE POWER SUPPLY CONTROLLER

- LOW START-UP CURRENT
- DIRECT CONTROL OF SWITCHING TRANSISTOR
- COLLECTOR CURRENT PROPORTIONAL TO BASE-CURRENT INPUT
- REVERSE-GOING LINEAR OVERLOAD CHARACTERISTIC CURVE



DIP 9+9



SIP-9

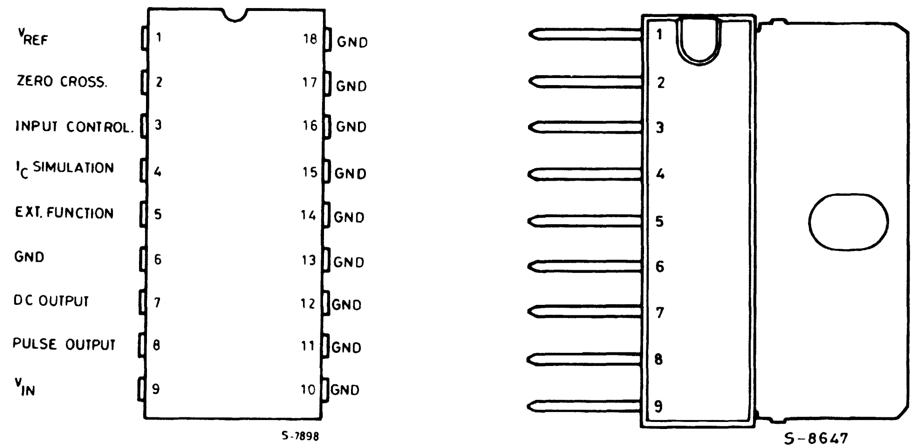
ORDER CODES : TDA4601 (SIP9)
TDA4601B (DIP 9+9)

DESCRIPTION

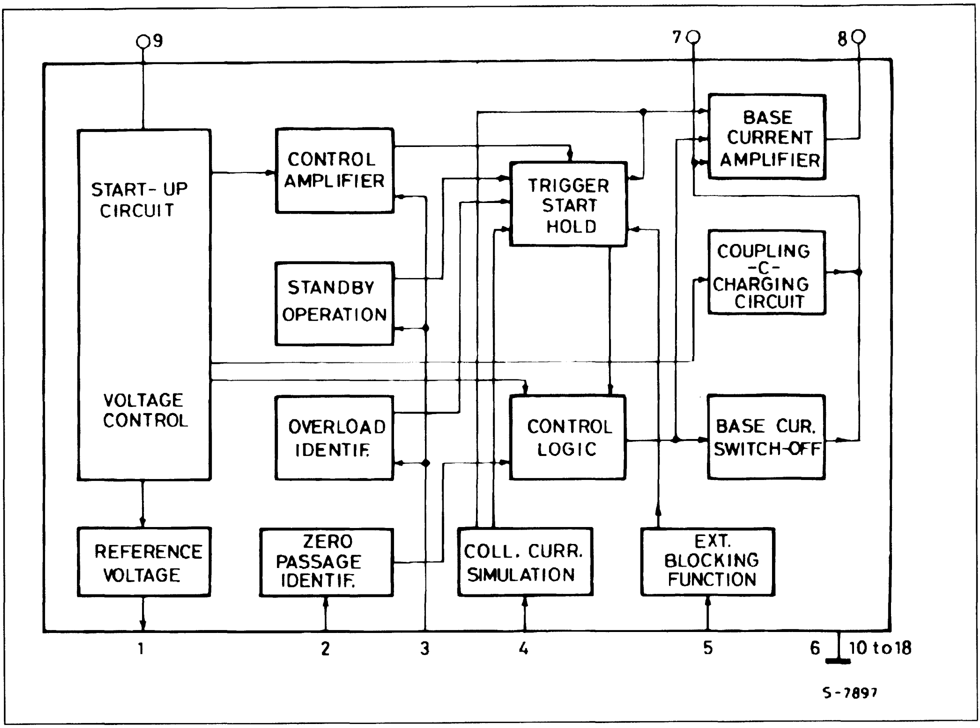
The TDA4601 is a monolithic integrated circuit designed to regulate and control the switching transistor a switching power supply.

Because of its wide operational range and high voltage stability even at high load changes : this IC can be used not only in TV receivers and video recorders but also in power supplies in Hi-Fi sets and active speakers.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Supply Voltage	20	V
V_1	Reference Output	6	V
V_2	Identification Input	– 0.6 to 0.6	V
V_3	Controlled Amplifier	3	V
V_4, V_5		8	V
V_7, V_8		V_9	
I_2, I_3		– 3 to 3	mA
I_4		5	mA
I_5		5	mA
I_7		1.5	A
I_8		– 1.5	A
T_{amb}	Operating Ambient Temperature	0 to 85	°C
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	– 40 to 125	°C
T_{amb}	Ambient Temperature	0 to 85	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction–ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_9	Operating Supply Voltage Range		7.8		18	V

START CONDITION (according to test circuit of fig. 1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_9	Supply Current (V_1 not yet switched on)	 V_9 = 2 V V_9 = 5 V V_9 = 10 V		 1.5 2.4	 0.5 2.0 3.2	 mA mA mA
V_9	Switch Threshold (V_1)		11	11.8	12.3	V

NORMAL OPERATION (V_9 = 10 V, V_{cont} = – 10 V, V_{clock} = ± 0.5 V, f = 20 KHz, duty cycle 1:2 after switch on)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_9	Supply Current	V_{cont} = – 10 V V_{cont} = 0 V	110 50	135 75	160 100	mA mA
V_{ref}	Voltage Reference at Pin 1	I_1 < 0.1 mA I_1 = 5 mA	4 4	4.2 4.2	4.5 4.4	V V
V_3	Control Voltage	V_{cont} = 0 V	2.3	2.6	2.9	V
V_4	Collector Current Simulation Voltage	V_{cont} = 0 V	1.8	2.2	2.5	V
ΔV_4	Collector Current Simulation Voltage	V_{cont} = 0 V to – 10 V	0.3	0.4	0.5	V
V_5	External Protection Threshold		6	7	8	V
V_7	Pin 7 Output Voltage	V_{cont} = 0 V	2.7	3.3	4.0	V
V_8	Pin 8 output Voltage	V_{cont} = 0 V	2.7	3.4	4.0	V
ΔV_8	Pin 8 Output Voltage Change	V_{cont} 0 V to – 10 V	1.6	2	2.4	V
V_2	Feedback Voltage			0.2		V
T_{K1}	Reference Voltage Temperature Coeffic.			10^{-3}		1/K

PROTECTION OPERATION (V_9 = 10 V ; V_{cont} = – 10 V ; V_{clock} = ± 0.5 V ; f = 20 KHz ; duty cycle 1 : 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_9	Supply Current	$V_5 \leq 1.8$ V	14	22	28	mA
V_7	Switch–off Voltage	$V_5 \leq 1.8$ V	1.3	1.5	1.8	V
V_4			1.8	2.1	2.5	V

ELECTRICAL CHARACTERISTICS (continued)

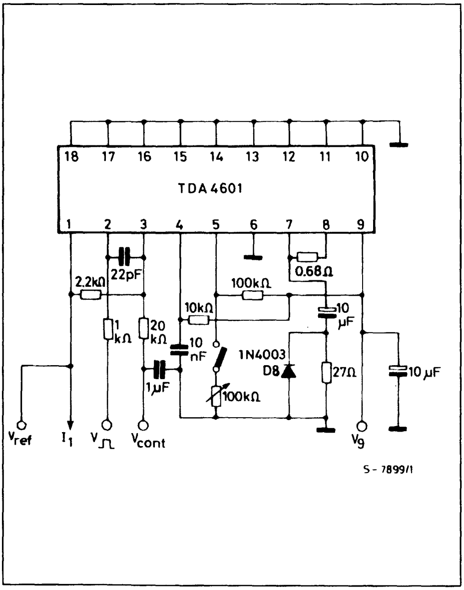
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5		$V_{cont} = 0$ V	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
V_9	Supply Voltage for V_8 Blocked	$V_{cont} = 0$ V	6.7	7.4	7.8	V
ΔV_9	Supply Voltage for V_1 off While Further Decreasing V_9		0.3	0.6	1	V

ELECTRICAL CHARACTERISTICS (according to test circuit of fig. 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Secondary Voltage Switching Time			350	450	ms
ΔV_2	Voltage Variation with Load	S_3 Closed $P_3 = 20$ W		0.1	0.5	V
		S_2 Closed $P_2 = 15$ W		0.5	1	V
ΔV_2	Stand by Condition	S_1 Open $P_{load} = 3$ W		20	30	V
f	Stand by Frequency		70	75		KHz
P_P	Primary Power Consumption in Stand by Condition			10	12	VA

Note : 1) Only DC component.

Figure 1 : Test Circuit.



Test Diagram : Overload Operation.

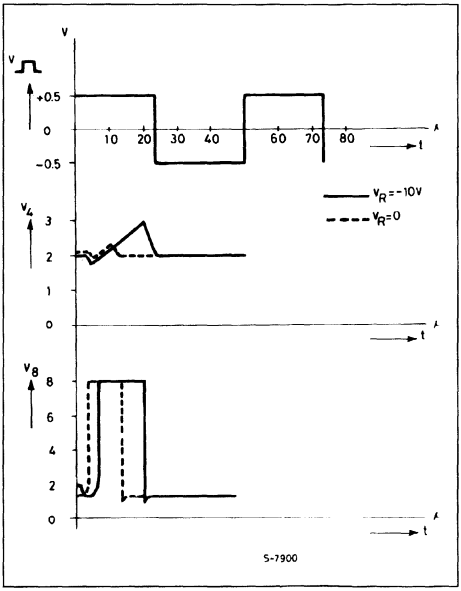
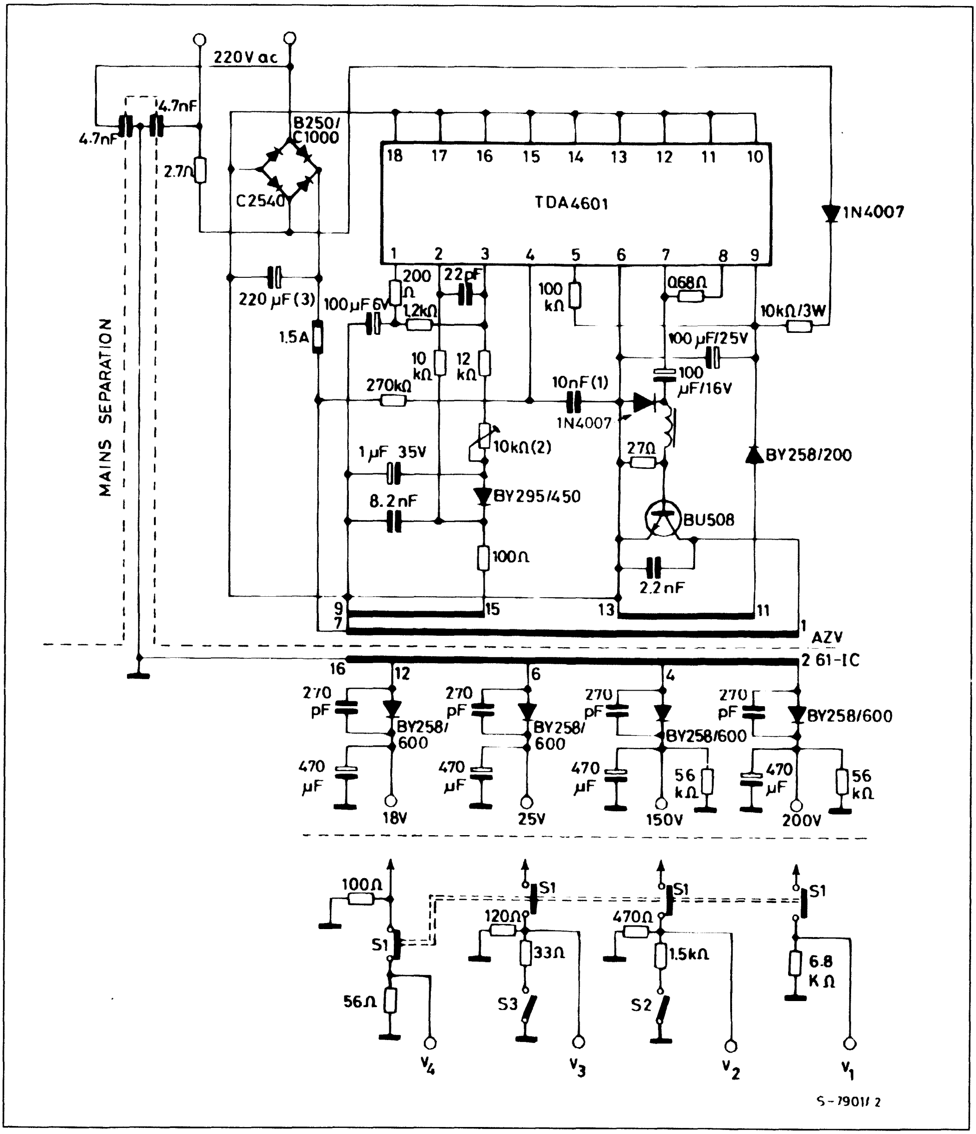


Figure 2 : Test and Application Circuit.



(1) C limits the max. collector current of BU508 at overshooting the permissible output power.
(2) Adjustement of secondary voltage.
(3) Must be discharged before IC change.

CIRCUIT DESCRIPTION

The TDA 4601 regulates, controls, and protects the switching transistor in reverse converter power supplies at starting, normal, and overload operation.

STARTING BEHAVIOUR

During the start-up three consecutive operation states are passed.

1. An internal reference voltage is built up which supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. Up to a supply voltage of $V_9 \approx 12$ V, the current I_9 is less than 3.2 mA.
2. Release of the internal reference voltage $V_1 = 4$ V. This voltage is abruptly available when $V_9 \approx 12$ V and enables all parts of the IC to be supplied from the control logic with a thermally stable and overload protected current supply.
3. Release of control logic. As soon as the reference voltage is available, the control logic is switched on through an additional stabilization circuit. Thus, the IC is ready for operation.

This start-up sequence is necessary to guarantee the supply through the coupling electrolytic capacitor to the switching transistor. Correct switching of the transistor is only in this way guaranted.

NORMAL OPERATION

Zero crossing of the feedback coil is registered at pin 2 and passed to the control logic.

At pin 3 (regulation of input, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating amplifier works with an input voltage of about 2 V and a current of about 1.4 mA.

Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 an internally set voltage level. By increasing the capacitance (10 nF) the max. collector current of the switching transistor rises, thus setting the required operating range. The extent of the regulation lies between a 2 V clamped DC voltage and an AC voltage rising in a sawtooth waveform, which may vary up to a maximum amplitude of 4 V (ref. voltage).

A reduction of the secondary load down to 20 watts causes the switching frequency to rise to about 50 KHz at an almost constant pulse duty factor (period to on-time approx. 3). A further reduction of the secondary load down to about 1 watt results in changing the switching frequency to approx. 70 KHz, and additionally the pulse duty factor rises to approx. 11. At the same time the collector peak current falls below 1 A.

In the trigger the output level of the regulating amplifier, the overload recognition, and the collector current simulation are compared and instructions are given to the control logic. There is an additional triggering and blocking possibility by means of pin 5. The output at pin 8 is blocked at a voltage of less than 2.2 V at pin 5.

Depending on the start-up circuit, the zero crossing identification, and the release with the aid of the trigger, the control logic flip flops are set which control the base current amplifier and the base current shutdown. The base current amplifier moves the sawtooth voltage V_4 to pin 8. A current feed-back having an external resistance of $R = 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determined the maximum amplitude of the base driving current for the switching transistor.

PROTECTIVE MEASURES

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks driving of the switching transistor. This protective measure will be released if the voltage at pin 9 reaches a value $\leq$ typ. 7.4 V or if voltages of $\leq$ typ. 2.2 V occur at pin 5. In the case of a short circuit of the secondary windings of the P.S.U., the IC continuously monitors the fault condition.

With the load completely removed from the secondary winding of the P.S.U., the IC is set to a low pulse duty factor. The total power consumption of the P.S.U. is held below 6 to 10 watts in both operating conditions. After having blocked the output, caused at a supply voltage $\leq$ typ. 7.4 V, a further voltage reduction with $\Delta V_9 = 0.6$ V results in switching off the reference voltage (4 V).

Figure 3 : Frequency vs. Output Power (test circuit of fig. 2).

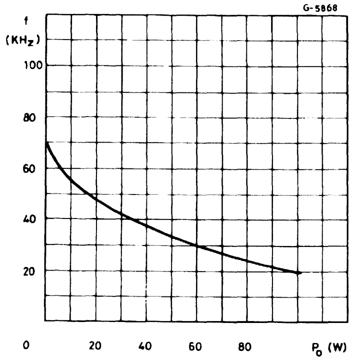


Figure 4 : Efficiency vs. Output Power Test Circuit (of fig. 2).

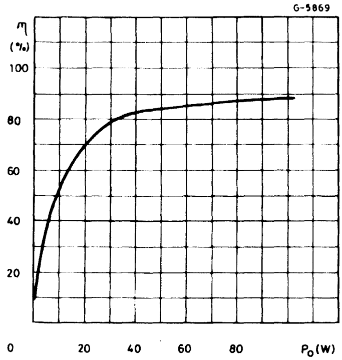


Figure 5 : Load Characteristics V_2-f (Iq2) (test circuit of fig. 2).

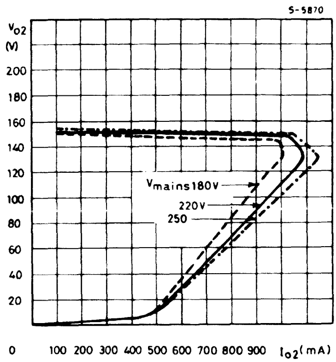


Figure 6 : Output Voltage V_2 (mains change) (test circuit of fig. 2).

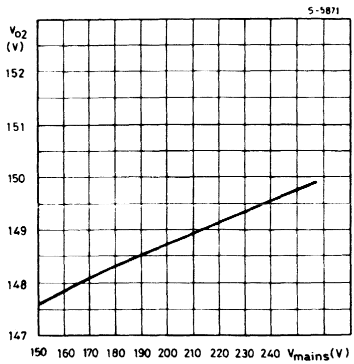
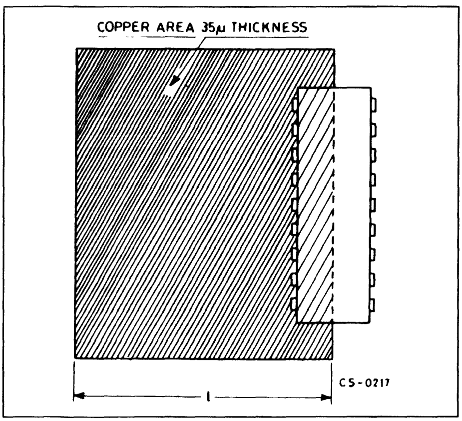
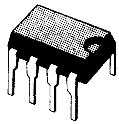


Figure 7 : Example of a PC Heatsink (35 °C/W).



TV EAST/WEST CORRECTION CIRCUIT

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT
- EXTERNAL KEYSTONE ADJUSTMENT (symmetry of the parabola)
- INPUT FOR DYNAMIC FIELD CORRECTION (beam current change)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY REDELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAWTOOTH



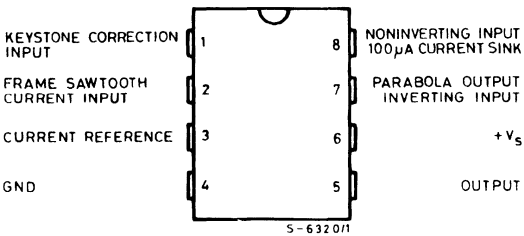
MINIDIP

ORDER CODE : TDA4950

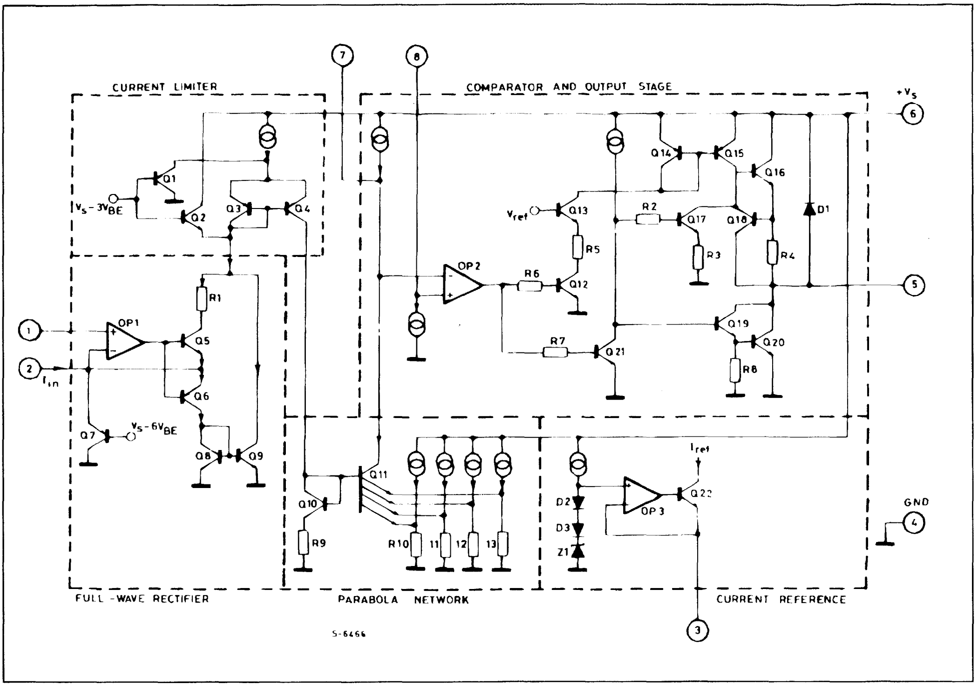
DESCRIPTION

The TDA4950 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

CONNECTION DIAGRAM (top view)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
I_S	Supply Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 70 °C	800	mW
T_{stg}, T_j	Storage and Junction Temperature	– 25 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pin 4	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_S = 24 V, V_{fr} = 0, S1 and S2 in "a" position, refer to test circuit unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		17	24	30	V
I_S	Supply Current			4.5	7	mA
V_{ref}	Internal Reference Voltage		7.6	8.0	8.8	V
$-I_{ref}$	Internal Reference Current	$V_{ref}/R3$		0.73		mA
$V_{7(A)}$ (*)	Pin 7 Output Voltage	$I_{fr} = 0\ \mu A$	15.3	16.0	16.7	V
$V_{7(B)}$ (*)	Pin 7 Output Voltage	$I_{fr} = 30\ \mu A$		15		V
K1	Parabola Coefficient (*)	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$		0.28		
K_2	Parabola Coefficient (*)	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$		0.71		
ΔV_7 (*)		$\Delta V_7 = V_{7E} - V_{7F}$	– 40		40	mV
I_8	Current Source	S1 → b		100		µA
V_{SATL}	Saturation Voltage	Io = 400 mA Sink S2 → b		1	2	V
V_{SATH}	Saturation Voltage	Io = 100 mA Source S1 → b S2 → c		0.8	1.5	V
V_F	Forward Voltage	I_o = 400 mA S2 → d S1 → b		1.2	1.7	V
I_{fr}	Frame Sawtooth Current	$V_{fr} = 6.6\ V_{PP}$		6.6		µA

(*) See figure 2.

Figure 1 : Test Circuit.

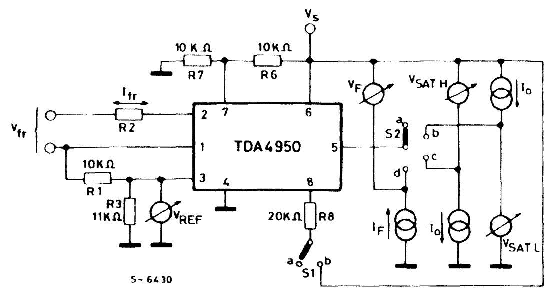
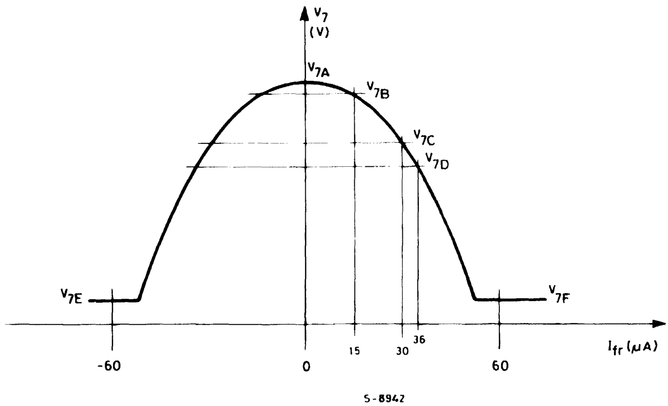


Figure 2 : Parabola Characteristics.



CIRCUIT OPERATION (see the schematic diagram)

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of ± 33 µA which is produced via an external resistor from the sawtooth voltage. The non-inverting input of this amplifier is connected with a reference voltage corresponding to the DC level of the sawtooth voltage. This DC voltage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current. This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

If the input is overmodulated (> 40 µA) the internal current is limited to 40 µA. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

The horizontal frequency pulse-width modulated output signal drives the final stage. It consists of a class D push-pull output amplifier that drives, via an external inductor, the diode modulator.

Figure 3 : Application Circuit with Keystone Correction.

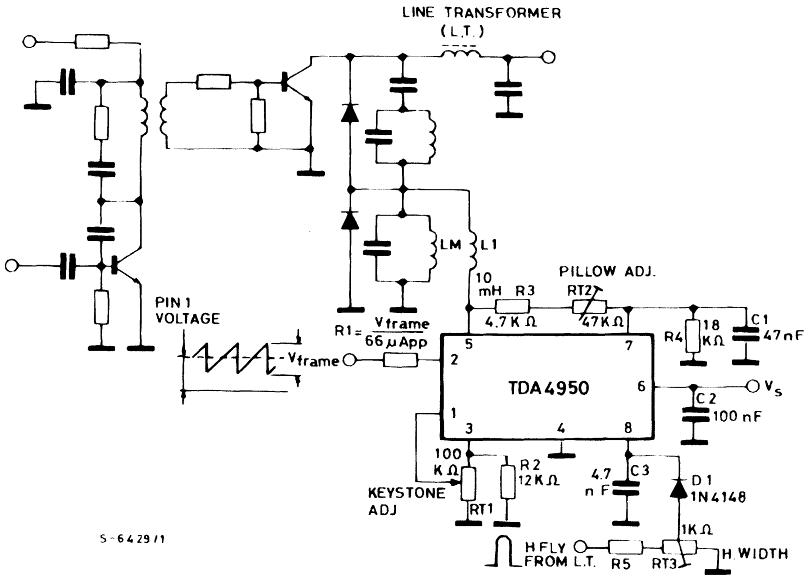
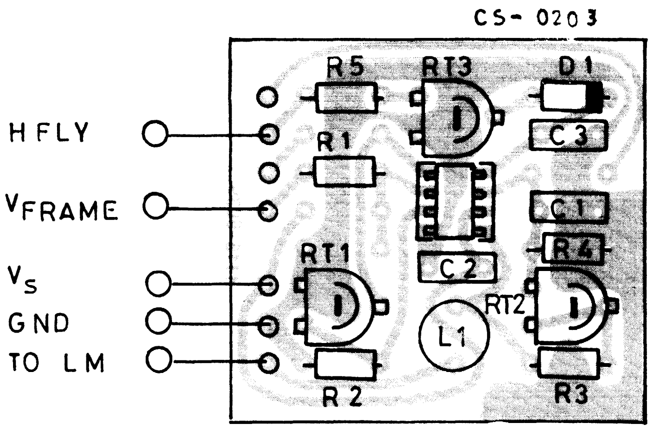
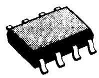


Figure 4 : P.C. Board and component Layout of the circuit of Figure 3 (1 : 1 scale).

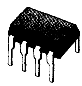


1W AUDIO AMPLIFIER WITH MUTE

- OPERATING VOLTAGE 1.8 TO 15 V
- EXTERNAL MUTE OR POWER DOWN FUNCTION
- IMPROVED SUPPLY VOLTAGE REJECTION
- LOW QUIESCENT CURRENT
- HIGH POWER CAPABILITY
- LOW CROSSOVER DISTORTION



SO – 8J



MINIDIP
(Plastic)

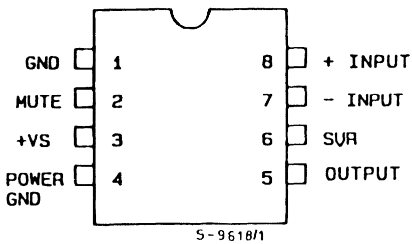
ORDER CODE : TDA7233 (Minidip)
TDA7233D (SO – 8)

DESCRIPTION

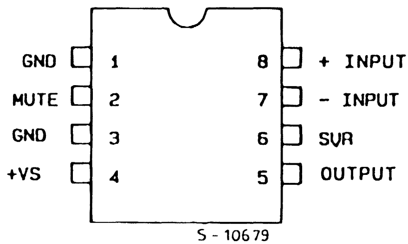
The TDA7233 is a monolithic integrated circuit in 8 pin Minidip or SO–8 package, intended for use as class AB power amplifier with a wide range of supply voltage from 1.8V to 15V in portable radios, cassette recorders and players.

PIN CONNECTIONS (top views)

MINIDIP



SO-8



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V
I_o	Output Peak Current	1	A
P_{tot}	Total Power Dissipation at T_{amb} = 50 °C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

			SO-8	Minidip
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	200 °C/W	100 °C/W

ELECTRICAL CHARACTERISTICS (V_s = 6 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		1.8		15	V
V_o	Quiescent Out Voltage			2.7		V
		V_s = 3 V V_s = 9 V		1.2 4.2		V V
I_d	Quiescent Drain Current	MUTE HIGH		3.6	9	mA
		MUTE LOW		0.4		
I_b	Input Bias Current			100		nA
P_o	Output Power	d = 10 % f = 1 KHz V_s = 12 V R_L = 8 Ω V_s = 9 V R_L = 4 Ω V_s = 9 V R_L = 8 Ω V_s = 6 V R_L = 8 Ω V_s = 6 V R_L = 4 Ω V_s = 3 V R_L = 4 Ω V_s = 3 V R_L = 8 Ω		 1.9 1.6 1 0.4 0.7 110 70		 W W W W W mW mW
d	Distortion	P_o = 0.5 W R_L = 8 Ω f = 1 kHz V_s = 9 V		0.3		%
G_v	Closed Loop Voltage Gain	f = 1 kHz		39		dB
R_{IN}	Input Resistance	f = 1 kHz	100			KΩ
e_N	Total Input Noise (R_s = 10 kΩ)	B = Curve A		2		µV
		B = 22 Hz to 22 kHz		3		
SVR	Supply Voltage Rejection	f = 100 Hz, R_g = 10 KΩ		45		dB
	MUTE Attenuation	V_o = 1 V f = 100 Hz to 10 kHz		70		dB
	MUTE Threshold			0.6		V
I_M	MUTE Current			0.4		mA

Figure 1 : Test and Application Circuit.

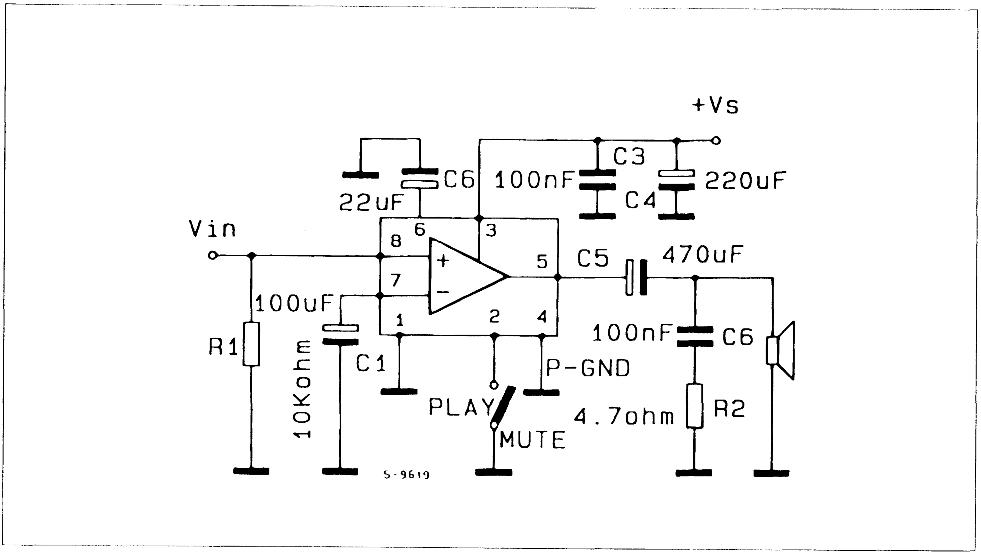


Figure 2 : Output Power vs Supply voltage.

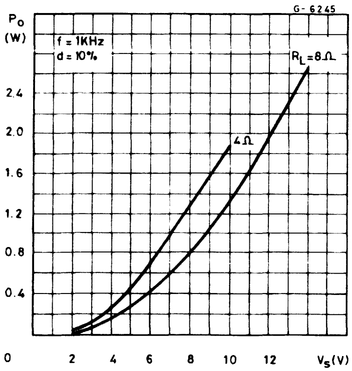


Figure 3 : Supply Voltage Rejection vs. Frequency.

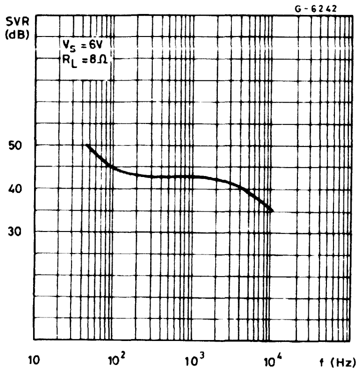


Figure 4 : DC Output Voltage vs Supply voltage.

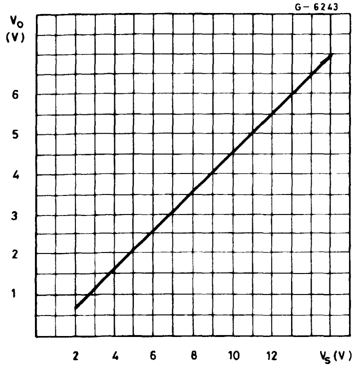


Figure 5 : Quiescent Current vs. Supply voltage.

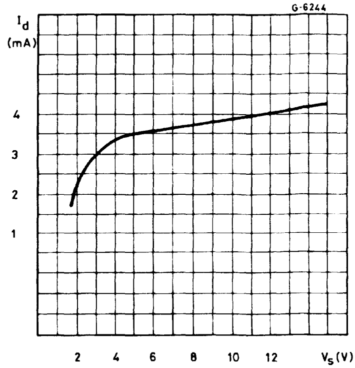
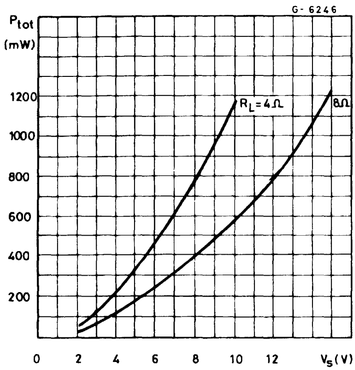


Figure 6 : Total dissipated Power vs. Supply voltage.



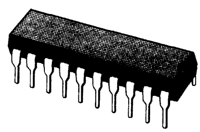
SGS-THOMSON
MICROELECTRONICS

TDA7250

60 W HI-FI DUAL AUDIO DRIVER

ADVANCE DATA

- WIDE SUPPLY VOLTAGE RANGE : 20 TO 90 V (± 10 to ± 45 V)
- VERY LOW DISTORTION
- AUTOMATIC QUIESCENT CURRENT CONTROL FOR THE POWER TRANSISTORS WITHOUT TEMPERATURE SENSE ELEMENTS
- OVERLOAD CURRENT PROTECTION FOR THE POWER TRANSISTORS
- MUTE/STAND-BY FUNCTIONS
- LOW POWER CONSUMPTION
- OUTPUT POWER 60 W/8 Ω AND 100 W/4 Ω



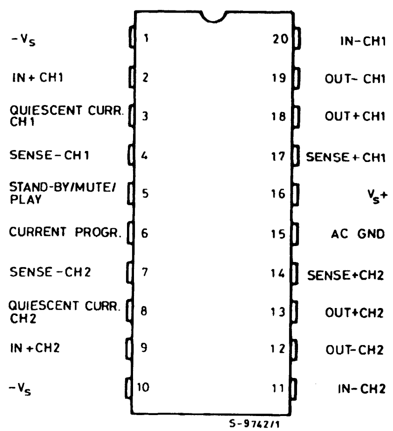
DIP-20
(Plastic 0.4)

ORDER CODE : TDA7250

DESCRIPTION

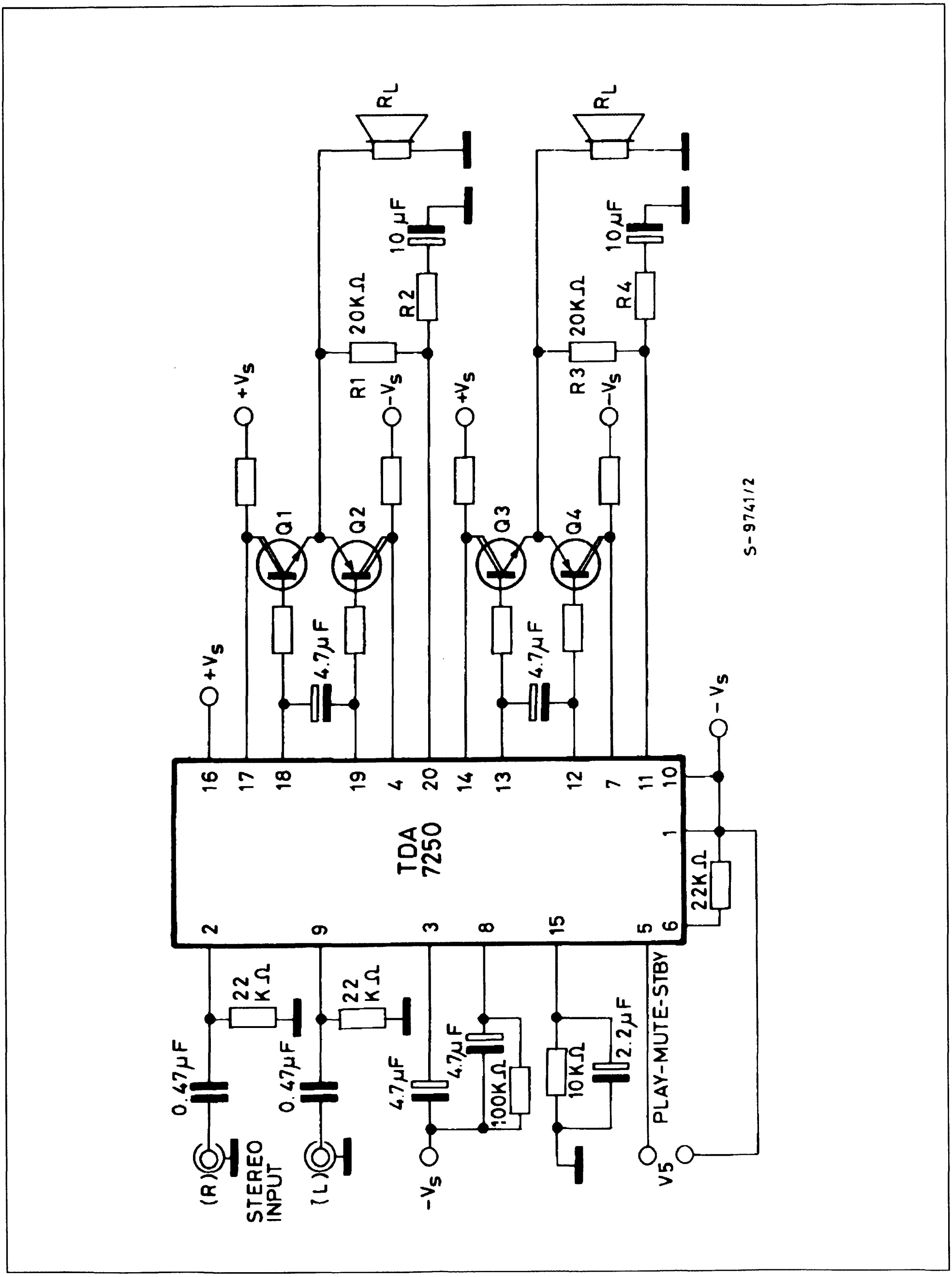
The TDA7250 stereo audio driver is designed to drive two pair of complementary output transistor in the Hi-Fi power amplifiers.

CONNECTION DIAGRAM (top view)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	100	V
P_{tot}	Power Dissipation at T_{amb} = 60 °C	1.4	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to + 150	°C

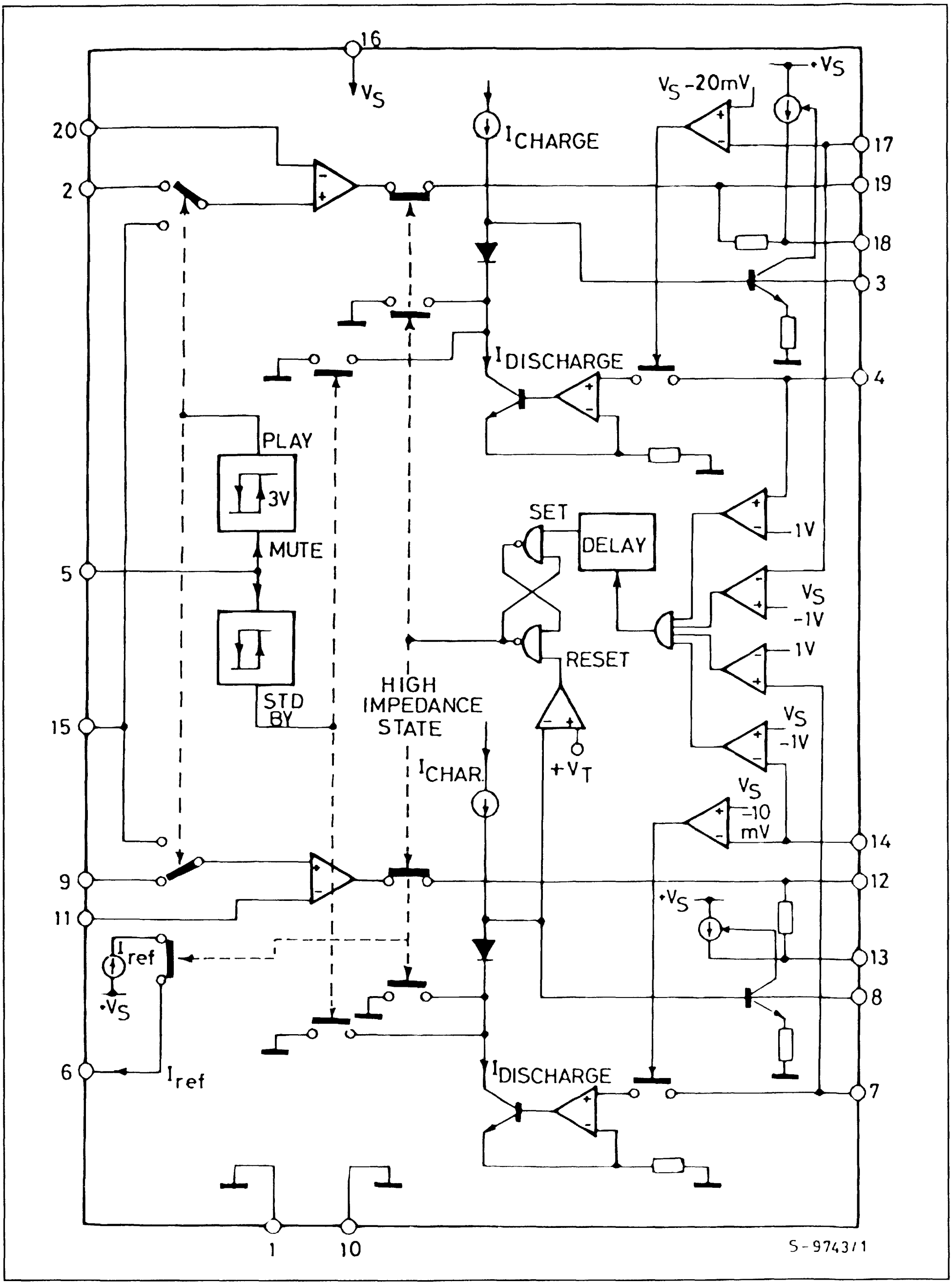
THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	65	°C/W

PIN FUNCTIONS

N°	NAME	FUNCTION
1	V_S – POWER SUPPLY	Negative Supply Voltage.
2	NON–INV. INP. CH. 1	Channel 1 Input Signal.
3	QUIESC. CURRENT CONTR. CAP. CH1	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 1.
4	SENSE (–) CH. 1	Negative voltage sense input for overload protection and for automatic quiescent current control.
5	ST. BY / MUTE / PLAY	Three-functions Terminal. For V_{IN} = 1 to 3 V, the device is in MUTE and only quiescent current flows in the power stages ; - for V_{IN} < 1 V, the device is in STAND-BY mode and no quiescent current is present in the power stages ; - for V_{IN} > 3 V, the device is fully active.
6	CURRENT PROGRAM	High Impedance Power-stages Monitor.
7	SENSE (–) CH. 2	Negative Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
8	QUIESC. CURRENT CONTR. CAP. CH. 2	This capacitor works as an integrator, to control the quiescent current to output devices in no-signal conditions on channel 2. If the voltage at its terminals drops under 250 mV, it also resets the device from high-impedance state of output stages.
9	NON–INV. INP. CH. 2	Channel 2 Input Signals.
10	V_s – POWER SUPPLY	Negative Supply Voltage.
11	INVERT. INP. CH. 2	Feedback from Output (channel 2).
12	OUT (–) CH. 2	Out Signal to Lower Driver Transistor of Channel 2.
13	OUT (+) CH. 2	Out Signal to Higher Driver Transistor of Channel 2.
14	SENSE (+) CH. 2	Positive Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
15	COMMON AC GROUND	AC Input Ground in MUTE Condition.
16	V_S + POWER SUPPLY	Positive Supply Voltage.
17	SENSE (+) CH. 1	Positive Voltage Sense Input for Overload Protection and for Automatic Quiescent Current Control.
18	OUT (+) CH. 1	Out Signal to High Driver Transistor of Channel 1.
19	OUT (–) CH. 1	Out Signal to Low Driver Transistor of Channel 1.
20	INVERT. INP. CH. 1	Feedback from Output (channel 1).

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = ± 35 V, play mode, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			± 10		± 45	V
I_d	Quiescent Drain Current	Stand-by Mode			8		mA
		Play Mode			10	14	mA
I_b	Input Bias Current				0.2	1	µA
V_{os}	Input Offset Voltage				1	± 10	mV
I_{os}	Input Offset Current				100	200	nA
G_v	Open Loop Voltage Gain	f = 100 Hz			90		dB
		f = 10 kHz			60		dB
e_N	Input Noise Voltage	R_G = 600 Ω B = 20 Hz to 20 kHz			3		µV
SR	Slew Rate				10		V/µs
d	Total Harmonic Distortion	G_v = 26 dB P_o = 40 W	f = 1 kHz		0.004		%
			f = 20 kHz		0.03		%
V_{opp}	Output Voltage Swing				60		V_{pp}
P_o	Output Power (*)	V_s = ± 35 V V_s = ± 30 V V_s = ± 35 V	R_L = 8 Ω R_L = 8 Ω R_L = 4 Ω		60 40 100		W
I_o	Output Current				± 5		mA
SVR	Supply Voltage Rejection	f = 100 Hz			75		dB
C_s	Channel Separation	f = 1 kHz			75		dB

MUTE / STANDBY/ PLAY FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_i	Input Current (pin 5)			0.1		µA
V_{th}	Comparator Standby / Mute Threshold (**)		1.0	1.25	1.5	V
H	Hysteresis Standby / Mute			200		mV
V_{th}	Comparator Mute / Play Threshold (**)		2.4	3.0	3.6	V
H	Hysteresis Mute / Play			300		mV
	Mute Attenuation	f = 1 kHz		60		dB
V_i	Input Voltage Max. (pin 5)		12 (**)			V

(*) Application circuit of fig. 1 f = 1 KHz ; d = 0.1 % ; G_v =26 dB.
(**) Referred to – V_s.

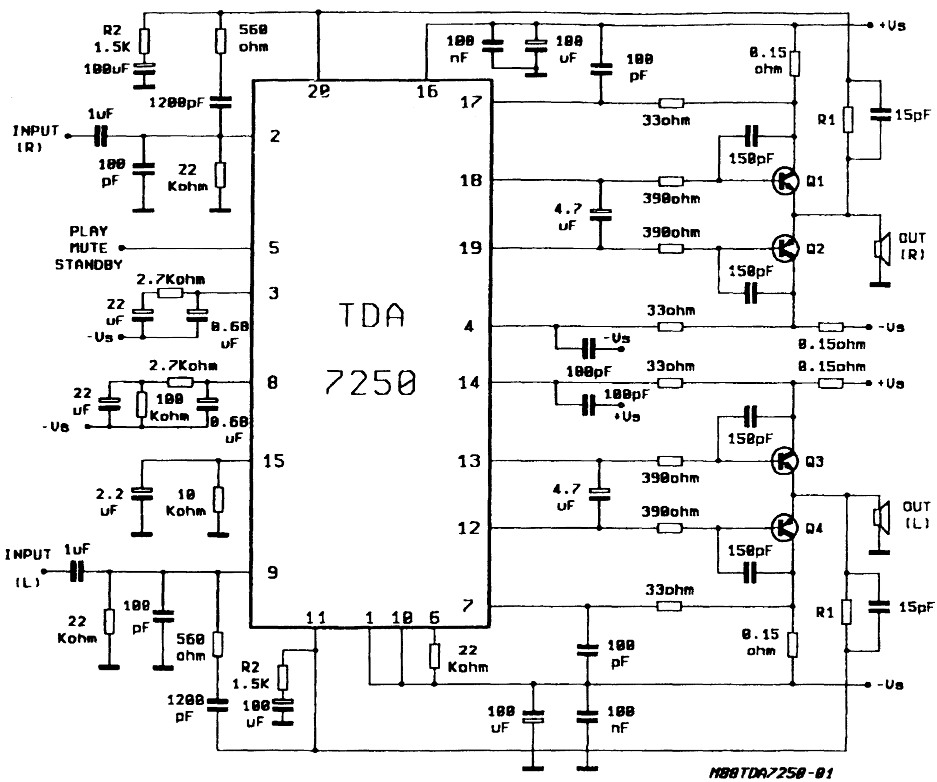
CURRENT SURVEY CIRCUITRY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Comparator Reference	to + V_S to – V_S	0.8 0.8	1 1	1.4 1.4	V V
t_d	Delay Time		10			µs

QUIESCENT CURRENT CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Capacitor Current	Charge Discharge	30 250	60 500		µA µA
	Comparator Reference	to + V_S to – V_S	10	20 10	25	mV mV

Figure 1 : Application Circuit with Power Darlingtons.



Note : Q1/Q2 = Q3/Q4 = TIP 142/TIP147
GV = 1 + R1/R2

Figure 2 : Output Power vs. Supply Voltage.

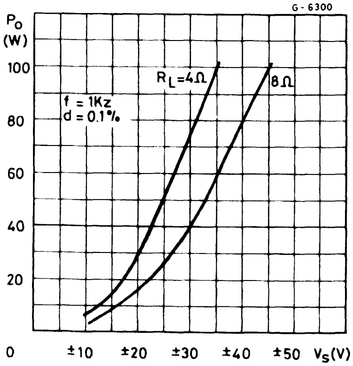


Figure 3 : Distortion vs.Output Power (*).

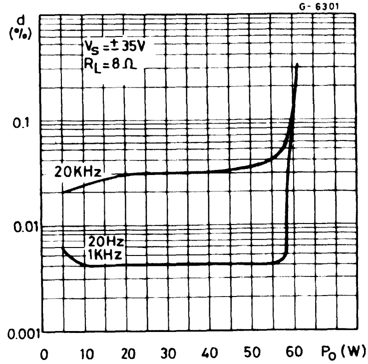


Figure 4 : Channel Separation.

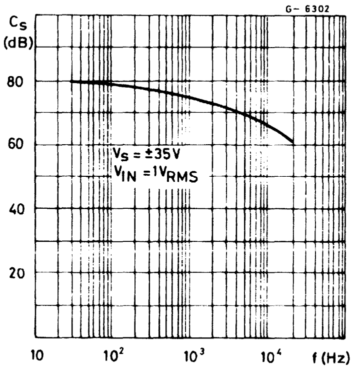


Figure 5 : Supply Voltage Rejection vs. Frequency.

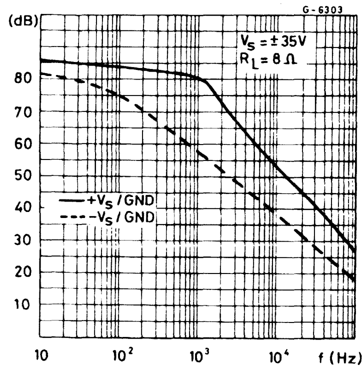


Figure 6 : Quiescent Current vs. Supply Voltage.

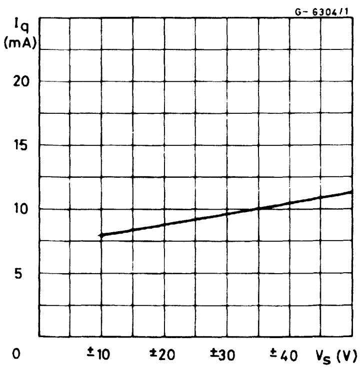


Figure 7 : Quiescent Current vs. T_{amb}.

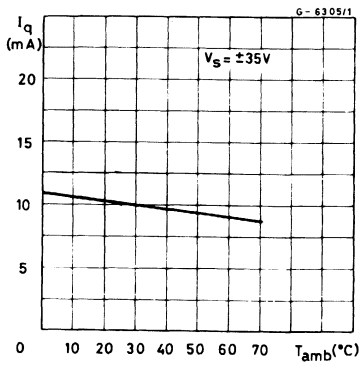


Figure 8 : Total Dissipated Power vs. Output Powe r (*).

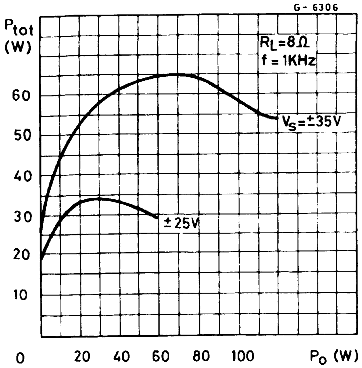


Figure 9 : Efficiency vs. Output Power (*).

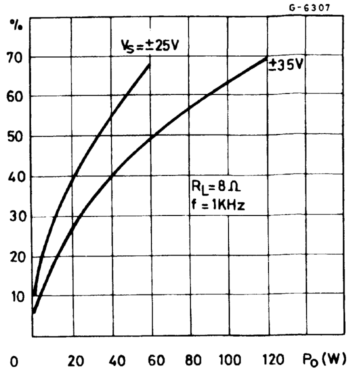


Figure 10 : Play-mute Standby Operation.

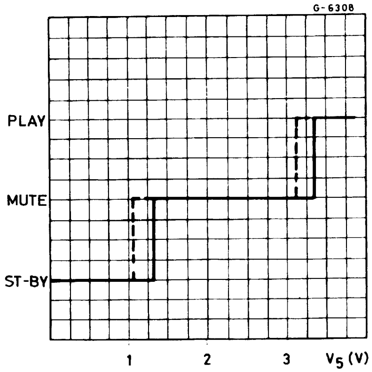


Figure 11 : Application Circuit Using Power Transistors.

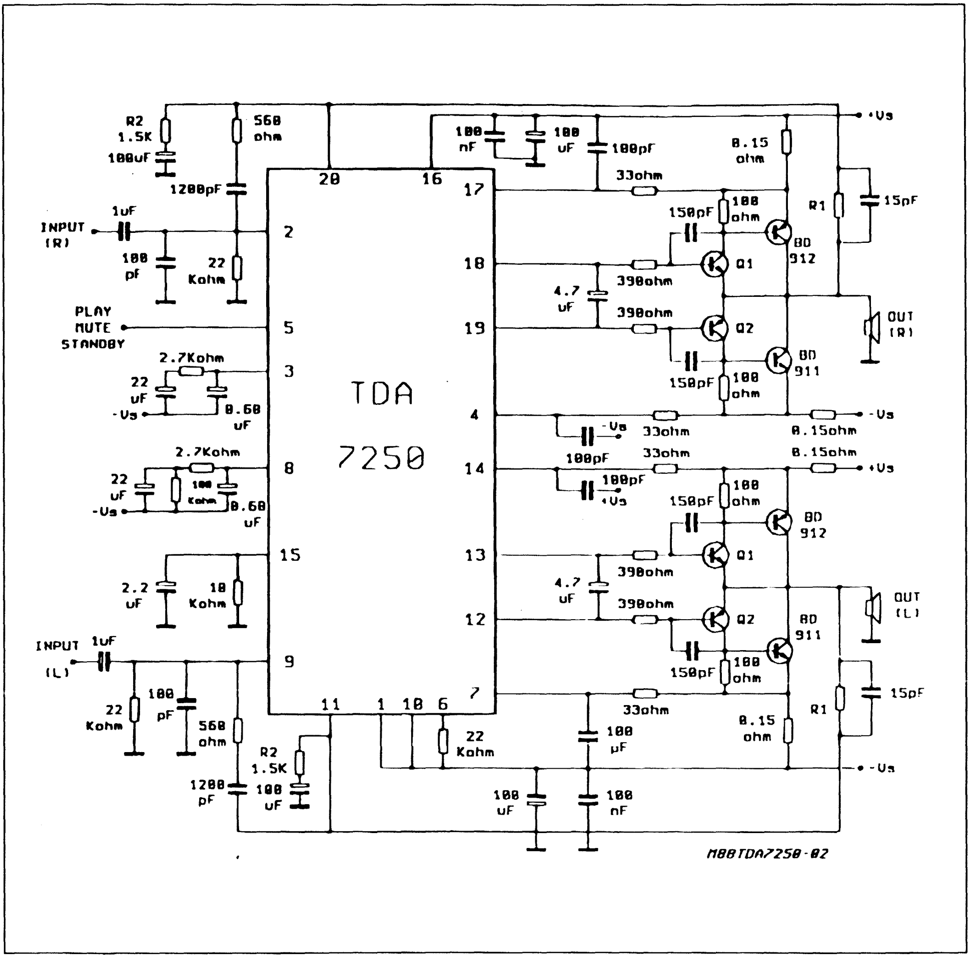


Figure 12 : Suggested Transistor Types for Various Loads and Powers.

$R_L = 8\ \Omega$

15W	30W	50W	70W
BDX 53/54A	BDX 53/54B	BDW 93/94B	TIP 142/147

$R_L = 4\ \Omega$

30W	50W	90W	130W
BDW 93/94A	BDW 93/94B	BDV 64/65B	MJ 11013/11014

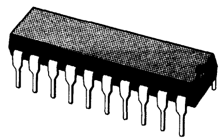
SGS-THOMSON MICROELECTRONICS

TDA8114

VCR PROCESSOR INTERFACE CIRCUIT

ADVANCE DATA

- CAPSTAN TACHO AMPLIFIER WITH OC OUTPUT
- CTL-PLAYBACK AMPLIFIER WITH OC OUTPUT
- CTL-RECORD AMPLIFIER WITH OC INPUT
- REEL TACHO AMPLIFIER WITH OC OUTPUT
- DRUM POSITION DETECTOR WITH OC OUTPUT + INTERNAL PULL UP RESISTOR
- RESET GENERATOR



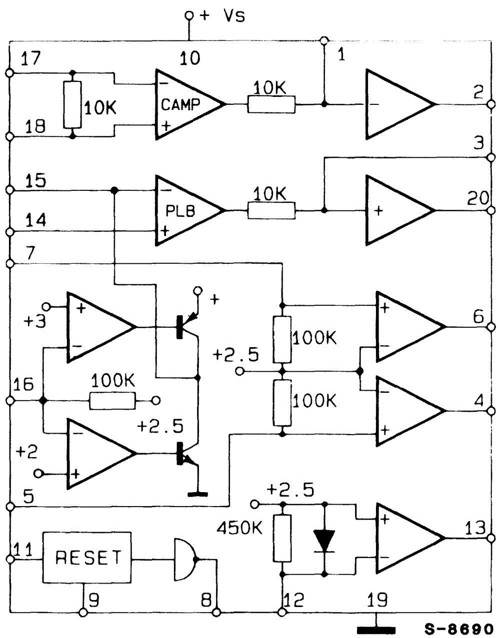
DIP20

ORDER CODE : TDA8114

DESCRIPTION

The TDA 8114 is a monolithic integrated circuit for VCR-applications. It is intended to convert signals from optical and magnetical sensors to µP TTL-level. A special circuit includes a supply voltage supervisor and generates a reset signal for µ-Processor.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	10	V
V_i	DC Input Voltage	7	V
V_O	Open Collector Output Voltage (all outputs high)	15	V
T_{op}	Operating Junction Temperature	0 to 85	°C
T_{stg}	Storage Temperature	– 55 to 125	°C

THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

PIN NAMES

N°	Name
1	Capstan Tacho Amplifier Output and Low Pass Filter
2	Capstan Tacho Amplifier OC Output
3	CTL Amplifier Output and Low Pass Filter
4	Reel Tacho OC Output
5	Reel Tacho Sensor Input
6	Reel Tacho OC Output
7	Reel Tacho Sensor Input
8	Reset Open Collector Output with Internal Pull Up
9	Reset Delay Time Capacitor
10	Supply Voltage
11	Reset Supply Voltage Store
12	Drum Position Sensor Input
13	Drum Position Open Collector Output with Internal Pull-up Resistor
14	CTL Tacho Reference Voltage
15	CTL Tacho Amplifier Input
16	CTL Record Amplifier TTL Input
17	Capstan Tacho Amplifier Input
18	Capstan Tacho Reference Voltage
19	Ground
20	CTL Playback Amplifier OC Output

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified V_S = 5V)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Operation Range	10		4.5		6	V
I_S	Supply Current	10					mA

CAPSTAN TACHO AMPLIFIER

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
R_i	Input Resistance	17			10		KΩ
V_R	Capstan Reference Voltage	18			2.5		V
V_i	AC-tacho Input Voltage	17	f Input 50 to 2500Hz	150			μV_{rms}
R_F	Filter Output Impedance	1			10		KΩ
V_{sat}	Output Saturation Voltage	2	Low State I_T = 1.8mA			0.4	V
V_O	Output Voltage	2	High State I_T = 0mA			15	V
	Negative slope of output signal pin T yields to zero crossing of input signal Input to output phase relation is non invert.						

CTL-PLAYBACK AMPLIFIER

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
R_i	Input Resistance	15		100			KΩ
V_R	CTL-Reference Voltage	14			2.5		V
V_i	Synchronous Peak Input Voltage	15	Pos. plus detected	200			μV
R_F	Filter Output Impedance	3			10		KΩ
V_{sat}	Output Saturation Voltage	20	Low State I_R = 1.8mA			0.4	V
V_O	Output Voltage	20	High State I_R = 0			15	V
	input to output phase relations is invert.						

CTL-RECORD AMPLIFIER

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
R_i	Input Resistance	16	V_i between V_S and GND		100		KΩ
V_R	Input Reference Voltage	16	Pin Open		2.5		V
V_i	Input Threshold for Output High State	16			3		V
V_{IL}	Input Threshold for Output Low State	16			2		V
$V_{sat\ L}$	Ouptut Saturation Voltage Low State	15	V_Q = L (I_{sink} 5mA)			0.4	V
$V_{sat\ H}$	Ouput Saturation Voltage	15	V_Q = H (I_{source} 5mA)			3.5	V
	Input to output phase relation is non invert.						

ELECTRICAL CHARACTERISTICS (continued)

REEL-TACHO AMPLIFIER

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
R_i	Input Resistance	5/14		100			KΩ
V_R	Input Reference Voltage	5/14			2.5		V
V_i	AC-tacho Input Voltage	5/14	f = 1Hz to 5KHz	1			V_{pp}
V_{sat}	Output Saturation Voltage	4/6	Low State $I_{O/P}$ = 1.8mA			0.4	V
V_O	Output Voltage	4/6	High State $I_{O/P}$ = 0			15	V
	Input to output phase relation is no invert.						

DRUM TACHO AMPLIFIER

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
R_i	Input Resistance	12	V_{IN} between 1 and 7V		450		KΩ
V_R	Input Reference Voltage	12			2.5		V
V_{ic}	Input Clamping Voltage	12	Sink Current 100μA		$V_R - 0.6$		V
V_{IP}	Input Peak Voltage	12				8	V
V_{sat}	Ouptut Saturation Voltage	13	Low State I_N = 1.8mA			0.4	V
V_O	Output Voltage	13	High State I_N = 0			15	V
V_i	AC-tacho Input Voltage	12		1			V_{pp}
	Input to output phase relation is non invert.						

RESET GENERATION

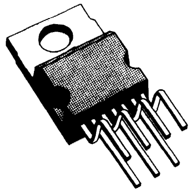
Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Reset Supply Voltage	11			$V_S - 0.6$		V
V_{SR}	Reset Supply Voltage Operation Range	11		3		V_S	V
I_R	Reset Supply Current	11			2		mA
I_C	Charging Current	9			25		μA
I_{DC}	Discharging Current	9	U_K = 2V Discharging current is present for $V_S < V_{sens}$		2.5		mA
V_{sen}	Reset Sense Voltage	10		4.5	4.6	4.7	V
V_{CH}	Comparator High Threshold	9	Output Low to High		2		V
V_{CL}	Comparator Low Threshold Output open Colletor with Intervall Pull up Resistor	9	Output High to Low		3		V
V_{sat}	Output Saturation Voltage	8	Low State I_M = 1.8mA			0.4	V

OPTIONAL OUTPUT (push-pull)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_{sat}	Output Saturation Voltage	8	Low State I_M = 1.8mA			0.4	V
V_{sat}	Output Saturation Voltage	8	High State I_M = 1.8mA	3.5			V

DUAL MOTOR DRIVER

- HIGH OUTPUT CURRENT, EACH CHANNEL UP TO 1 A
- WIDE SUPPLY VOLTAGE RANGE, 4 V UP to 28 V
- SHORT CIRCUIT PROTECTION
- SAFE OPERATING AREA CURRENT LIMITING
- TEMPERATURE SHUT DOWN WITH HYSTERESIS
- HIGH INPUT IMPEDANCE
- GROUND COMPATIBLE INPUT



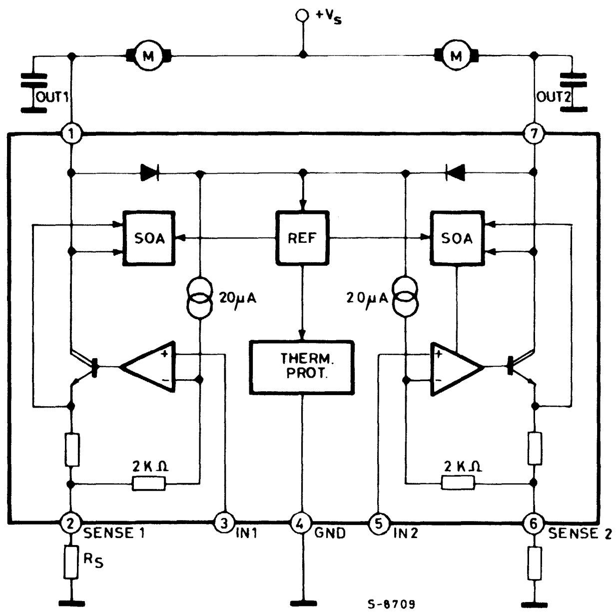
Heptawatt

ORDER CODE : TDA8115

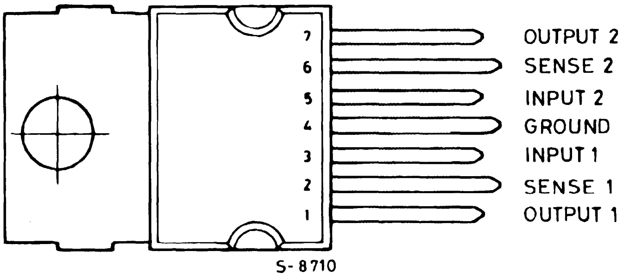
DESCRIPTION

The TDA8115 is a monolithic integrated circuit which realizes two independent programmable current sources. The device is well suited for motor driving applications such as reel motors in video recorders. A wide supply voltage range permits battery operation.

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	28	V
I_O	Output Current (each channel)	Internally Limited	
P_{tot}	Power Dissipation	internally Limited	
T_{op}	Operation Junction Temperature	– 40 to + 150	°C
T_{stg}	Storage Temperature	– 40 to + 150	°C

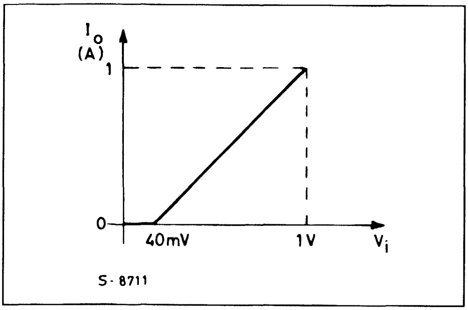
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction–case	Max	3	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

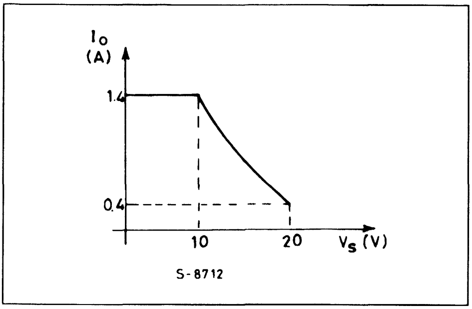
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		4		23	V
I_Q	Quiescent Current			2	5	mA
I_O	Output Current Range				1	A
V_{IR}	Input Voltage Range		0		$V_S - 3$	V
V_{OS}	Positive Input Offset for Current Starting Point		50	60	80	mV
	Thermal Shut Down			150		°C
	Hysteresis			20		°C
I_L	Output Current Limit V_S = 10 V V_S = 20 V			 1.4 0.4		 A A
I_b	Input Bias Current				1	µA
V_{sat}	Saturation Voltage	I_{OUT} = 0.9 A		1.4	2	V
R_B	Bond Resistance			60		mΩ

Figure 1 : Transconductance Characteristic.



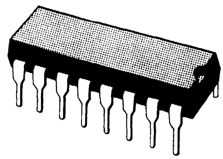
with $I_O = \dfrac{V_{IN} - 40mV}{(R_S + 60m\Omega)}$

Figure 2 : Max Output Current vs. Supply Voltage (SOA).



VIDEO HEAD SERVO CONTROLLER

- WIDE OPERATING VOLTAGE RANGE 6V to 14V
- HIGH CURRENT CAPABILITY UP TO 1A
- OUTPUT DC CURRENTS UP TO 0.4A
- TWO LOGICAL INPUTS FOR THE CODED COMMUNICATION SIGNAL
- LIMITED SLEW RATE OF THE OUTPUT VOLTAGE
- ANALOG INPUT WITH FIXED VOLTAGE GAIN
- INTEGRATED FLYBACK DIODES AT EACH OUTPUT
- THERMAL PROTECTION



Powerdip
12 + 2 + 2

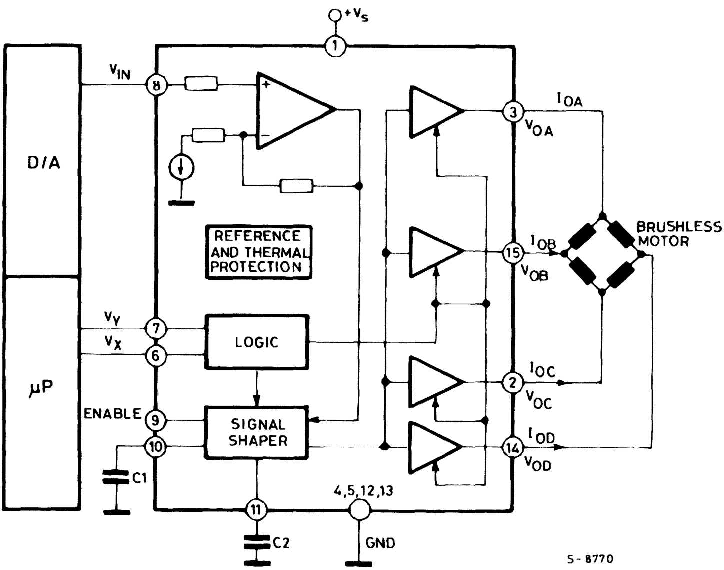
ORDER CODE : TDA8116

DESCRIPTION

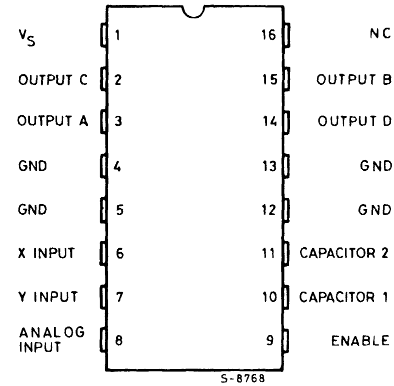
The TDA8116 is a monolithic integrated circuit in bipolar technology.

It is intended for driving a four phase brushless video head motor in microcomputer controlled servo systems.

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	– 0.3 to 18	V
I_O	Output Current DC	± 0.4	A
I_O	Pulse Output Current (during start)	± 1	A
T_{JOP}	Operating Junction Temperature	0 to 150	°C
T_{stg}	Storage Junction Temperature	– 40 to 150	°C
$V_{EN,\ IN,\ X,\ Y}$	Input Voltage	– 0.3 to 7	V
P_{tot}	Power Dissipation at T_{case} = 80 °C	5	W

THERMAL DATA

T_{JSTD}	Thermal Shut Down Threshold		150		°C
T_{JSDH}	Thermal Shut Down Hysteresis		20		°C
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-ground Pins			14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient			80	°C/W

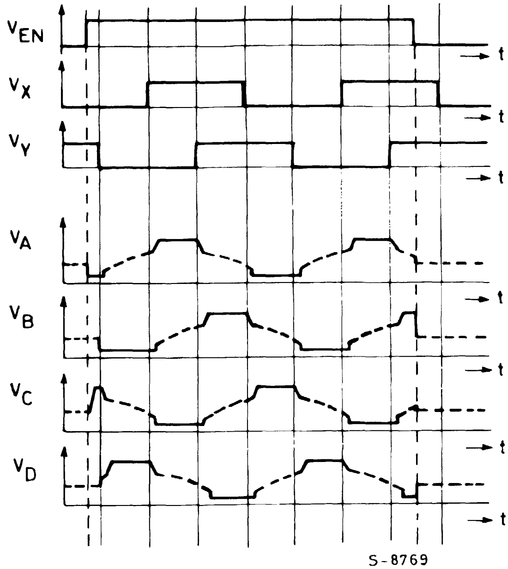
PIN FUNCTION

N°	Name	Function
1	V_S	Supply Voltage Connection
2	OUTC	Push-pull Type Output for the C Phase
3	OUTA	Push-pull Type Output for the A Phase
4, 5, 12, 13	GND	Ground Connection
6	X INPUT	Commutation Signal X Input
7	Y INPUT	Commutation Signal Y Input
8	INPUT	Analog Control Signal Input
9	ENABLE	Enable input, with low level (< 1.5 V) at this pin the device outputs are set into TRISTATE.
10, 11	CAPACITOR 1, 2	The shaping capacitors at these pins define the output signal shape of the A, C and B, D outputs respectively.
14	OUTD	Push-pull Type Output for the D Phase
15	OUTB	Push-pull Type Output for the B Phase
16	N.C.	No Connection at this Pin

ELECTRICAL CHARACTERISTICS (6 V < V_S < 14 V, T_j = 25 °C, unless otherwise specified))

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Sop}	Operating Supply Voltage Range		6		14	V
V_{SO}	Source Stage Saturation Voltage	V_{IN} = 5 V, I_O = 1 A I_O = 0.4 A		1.4 1	2 1.4	V V
V_O	Sink Stage Saturation Voltage	V_{IN} = 5 V, I_O = 1 A I_O = 0.4 A		1.4 1	2 1.4	V V
A_V	Voltage Gain	V_{IN} = 1 V, R_L = 50 Ω	2.5	2.75	3.0	V
V_{INth}	Input Voltage Threshold		0.6	0.7	0.8	V
I_N	Input Current	V_{IN} = 5 V	– 5	– 1	+ 5	µA
V_{IN}	Input Voltage Operating Voltage Range		0		V_S – 1	V
$V_{X,Y\,High}$	Control Input HIGH Level		1.7	2.4	7	V
$I_{X,Y\,High}$	Control Input HIGH Current	V_{IN} = 5 V			20	µA
$V_{X,Y\,Low}$	Control Input LOW Level		0.3		0.8	V
$I_{X,Y\,Low}$	Control Input LOW Current	V_{IN} = 0.4 V	– 20		20	µA
$V_{EN\,Low}$	Enable Input LOW Level		– 0.3		1.5	V
$V_{EN\,High}$	Enable Input HIGH Level		2.4		7	V
$I_{EN\,Low}$	Enable Input LOW Current	V_{EN} = 0 V		– 20	– 40	µA
$I_{EN\,High}$	Enable Input HIGH Current	V_{EN} = 5 V		1		µA
$VH_{X,\,Y,\,EN}$	Control and Enable Inputs Hysteresis			150		mV
$\frac{dV_{out}}{d_t}$	Output Voltage Slope	$C_{1,2}$ =10 nF		6		V/ms
$\lvert I_{OST}\rvert$	Starting Output Current	V_{IN} = 5 V V_S = 12 V			1	A
I_S	Quiescent Supply Current	V_{IN} = 0		3	5	mA
I_S	Supply Current	V_{IN} = 5 V		8	15	mA

TYPICAL WAVEFORMS



MULTISTANDARD VIDEO IF SYSTEM

- GAIN CONTROLLED IF AMPLIFIER
- VIF OPERATING FREQUENCY UP TO 50 MHz
- SYNCHRONOUS DETECTOR
- WHITE SPOT INVERTER
- VERY LOW DIFFERENTIAL ERROR
- VERY LOW PHASE ERROR
- INTERNAL AGC SWITCH (B/G - L)
- AGC TOP. SYNCH. FOR STANDARD B/G
- AGC TOP WHITE FOR STANDARD L
- QUASI SPLIT SOUND FOR STANDARD B/G
- SOUND DETECTOR FOR STANDARD L
- VIDEO MUTING FACILITY
- SEPARATED SOUND OUTPUT
- OPERATES WITHOUT EXTERNAL GATING PULSE

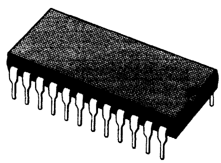
DESCRIPTION

The TDA8120 is a monolithic IC for TV video IF and Sound IF amplification and demodulation that can operate with all the TV standards.

The Video IF section can handle negative (B/G) or positive (L) modulated video signals by means of DC switching.

The Sound IF section acts as a Quasi Split Sound (QSS) subsystem in B/G transmission and allows a second Sound IF with high rejection of the video information.

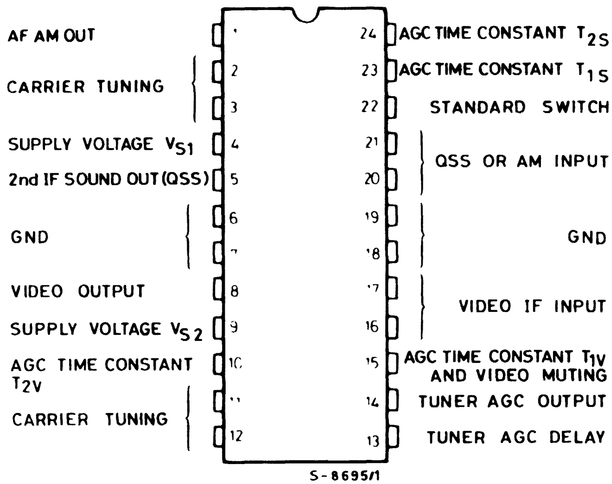
The DC switch can modify the Sound IF configuration to process AM modulated Sound signals (L). The TDA8120 is assembled in a 24 pin dual in line power package.



DIP24

ORDER CODE : TDA8120

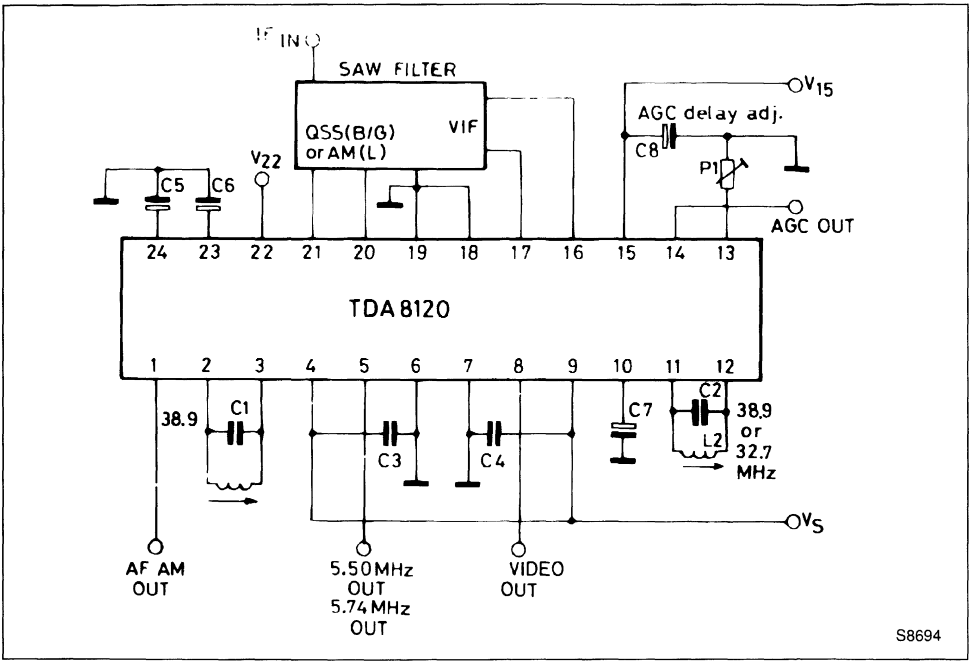
CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_4, V_9	Supply Voltage V_s	15	V
I_8, I_5, I_1	Video Out, QSS_{out}, AF AM Out, DC Output Current	10	mA
I_{22}, I_{15}	Pin 22 and Pin 15 Input Current	1	mA
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	2	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C
V_{14}	Voltage at Pin 14	V_s	

TEST CIRCUIT



THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance	Max	40	°C/W

CIRCUIT OPERATION

The TDA8120 (see block diagram) consists of a video section and a sound section. The integration of both sections on the same chip requires a high isolation at IF frequencies. This is achieved by physically separating the two sections, with separate power supplies and ground pins. In addition, special care has been taken in the choice of pad positions for the IF inputs and sound/video outputs.

The video section consists of three AC-coupled IF stages with more than 60 dB AGC range, flat amplitude/frequency response from 10 to 85 MHz and linearized phase slope from 30 to 50 MHz. Video carrier regeneration is performed by a tuned limiter. The carrier is then applied to the video demodulator through a special circuit which switches the carrier phase from 0 to 180° so that the video polarity can be maintained constant when the standard switches from B/G to L. A noise inverter and a white spot inverter are included to eliminate ultra-black and white pulses.

A top sync or a top white clamping circuit and a minimum DC video component detector are implemented by two double comparators the characteristics of which may be controlled by an external control input to adapt to the modulation type for each standard. The voltage at the output of the two comparators is memorized by an external capacitor and used to drive the AGC network, which allows an input regulation of the video carrier from less than 100 μV to 100 mV. A delayed control storage with current output for the turner AGC completes the video section.

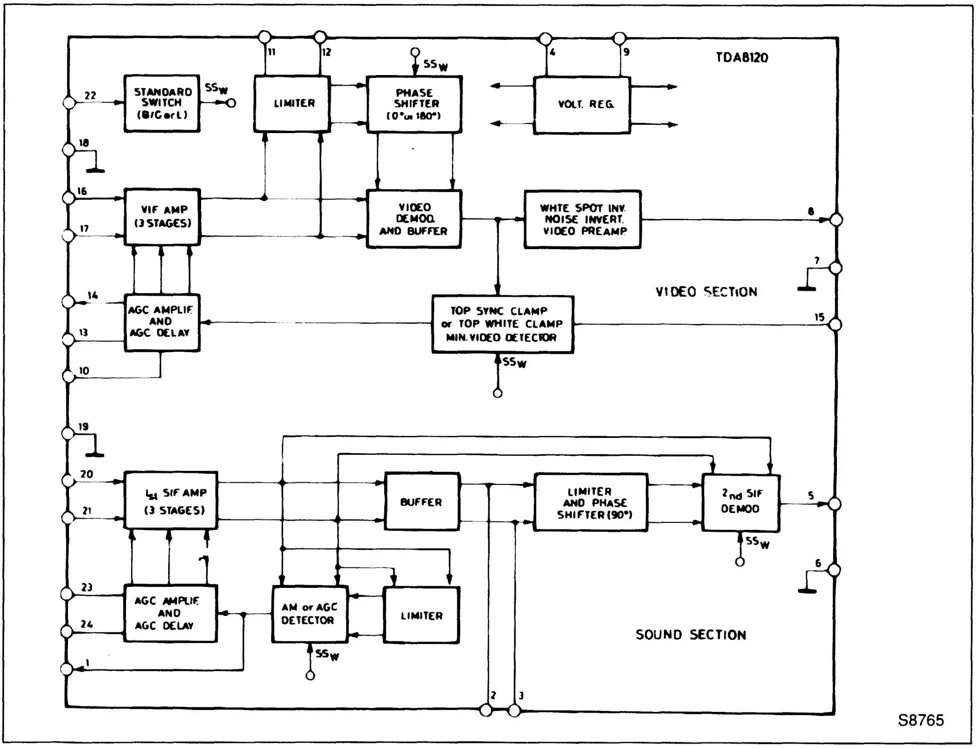
The sound section consists of three IF stages with the same characteristics as the video IF stages and an identical network to control and set the gains of the three IF amplifiers. The output of the third IF stage feeds the AM/AGC detector and the QSS section.

The AM/AGC detector consists of a wideband limiter for AM sound regeneration or video carrier regeneration used to feed the synchronous multiplier and consequently to obtain the AM demodulated audio signal. In addition, a DC voltage proportional to the peak-to-peak value of the video carrier is produced. Two comparators complete the sound AGC loop.

The subsequent QSS section consists of a reference amplifier tuned to the video IF which buffers a wideband limiter to reject completely the video AM information without introducing incidental phase modulation (IPM).
Following the limiter there are a 90° phase shifter and a linear-to-logarithmic converter which drives a linear multiplier as a demodulator for the intercarrier 2nd sound IF. This quadrature multiplier rejects all video components transmitted in DSB that is low frequency components of the video signal.

In addition to the sound and video sections, the TDA8120 includes a block for standard switching (B/G or L) controlled by a TTL-compatible input.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_s = 12 V, T_{amb} = 25 °C)

VIDEO IF SECTION V_I = 10 mV_{rms} (black field), F_o = 38.9 MHz ; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 4 and pin 9)		10.8	12	13.2	V
I_s	Supply Current	V_I= 0		120		mA
$V_{8\,H}$	Top White Level	V_I = 0 R_L = 1.5 KΩ		6		V
$V_{8\,L}$	Top Synchronous Level			3		V
V_8	Video Output B/G	Modulation Depth D = 90 % R_L = 1.5 KΩ		3		V_{pp}
V_8	Video Output L	R_L = 1.5 KΩ M = 100 %		3		V_{pp}
ΔV_8	Video Output Variat. between Standards B/G and L	M = 100 %		± 2	10	%
$-I_8$	Output Current	R_L = 1.5 KΩ		4		mA
I_8	Input Current		2			mA
I_{14}	Turner AGC Current Capability			10		mA
S/N	Signal to Noise Ratio	B = 5 MHz D = 90 %	50			dB
ΔV_I	AGC Range	ΔV_8 = 1 dB D = 90 %	60			dB
B	Bandwidth	ΔV_8 = – 3 dB D = 90 %	7			MHz
V_{16-17}	Input Sensitivity for Full Output Signal	D = 90 %		50		µV
V_8	Carrier Leakages	F_o = 38.9 MHz		20		mV
		F_o = 77.8 MHz		50		mV
dG	Differential Gain	Subcarrier Modulated Staircase Video Signal D = 90 %			10	%
dφ	Differential Phase	Subcarrier Modulated Staircase Video Signal D = 90 %			10	degree
d_{IM}	Intermodulation Product 1.07 MHz	Video Carrier Relative Level = 0 dB Chroma Subcarrier Relative Level = – 3.2 dB Sound Carrier Relative Level = – 20 dB		50		dB
R_i	Input Resistance (between pin 16 and pin 17)			1.5		KΩ
C_i	Input Capacitance (between pin 16 and pin 17)			2		pF

QUASI SPLIT SOUND CHANNEL OR FRENCH SOUND CHANNEL (see notes 1 and 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{20-21}	Input Sensitivity for Full Output Signal (between pin 20 and 21)	R Channel Missing		50		µV
ΔV_i	AGC Range	ΔV_5 = 1 dB R Channel Missing	60			dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_5	Output Voltage Standard B/G	R_L = 600 Ω, F_o = 5.5 MHz, AC Coupled		100		mVrms
V_5	Output Voltage Standard B/G	R_L = 600 Ω, F_o = 5.74 MHz, AC Coupled		50		mVrms
I_5	Output Current			2.5		mA
Z_5	Small Signal Output Impedance (QSS)	F_o = 5.5 MHz or F_o = 5.74 MHZ			50	KΩ
R_i	Input Resistance (between pin 21 and pin 20)			1.5		KΩ
C_i	Input Capacitance (between pin 21 and 20)			2		pF
S/N	Noise Ratio QSS (after SIF limitation and FM demodulation) F_o = 5.50 MHz F_o = 5.74 MHz	Channel R or Channel L Switched off F_m = 1 kHz Δ_f = ± 30 kHz Carrier Modulated with Syncs. Pulses Only. CCIR 468–2 Recomendant.	60 58			dB dB
V_1	Output Voltage Standard L			0.7		V_{rms}
I_1	Output Current			2.5		mA
Z_1	AF Output Impedance (L)				50	Ω
S/N	Noise Ratio AM Standard L	B_N = 20 KHz	46			dB
d	Distortion				3	%
V_{22}	B/G Operation		2		5	V
V_{22}	L Operation		0		0.8	V
V_{15}	Video Muting		8		V_s	V

Notes : 1. QUASI SPLIT SOUND CHANNEL

Video carrier relative level = 0 dB f= 38.9 MHz

Δf = 0 { Sound carrier relative level = – 13 dB (mono or L) f = 33.4 MHz
Sound carrier relative level = – 20 dB (R) f= 33.16 MHz }

V_I = 10 mV Video carrier modulated with syncs ; V_{22} = 2 V, unless otherwise specified.

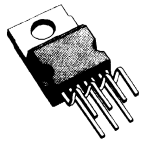
2. FRENCH SOUND CHANNEL

V_I = 10 mV (Carrier level) ; f_o = 39.2 MHz ; F_m = 1 KHz ; m = 80 % ; V_{22} = 0.8 V, unless otherwise specified.

5.1V + 8.5V REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 8.5V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT

ORDER CODE : TDA8133

DESCRIPTION

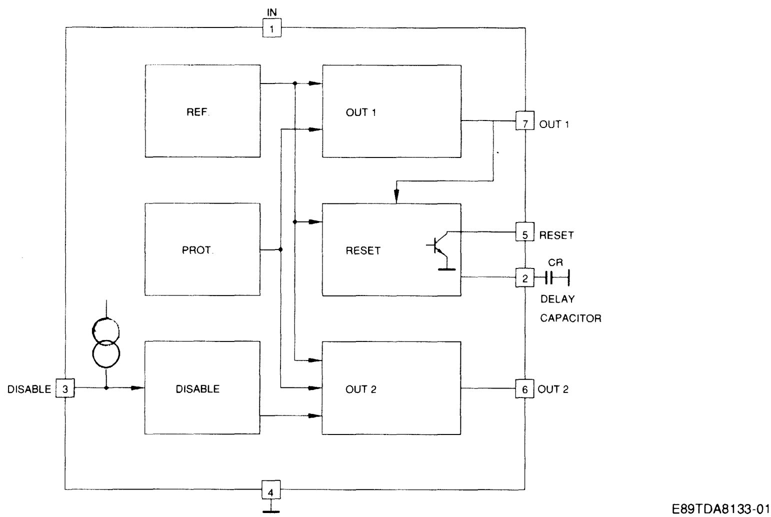
The TDA8133 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 8.5V at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

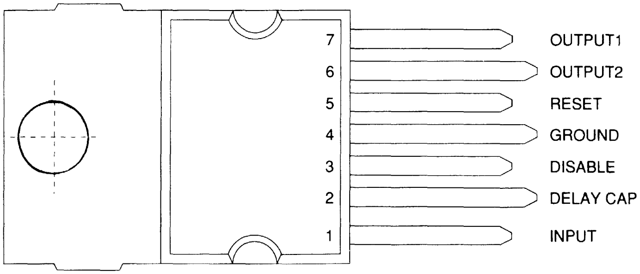
Short circuit and thermal protections are included.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at pin 5	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{01}	Output Voltage	I_{01} = 10mA	5	5.1	5.2	V
V_{02}	Output Voltage	I_{02} = 10mA	8.33	8.5	8.67	V
V_{01}	Output Voltage	7V < V_{IN1} < 14V 10.5V < V_{IN2} < 18V 5mA < $I_{01,2}$ < 750mA	4.9		5.3	V
V_{02}	Output Voltage		8.15		8.85	V
$V_{I01,2}$	Dropout Voltage	$I_{01,2}$ = 750mA			1.4	V
		$I_{01,2}$ = 1A			2	V
V_{01LI}	Line Regulation	7V < V_{IN1} < 14V 10.5V < V_{IN2} < 18V $I_{01,2}$ = 200mA			50	mV
V_{02LI}	Line Regulation				85	mV
V_{01LO}	Load Regulation	5mA < $I_{01,2}$ < 0.6A			100	mV
V_{01LO}	Load Regulation				170	mV
I_Q	Quiescent Current	I_{01} = 10mA Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at pin 5	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at pin 5 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at pin 5 in Normal Condition	V_5 = 10V			10	µA
$V_{01,2}/T$	Output Voltage Thermal Drift			100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN1} = 7V ; V_{IN2} = 10.5V			1.6	A
		$V_{IN1,2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable bias Current at Pin 3	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (VOUT – 0.25V) the comparator "a" (see fig. 1) discharges rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law :

$$t_d = \frac{Ce \,.\, 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time.
During a short circuit a large consomption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

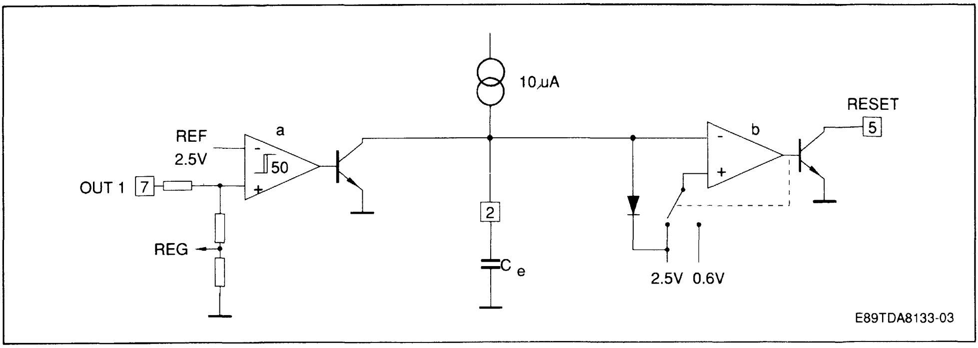
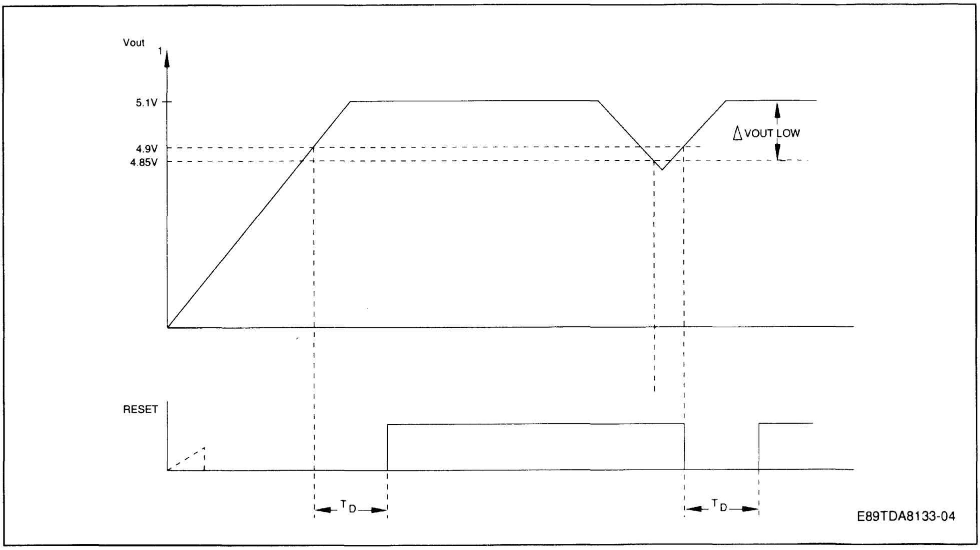


Figure 2.



CIRCUIT DESCRIPTION

The TDA8133 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

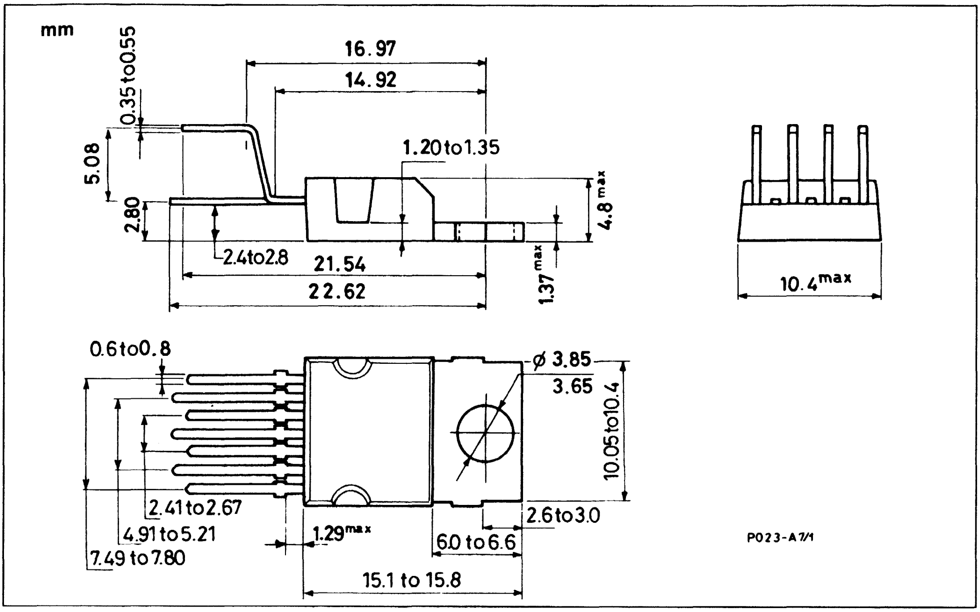
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3.

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 5 (open collector) with a certain delay depending by an external capacitor connected at pin 2.

PACKAGE MACHANICAL DATA

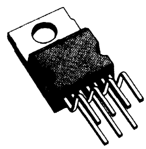
HEPTAWATT – PLASTIC PACKAGE



5V + 12V REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

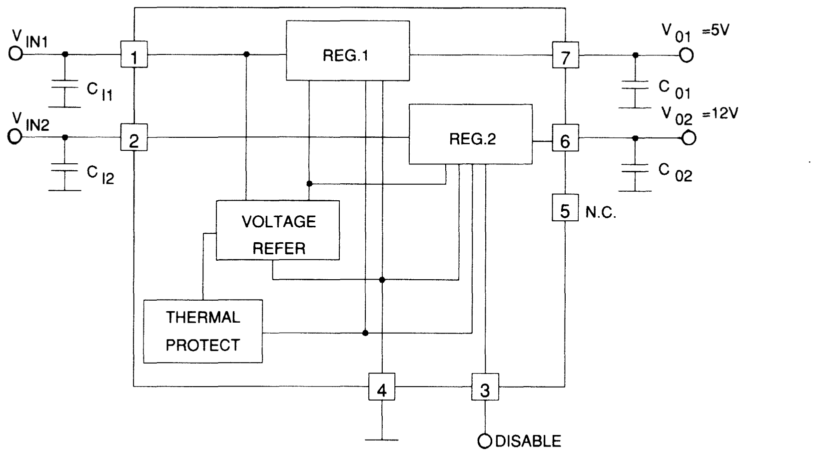
ORDER CODE : TDA8134

DESCRIPTION

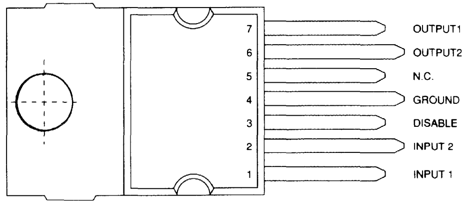
The TDA8134 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, 5V + 12V at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

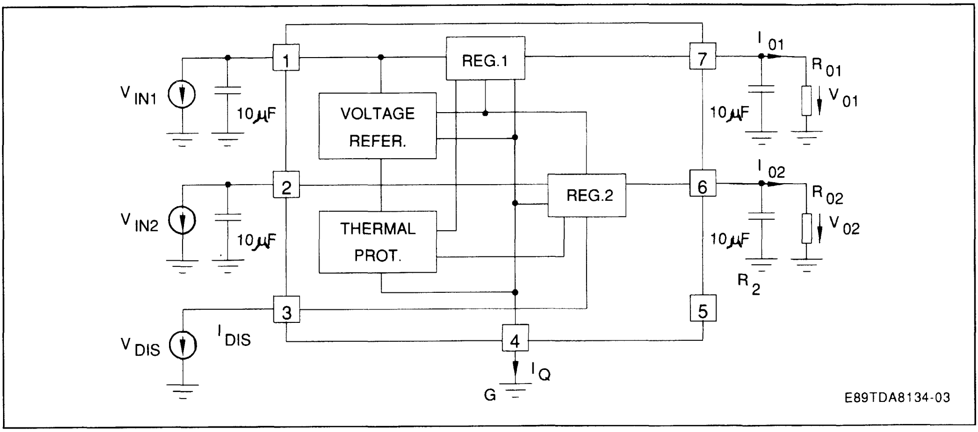
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.9	5	5.1	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	7V < V_{IN1} < 14V I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} < 18V I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} < 600mA			100	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} < 600mA			240	mV
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} < 18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} < 18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 9V_{DC} + 1V_{PP} SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = 16V_{DC} + 1V_{PP} SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	V_{IN1} = V_{IN2} = 14V_{DC} I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

Note 1 : SVR supply voltage rejection :

$$20 \,.\, LOG \,.\, \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output

Figure 1 : Test Specification.



CIRCUIT DESCRIPTION

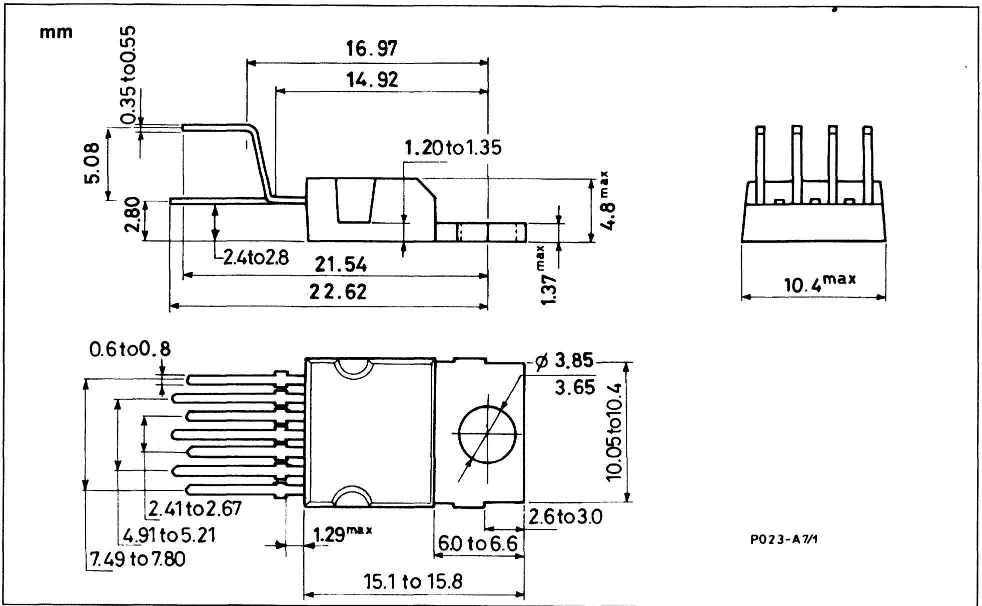
The TDA8134 is a dual voltage regulator with disable.

The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (V_{IN1}), the regulator 2 will not work if the pin 1 is not supplied.

It is possible switch-off the output voltage 2 (V_{O2}) appling at pin 3 (disable input) a low TTL level.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



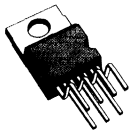
ST SGS-THOMSON MICROELECTRONICS

TDA8135

5V + ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5V ± 3%
- OUTPUT 2 - VOLTAGE PROGRAMMABLE FROM 5V TO 14V
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

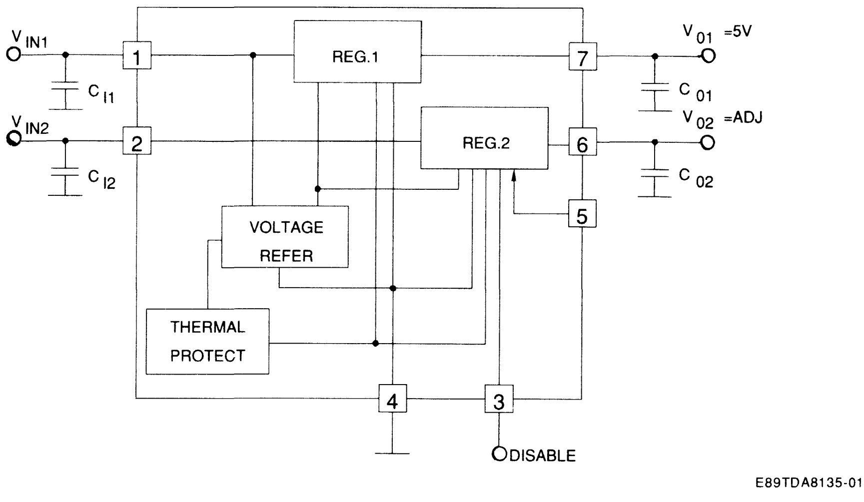
ORDER CODE : TDA8135

DESCRIPTION

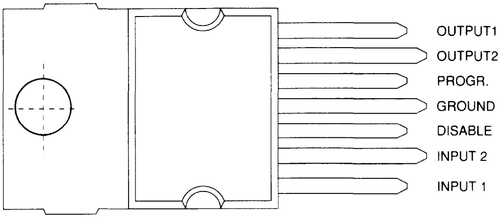
The TDA8135 is a monolithic dual positive voltage regulator designed to provide precision output voltages, 5V + adjustable outputs at currents up to 600mA.

Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = V_{O2} + 2V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

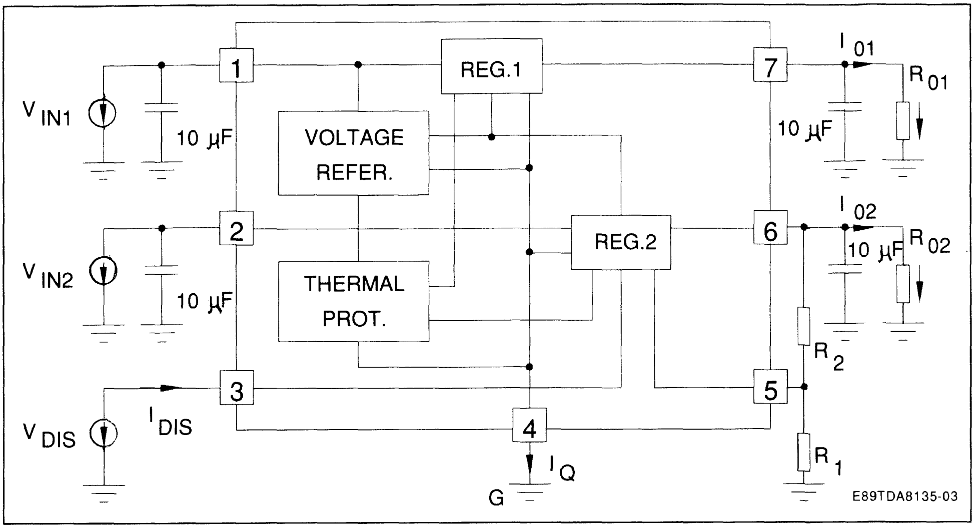
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		4.85	5	5.15	V
V_{O2}	Output Voltage at Pin 6	Adjustable	5		14	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation	7V < V_{IN1} < 14V I_{O1} = 200mA			90	mV
ΔV_{O2LI}	Line Regulation	12V < V_{IN2} < 20V I_{O2} = 200mA V_{O2} = 10V			200	mV
ΔV_{O1LO}	Load Regulation	0 < I_{O1} < 600mA			100	mV
ΔV_{O2LO}	Load Regulation	0 < I_{O2} < 600mA V_{O2} = 10V			200	mV
I_{O1SC}	Short Circuit Current 1	7V < V_{IN1} < 14			1.3	A
I_{O2SC}	Short Circuit Current 2	V_{O2} + 2V < V_{IN2} < 20V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
V_{PROG}	Reference Voltage at Pin 5			2.5		V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 9V_{DC} + 1V_{PP} SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = 16V_{DC} + 1V_{PP} SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

Note 1:
SVR supply voltage rejection

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{O\,ac}} \right|$$

where :
- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output

TEST SPECIFICATION



CIRCUIT DESCRIPTION

The TDA8135 is a dual voltage regulator with disable.

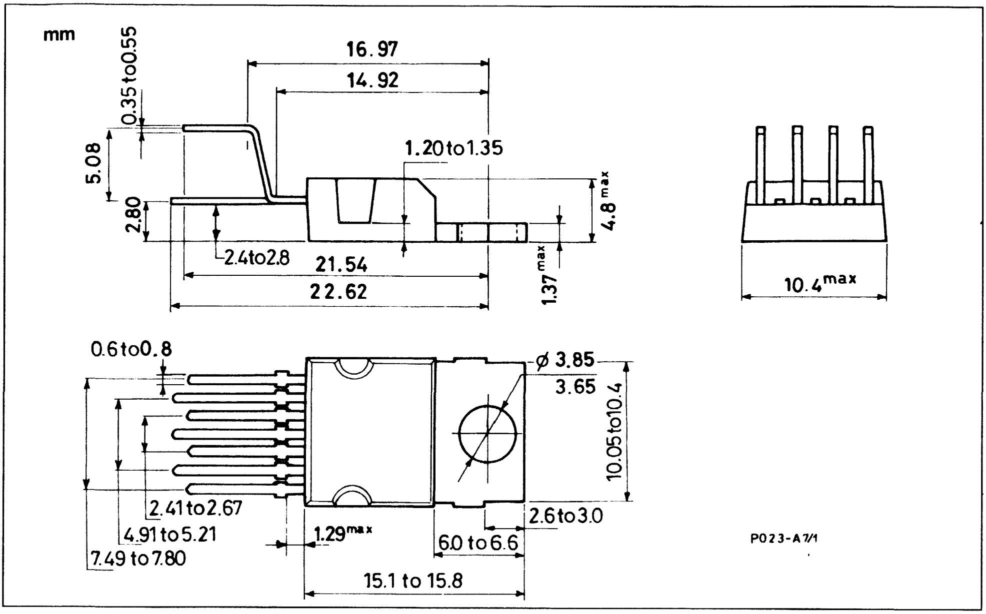
The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (Vin1), the regulator 2 will not work if the pin 1 is not supplied.

It is possible switch-off the output voltage 2 (V_{O2}) appling at pin 3 (disable input) a low TTL level.

$$V_{O2} = V_{PROG} \frac{R1 + R2}{R1}$$

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



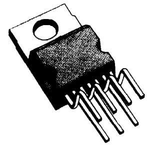
SGS-THOMSON MICROELECTRONICS

TDA8136

DUAL 12V REGULATOR WITH DISABLE

ADVANCE DATA

- OUTPUT CURRENTS UP TO 600mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 12V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 2 VOLTAGE DISABLED BY A TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUT 1.5V AT 400mA
- HIGH SUPPLY VOLTAGE REJECTION



HEPTAWATT

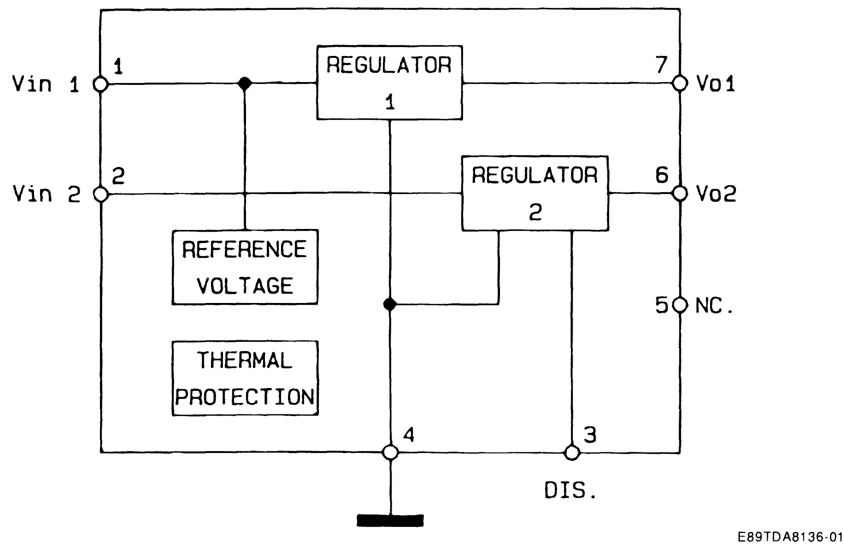
ORDER CODE : TDA8136

DESCRIPTION

The TDA8136 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages, both 12V at currents up to 600mA.

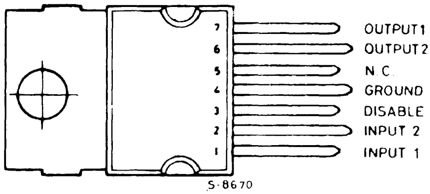
Output 2 can be disabled by a TTL input. Both output currents are limited by an internal short circuit protection.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



Tab connected to pin 4.

E89TDA8136-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{IN1,\,2}$	DC Input Voltages	24	V
V_{DIS}	Disable Input Voltage Pin 3	24	V
$I_{O1,\,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j\text{-}c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS

($V_{IN1,2}$ = 14V ; V_{DIS} = 2.5V ; $I_{O1,2}$ = 0 ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage at Pin 7		11.76	12	12.24	V
V_{O2}	Output Voltage at Pin 6		11.76	12	12.24	V
I_{Q1}	Quiescent Current	V_{IN2} = 0 V_{DIS} = 0 I_{O1} = 10mA (see fig. 1)			2	mA
I_{Q2}	Quiescent Current	I_{O2} = 10mA (see fig. 1)			2	mA
V_{IN1}-V_{O1}	Drop Out Voltage 1	I_{O1} = 400mA			1.5	V
V_{IN2}-V_{O2}	Drop Out Voltage 2	I_{O2} = 400mA			1.5	V
ΔV_{O1LI}	Line Regulation 1	14V < V_{IN1} < 18V I_{O1} = 200mA			120	mV
ΔV_{O2LI}	Line Regulation 2	14V < V_{IN2} < 18V I_{O2} = 200mA			120	mV
ΔV_{O1LO}	Load Regulation 1	0 < I_{O1} < 600mA			240	mV
ΔV_{O2LO}	Load Regulation 2	0 < I_{O2} < 600mA			240	mV
I_{O1SC}	Short Circuit Current 1	14V < V_{IN1} < 18V			1.3	A
I_{O2SC}	Short Circuit Current 2	14V < V_{IN2} < 18V			1.3	A
V_{DISH}	Disable Voltage HIGH at Pin 3		2			V
V_{DISL}	Disable Voltage LOW at Pin 3				0.8	V
I_{DISH}	Bias Current at Pin 3	V_{DIS} = 5.3V			10	µA
I_{DISL}	Bias Current at Pin 3	V_{DIS} = 0.4V	– 80			µA
SVR_1	Supply Voltage Rejection 1 (see note 1)	V_{IN1} = 16 V_{DC} + 1V_{PP} SIN f = 120Hz I_{O1} = 200mA	50			dB
SVR_2	Supply Voltage Rejection (see note 1)	V_{IN2} = 16 V_{DC} + 1V_{PP} SIN f = 120Hz I_{O2} = 200mA	50			dB
I_Q	Quiescent Current	I_{O1} = I_{O2} = 200mA			6	mA
T_{JSD}	Thermal Shut-down Junction Temperature			145		°C

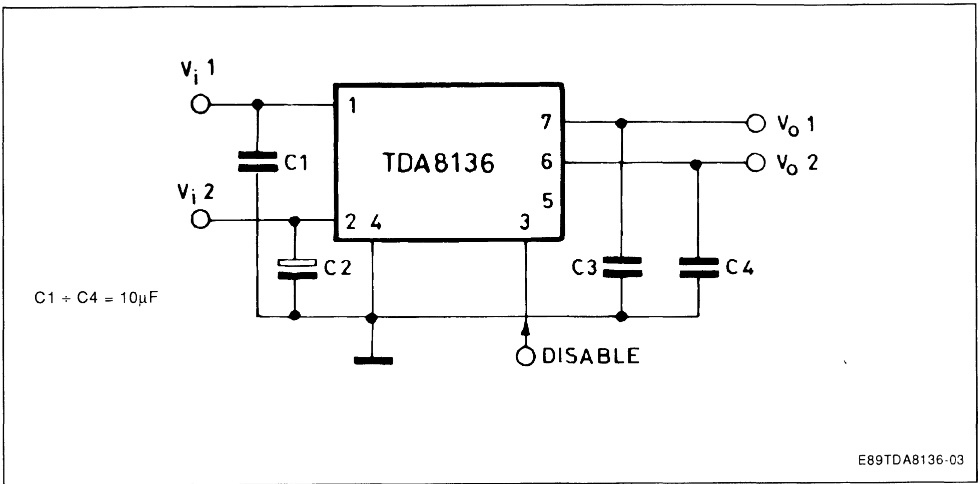
Note 1 : SVR supply voltage rejection

$$20 \cdot LOG \cdot \left| \frac{V_{IN\,ac}}{V_{o\,ac}} \right|$$

where :

- $V_{IN\,ac}$ is the value of the sinusoidal signal forced at the input. (120Hz, 1V_{PP})
- $V_{O\,ac}$ is the peak-peak ripple voltage present at the output.

TYPICAL APPLICATION CIRCUIT



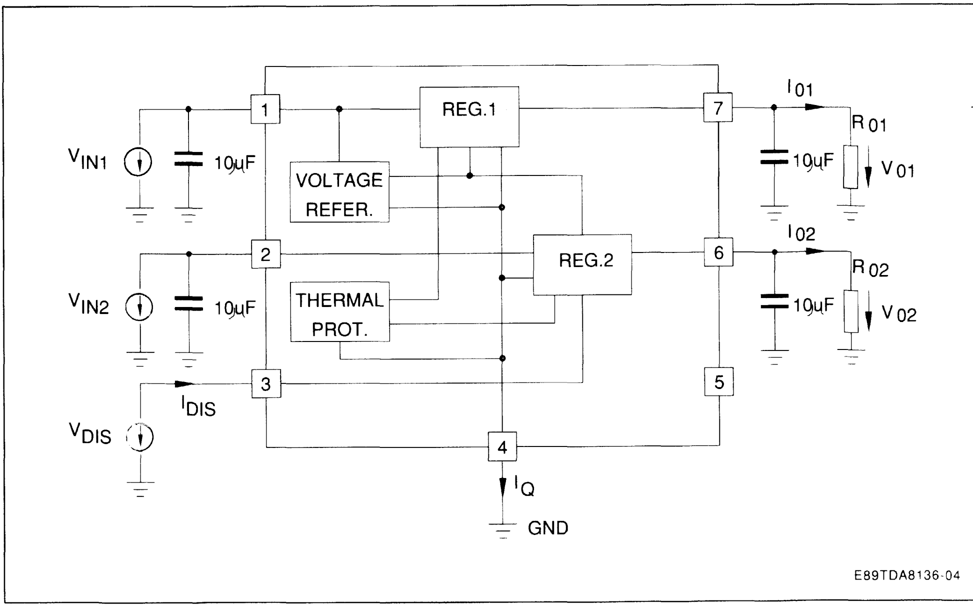
CIRCUIT DESCRIPTION

The TDA8136 is a dual voltage regulator with disable.

The two regulation parts are supplied from one voltage reference circuit, trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at pin 1 (V_{IN1}), the regulator 2 will not work if the pin 1 is not supplied.

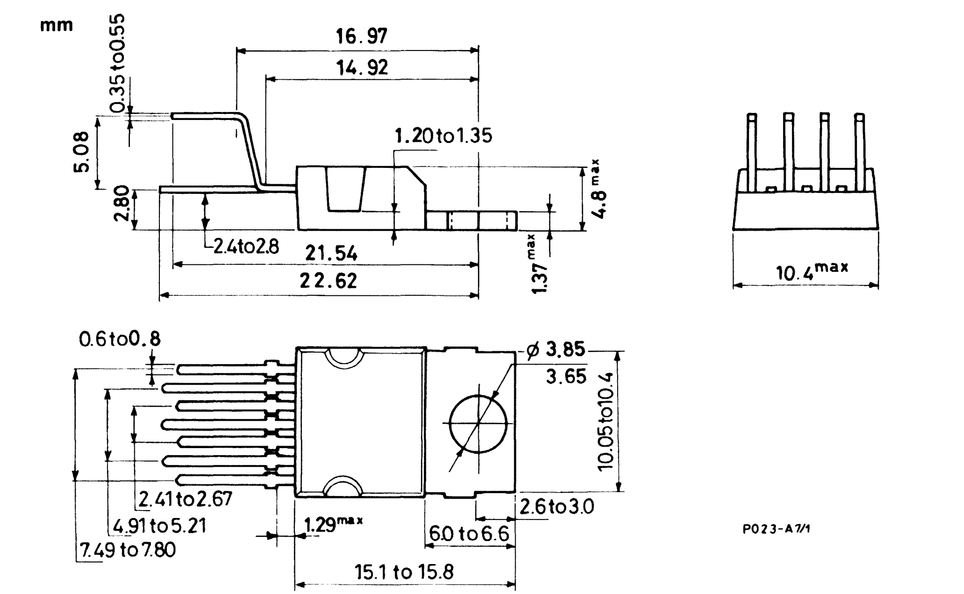
It is possible switch-off the output voltage 2 (V_{O2}) applying at pin 3 (disable input) a low TTL level.

Figure 1 : Test Circuit.



PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



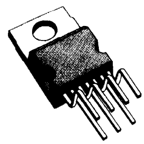
SGS-THOMSON MICROELECTRONICS

TDA8137

DUAL 5.1V REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT VOLTAGES 5.1V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



HEPTAWATT

ORDER CODE : TDA8137

DESCRIPTION

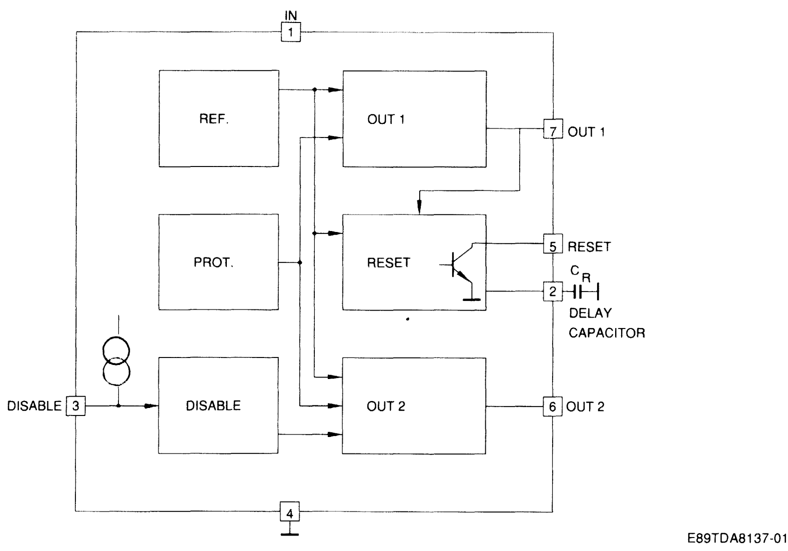
The TDA8137 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

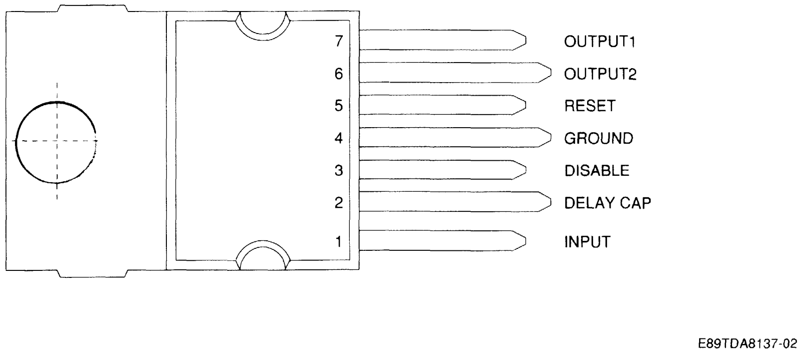
Short circuit and thermal protections are included.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3	20	V
V_{RST}	Output Voltage at Pin 5	20	V
$I_{01,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	3	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{01,2}$	Output Voltage	$I_{01,2}$ = 10mA	5	5.1	5.2	V
		7V < V_{IN} < 14V 5mA < I_0 < 750mA	4.9		5.3	V
$V_{I01,2}$	Dropout Voltage	$I_{01,2}$ = 750mA			1.4	V
		$I_{01,2}$ = 1A			2	V
$\Delta V_{01,2LI}$	Line Regulation	7V < V_{IN} < 14V $I_{01,2}$ = 200mA			50	mV
$\Delta V_{01,2LO}$	Load Regulation	5mA < $I_{01,2}$ < 0.6A			100	mV
I_Q	Quiescent Current	I_{01} = 10mA Output 2 Disabled			2	mA
V_{01RST}	Reset Threshold Voltage	(K = V_{01})	K–0.4	K–.25	K–0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20		75	mV
t_{RD}	Reset Pulse Delay at Pin 5	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 5 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$K_{01,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta Vo \cdot 10^6}{\Delta T \cdot Vo}$ T_j = 0 to + 125°C		100		ppm/°C
$I_{01,2SC}$	Short Circ. Output Current	V_{IN} = 7V			1.6	A
		V_{IN} = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 3 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 3 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 3	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig. 1) discharge rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law :

$$t_d = \frac{Ce \cdot 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V_2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

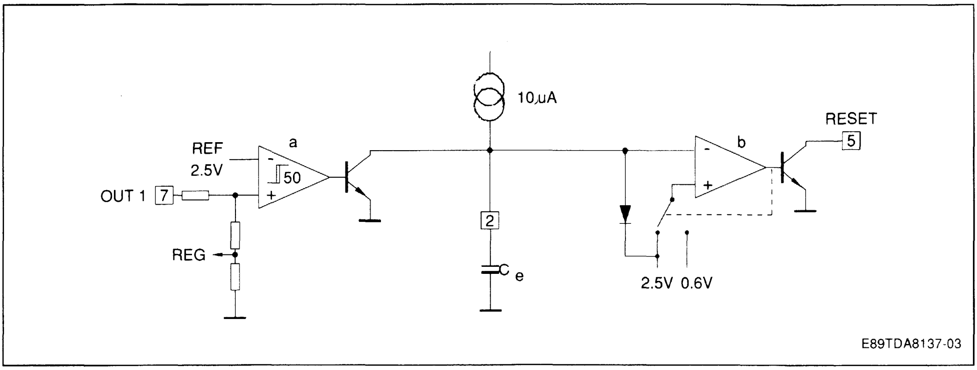
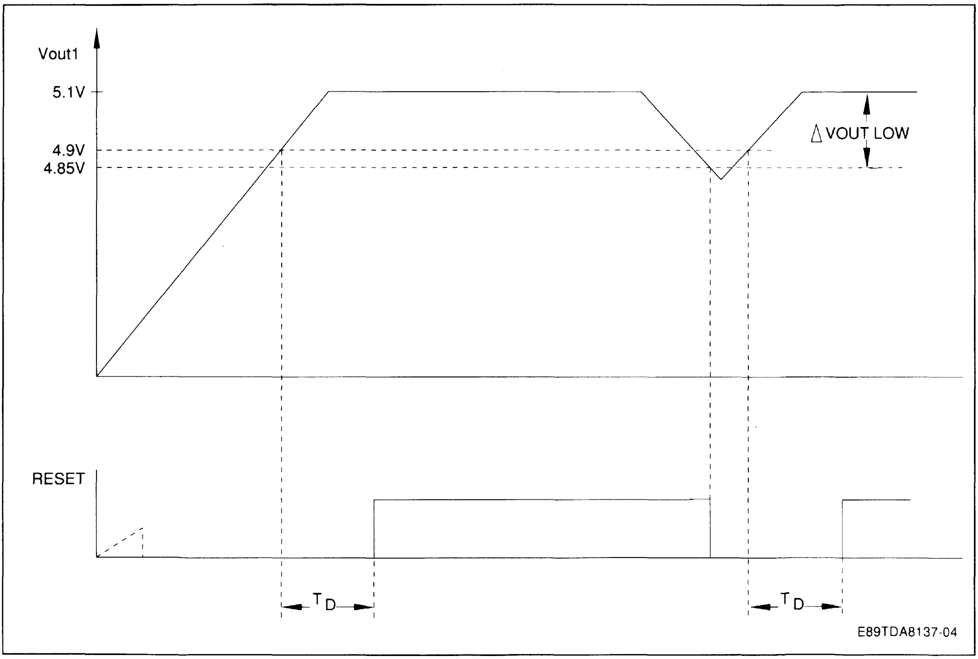
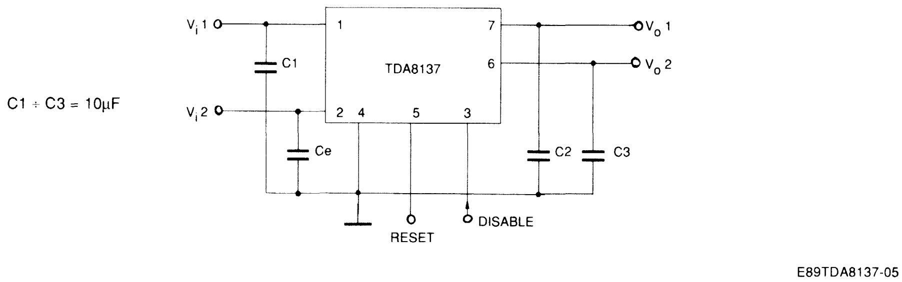


Figure 2.



TYPICAL APPLICATION CIRCUIT



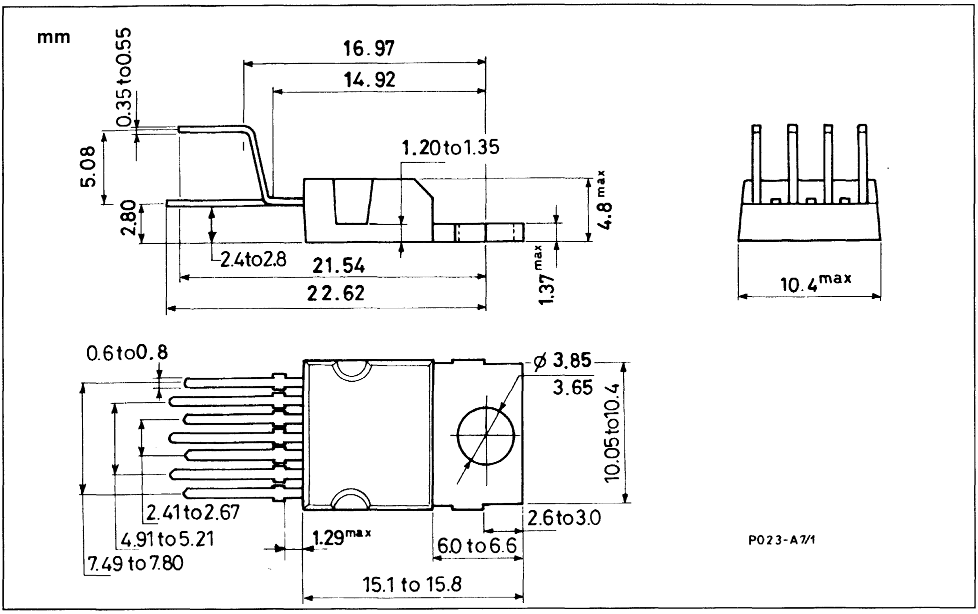
CIRCUIT DESCRIPTION

The TDA8137 is a dual voltage regulator with Reset and Disable.
The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3.
The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 5 (open collector) with a certain delay depending by an external capacitor connected at pin 2.

PACKAGE MECHANICAL DATA

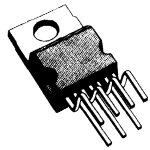
HEPTAWATT – PLASTIC PACKAGE



DEDICATED VIDEO PRODUCTS
5.1V + 12V REGULATOR WITH DISABLE AND RESET

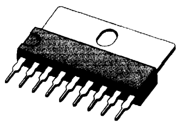
ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V ± 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT-CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROPOUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE (but without reset facility)



HEPTAWATT

ORDER CODE : TDA8138



SIP-9

ORDER CODE : TDA8138S

DESCRIPTION

The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

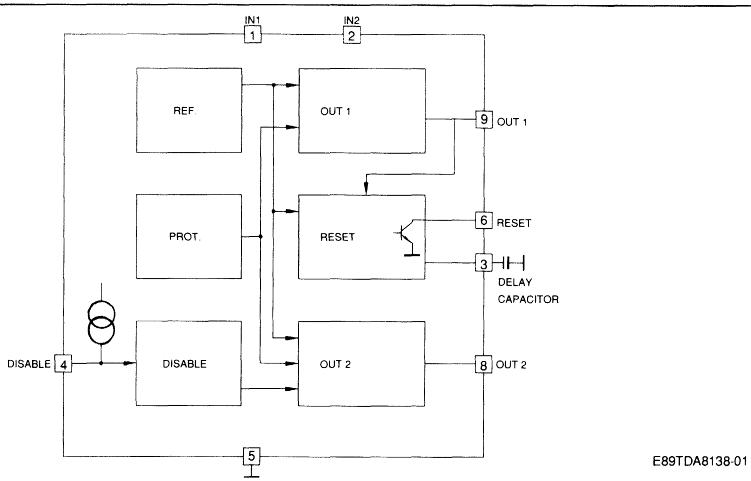
An internal reset circuit generates a delayed reset pulse when the output 1 falls below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short-circuit and thermal protections are included.

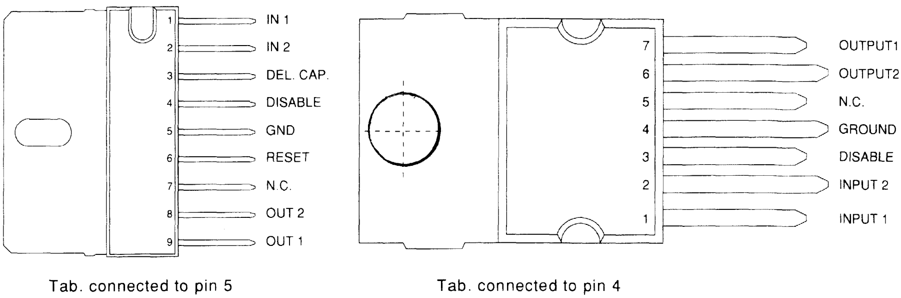
BLOCK DIAGRAM

SIP-9 Package



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3 (HEPTAWATT) or Pin 4 (SIP-9)	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_j	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$	Maximum Thermal Resistance Junction-case for Sip-9	8	°C/W
	for Heptawatt	3	°C/W
$R_{th(j-a)}$	Maximum Thermal Resistance Junction-ambient for Sip-9	60	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN1} = 7V ; V_{IN2} = 14V ; T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	11.76	12	12.24	
V_{O1}	Output Voltage	7V < V_{IN1} < 14V	4.9		5.3	V
V_{O2}	Output Voltage	14 < V_{IN2} < 18 5mA < $I_{O1,2}$ < 750mA	11.5		12.5	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA			1.4	V
		$I_{O1,2}$ = 1A			2	V
$V_{O1,2LI}$	Line Regulation	7V < V_{IN1} < 14V			50	mV
		14V < V_{IN2} < 18V			120	mV
		$I_{O1,2}$ = 200mA				
$V_{O1,2LO}$	Load Regulation	5mA < I_{O1} < 0.6A 5mA < I_{O2} < 0.6A			100 250	mV mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 6 in Normal Condition	V_5 = 10V			10	µA
$V_{O1,2}/T$	Output Volt. Thermal Drift			100		ppm/°C
$I_{O1,2SC}$	Short Circ. Output Current	V_{IN1} = 7V V_{IN2} = 14V			1.6	A
		$V_{IN1,2}$ = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. High (out 2 active)		2			V
V_{DISL}	Disable Volt. Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0V < V_{DIS} < 7V	– 100		2	µA
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig. 1) discharges rapidly the capacitor Ce and the Reset output (pin 6) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 3 increases with this law :

$$t_d = \frac{Ce \, . \, 2.5V}{10/\mu A} \quad \text{(see fig. 2)}$$

as V_2 reach 2.5V the Reset output (pin 6) goes HIGH again.To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at a time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

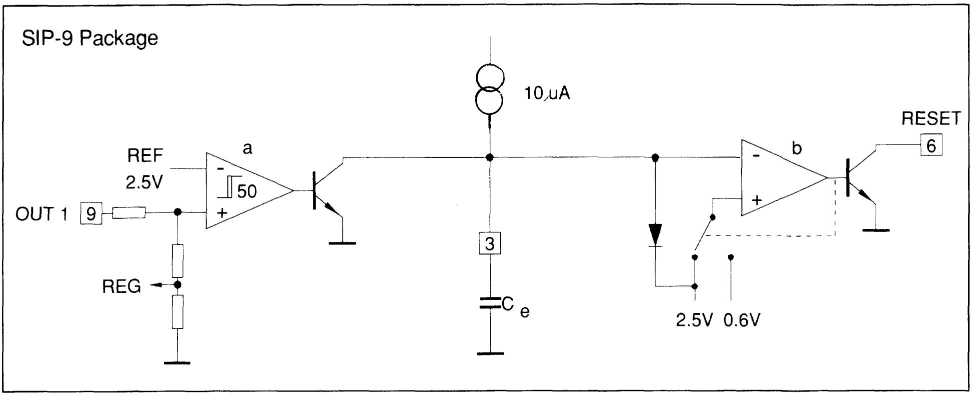
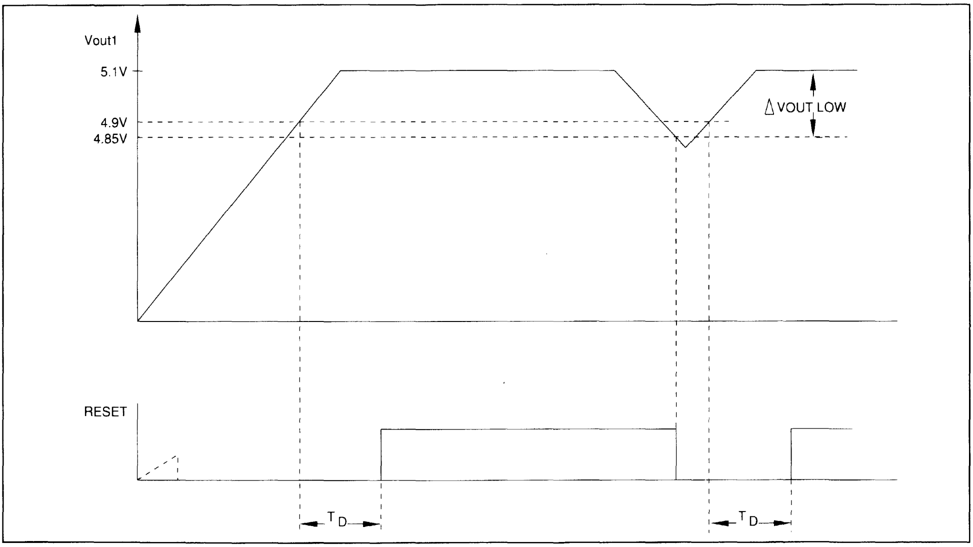


Figure 2.



CIRCUIT DESCRIPTION

The TDA8138 is a dual voltage regulator with Reset and Diasable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

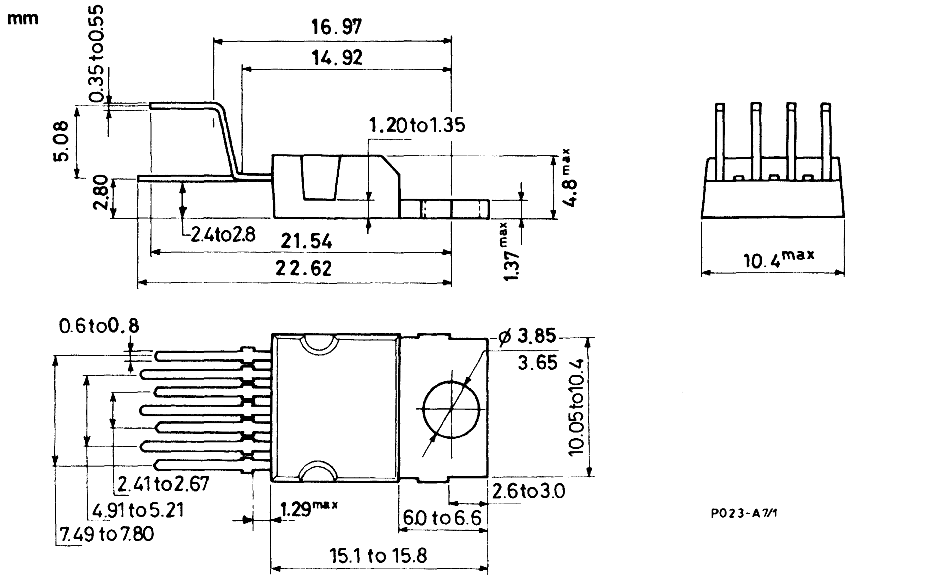
The output stages have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 3 (HEPTAWATT) or pin 4 (SIP-9).

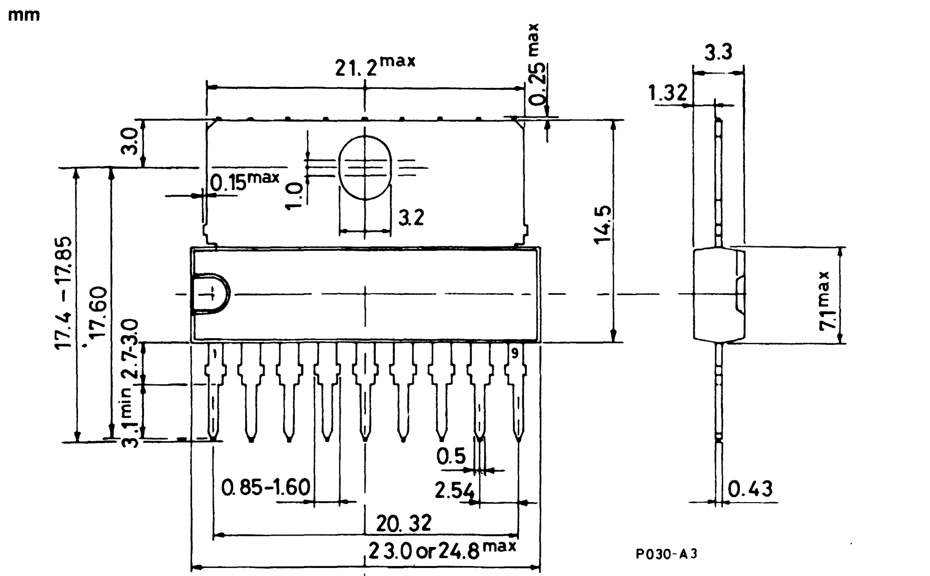
The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 6 (open collector) with a certain delay depending by an external capacitor connected at pin 3.

PACKAGE MECHANICAL DATA

HEPTAWATT – PLASTIC PACKAGE



9 PINS – PLASTIC SIP



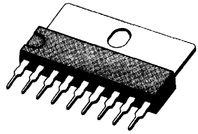
SGS-THOMSON
MICROELECTRONICS

TDA8139

5.1V AND ADJUSTABLE VOLTAGE REGULATOR WITH DISABLE AND RESET

ADVANCE DATA

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- OUTPUT 2 VOLTAGE PROGRAMMABLE FROM 2.5 TO 16V
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE



SIP-9

ORDER CODE : TDA8139

DESCRIPTION

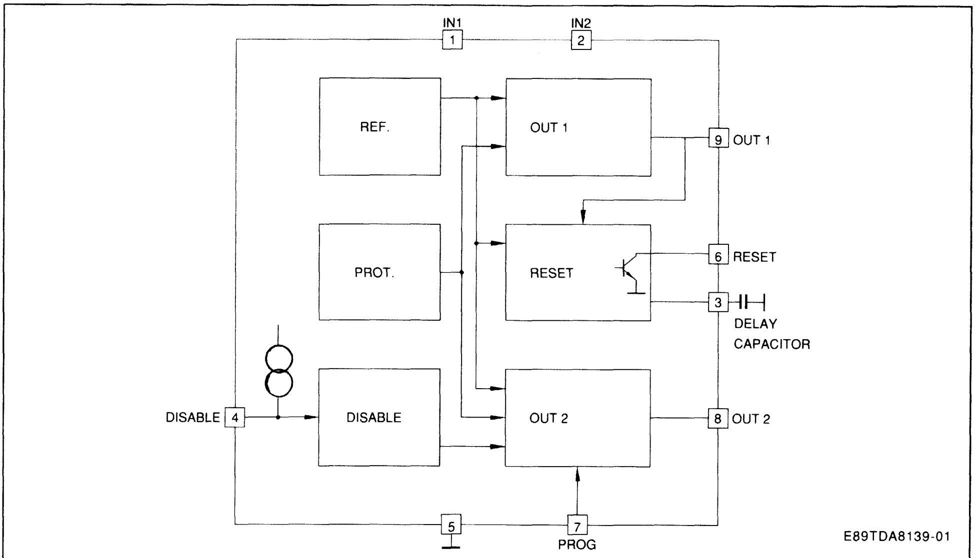
The TDA8139 is a monolithic dual positive voltage regulator designed to provide precision output voltages of 5.1V and adjustable at currents up to 1A.

An internal reset circuit generates a delayed reset pulse when the output 1 decreases below the regulated voltage value.

Output 2 can be disabled by TTL input.

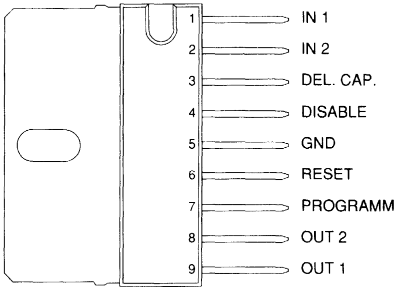
Short circuit and thermal protections are included.

BLOCK DIAGRAM



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1, 2	20	V
V_{DIS}	Disable Input Voltage Pin 4	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1,2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	– 65 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C

THERMAL DATA

$R_{TH(j-c)}$	Maximum Thermal Resistance Junction-case	8	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 7V ; T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	2.5		16	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA			1.4	V
		$I_{O1,2}$ = 1A			2	V
V_{O1}	Line Regulation	7V < V_{IN1} < 14V 12V < V_{IN2} < 18V @ V_{O2} : 10V $I_{O1,2}$ = 200mA			50	mV
V_{O2}	Line Regulation				100	mV
V_{O1}	Load Regulation	5mA < $I_{O1,2}$ < 0.6A @ V_{O2} = 10 V			100	mV
V_{O2}	Load Regulation				200	mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Threshold Voltage	(K = V_{O1})	K – 0.4	K – .25	K – 0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see note 1)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	C_e = 100nF (see note 1)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current at Pin 5 in Normal Condition	V_5 = 10V			10	µA
$V_{O1,2}/T$	Output Volt. Thermal Drift			100		ppm/°C
$I_{O1,2\,sc}$	Short Circ. Ouput Current	V_{IN} = 7V			1.6	A
		V_{IN} = 18V (see note 2)			0.7	A
V_{DISH}	Disable Volt. at Pin 4 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 4 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 4	0V < V_{DIS} < 7V	– 100		2	µA
V_{ref}	Pin 7			2.5		V
T_{jsd}	Junction Temp. for Thermal Shut Down			145		°C

Notes : 1. If the output voltage OUT 1 goes below 4.85V (V_{OUT} - 0.25V) the comparator "a" (see fig 1) discharges rapidly the capacitor Ce and the Reset output (pin 5) goes at once LOW.
When the voltage at the OUT 1 rises above 4.9V, the voltage at pin 2 increases with this law ;

$$t_d = \frac{Ce \,.\, 2.5V}{10\mu A} \quad \text{(see fig. 2)}$$

as V_2 reach 2.5V the Reset output (pin 5) goes HIGH again. To avoid glitches in the Reset output the second comparator "b" has a large hysteresis (1.9V).

2. The output short circuit currents are tested one channel at time.
During a short circuit a large consumption of power occurs, anyway the thermal protection circuit guarantees the temperature not overcomes high value.

Figure 1.

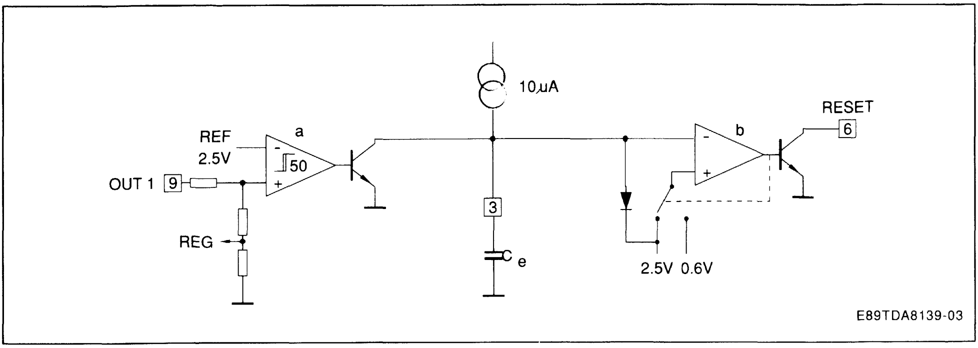
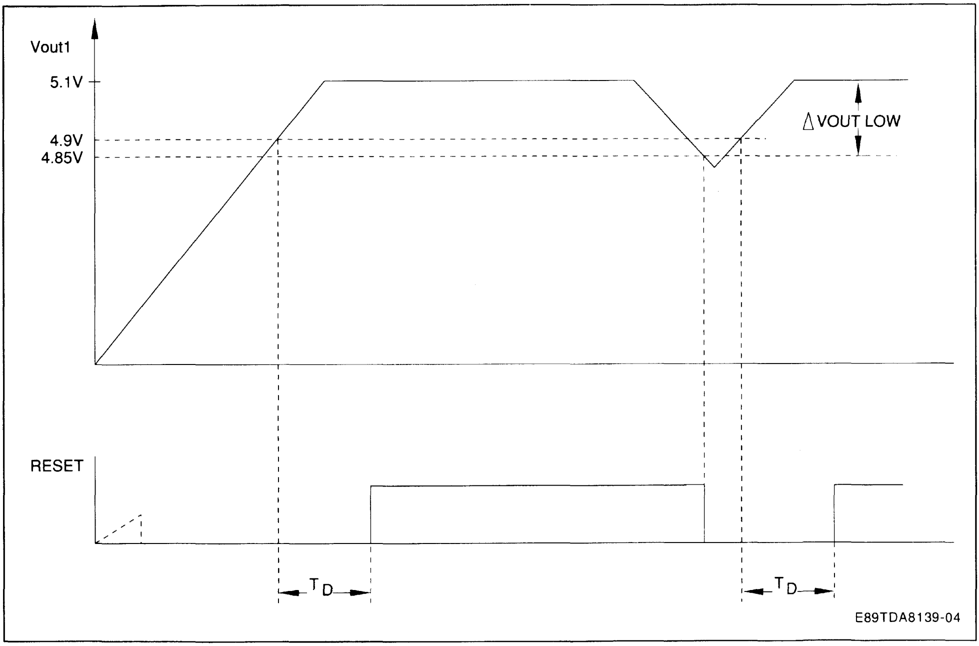
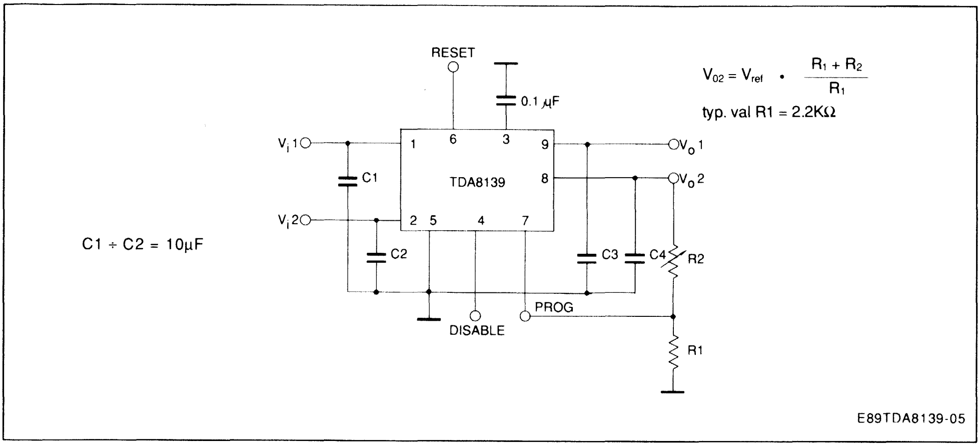


Figure 2.



TYPICAL APPLICATION CIRCUIT



CIRCUIT DESCRIPTION

The TDA8139 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.

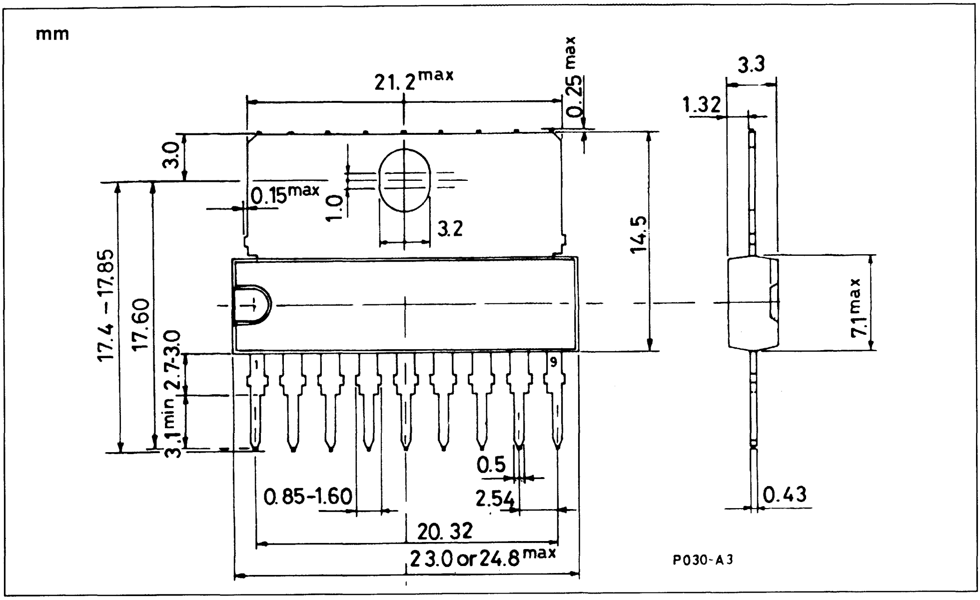
The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 4.

The Reset circuit controls the voltage at the output 1, if this one decrease below 4.85V provides to generate a reset pulse at pin 6 (open collector) with a certain delay depending by an external capacitor connected at pin 3.

PACKAGE MECHANICAL DATA

9 PINS – PLASTIC SIP



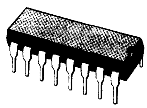
HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH ON THE OUTPUT

DESCRIPTION

The TDA 8140 is a monolithic integrated circuit designed to drive the horizontal deflection power transistor.

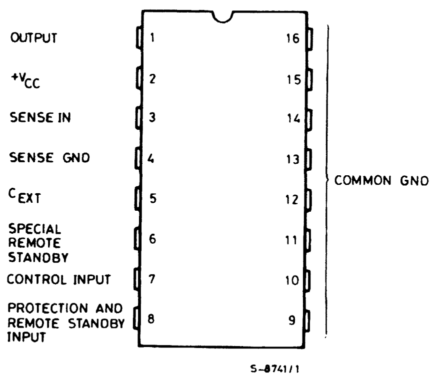
The current source characteristic of this device is adapted to the on-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA 8140 is internally protected against short circuit and thermal overload.



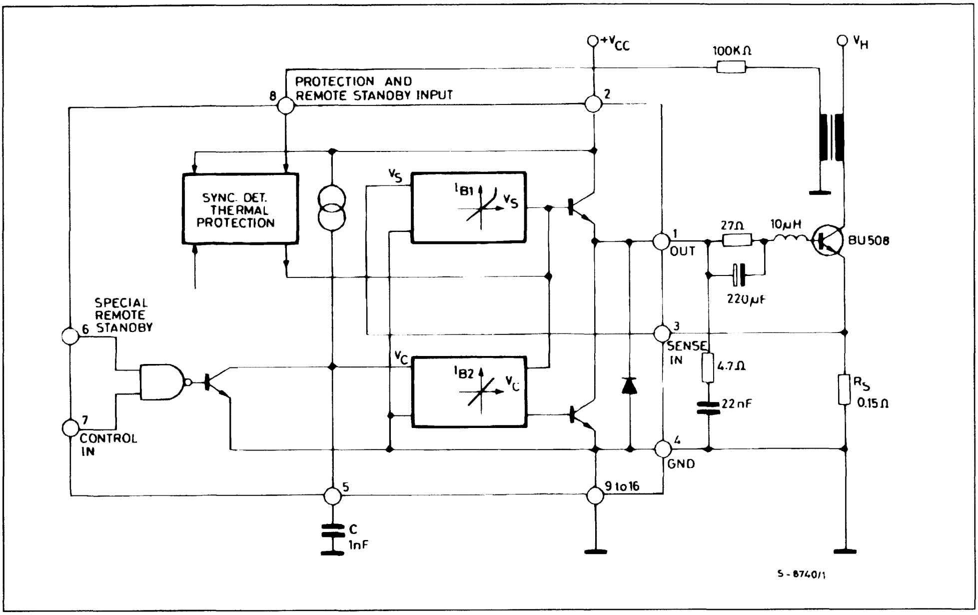
POWERDIP
(8 + 8)

ORDER CODE : TDA8140

CONNECTION DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	– 40 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	15	°C/W

PIN FUNCTION

Pin	Name	Function
1	Output	Device Output
2	V_{CC}	Supply Voltage
3	Sense Input	Input voltage that determines output current.
4	Sense GND	Reference Ground for Input Voltage at Sense Input
5	C_{EXT}	Capacitor between this terminal and Sense Ground determines the current slope dI_o/d_t during off phase.
6	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from control input (2nd priority) (in standard applications pin 6 must be left unconnected).
7	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
8	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).
9-16	Power Ground	Common Ground

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{po}	Positive Output Current (source)		1.5			A
I_{no}	Negative Output Current (sink)		2			A
I_{oo}	Positive quiescent output current forcing the output to 6 V and the sense input to ground output externally forced to 6 V.	Remote Input 1 Remote Input 0	120 50	150 80	200 100	mA mA
g_{ON}	Transconductance ON Phase	Remote Input 1	1.8	2.0	2.2	A/V
g_{OFF}	Transconductance OFF Phase	Remote Input 1	1.8	2.0	2.2	A/V
g_{REMOTE}	Transconductance Standby Mode	Remote Input 0	0.675	0.75	0.825	A/V
I_5	Current Source Pin 5	V_6 = 500 mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	$V_S = 0$ Remote Input = 1	– 200	– 300	– 400	µA
R_{SYN}	Synchronous Detection Input Resistance	$V_{SYN} < 7$ V $V_{SYN} > 7$ V	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	Sync Detect Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA} + 0.5$ V	– 50 - 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{INB}	Pull up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB} + 0.5$ V	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time 1)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
$V_{CC}–V_{OUT}$	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_0 \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage 2)		0.8	0.9	1	V

Notes : 1. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
2. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_0 is going to the positive quiescent current I_{00}.

TRUTH TABLE

Logic Inputs		Output I_o		Mode
Control Input	Remote/Standby			
0 Floating or 1	Floating or 1 Floating or 1	$I_o > 0$ $I_o < 0$ 3)	BU508 ON BU508 OFF	Normal Function
X	0	$I_o < 0$ 3) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_o > 0$ $t > td_r$	BU508 ON	

3) $I_O < 0$ means that the sink current flows into the output to ground.

Figure 1 : Large Screen Application.

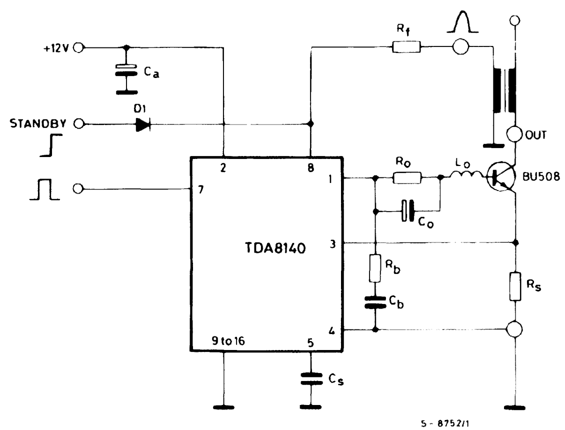
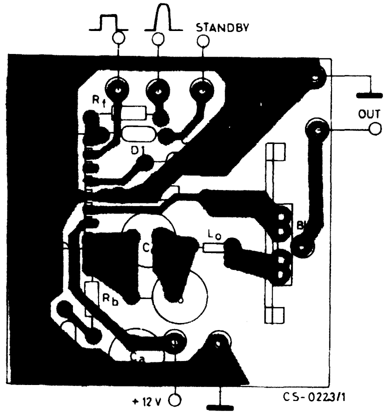


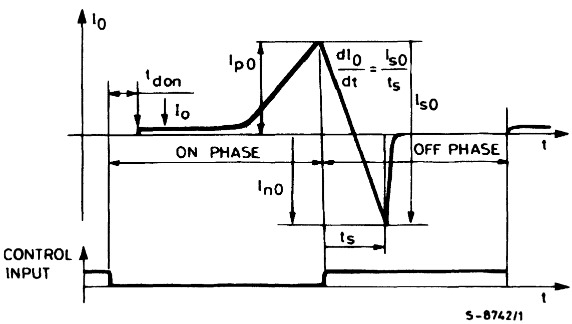
Figure 2 : P.C. Board and Components Layout of the Fig. 1 (1 : 1 scale).



COMPONENTS LIST FOR TYPICAL APPLICATION

CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 μF	47 μF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 μF	220 μF	R_s	0.15 Ω	0.1 Ω
L_o	10 μH	10 μH	C_s	1 nF	1 nF

Figure 3.



APPLICATION INFORMATION

The conventional deflection system is shown in fig. 4 the driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

During the active deflection phase the collector current of the power transistor is linear rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.

According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in fig. 5 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.

The marked area represents a useless base current which gives an additional power dissipation on the power transistor.

Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the conventional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.

The new approach, using the TDA 8140, overcomes these restrictions by means of a feedback principle.

As shown in fig. 5, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_s at the emitter of the power transistor and delivers :

$$I_b = R_S \cdot g_m \cdot I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1+\beta min} \cdot \frac{1}{R_S} < gm < \frac{1}{R_S}$$

Where β_{min} is the minimum current gain of the transistor. This method always ensures the correct base current and acts time independent on principle.

For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in fig. 3.

Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.

This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.

As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 4 : Conventional Horizontal Deflection System For TVs.

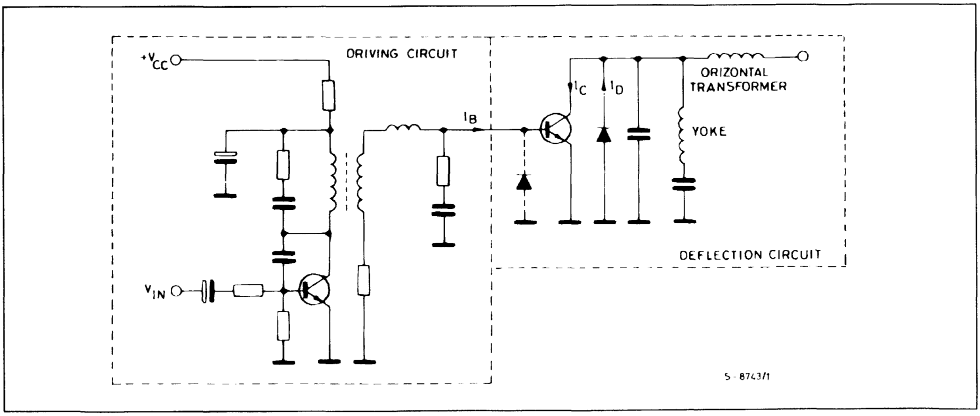
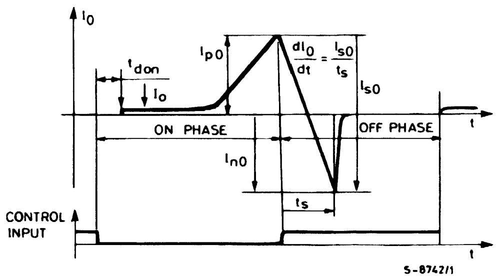


Figure 5 : Waveforms of Collector and Base Current.



CIRCUIT DESCRIPTION

Fig. 6 show the block diagram of the TDA 8140, the circuit consists of an input traansconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2 A sink current and 2 A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \cdot \frac{1}{R5}$$

A current source I_1 generates a drop of 70 mV across the resistor R4 which provides an output bias current of 140 mA ; the control input determines the turn ON/OFF function.

In the ON phase, Q5 shorts the external capacitor C_t, within the input voltage range $0 < V_{in} < 750$ mV the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750 mV, Q7 limits the maximum output current at 1.5 A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linear and the system stability is reached.

During the flyback phase, the IC is enabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

In fig. 7 is shown the application diagram of the TDA 8140, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in fig. 4.

In fig. 5 is shown the currents and voltages waveforms of the driver circuit of fig. 7, as to be seen, the driving charge $I_b \cdot t_{on}$ has been reduced at minimum.

The power dissipation on this application condition is about 1.3 W and fig. 9 and 10 show two ways of heatsinking.

In the first case, a PCB copper area is used as a heatsink L= 65 mm while in the second case, the device is soldered to an external heatsink ; in both examples, the thermal resistance junction ambient is 35 °C/W.

The presence of thermal shut-down circuit does mean that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply switched-OFF the device.

Figure 6 : Block Diagram of the Integrated Horizontal Driver.

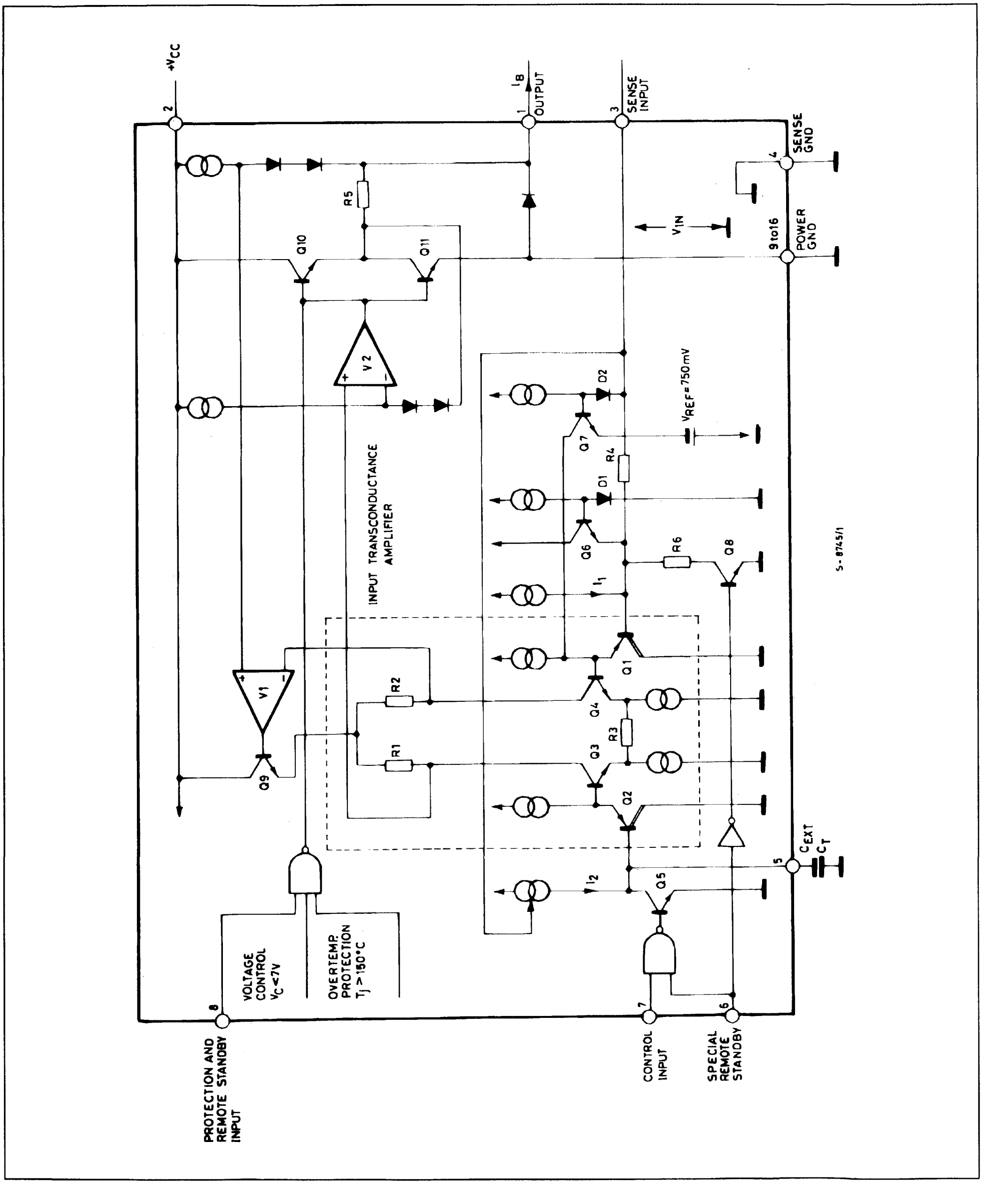


Figure 7 : Integrated Horizontal Driver.

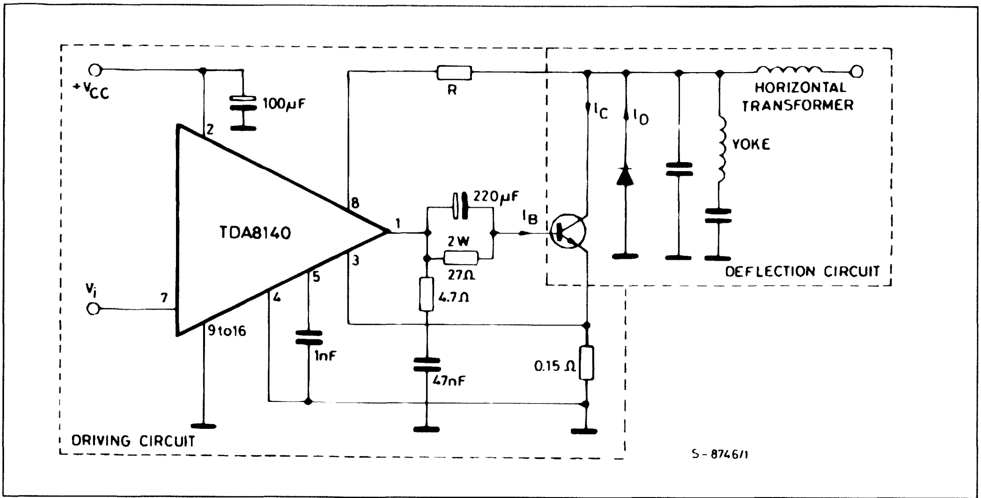
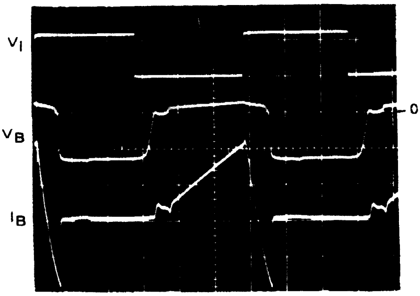
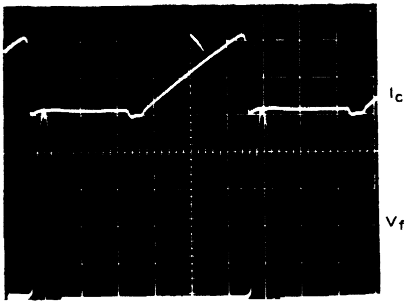


Figure 8 : Signal Diagrams of the Driver Circuits.



V_i = 10V/cm; V_B = 5V/cm; I_B = 0.5A/cm.



I_C = 1.5A/cm

Figure 9 : Example of Heatsink Using P.C Board Copper (L = 65 mm).

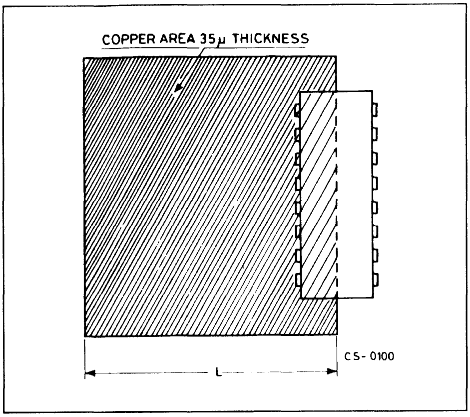
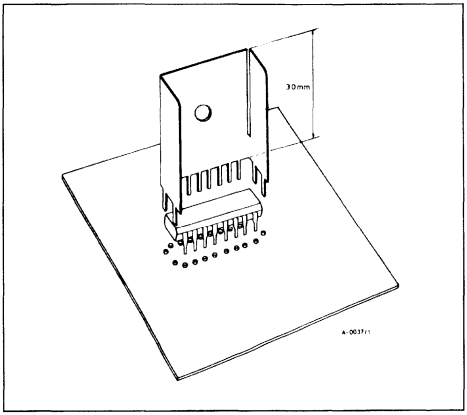


Figure 10 : Example of an External Heatsink.



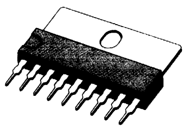
HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH ON THE OUTPUT

DESCRIPTION

The TDA8143 is a monolithic integrated circuit designed to drive the horizontal deflection power transistor.

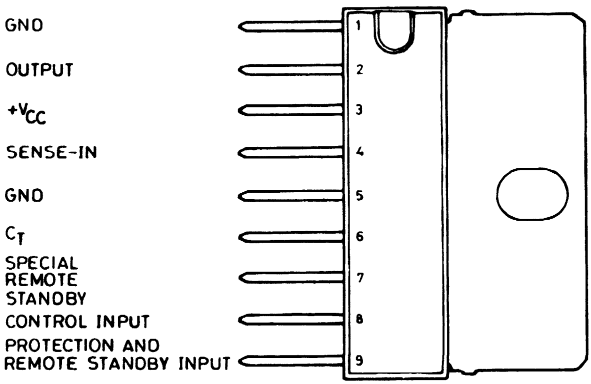
The current source characteristic of this device is adapted to the non-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA8143 is internally protected against short circuits and thermal overload.



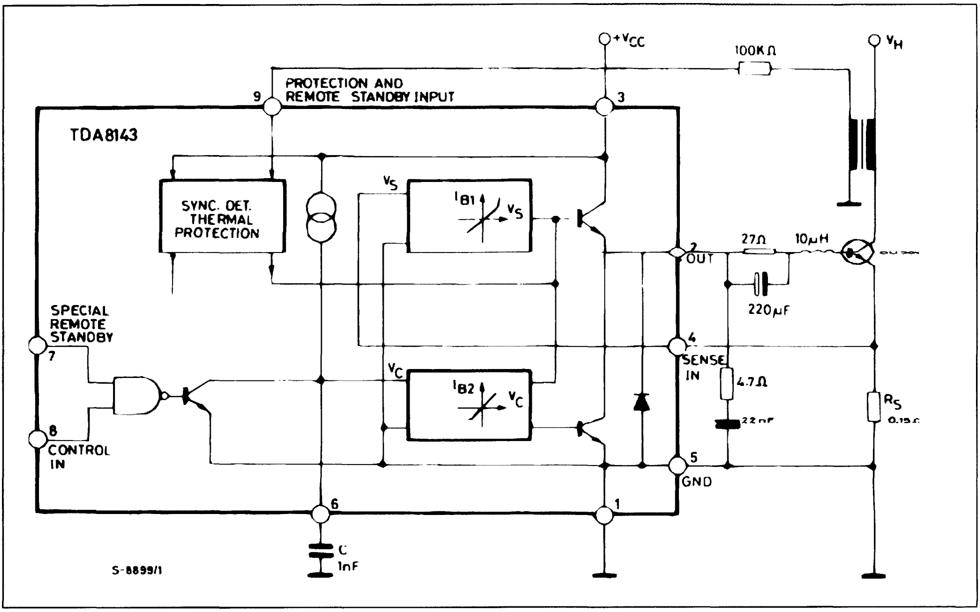
SIP 9

ORDER CODE : TDA8143

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	– 40 to 150	°C
T_{op}	Operating Temperature	0 to 70	°C

THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W
$R_{th\ j-case}$	Thermal Resistance Junction–case	Max	15	°C/W

PIN FUNCTIONS

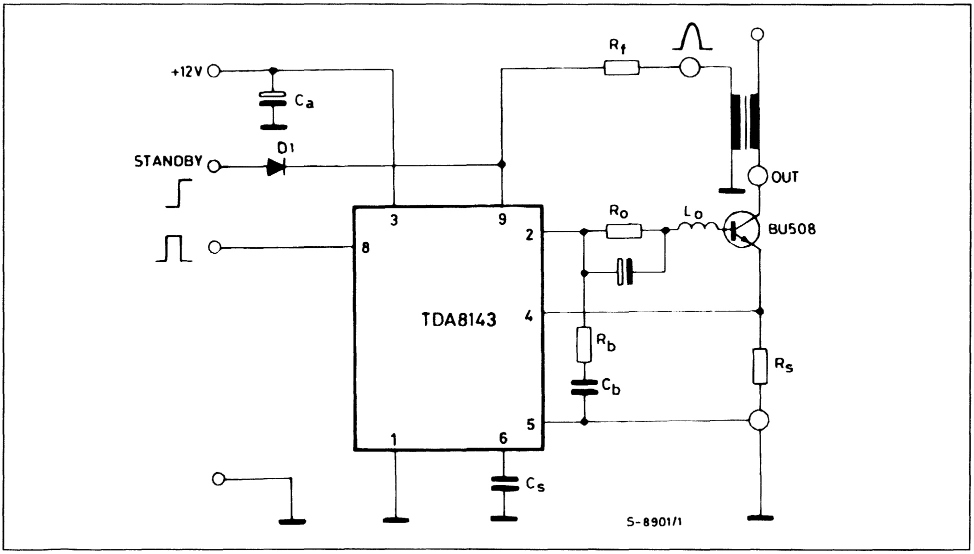
Pin	Name	Function
1	Power Ground	Common Ground
2	Ouptut	Device Output
3	V_{CC}	Supply Voltage
4	Sense Input	Input voltage that determines output current.
5	Sense GND	Reference Ground for Input Voltage at SENSE INPUT.
6	C_{EXT}	Capacitor between this terminal and SENSE GROUND determines the current slope dI_O/dt during OFF phase.
7	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from CONTROL INPUT (2nd priority).
8	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
9	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).

TRUTH TABLE

Logics Inputs		Output I_0		Mode
Control Input	Remote/Standby			
0 Floating or 1	Floating or 1 Floating or 1	$I_0 > 0$ $I_0 < 0$ 3)	BU508 ON BU508 OFF	Normal Function
X	0	$I_0 < 0$ 3) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_0 > 0$ $t > t_{dr}$	BU508 ON	Remote/Standby Function

3) $I_0 < 0$ means that the sink current flows into the output to ground.

Figure 1 : Large Screen Application.



ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_{amb} = 25 °C unless otherwise specified)

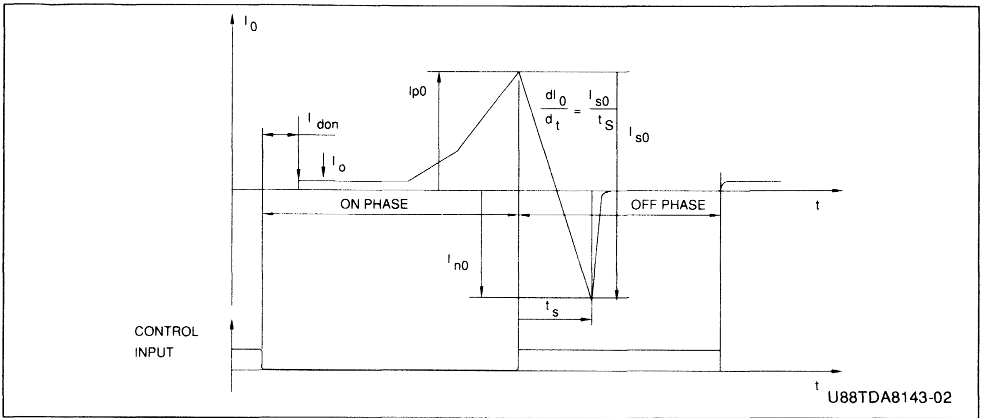
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{p0}	Positive Output Current (source)		1.5			A
I_{n0}	Negative Output Current (sink)		2			A
I_{o0}	Positive quiescent output current forcing the output to 6 V and the sense input to ground output externally forced to 6 V.	Remote Input 1 Remote Input 0	120 50	150 80	200 100	mA mA
g_{ON}	Transconductance ON Phase	Remote Input 1	1.8	2.0	2.2	A/V
g_{OFF}	Transconductance OFF Phase	Remote Input 1	1.8	2.0	2.2	
g_{REMOTE}	Transconductance Standby Mode	Remote Input 0	0.675	0.75	0.825	
I_5	Current Source Pin 5	V_6 = 500 mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	$V_S = 0$ Remote Input = 1	– 200	– 300	– 400	µA
R_{SYN}	Synchronous Detection Input Resistance	$V_{SYN} < 7$ V $V_{SYN} > 7$ V	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	SYNC DETECT Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA} + 0.5$ V	– 50 – 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V
I_{INB}	Pull-up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB} + 0.5$ V	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time 1)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
$V_{CC}–V_{OUT}$	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_0 \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage 2)		0.8	0.9	1	V

Notes : 1. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
2. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g. V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_0 is going to the positive quiescent current I_{o0}.

COMPONENTS LIST FOR TYPICAL APPLICATION

CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 µF	47 µF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 µF	220 µF	R_s	0.15 Ω	0.1 Ω
L_o	10 µH	10 µH	C_s	1 nF	1 nF

Figure 2.



APPLICATION INFORMATION

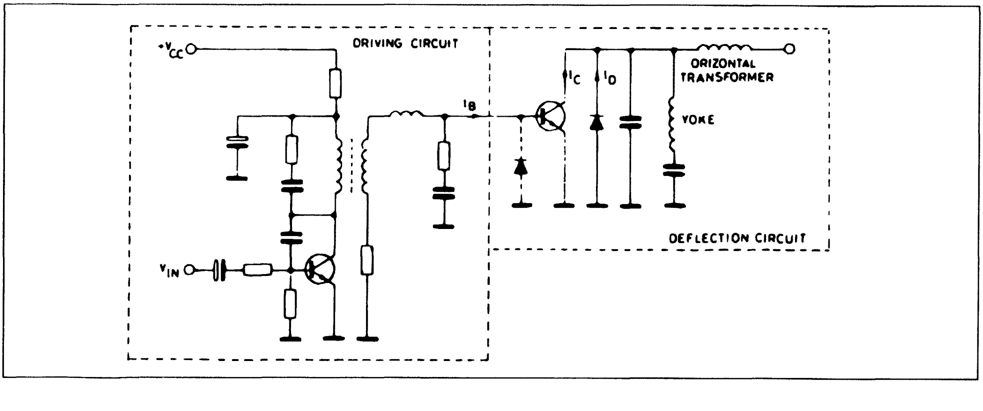
The conventional deflection system is shown in fig. 3 the driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

During the active deflection phase the collector current of the power transistor is linear rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.

According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in fig. 4 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.

The marked area represents a useless base current which gives an additional power dissipation on the power transistor.

Figure 3 : Conventional Horizontal Deflection System for TVs.



Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the convenctional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.

The new approach, using the TDA 8143, overcomes these restrictions by means of a feedback principle.

As shown in fig. 4, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_S at the emitter of the power transistor and delivers :

$$I_b = R_S \cdot g_m \cdot I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1 + \beta_{min}} \cdot \frac{1}{R_S} < g_m < \frac{1}{R_S}$$

where β is the minimum current gain of the transistor. This method always ensures the correct base current and acts time independent on principle.

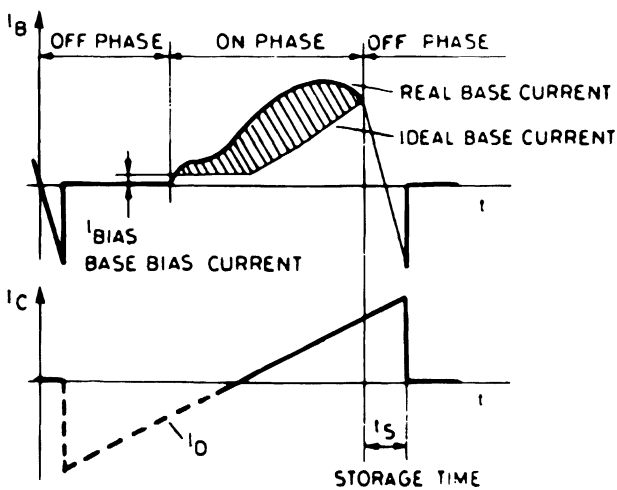
For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in fig. 2.

Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.

This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.

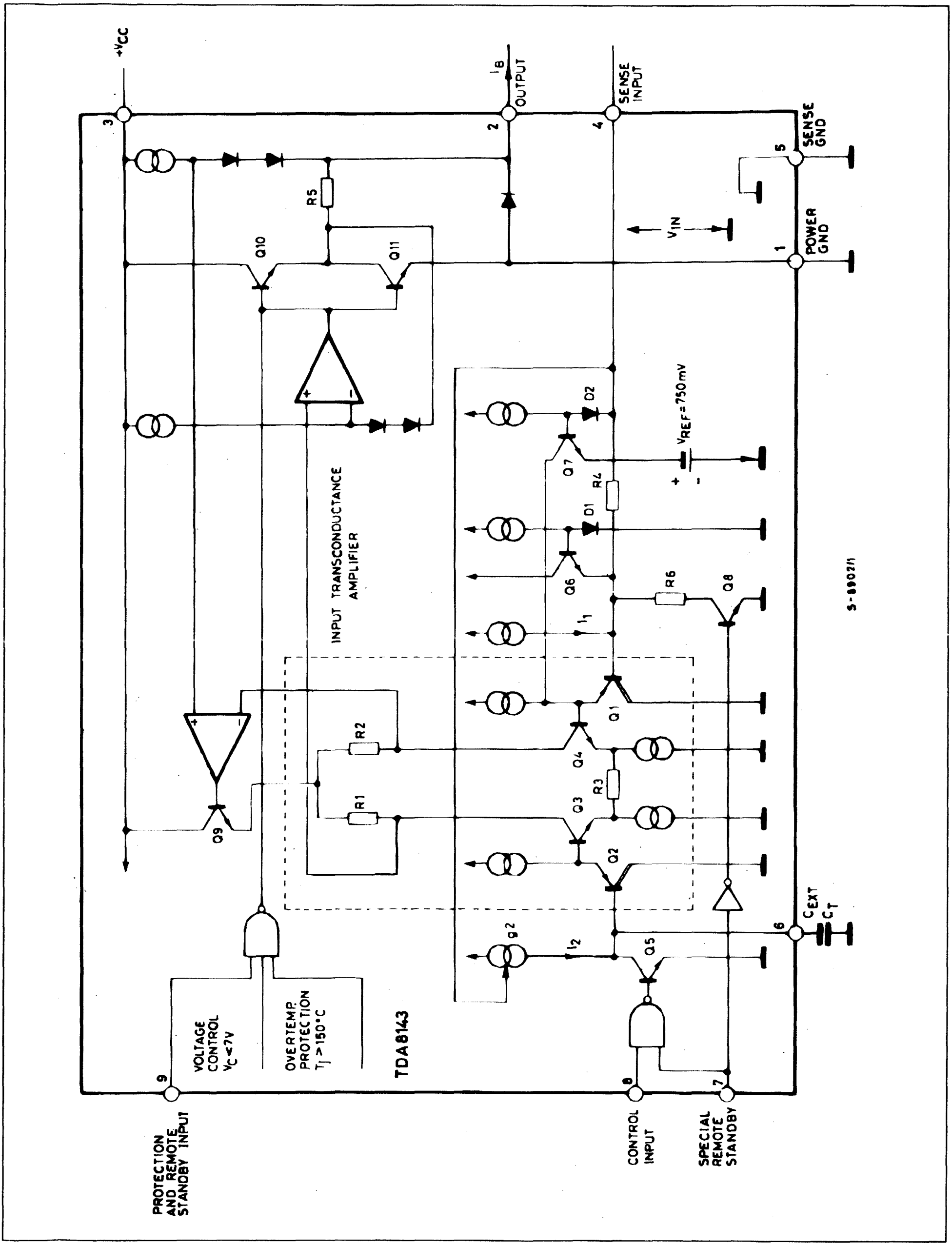
As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 4 : Waveforms of Collector and Base Current.



CIRCUIT DESCRIPTION

Figure 5 : Block Diagram of the Integrated Horizontal Driver.



CIRCUIT DESCRIPTION

Fig. 5 show the block diagram of the TDA 8143, the circuit consists of an input transconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2 A sink current and 2 A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \quad \frac{1}{R5}$$

A current source I_1 generates a drop of 70 mV across the resistor R4 which provides an output bias current of 140 mA ; the control input determines the turn ON/OFF function.

In the ON phase, Q5 shorts the external capacitor C_t, within the input voltage range $0 < V_{in} < 750$ mV the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750 mV, Q7 limits the maximum output current at 1.5 A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linear and the system stability is reached.

During the flyback phase, the IC is enabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

In fig. 6 is shown the application diagram of the TDA 8143, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in fig. 1.

In fig. 4 is shown the currents and voltage waveforms of the driver circuit of fig. 6 as to be seen, the driving charge $I_b \cdot t_{on}$ has been reduced at minimum.

The power dissipation on this application condition is about 1.3 W.

The presence of thermal shut-down circuit does means that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

If for any reason, the junction temperature increases up to 150 °C, the thermal shut-down simply switched-OFF the device.

Figure 6 : Integrated Horizontal Driver.

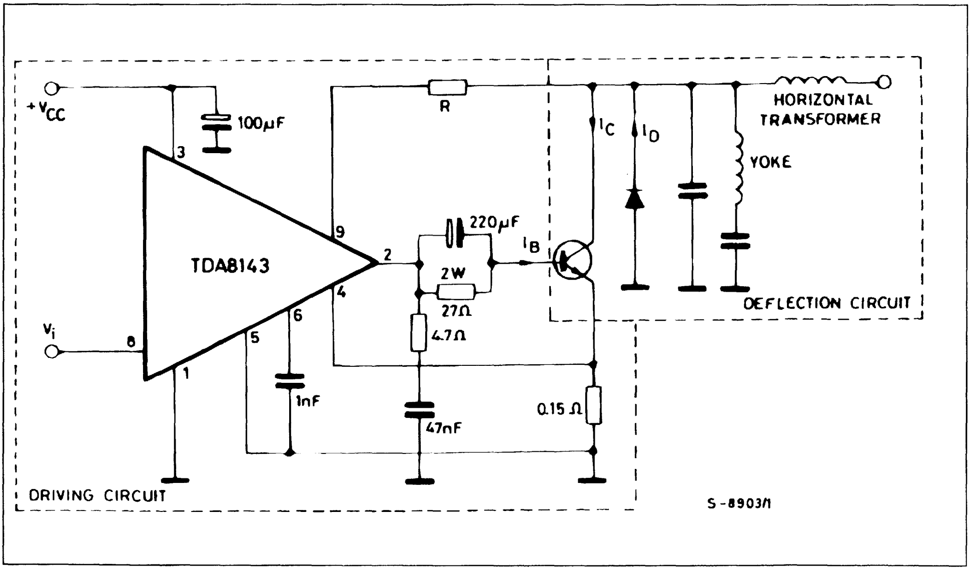
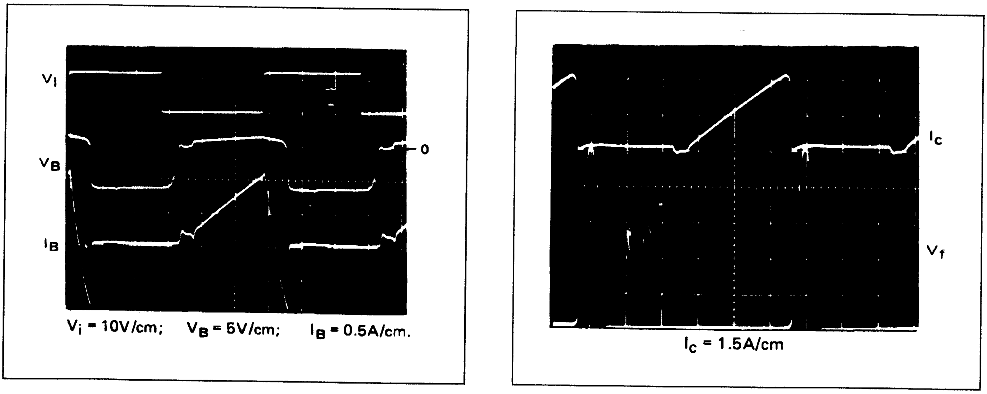


Figure 8 : Signal Diagrams of the Driver Circuits.



SGS-THOMSON MICROELECTRONICS

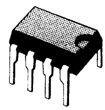
TDA8145

TV EAST/WEST CORRECTION CIRCUIT FOR SQUARE TUBES

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT SPECIALLY DESIGNED FOR SQUARE C.R.T. CORRECTION
- EXTERNAL KEYSTONE ADJUSTMENT (symmetry of the parabola)
- INPUT FOR DYNAMIC FIELD CORRECTION (beam current change)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY REDELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAWTOOTH

DESCRIPTION

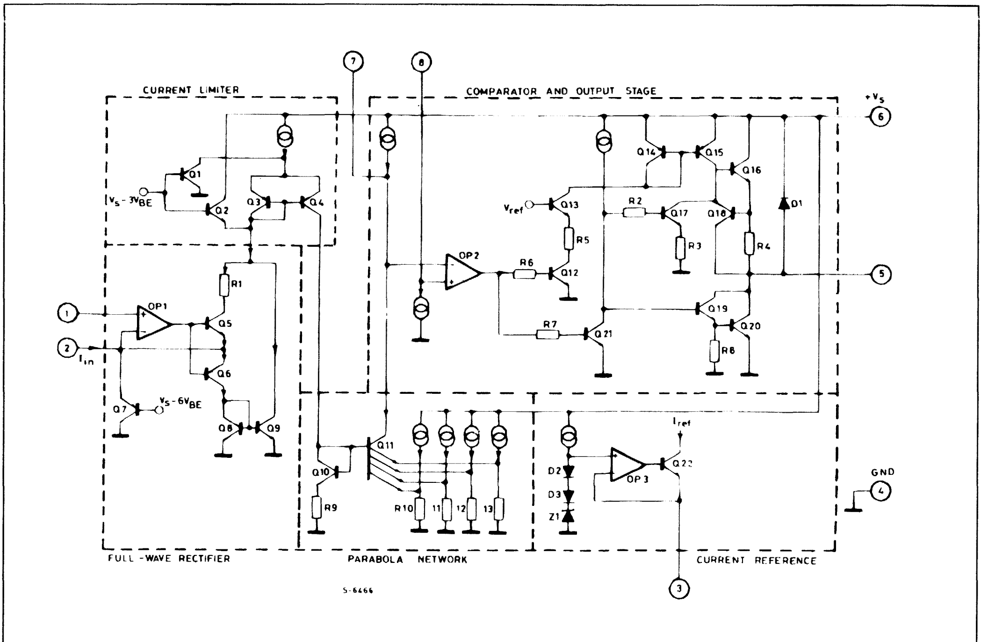
The TDA8145 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the square C.R.T. east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.



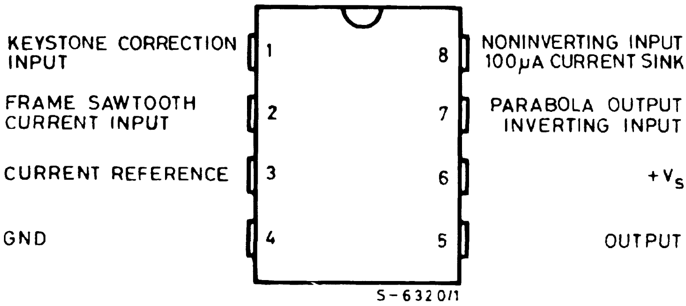
MINIDIP

ORDER CODE : TDA8145

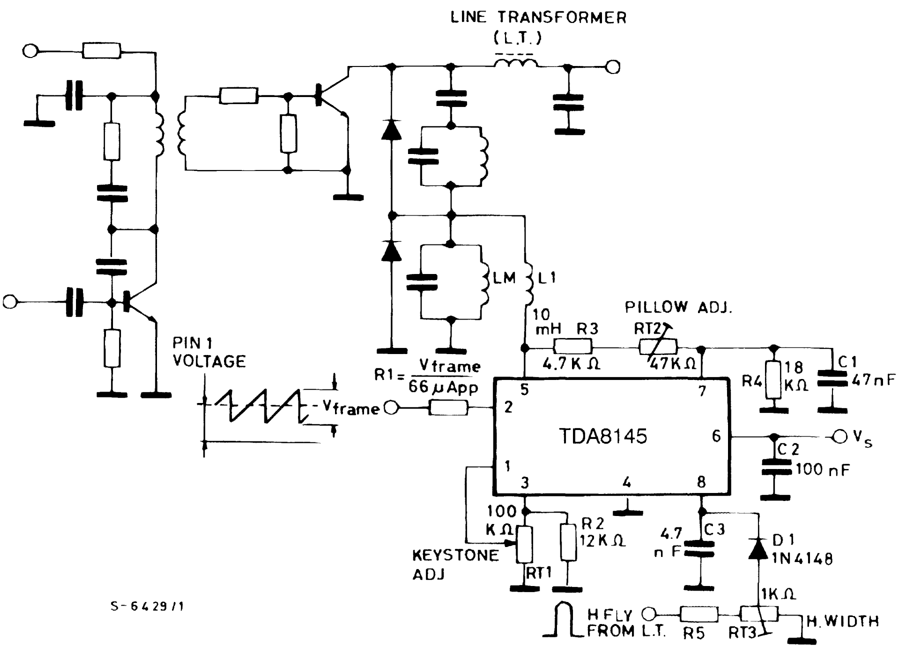
SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (top view)



APPLICATION CIRCUIT WITH KEYSTONE CORRECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	35	V
I_s	Supply Current	500	mA
P_{tot}	Power Dissipation at T_{amb} = 50 °C	500	mW
T_{stg}, T_j	Storage and Junction Temperature	– 25 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction-ambient	Max	100	°C/W
$R_{th\ j-amb}$	Thermal Resistance Junction-pin 4	Max	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, V_s = 26 V, V_{fr} = 0, S1 and S2 in "a" position, refer to the test circuit unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		17	24	30	V
I_S	Supply Current			4.5	7	mA
V_{ref}	Internal Reference Voltage		7.6	8.0	8.8	V
$-I_{ref}$	Internal Reference Current	V_{ref}/R3		0.73		mA
$V_{7(A)}$ (*)	Pin 7 Output Voltage	I_{fr} = 0 µA	15.3	16.0	16.7	V
$V_{7(B)}$ (*)	Pin 7 Output Voltage	I_{fr} = 30 µA		15		V
K_1	Parabola Coefficient (*)	$K_1 = \frac{V_{7A} - V_{7B}}{V_{7A} - V_{7C}}$		0.26		V
K2	Parabola Coefficient (*)	$K_2 = \frac{V_{7A} - V_{7C}}{V_{7A} - V_{7D}}$		0.70		V
ΔV_7 (*)		$\Delta V_7 = V_{7E} - V_{7F}$	– 40		40	mV
I_8	Current Source	S1 → b		100		µA
V_{SATL}	Saturation Voltage	I_o = 400 mA Sink S2 → b		1	2	V
V_{SATH}	Saturation Voltage	I_o = 100 mA Source S2 → c S1 → b		0.8	1.5	V
V_F	Forward Voltage	I_o = 400 mA S2 → d S1 → b		1.2	1.7	V
I_{fr}	Frame Sawtooth Current	V_{fr} = 6.6 V_{pp}		6.6		µA

* See fig.2.

Figure 1 : Test Circuit.

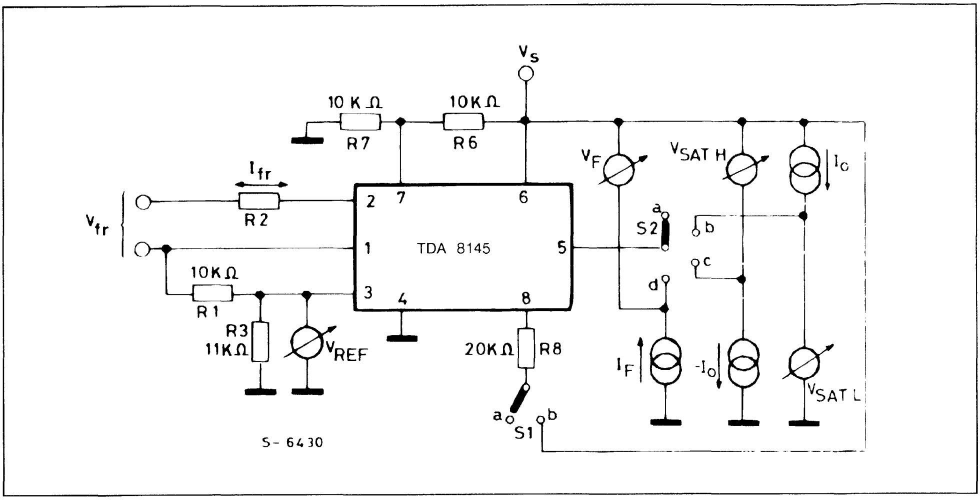
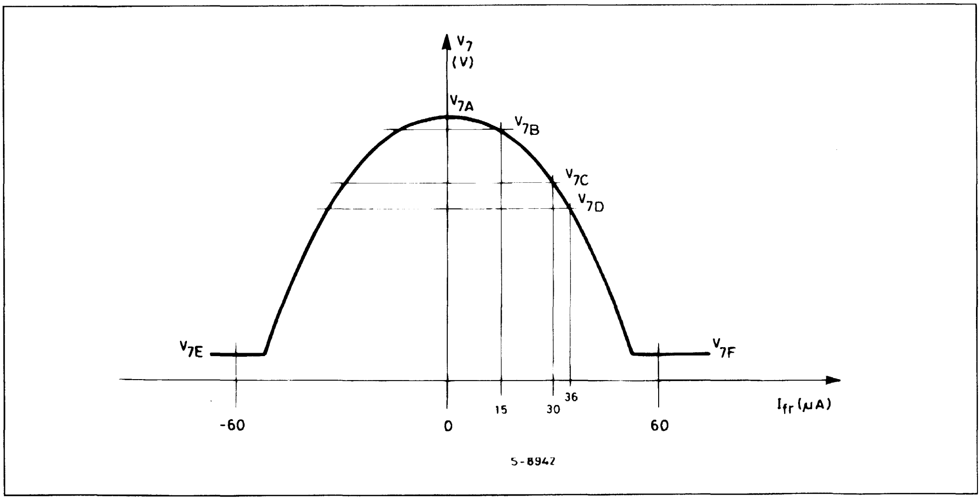


Figure 2 : Parabola Characteristics.



CIRCUIT OPERATION (see the schematic diagram).

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of ± 33μA which is produced via an external resistor from the sawtooth voltage. The non–inverting input of this amplifier is connected with a reference voltage corresponding to the DC level of the sawtooth voltage. This DC vol tage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current.

This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

If the input is overmodulated (> 40μA) the internal current is limited to 40μA. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

The horizontal frequency pulse–width modulated output signal drives the final stage. It consists of a class D push–pull output amplifier that drives, via an external inductor, the diode modulator.

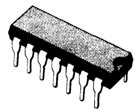
SGS-THOMSON MICROELECTRONICS

TDA8146

EAST/WEST CORRECTION FOR RECTANGULAR TV-TUBES

ADVANCE DATA

- LOW POWER DISSIPATION
- PULSE WIDTH MODULATOR FOR SWITCH MODE OPERATION
- OUTPUT SINK CURRENT UP TO 800mA
- OUTPUT SOURCE CURRENT UP TO 100mA
- PARASITIC PARABOLA SUPPRESSION DURING VERTICAL FLYBACK
- VERTICAL CURRENT SENSE INPUTS GROUND COMPATIBLE
- PROGRAMMABLE PARABOLA CURRENT GENERATOR FOR DIFFERENT TV-TUBES
- EXTERNAL KEYSTONE ADJUSTMENT



DIP 14
(Plastic Package)

ORDER CODE : TDA8146

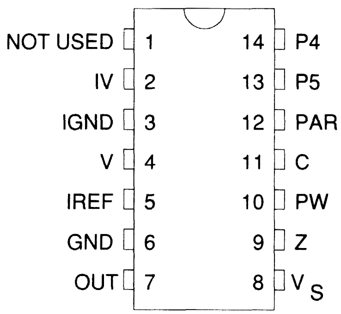
DESCRIPTION

The TDA8146 is a monolithic integrated circuit in a 14 pin dual-in-line plastic package.

The TDA8146 is designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

Since the parabola current generator is programmable the device can operate with different CRTs.

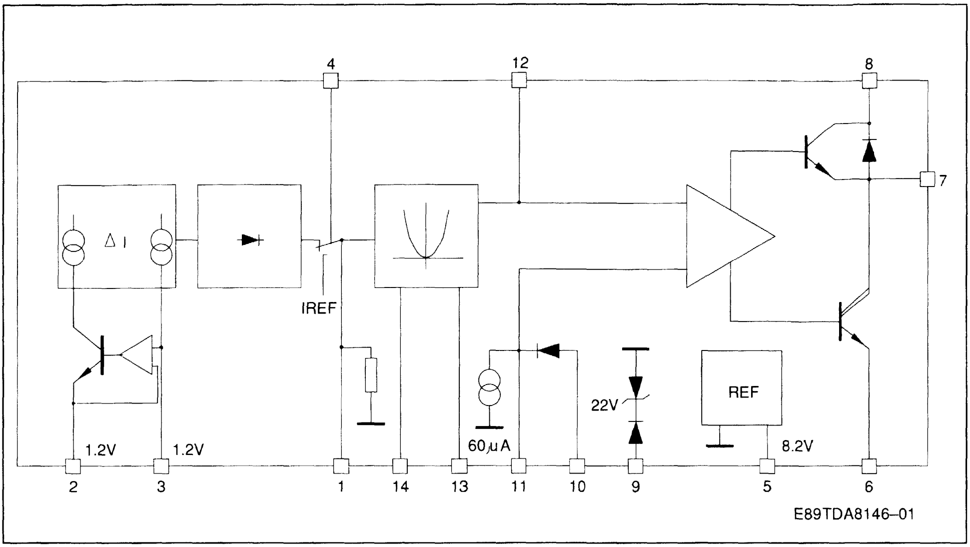
PIN CONNECTIONS



E89TDA8146–02

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_7	Output Sink Current	800	mA
I_7	Output Source Current	100	mA
V_S	Supply Voltage	28	V
V_4	Vertical Flyback Input Voltage	– 0.3 to 60	V
V_{10}	Input Voltage at Pin 10	– 10 to V_S	V
V_9	Input Voltage at Pin 9	– 10 to 20	V
V_{in}	Input Voltage at all other Pins	– 0.3 to V_S	V
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

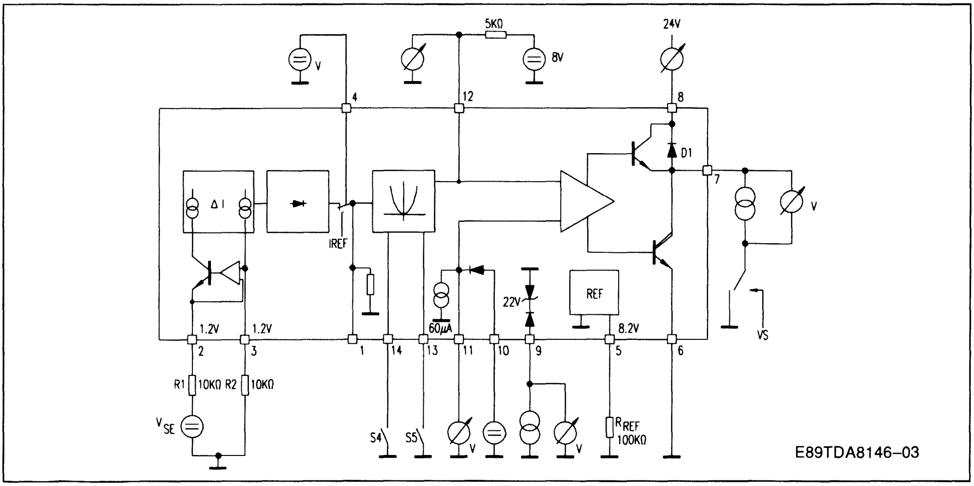
THERMAL DATA

$R_{thJ\text{-}amb}$	Junction-ambient Thermal Resistance	Max	80	°C/W

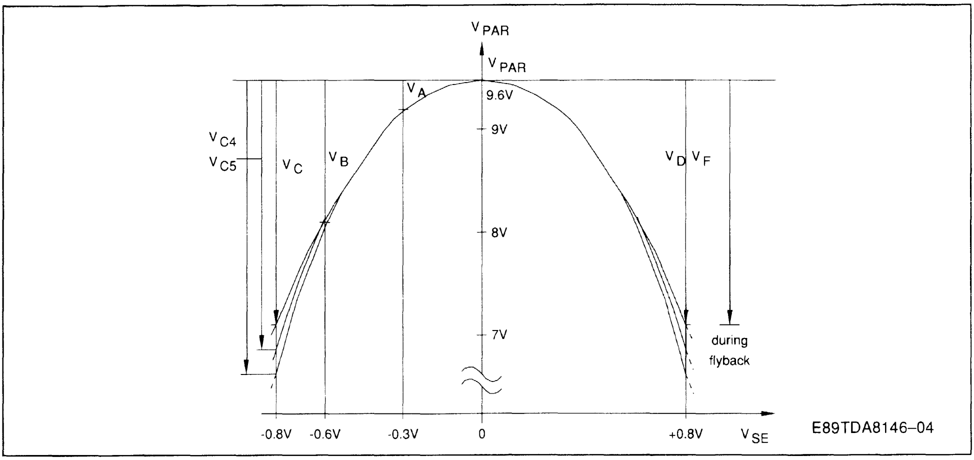
ELECTRICAL CHARACTERISTICS
(refer to test circuit V_S = 24V, T_j = 25°C ; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		15	24	26	V
I_S	Supply Current	V_{out} = LOW		4	7	mA
V_5	Reference Voltage			8.2		V
V_{7L}	Saturation Voltage	I_O = 800mA Sink		1.2	2	V
V_{SAT}	Diode Forward Voltage	I_O = – 800mA		1.1	1.7	V
V_{7H}	Saturation Voltage	I_O = 100mA Source		0.8	1.25	V
I_{11}	Current Sink Pin 11		40	60	80	μA
V_9	Zener Voltage	I_9 = 5mA	20	22	24	V
V_{4T}	Vertical Blanking Threshold Voltage		V_S – 0.5	V_S	V_S + 0.5	V
I_4	Vertical Blanking Input Current	V_4 = 50V	25	50	100	μA
V_2	Reference Voltage at Pin 2	R1 = R2 = 10K		1.3		V
V_3	Reference Voltage at Pin 3			1.3		V
V_{PARO}	Parabola Voltage at Pin 12	$\Delta V_{SE} = 0$		9.7		V
V_C	Parabola Voltage at Pin 12	$\Delta V_{SE} = +0.8V$		7.05		V
K_A	Parabola Coefficient	$K_A = \frac{VA}{VB}$		0.25		
K_C	Parabola Coefficient	$K_C = \frac{VC}{VB}$		1.75		
K_5	Parabola Coefficient	$K_5 = \frac{VC5}{VC}$; S4 or S5 Closed		1.07		
K_4	Parabola Coefficient	$K_4 = \frac{VC4}{VC}$; S4 + S5 Closed		1.17		
K_S	Parabola Symmetry	$K_S = \frac{VC}{VD}$	0.94	1.0	1.06	
K_F	Flyback Coefficient	$K_F = \frac{VC}{VF}$; V4 = 15V		1.0		

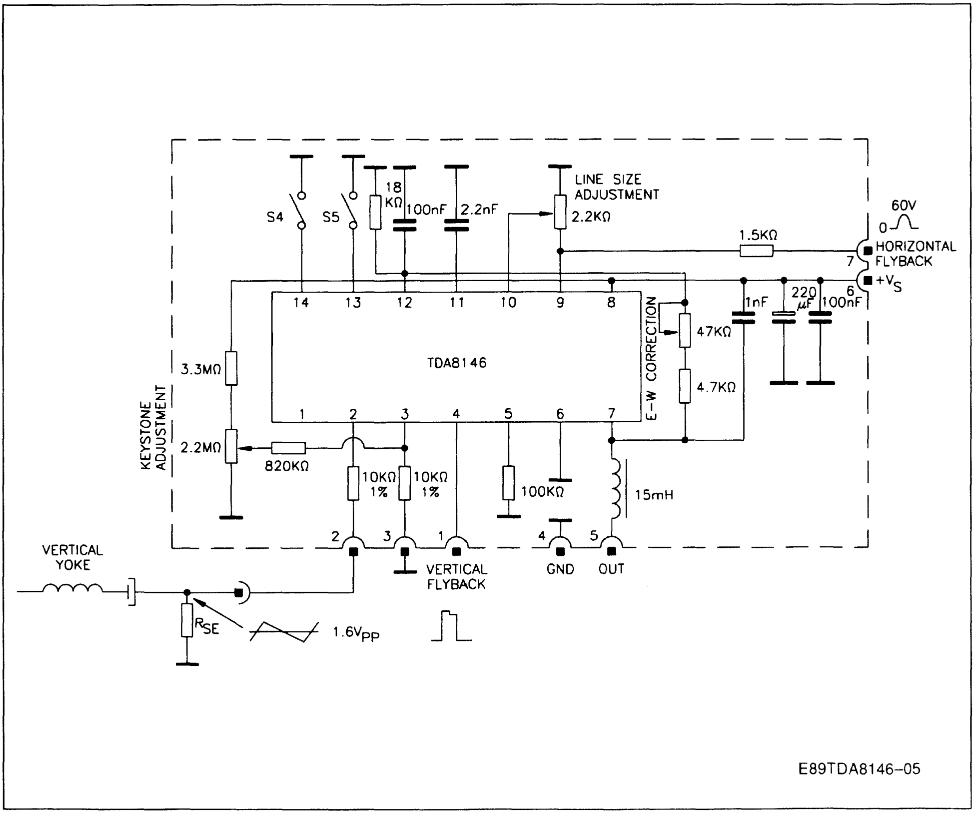
TEST CIRCUIT



PARABOLA CHARACTERISTICS



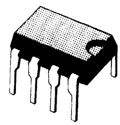
APPLICATION DIAGRAM



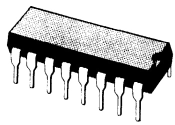
EAST/WEST CORRECTION FOR DIGITAL TV-SETS

ADVANCE DATA

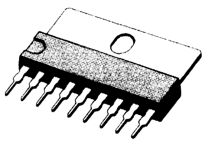
- LOW POWER DISSIPATION
- PULSE WIDTH MODULATOR FOR SWITCH MODE OPERATION
- OUTPUT SINK CURRENT UP TO 800mA
- OUTPUT SOURCE CURRENT UP TO 100mA
- HIGH IMPEDANCE INPUT AMPLIFIER



Minidip



Powerdip
8 + 8



SIP.9

ORDER CODES :		
	Powerdip	TDA8147
	Minidip	TDA8147M
	Sip.9	TDA8147S

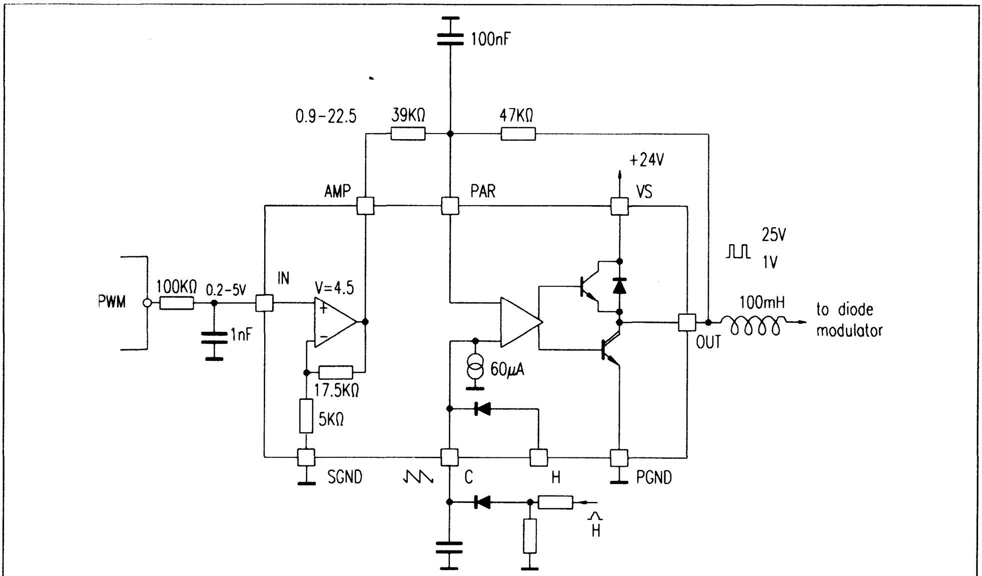
DESCRIPTION

The TDA8147 is a monolithic integrated circuit available in three different packages : minidip, powerdip, SIP.

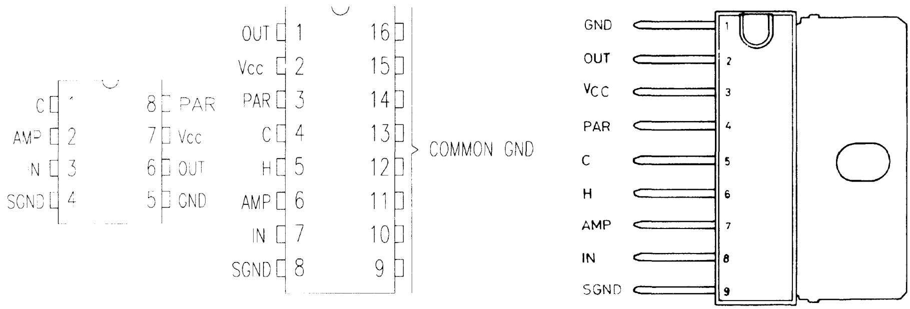
The TDA8147 is designed for use in the east-west pin-cushion correction by driving a diode modulator in TV application.

Since this device has not the parabole generator end is drived by a PWM, it is very useful in digital TV-sets.

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



MINIDIP

POWERDIP 8 + 8

SIP.9

ELECTRICAL CHARACTERISTICS

V_S = 24V, T_j = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		15	24	26	V
I_S	Supply Current	V_{out} = LOW		4	7	mA
V_{SATL}	Saturation Voltage	I_O = 800mA Sink		1.2	2	V
V_{DSAT}	Diode Forward Voltage	I_O = – 800mA		1.1	1.75	V
V_{SATH}	Saturation Voltage	I_O = 100mA Source		0.8	1.25	V
I_C	Current Sink Pin C		40	60	90	µA
I_{IN}	Input Current			0.1		µA
G	Opamp Gain		4.3	4.5	4.7	
V_O	Output Voltage Swing	I_{out} = ± 1mA	0.9		V_S – 1.5	V

ABSOLUTE MAXIMUM RATINGS

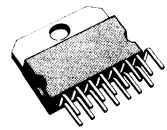
Symbol	Parameter	Value	Unit
I_{outL}	Output Sink Current	800	mA
I_{outH}	Output Source Current	100	mA
V_S	Supply Voltage	28	V
V_{IN}	Input Voltages	0.3 to V_S	V
P_{tot}	Power Dissipation at T_{amb} = 70°C	0.8 minidip 1.1 powerdip 1.1 SIP9	W W W
T_{stg}, T_j	Storage and Junction Temperature	– 25 to + 150	°C

THERMAL DATA

$R_{th(j\text{-}amb)}$	Minidip Powerdip SIP9	100 70 70	°C/W °C/W °C/W

RGB VIDEO OUTPUT AMPLIFIER

- THREE INDEPENDENT VIDEO AMPLIFIERS WITH TYPICAL SR > 1000V/μs
- CRT-CATHODE SENSING OUTPUT FOR SEQUENTIAL SAMPLING
- INTERNAL GI VOLTAGE GENERATOR
- CATHODE SHORT CIRCUIT PROTECTION
- FLASHOVER PROTECTION OF THE OUTPUT STAGES
- COMPENSATES POSITIVE AND NEGATIVE TUBE LEAKAGES



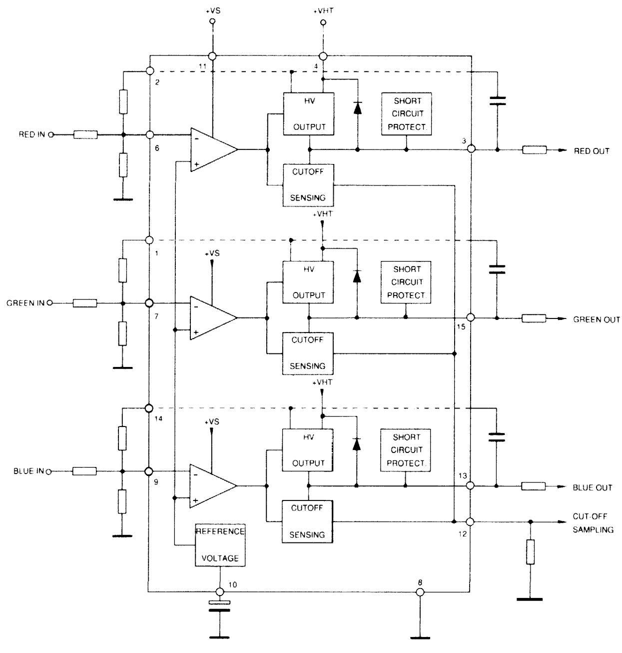
Multiwatt 15

ORDER CODE : TDA8153

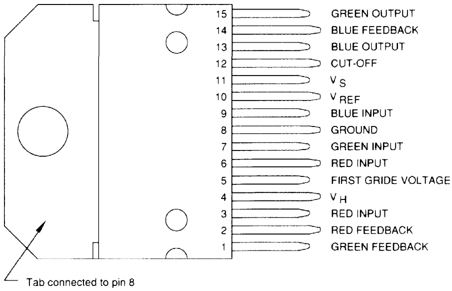
DESCRIPTION

Realized with a high voltage bipolar technology, the TDA8153 is a monolithic RGB video output stage for TV color applications. It drives the CRT cathodes directly and offers a video bandwidth compatible with CCIR standards. In addition to three independent video amplifiers, the device features an internal generator for the first grid voltage, flashover protection, cathode short circuit protection and a common cut-off sensing output for use in sequential sampling applications.

BLOCK DIAGRAM



PIN CONNECTIONS (top view)



ELECTRICAL CHARACTERISTICS (ref. to test and application circuits, V_{HT} = 200V, V_s = 12V, CL = 10pF *, heatsink Rth = 9°C/W, Tamb = 25°C unless otherwise specified).

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit	Fig.
V_{HT}	High Voltage Supply		4		200	220	V	1-2
V_S	Low Voltage Supply		11	10.8	12	13.2	V	1-2
I_{HT}	Quiescent Drain Current	Vin = 0 Vodc = Vsat H	4		10	15	mA	1
I_S	Quiescent Drain Current	Vin = 0 Vodc = Vsat H	11		10	17	mA	1
Vref	Reference Voltage		10	1.4	1.6	1.9	V	1
Vg1	CRT G1 Voltage Supply		5		V_s + Vbe		V	1
Vsat	H Output Saturation	Vin = 0 Vdc = – 3V	3 13 15		V_{HT} – 3V		V	1
Vsat	L Output Saturation	Vin = 0 Vdc = 9V	3 13 15		V_s		V	1
I_1, I_2, I_3		See schematic diagr. Vin = 0 ; Vodc = 150V	12	7	15	20	µA	1
Vodc	Quiescent Output Voltage	Inputs Floating	3 13 15		123		V	1
Vo	Peak-to-peak Output Swing	f = 10KHz	3 13 15	170			Vpp	1
$\frac{\Delta Vodc}{\Delta T}$	DC Output Voltage vs. Temperature	Vodc = 150V Tamb = 0 ÷ 70°C	3 13 15		0.03		V/°C	1
$\frac{\Delta Vodc}{\Delta T}$	DC Differential Voltage vs. Temperature	Vodc = 150V Tamb = 0 ÷ 70°C	3 13 15			0.015	V/°C	1
GVo	Open-loop Gain	Vin = 50mVpp f = 10KHz		50	56		dB	1
GVc	Closed-loop Gain	Vin = 1.5Vpp f = 10KHz		20	25		dB	1

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Pin	Min.	Typ.	Max.	Unit	Fig.
Bw	Video Bandwidth (– 3 dB)	Vobl = 125V 0dB at f = 100KHz Vo = 80Vpp 50Vpp 10Vpp		4.5 6.5 12	6.0 8.0 15		MHz	2
tr	Rise Time	Vo = 100Vpp ; Vobl = 150V f = 100KHz Duty Cycle = 0.5			80	120	ns	2
tf	Fall Time	Vo = 100Vpp ; Vobl = 150V f = 100KHz Duty Cycle = 0.5			80	120	ns	2
ΔT	Differential Rise and Fall Time					20	ns	2
	Overshoot	Vo = 100Vpp ; Vobl = 150V f = 100KHz Duty Cycle = 0.5				5	%	2
	Undershoot	Vo = 100Vpp ; Vobl = 150V f = 100KHz Duty Cycle = 0.5				5	%	2

* CL = 10pF is the sum of the P.C. board capacitance (with socket) and the cathode capacitance of the CRT.

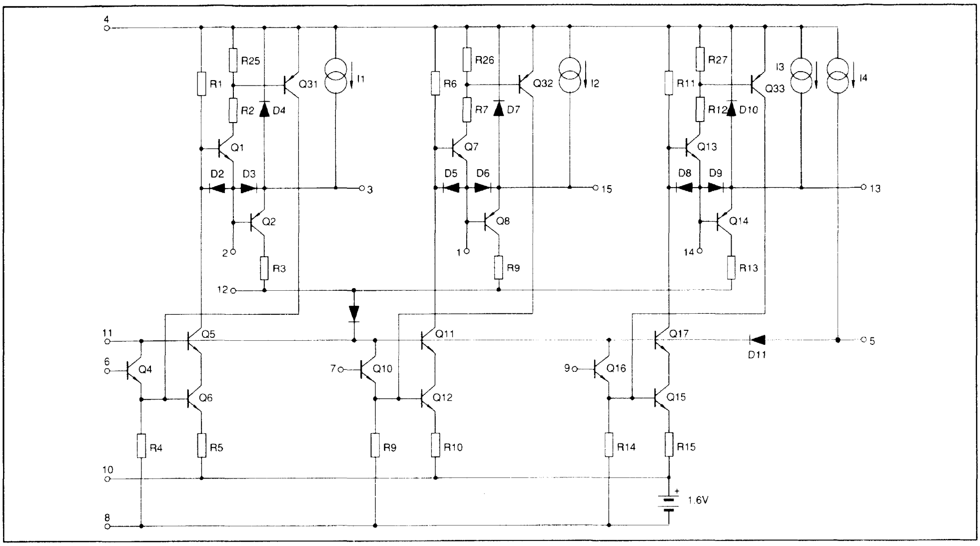
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_h	High Voltage Supply	250	V
V_s	Low Voltage Supply	35	V
P_{tot}	Power Dissipation at T_{case} = 90°C	20	W
V_I	Input Voltage	V_s	
T_{stg}, T_j	Storage and Junction Temperature	– 25 to 150	°C
Top	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W

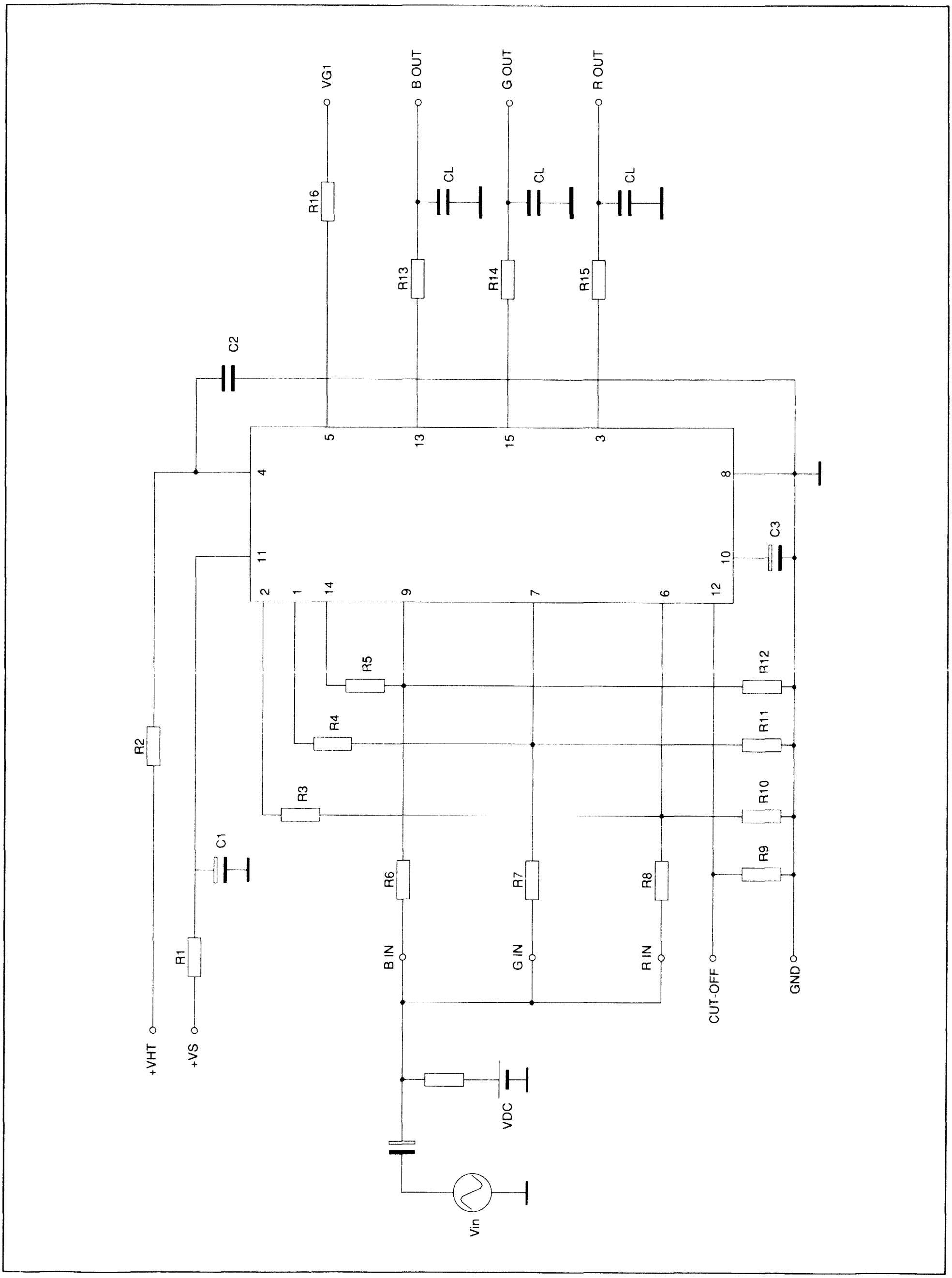
SCHEMATIC DIAGRAM



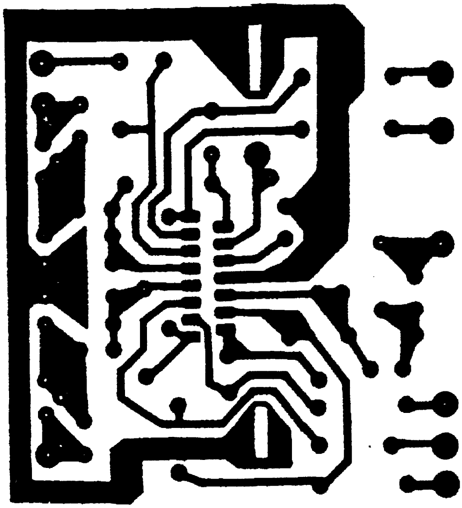
PIN FUNCTIONS

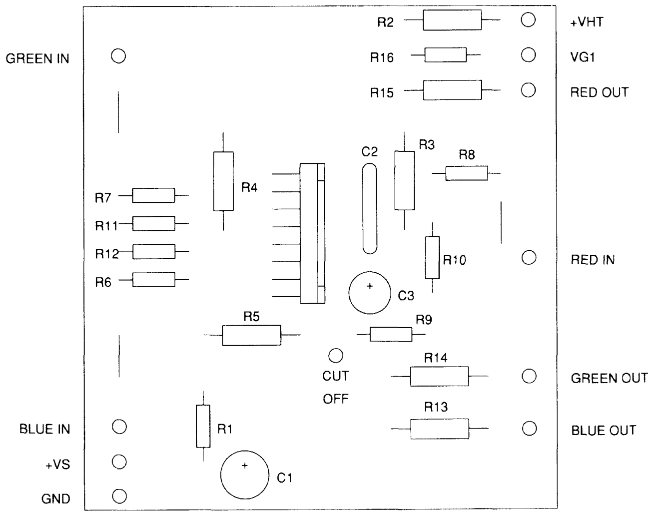
N°	Name	Function
1	GREEN FEEDBACK	Feedback Output for 'Green' Amplifier. The optimal value for the resistor connected here to set gain 68KΩ as shown in fig. 1.2. Other feedback connections are pin 2 (red) and pin 14 (blue).
2	RED FEEDBACK	Feedback Output for 'Red' Amplifier. See pin 1.
3	RED OUTPUT	Output of 'Red' Video Amplifier. See pin 15.
4	V_h	High Voltage Supply for Amplifier Stages, Typically 200V (see fig. 1.2).
5	FIRST GRID VOLTAGE	Output providing DC voltage for first grid of CRT, typically $V_s + V_{BE}$.
6	RED INPUT	Input of 'Red' Video Amplifier. See pin 7.
7	GREEN INPUT	Input of "Green" Video Amplifier. The bias voltage at the inputs is equal to $V_{ref} + 2_{VBE}$. Other inputs are pin 6 (red) and pin 9 (blue).
8	GROUND	Ground Connection (pin 8 is also connected to the tab).
9	BLUE INPUT	Input of 'Blue' Video Amplifier. See pin 7.
10	V_{ref}	The reference voltage for the three amplifiers is available on this pin. Typical value is 1.6V. The capacitor connected between pin 10 and ground eliminates AC crosstalk between the amplifiers.
11	V_s	Supply Voltage Input for Low Voltage Circuitry, typically 12V.
12	SAMPLING	Cathode Current Sampling Output. Provides sum of cathode currents for automatic cut-off adjustment with video processors using the sequential system. The three current generators I_1, I_2 and I_3 bias the inputs of this circuit which performs the cut-off adjustment, allowing adjustment also with inflowing CRT leakages.
13	BLUE OUTPUT	Output of 'Blue' Video Amplifier. See pin 15.
14	BLUE FEEDBACK	Feedback Output for 'Blue' Amplifier. See pin 1.
15	GREEN OUTPUT	Output of the 'Green' Video Amplifier. The output is protected against CRT tlashovers. Other outputs are pin 3 (red) and pin 13 (blue).

Figure 1 : Test Circuit.



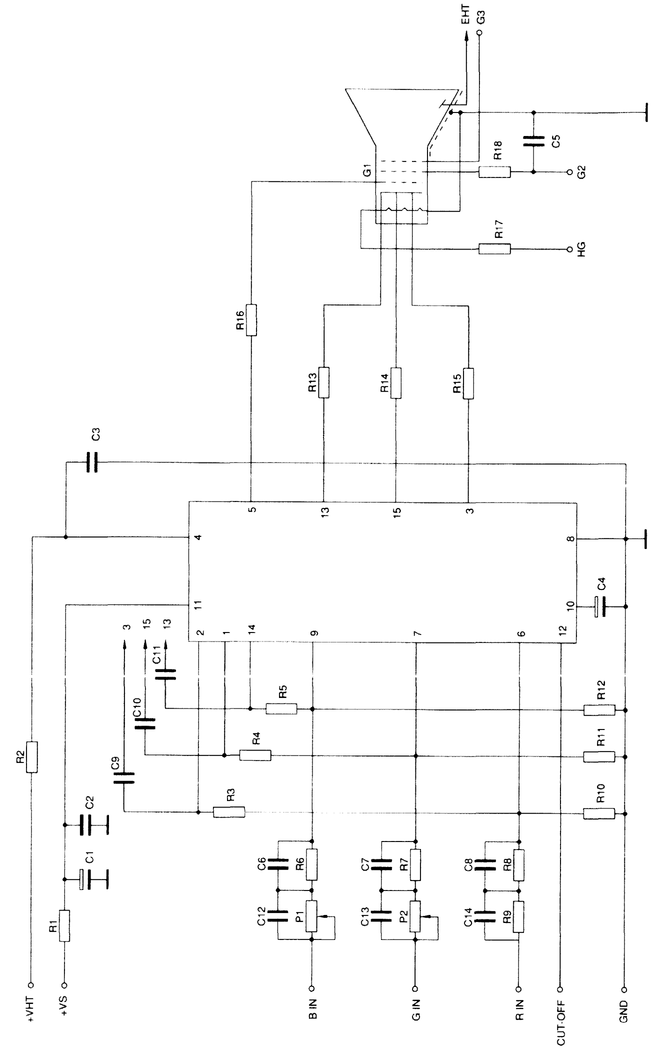
TEST CIRCUIT





R1 = 10 ohm		R9 = 47 Kohm		C1 = 47µF 16V
R2 = 220 ohm	1/2W	R10 = 1.8 Kohm	1/2W	C2 = 100nF 250V
R3 = 68 Kohm	1/2W	R11 = 1.8 Kohm	1/2W	C3 = 10µF 16V
R4 = 68 Kohm	1/2W	R12 = 1.8 Kohm	1/2W	
R5 = 68 Kohm	1/2W	R13 = 1 Kohm	1/2W	
R6 = 3 Kohm		R14 = 1 Kohm	1/2W	
R7 = 3 Kohm		R15 = 1 Kohm	1/2W	
R8 = 3 Kohm		R16 = 2.2 Kohm		

Figure 2 : Application Circuit.



R1 = 10 ohm
R2 = 220 ohm 1W
R3 = 68 Kohm 1/2W
R4 = 68 Kohm 1/2W
R5 = 68 Kohm 1/2W
R6 = 2.2 Kohm
R7 = 2.2 Kohm
R8 = 2.2 Kohm
R9 = 680 ohm
R10 = 1.8 Kohm
R11 = 1.8 Kohm
R12 = 1.8 Kohm

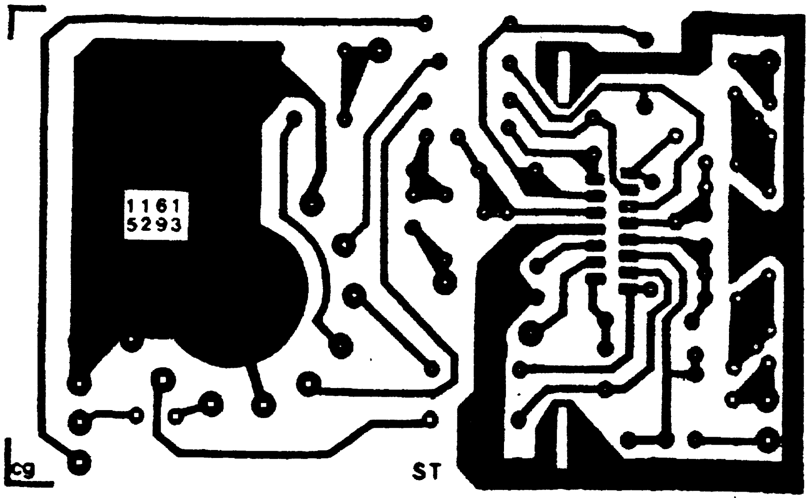
R13 = 1 Kohm 1/2W
R14 = 1 Kohm 1/2W
R15 = 1 Kohm 1/2W
R16 = 2.2 Kohm
R17 = 0.1 ohm 2W
R18 = 10 Kohm 2W

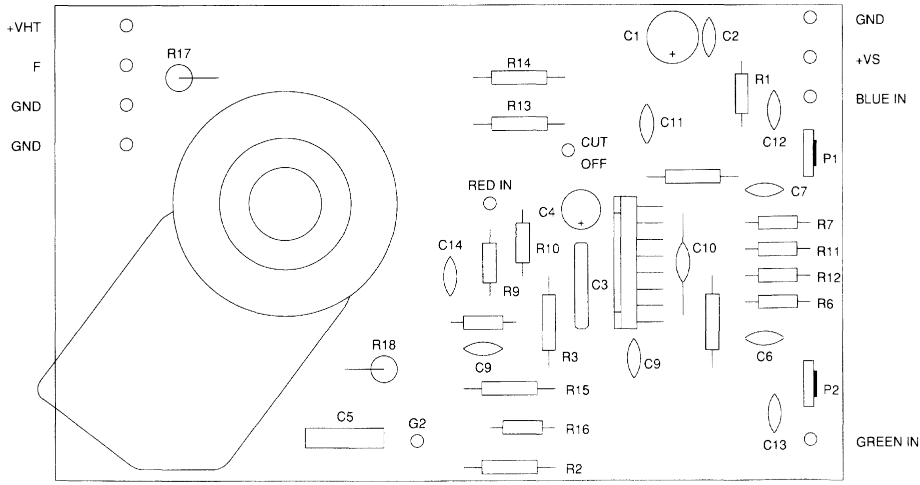
C1 = 47µF 16V
C2 = 0.1µF
C3 = 0.1µF 250V
C4 = 10µF 16V
C5 = 2.2nF 1KV

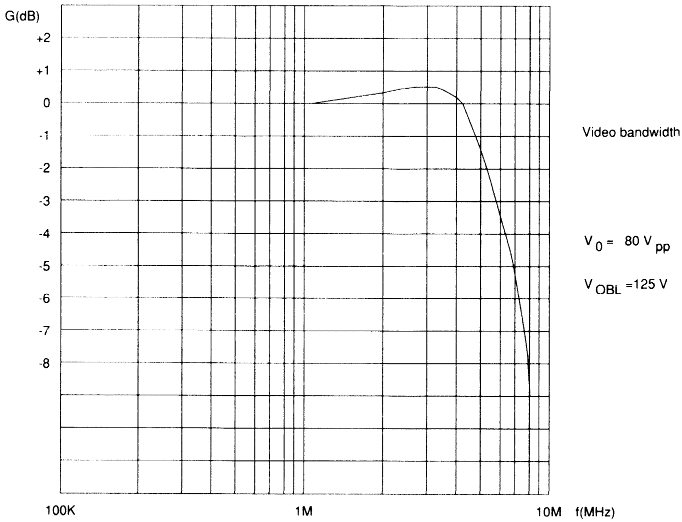
C6 = 22pF
C7 = 22pF
C8 = 22pF
C9 = 100pF
C10 = 100pF
C11 = 100pF
C12 = 68pF
C13 = 39pF
C14 = 68pF

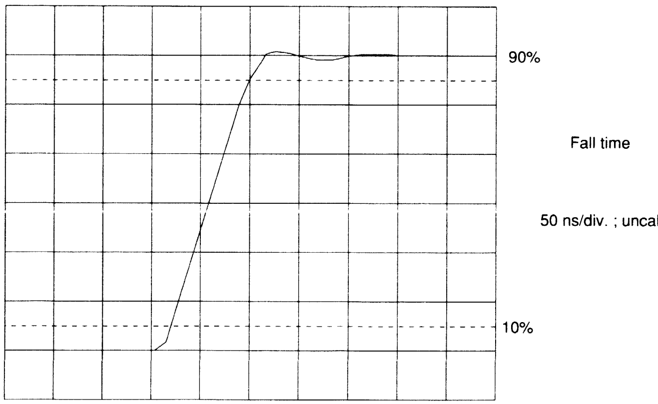
P1 = 2.2 Kohm pot. lin.
P2 = 2.2 Kohm pot. lin.

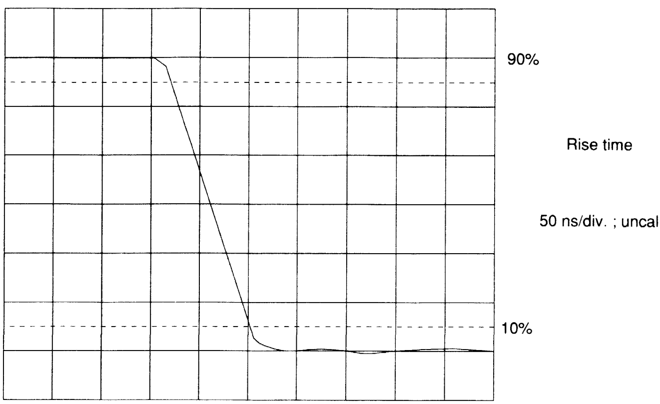
APPLICATION CIRCUIT






G(dB)
+2
+1
0
-1
-2
-3
-4
-5
-6
-7
-8
100K
1M
10M
f(MHz)
Video bandwidth
V_0 = 80 V_{pp}
V_{OBL} =125 V


90%
10%
Fall time
50 ns/div. ; uncal


90%
10%
Rise time
50 ns/div. ; uncal

TDA8153 - APPLICATION NOTES

P. C. BOARD

The best performance of the RGB video amplifier can be obtained only with a carefully designed P.C. board. The layout of the printed circuit must be realized to achieve the best possible symmetry of the three channels.

Output to input capacitances are of particular importance. The input-output capacitances, in parallel with the relative high feedback resistances, create poles in the closed loop transfer function.

To optimize the band response and to minimize the channels crosstalk a low parasitic capacitance feedback resistors of not inductive type is necessary.

Capacitive coupling from the output of an amplifier and the input of another one may induce excessive crosstalk. It advisable to keep the amplifier outputs away from amplifier inputs.

The small size of the P.C. board allows you to mount the TDA8153 directly beside the picture tube socket, to minimize the capacitances of the connections between the video amplifiers and the picture tube cathodes.

The capacitors connected in parallel with the input resistors compensate the effects of the distribute constants of the printed circuit on the step response times. Their values must be selected on the basis of the layout and can be considered as function of the printed circuit.

The three capacitors (C9, C10, C11) between the amplifier outputs and the feedback resistors reduces the noise effect on the cut-off control, their value, of course, depends on the noise amplitude and spectrum coming from the I.F. video stage.

To prevent possible oscillation problems, it is necessary to place the high voltage filter capacitor (C3) as near as possible to the IC ground and the latter must be of a substantial width.

POWER DISSIPATION

Taking as reference the IC internal schematic diagram we can calculate the power dissipated by the video amplifiers.

The power dissipation of the IC is defined by a static an a dynamic part.

The statically dissipated power is given by :

$$PS = 3\,Vht\left(\frac{Vht - Vobl}{R1} + \frac{Vobl}{Rf}\right) - 3\,\frac{Vobl^2}{Rf} - 3\,\frac{(Vref + 2Vbe)^2}{Rb}$$

Where Rf is the feedback resistance and Rb the input to ground resistance with a black level Vobl = 150V, Vht = 200V, Rf = 68 Kohm and Rb = 1.8 Kohm we have :

Ps = 1.75W

The dynamic power dissipation has been calculated with a 5MHz, 80Vpp sinusoidal output signal and a load capacitor C_L = 10pF with the following expression :

$$Pd = 3\left[0.8\,Vht\,(2\,f\,C_L\,Vop) - 0.8\,\frac{Vop^2}{2Rf}\right] = 1.90W$$

The value is reduced by 20% (0.8 factor) because during the flyback time there is not signal.

The total power dissipated by the IC is therefore :

PT = Ps + Pd = 1.75 + 1.90 = 3.65W

One of the worst working condition of the TV set as regards the power dissipation, is when you get white noise on the screen, for example, when you disconnected the TV aerial or the channels are not properly tuned.

In these cases if we set the TV receiver for 80Vpp white noise output signal with a black level Vob1 = 125V, the total power dissipated by the IC can be measured.

It results about PT = 4.8W.

With a maximum ambient temperature of 70°C and a junction temperature of 150°C a 15°C/W heatsink is required.

Figure 3 : Maximum Allowable Power Dissipation vs. Ambient Temperature.

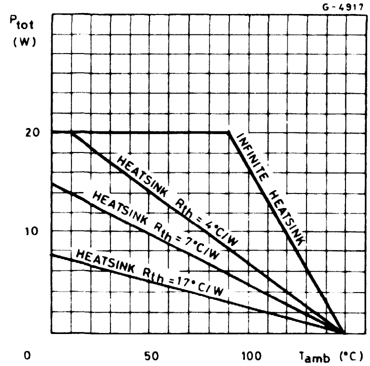
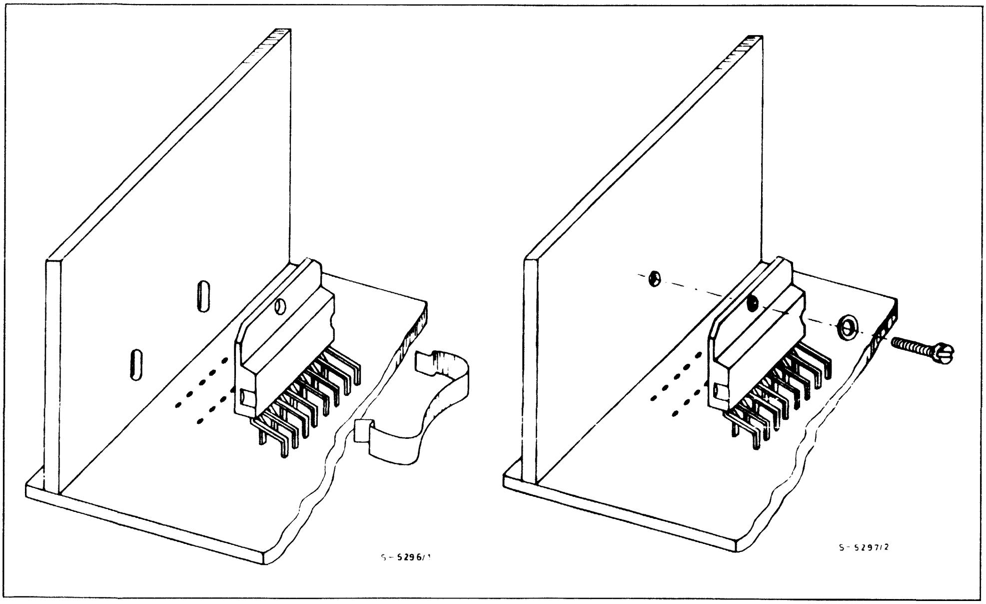


Figure 4 : Mounting Examples.



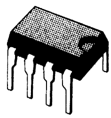
SGS-THOMSON
MICROELECTRONICS

TDA8160

INFRARED REMOTE CONTROL RECEIVER

ADVANCE DATA

- LOW SUPPLY VOLTAGE (V_S = 5V)
- LOW CURRENT CONSUMPTION (I_S = 6mA)
- INTERNAL 5.5 V SHUNT REGULATOR
- PHOTODIODE DIRECTLY COUPLED WITH THE I.C.
- INPUT STAGE WITH GOOD REJECTION AT LOW FREQUENCY
- LARGE INPUT DYNAMIC RANGE
- FEW EXTERNAL COMPONENTS



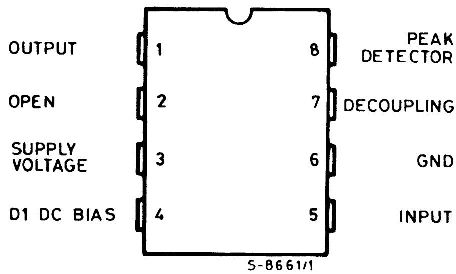
MINIDIP
(Plastic)

ORDER CODE : TDA 8160

DESCRIPTION

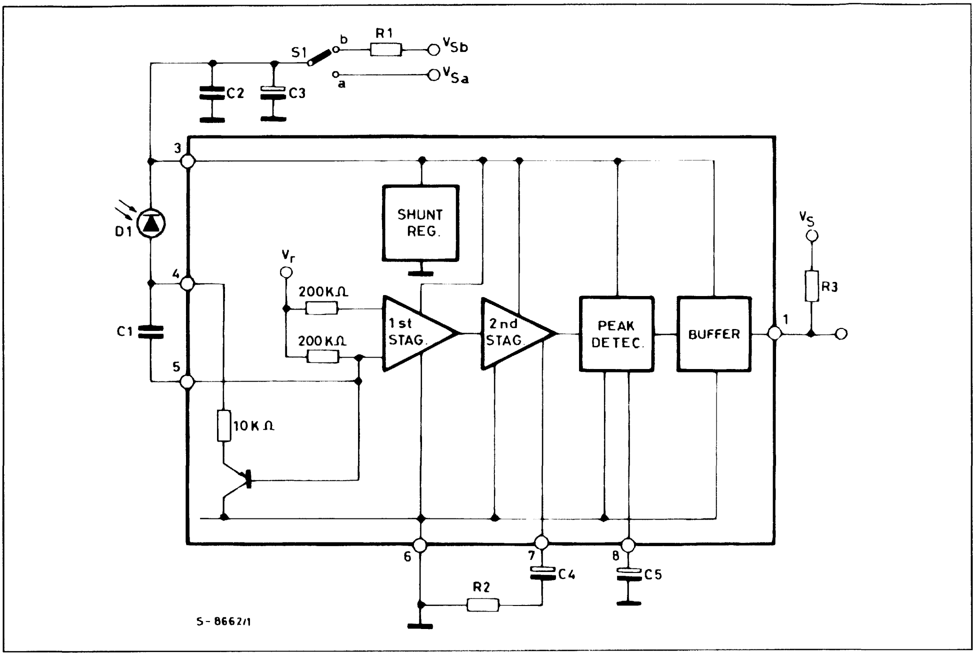
The TDA 8160 is a monolithic integrated circuit in-lead minidip plastic package specially designed to amplify the infrared signals in remote controlled TV, Radio or VCR sets. It can be used in flash transmission mode in conjunction with dedicated remote control circuits (for example : M491-494).

CONNECTION DIAGRAM (top view)

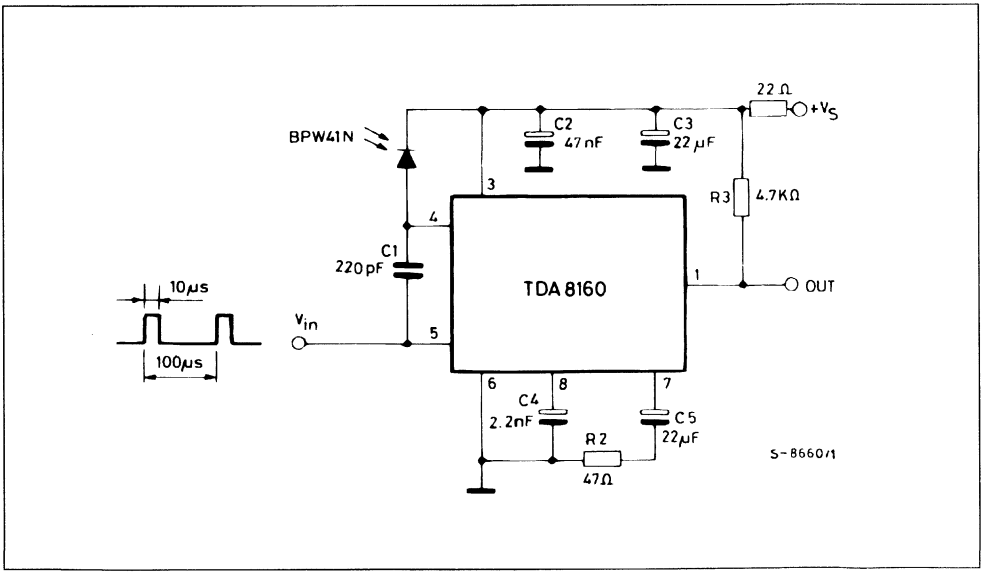


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



TEST CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
T_{stg-j}	Storage and Junction Temperature	– 40 to 150	°C
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	400	mW

THERMAL DATA

$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

ELECTRICAL CHARACTERISTICS
(refer to the test circuits ; V_S = 5 V, f_o = 10 kHz, T_{amb} = 25 °C, unless otherwise specified)

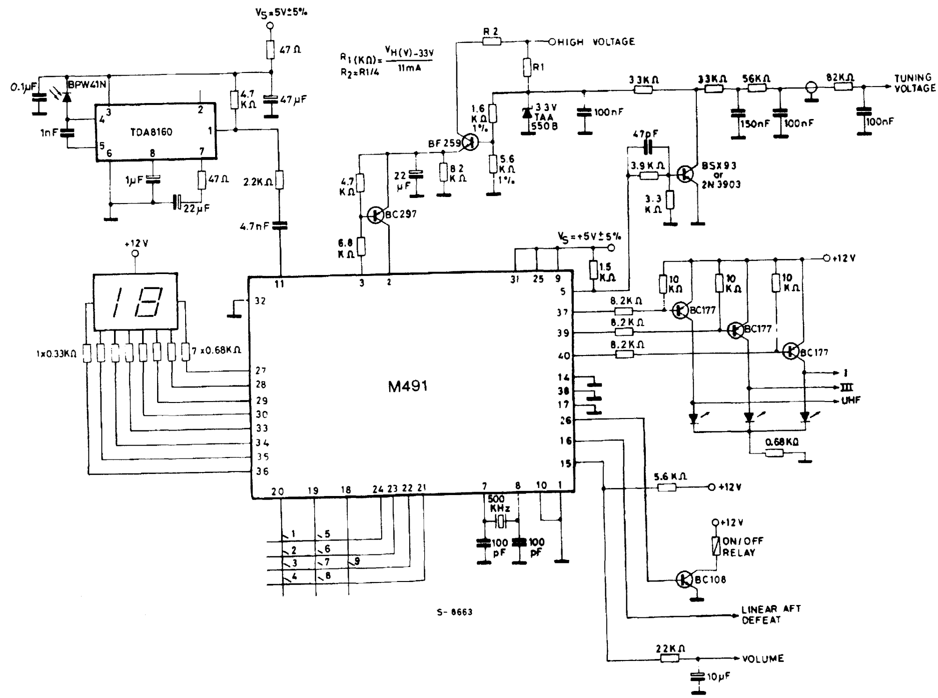
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	Applied between Pin 3 and 6	4	5	5.25	V
I_S	Suppply Current (pin 3)			6		mA
V_3	Stabilized Voltage at Pin 3	I_3 = 8 mA		5.5		V
G_V1st	Voltage Gain (1st stage)			28		dB
g_m2nd	Transconductance (2nd stage)			15		mA/V
V_{in}	Input Voltage Sensitivity (pin 5)	For Full Swing at the Output Pin 1 R_{gen} = 600 Ω		2		mV_p
I_{in}	Input Current Sensitivity (pin 5)	For Full Swing at the Output Pin 1		10		nA_p
R_{in}	Input Impedance			200		KΩ
L_fR	Low Frequency Rejection at the input Stage	C1 = 100 pF f = 100 Hz		30		dB
N	Noise Signal at Pin 7	C4 missing		200		mV_{pp}

CIRCUIT DESCRIPTION (see the block diagram)

The infrared light received from D1 generates an AC signal that comes in to the device at pin 5. The capacitor C1 and the integrated 10KΩ resistor (pin 4) filter out the low frequency noise.

The first stage shows a voltage gain of about 28dB ; the second stage is a voltage to current converter of 50mA/V (R_2 = Zero). A sensitive peak detector detects the amplifier signal ; one open collector output (pin 1) gives out the recovered pulses.

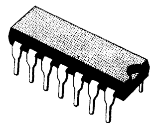
Figure 1 : Recommended Application Circuit for the Drive of the IC M491 by Means of a Flash Mode IR. Transmitter only, in a TV 16 Station Memory Remote Control Subsystem. The Above Shown IR Receiver Application must be Housed Inside a Metal Can Shield.



INFRARED REMOTE CONTROL RECEIVER

ADVANCE DATA

- LOW SUPPLY VOLTAGE (V_S = 5V)
- LOW CURRENT CONSUMPTION (I_S = 4mA)
- INTERNAL 5.5V SHUNT REGULATOR
- INPUT STAGE WITH GOOD REJECTION AT LOW FREQUENCY
- SELECTIVE AMPLIFIER
- LARGE INPUT DYNAMIC RANGE
- HIGH INPUT SENSITIVITY
- A.G.C. FACILITY



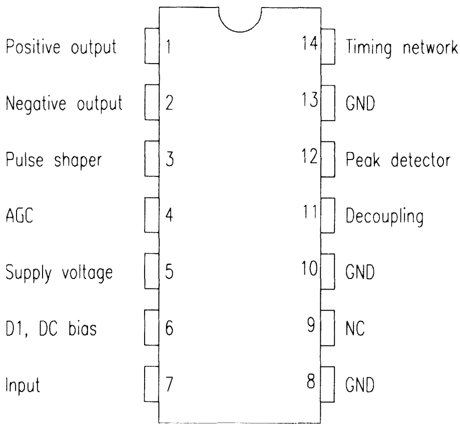
DIP14
(Plastic Package)

ORDER CODE : TDA8162

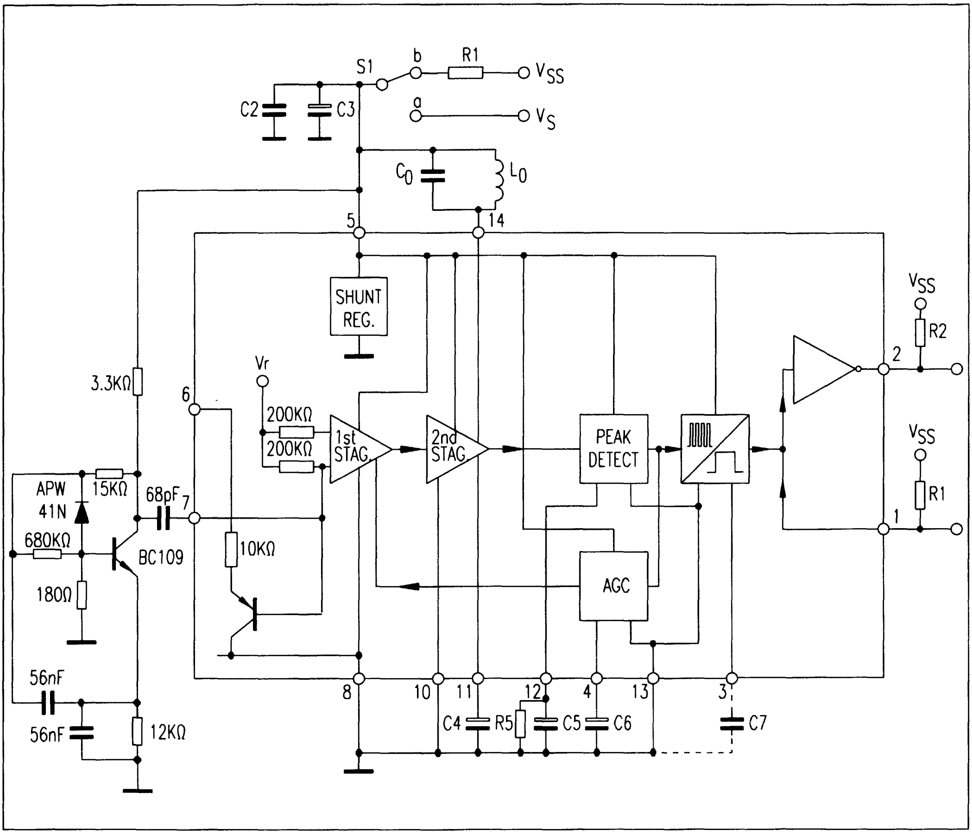
DESCRIPTION

The TDA8162 is a monolithic integrated circuit in 14-lead dual in line plastic package specially designed to amplify the infrared signals in remote controlled TV, Radio or VCR sets.
It is properly designed to work in "CARRIER" transmission mode and the open collector output allows direct operation with dedicated remote control circuit (for example M206) or microprocessor systems.

PIN CONNECTION



BLOCK DIAGRAM



The infrared light received from D1 generates an alternate current that, through the transistor T1, comes into the device at pin 7.

The capacitor C1 and an internal network filter out the low frequency noise.

The first stage, the gain of which is controlled by AGC, shows a maximum voltage gain of about 30dB.

The second stage is a selective amplifier (the frequency is generally included between 30kHz and 40kHz), with an voltage gain of about 50dB, loaded by Lo, Co.

A sensitive peak detector detects the amplified signal, two open collector outputs (pin 1, 2) allow positive and negative signals respectively.

The recovered signal drives the AGC block that controls the gain of the first stage when too strong signal is received.

This block (AGC) is a block at fast charge and slow discharge.

The detected information can be reshaped by connecting a suitable capacitor at pin 3 ; in such a way the carrier is integrated and the outputs become square wawes that can directly drive one microprocessor (avoiding a digital filter otherwise needed).

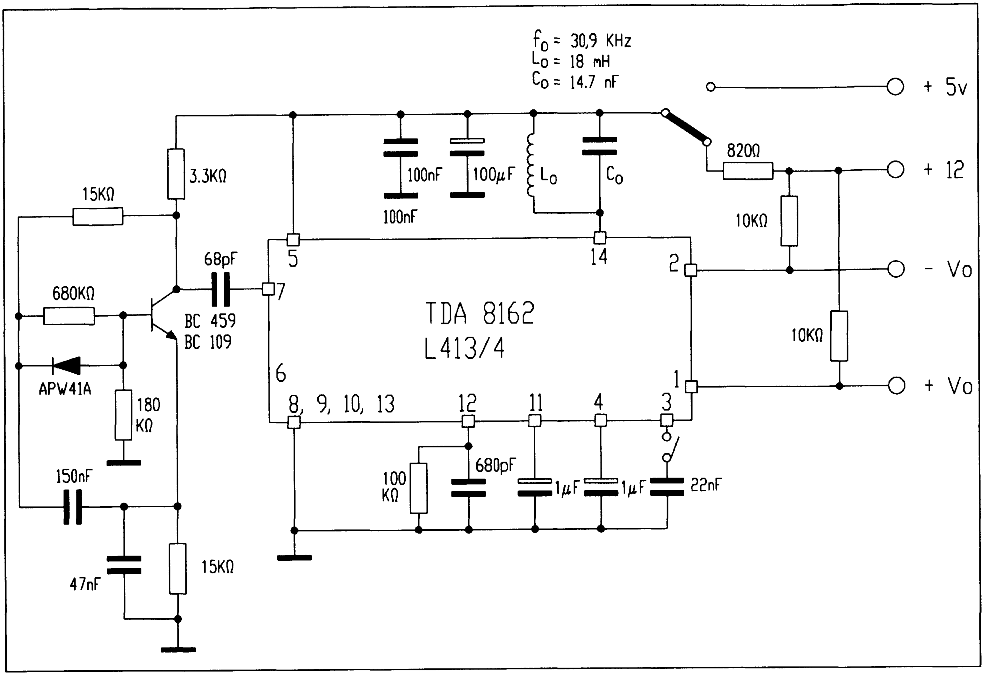
A voltage Regulator is also integrated, when you use a 5V of alimentation, this regulator is automatically disabled.

ELECTRICAL CHARACTERISTICS

Refer to the test circuit ; S1 to "a" ; V_{ss} = 12V ; V_s = 5V ; fo = 38.43kHz, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage	Applied between Pin 5 and 8	4	5	5.25	V
I_s	Supply Current (pin 5)	V_s = 5V V_i = 0V		4	8	mA
V_5	Stabilized Voltage at Pin 5	I_5 = 8mA S_1 to "b" ;		5.5		V
	First Stage Voltage Gain	Pin 4 to GND		30		dB
	2nd Stage Voltage Gain	V_{14} = 500mV$_{PP}$		50		dB
	2nd Stage Bandwidth	Co = 9.53nF Lo : L_s = 1.8mH ; R_s = 24.5Ω		2.2		KHZ
	Input Voltage Sensitivity (pin 7)	For 500mV$_{PP}$ at Pin 14		100		μV$_{PP}$
	Input Current Sensitivity (pin 7)	For 500mV$_{PP}$ at Pin 14		1		nA$_{PP}$
	Input Impedance			100		kΩ
	AGC Range		80			dB
	Low Frequency Rejection at the Input Stage	C_1 = 2.2nF, f = 100Hz ;		30		dB
	Peak Detector Sensitivity (pin 12)	Full Swing at Pin 1 and at Pin 2		150		mV
	Noise Signal at Pin 14	V_{in} = 0		150		mV$_{PP}$
	Threshold Comparator			500		mV$_{PP}$

TYPICAL APPLICATION



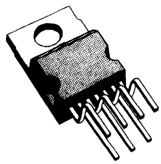
SGS-THOMSON MICROELECTRONICS

TDA8170

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The functions incorporated are :

- POWER AMPLIFIER
- FLYBACK GENERATOR
- REFERENCE VOLTAGE
- THERMAL PROTECTION



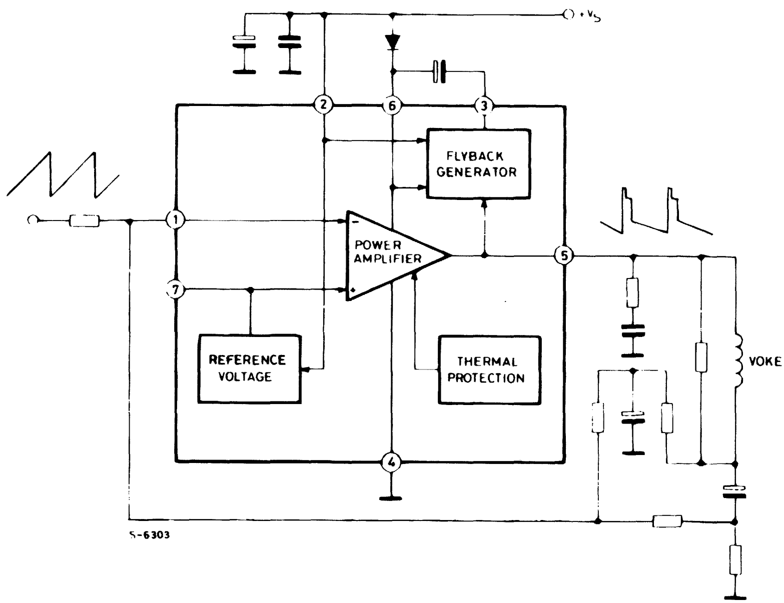
HEPTAWATT

ORDER CODE : TDA8170

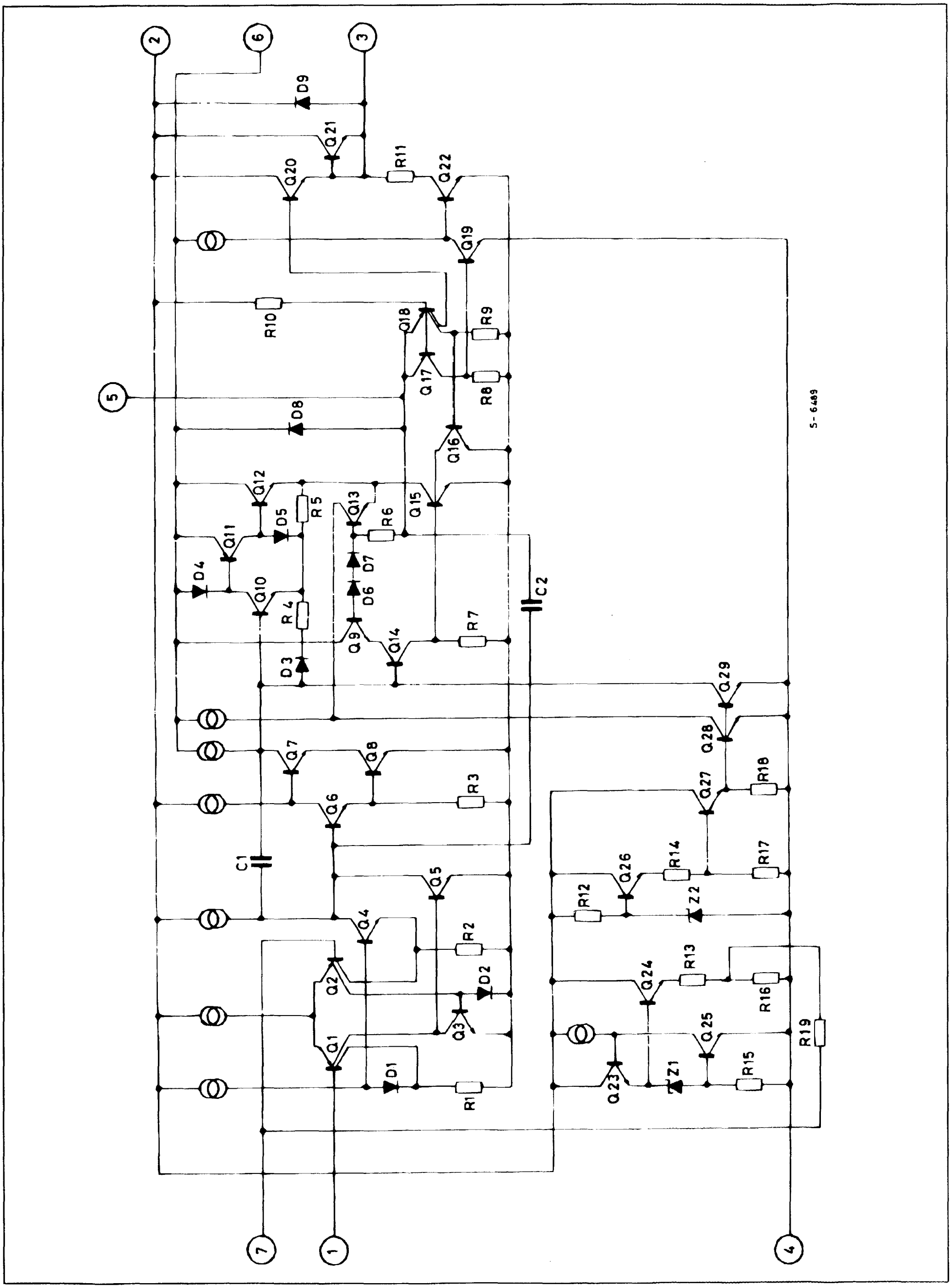
DESCRIPTION

The TDA8170 is a monolithic integrated circuit in HEPTAWATT™ package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour and B & W television receivers as well as in monitors and displays.

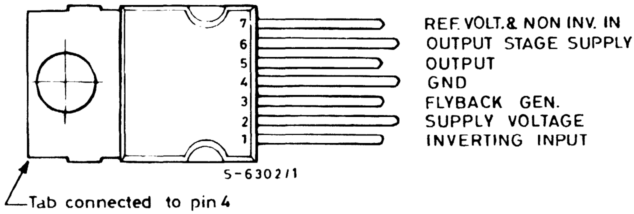
BLOCK DIAGRAM



SCHEMATIC DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+ V_s$	
V_1, V_7	Amplifier Input Voltage	$+ V_s$ $- 0.5$	V
I_o	Output Peak Current (non repetitive, t = 2 msec)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, t ≤ 10 µsec	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µsec	2	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$msec	3	A
P_{tot}	Total Power Dissipation at T_{case} = 70 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	4	°C/W

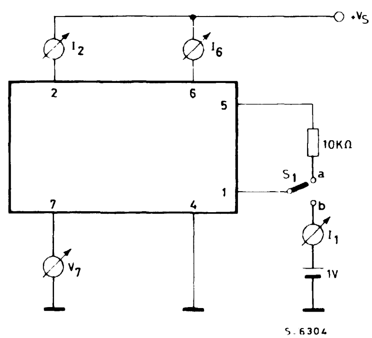
ELECTRICAL CHARACTERISTICS

(refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$	$I_5 = 0$		8	16	mA	1a
I_6	Pin 6 Quiescent Current	$I_3 = 0$	$I_5 = 0$		16	36	mA	1a
I_1	Amplifier Input Bias Current	$V_1 = 1$ V			– 0.1	– 1	µA	1a
V_7	Reference Voltage				2.2		V	1a
$\frac{\Delta V_7}{\Delta V_s}$	Reference Voltage Drift vs. Supply Voltage	V_s = 15 to 30 V			1	2	mV/V	1a
V_{3L}	Pin 3 Saturation Voltage to GND	I_3 = 20 mA			1		V	1c
V_5	Quiescent Output Voltage	V_s = 35V ;	R_a = 39 kΩ		18		V	1d
		V_s = 15 V ;	R_a = 13 kΩ		7.5		V	1d
V_{5L}	Output Saturation Voltage to GND	I_5 = 1.2 A			1	1.4	V	1c
		I_5 = 0.7 A			0.7	1	V	1c
V_{5H}	Output Saturation Voltage to Supply	$- I_5$ = 1.2 A			1.6	2.2	V	1b
		$- I_5$ = 0.7 A			1.3	1.8	V	1b
T_j	Junction Temperature for Thermal Shut Down				140		°C	

FIGURE 1 : DC TEST CIRCUITS.

Figure 1 a : Measurement of I_1 ; I_2 ; I_6 ; V_7 ; $\Delta V_7/\Delta V_S$.



S_1 : (a) I_2 and I_6 ; (b) I_1

Figure 1 b : Measurement of V_{5H}.

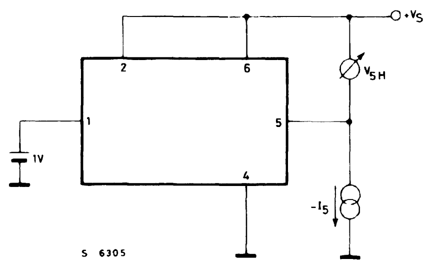
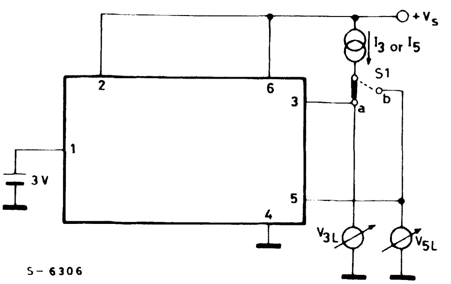


Figure 1 c : Measurement of V_{3L} ; V_{5L}.



S_1 : (a) V_{3L} ; (b) V_{5L}

Figure 1 d : Measurement of V_5.

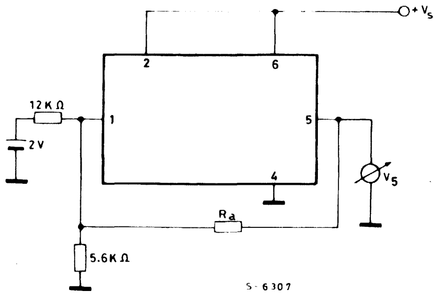


Figure 2 : AC Test Circuit.

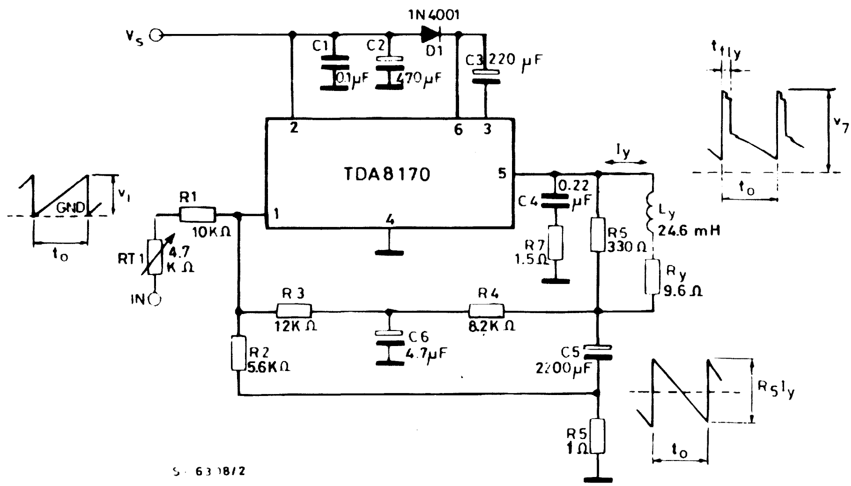
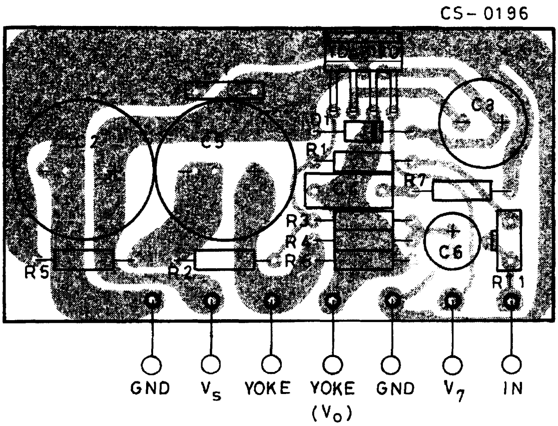


Figure 3 : PC Board and Component layout of the Circuit of fig. 2(1 : 1 scale).



COMPONENTS LIST FOR TYPICAL APPLICATIONS

Component	110 ° TVC 5.9 Ω/10mH 1.95 App	110 ° TVC 9.6 Ω/24.6 mH 1.2 App	90 ° TVC 15 Ω/30 mH 0.82 App	Unit
RT1	10	4.7	10	kΩ
R1	12	10	12	kΩ
R2	10	5.6	5.6	kΩ
R3	27	12	18	kΩ
R4	12	8.2	5.6	kΩ
R5	0.82	1	1	Ω
R6	270	330	330	Ω
R7	1.5	1.5	1.5	Ω
D1	1N 4001	1N 4001	1N 4001	–
C1	0.1	0.1	0.1	µF
C2 el.	1000/25 V	470/25 V	470/25 V	µF
C3 el.	220/25 V	220/25 V	220/25 V	µF
C4	0.22	0.22	0.22	µF
C5 el.	200/25 V	2200/25 V	1000/16 V	µF
C6 el.	4.7/16 V	4.7/16 V	10/16 V	µF

TYPICAL PERFORMANCES

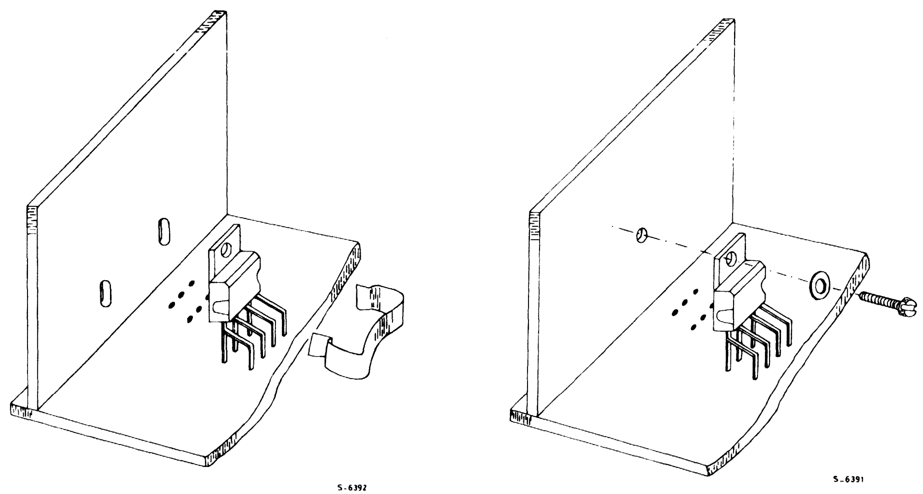
Parameter	110 ° TVC 5.9 Ω/10mH	110 ° TVC 9.6 Ω/27 mH	90 ° TVC 15 Ω/30 mH	Unit
V_s - Supply Voltage	24	22.5	25	V
I_s - Current	280	175	125	mA
t_{fly} - Flyback Time	0.6	1	0.7	ms
P_{tot} - Power Dissip.	4.2	2.5	2.05	W
$R_{th\ c-a}$ - Heatsink	7	13	16	°C/W
T_{amb}	60	60	60	°C
$T_{j\ max}$	110	110	110	°C
t_o	20	20	20	ms
v_i	2.5	2.5	2.5	V_{pp}
v_7	2.5	2.5	2.5	V_p

MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the HEPTAWATT^{TM} package attaching the heatsink is very simple, a screw a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 3 : Mounting Examples.

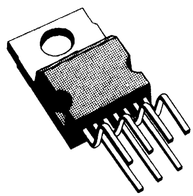


SGS-THOMSON MICROELECTRONICS

TDA8172

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION



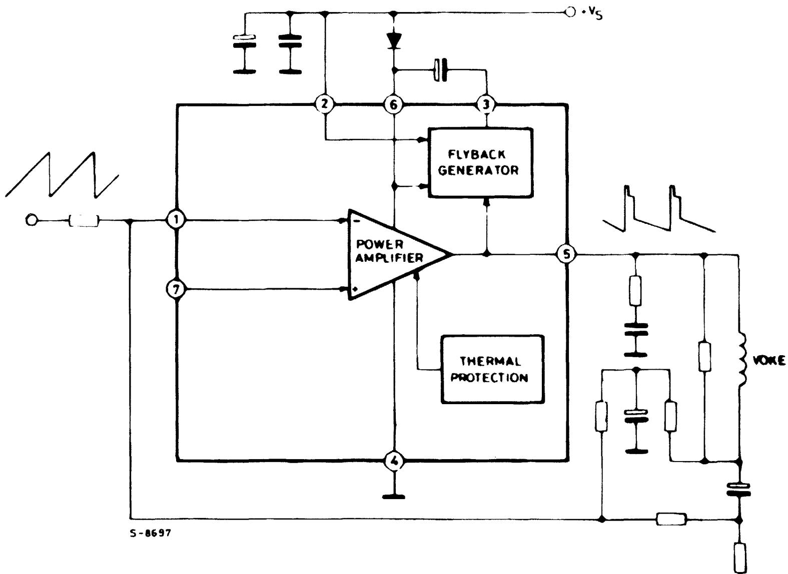
Heptawatt

ORDER CODE : TDA8172

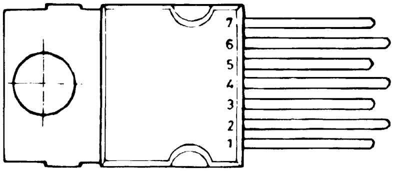
DESCRIPTION

The TDA8172 is a monolithic integrated circuit in HEPTAWATT® package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television as well as in monitors and displays.

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



Tab connected to pin 4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+V_s$	
V_1, V_7	Amplifier Input Voltage	$+V_s$ -0.5	V
I_o	Output Peak Current (non repetitive, t = 2 ms)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, t ≤ 10 µs	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µs	2	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$ ms	3	A
P_{tot}	Total Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	3	°C/W

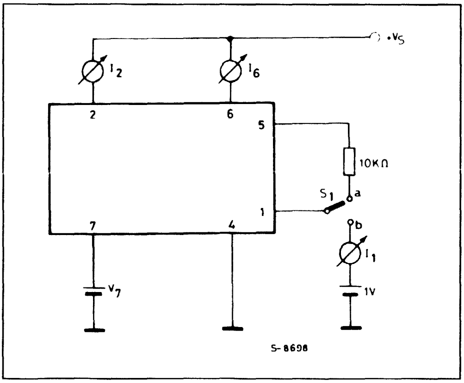
ELECTRICAL CHARACTERISTICS

(refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_2	Pin 2 Quiescent Current	$I_3 = 0$ $I_5 = 0$		8	16	mA	1a
I_6	Pin 6 Quiescent Current	$I_3 = 0$ $I_5 = 0$		16	36	mA	1a
I_1	Amplifier Input Bias Current	$V_1 = 1$ V $V_7 = 2$ V $V_1 = 2$ V $V_7 = 1$ V		– 0.1 – 0.1	– 1 – 1	µA	1a
V_{3L}	Pin 3 Saturation Voltage to GND	$I_3 = 20$ mA		1	1.5	V	1c
V_5	Quiescent Output Voltage	$V_s = 35$V $R_a = 39$ kΩ		18		V	1d
V_{5L}	Output Saturation Voltage to GND	$I_5 = 1.2$ A		1	1.4	V	1c
		$I_5 = 0.7$ A		0.7	1	V	1c
V_{5H}	Output Saturation Voltage to Supply	$-I_5 = 1.2$ A		1.6	2.2	V	1b
		$-I_5 = 0.7$ A		1.3	1.8	V	1b
T_j	Junction Temperature for Thermal Shut Down			140		°C	

Figure 1 : DC Test Circuits.

Figure 1 a : Measurement of I_1 ; I_2 ; I_6.



S_1 : (a) I_2 and I_6 ; (b) I_1

Figure 1 b : Measurement of V_{5H}.

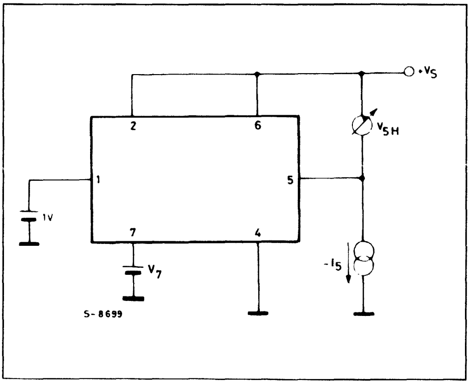
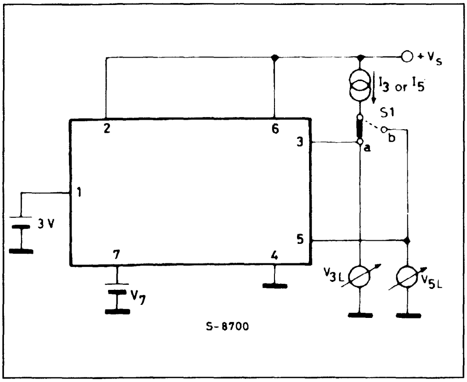


Figure 1 c : Measurement of V_{3L} ; V_{5L}.



S1 : (a) V_{3L} ; (b) V_{5L}

Figure 1 d : Measurement of V_5.

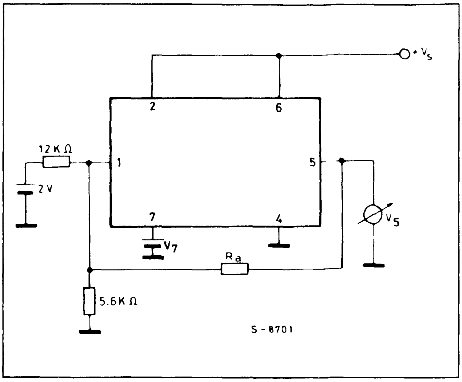
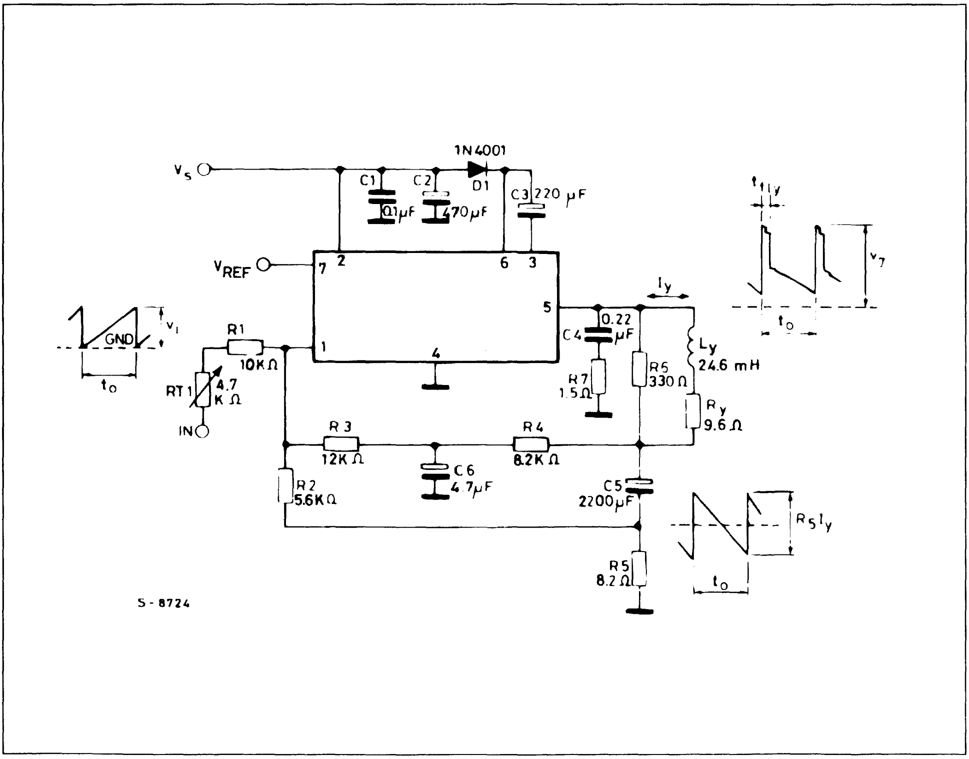


Figure 2 : AC Test Circuit.



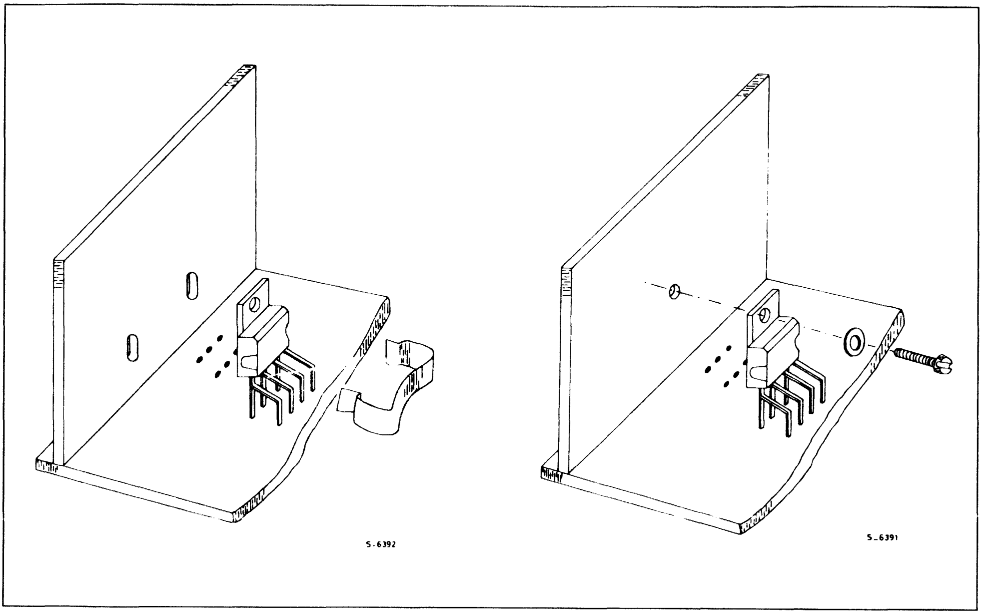
MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.

Thanks to the HEPTAWATT™ package attaching the heatsink is very simple, a screw a compression spring (clip) being sufficient.

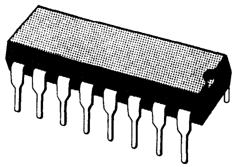
Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact ; no electrical isolation is needed between the two surfaces.

Figure 3 : Mounting Examples.



TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- THERMAL PROTECTION



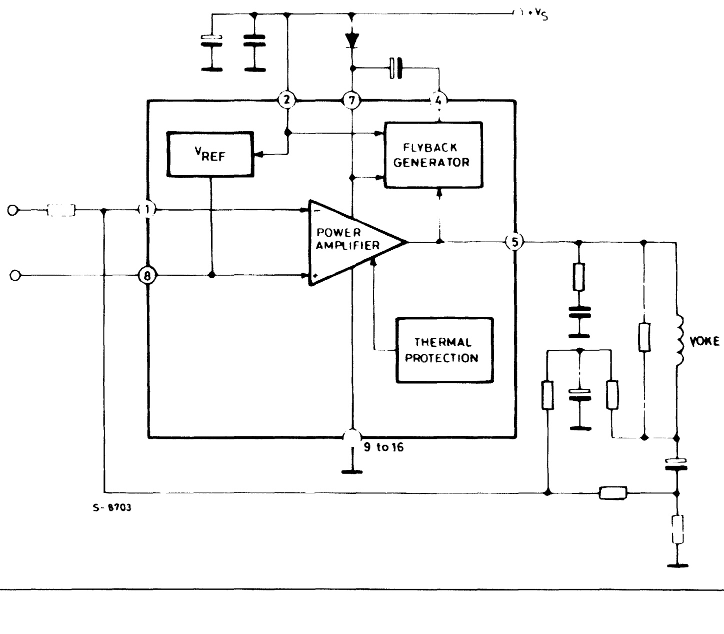
Dip – 16

ORDER CODE : TDA8173

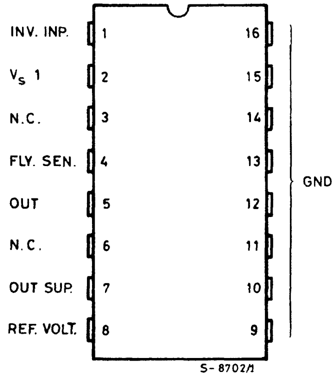
DESCRIPTION

The TDA8173 is a monolithic integrated circuit in POWERDIP package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Color and B & W television sets as well as in monitors, and displays.

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5	Flyback Peak Voltage	60	V
V_4	Voltage at Pin 4	+ V_s	
V_1, V_8	Amplifier Input Voltage	+ V_s – 0.5	V
I_o	Output Peak Current (non repetitive, t = 2 ms)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, t ≤ 10 µs	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µs	2	A
I_4	Pin 4 DC Current at $V_5 < V_2$	100	mA
I_4	Pin 4 Peak to Peak Flyback Current at f = 50 or 60 Hz, t_{fly} ≤ 1.5 ms	3	A
P_{tot}	Total Power Dissipation at T_{case} = 60 °C	6	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

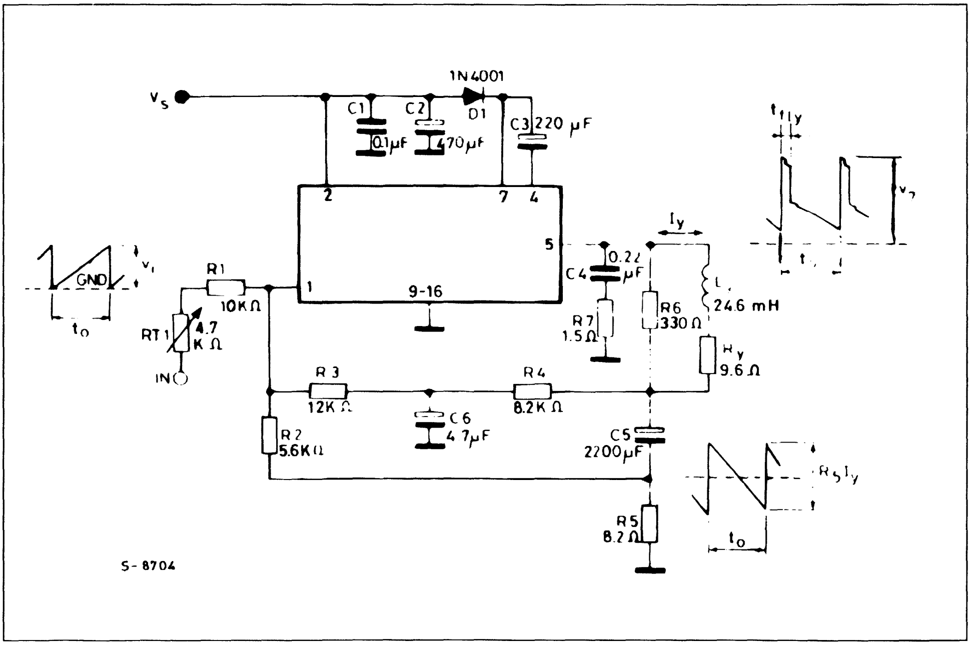
THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max	15	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	70	°C/W

ELECTRICAL CHARACTERISTICS
(refer to the test circuits, V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I = 0 I_5 = 0		8	16	mA
I_7	Pin 7 Quiescent Current	I = 0 I_5 = 0		16	36	mA
I_1	Amplifier Input Bias Current	V_1 = 1 V		– 0.1	– 1	µA
V_{4L}	Pin 4 Saturation Voltage to GND*	I_4 = 20 mA		1		V
V_5	Quiescent Output Voltage	V_s = 35 V R_a = 39 kΩ		18		V
V_{5L}	Output Saturation Voltage to GND	I_5 = 1.2 A		1	1.4	V
		I_5 = 0.7 A		0.7	1	V
V_{5H}	Output Saturation Voltage to Supply	– I_5 = 1.2 A		1.6	2.2	V
		– I_5 = 0.7 A		1.3	1.8	V
T_j	Junction Temperature for Thermal Shut Down			140		°C
V_8	Reference Voltage			2.2		V
$\frac{\Delta V_8}{\Delta V_s}$	Reference Voltage Drift vs. Supply Voltage	V_s = 15 to 30 V		1	2	mV

TEST CIRCUITS

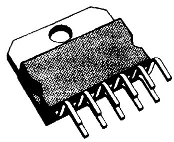


SGS-THOMSON
MICROELECTRONICS

TDA8174

VERTICAL DEFLECTION CIRCUIT

- RAMP GENERATOR
- INDEPENDENT AMPLITUDE ADJUSTEMENT
- BUFFER STAGE
- POWER AMPLIFIER
- FLYBACK GENERATOR
- INTERNAL REFERENCE VOLTAGE
- THERMAL PROTECTION



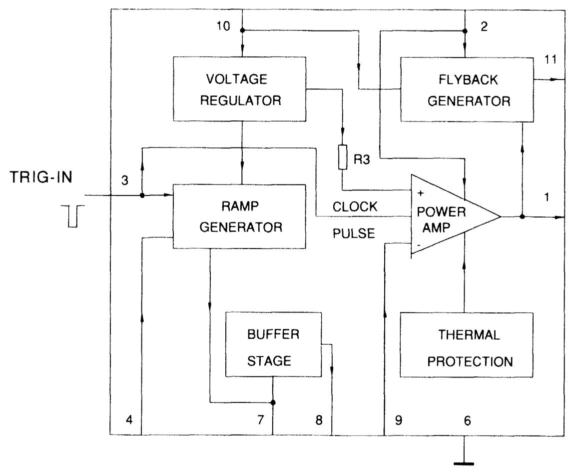
Multiwatt-11
ORDER CODE :TDA8174

DESCRIPTION

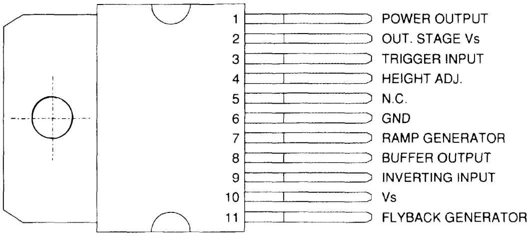
The TDA8174 is a monolithic integrated circuit in MULTIWATT-11 package.

It is a full performance and very efficient vertical deflection circuit intended for direct drive of a TV picture tube in Color and B & W television as well as in Monitor and Data displays.

BLOCK DIAGRAM



PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	35	V
V_1, V_2	Flyback Peak Voltage	65	V
V_3	Trigger Input Voltage	20	V
V_9	Amplifier Input Voltage	GND to V_S	V
I_0	Output Peak to Peak Current (non repetitive t = 2ms)	6	A
I_0	Output Peak to Peak Current t > 10μs	4	A
I_{11}	Pin 11 DC Current at $V_1 < V_{10}$	100	mA
I_{11}	Pin 11 Peak to Peak Current @ t_{fly} < 1.5ms	3	A
P_{tot}	Total Power Dissipation @ T_{tab} = 60°C	30	W
T_s	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C
T_{AMB}	Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{TH(j\text{-}tab)}$	Thermal Resistance Junc.-tab	Max	3	°C/W
$R_{TH(j\text{-}amb)}$	Thermal Resistance Junc.-amb	Max	40	°C/W

DC ELECTRICAL CHARACTERISTICS (V_S = 35V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current	I_1 = 0 I_{11} = 0		16	36	mA
I_{10}	Pin 10 Quiescent Current	I_1 = 0 I_{11} = 0		15	30	mA
$-I_7$	Ramp Generator Bias Current	V_7 = 0			0.5	µA
$-I_7$	Ramp Generator Current	V_7 = 0 $-I_4$ = 20µA	18.5	20	21.5	µA
dI_7/I_7	Ramp Gener. Linearity	V_6 = 0 to 15V $-I_4$ = 20µA		0.2	1	%
V_1	Quiescent Output Voltage	R_a = 30k R_b = 10k V_s = 35V	17.0	17.8	18.6	V
		R_a = 6.8k R_b = 10k V_s = 15V	7.2	7.5	7.8	V
V_{1L}	Out Saturation Voltage to GND	I_1 = 0.5A		0.5	1	V
		I_1 = 1.2A		1	1.4	V
V_{1H}	Out Saturation Voltage to V_s	$-I_1$ = 0.5A		1.1	1.6	V
		$-I_1$ = 1.2A		1.6	2.2	V
V_4	Reference Voltage	$-I_4$ = 20µA	6.3	6.6	6.9	V
dV_4/V_s	Reference Voltage Drift Versus V_s	V_s = 10V to 35V		1	2	mV/V
dV_4/d_{I4}	Reference Voltage Drift Versus I_4	I_4 = 10µA to 30µA		1.5	2	mV/µA
V_r	Internal Ref. Voltage		4.26	4.40	4.54	V
$V_{D11\text{-}10}$	Diode Fwd Voltage	I_D = 1.2A		2.2	3	V
$V_{D1\text{-}2}$	Diode Fwd Voltage	I_D = 1.2A		2.2	3	V
G_V	Output Stage Open Loop Gain	f = 100Hz		60		dB
V_{fs}	$V_{10\text{-}11}$ Saturation Voltage	$-I_{11}$ = 1.2A		1.5	2.5	V
V_{11}	Pin 11 Scanning Voltage	I_{11} = 20mA		1.7	3	V
V_3	Trigger Input Threshold	(see note 1)	2.6	3.0	3.4	V
I_3	Trigger Input Bias Current	V_{IN} = V_3 - 0.2V			30	µA
t_3	Trigger Input Width	(see note 2)	20	60	Th	µS

AC ELECTRICAL CHARACTERISTICS (V_s = 24V ; T_{amb} = 25°C unless otherwise specified)

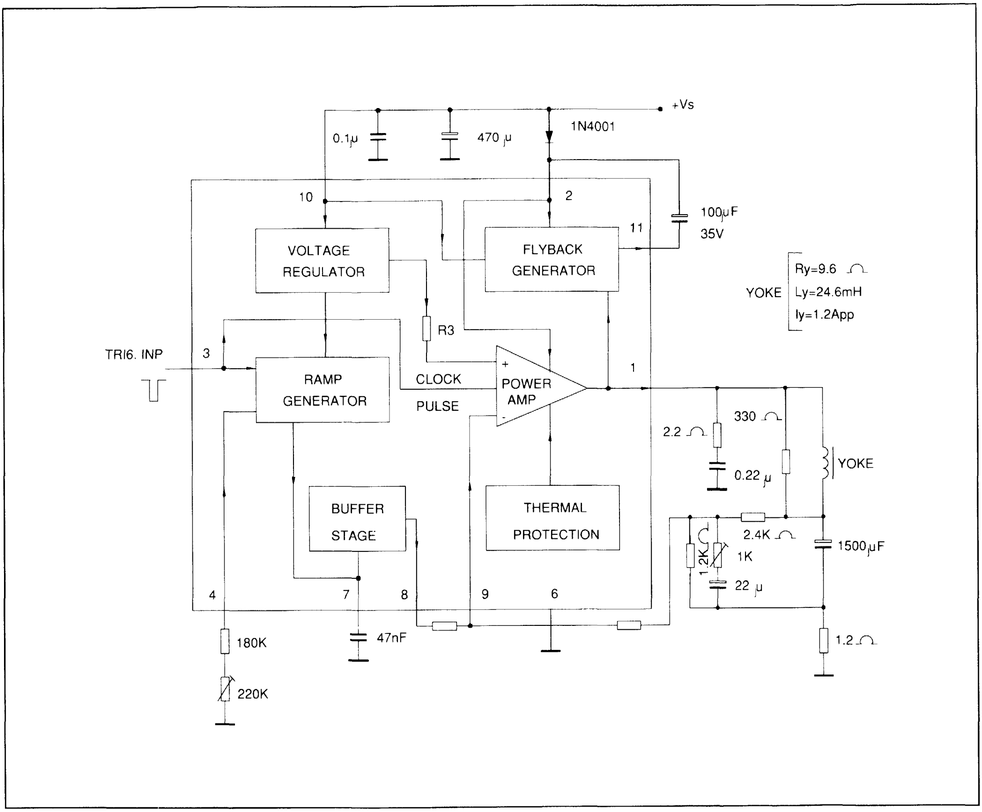
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage Range		10		30	V
I_1	Peak-to-peak Operating Current Range		0.4		2.5	A
I_s	Supply Current	I_y = 2.4A_{pp}		315		mA
V_1	Flyback Voltage	I_y = 2.4A_{pp}		51		V
V_8	Sawtooth Pedestall Voltage			1.85		V
T_{js}	Junction Temp. for Thermal Shutdown			145		°C

APPLICATION NOTES

Notes : 1. The trigger input circuit can accept, with a metal option, positive and negative going input pulses.

2. $Th = \frac{1.2 \cdot Ts}{V_{PP}}$ where : Ts is the vertical period
V_{PP} is ramp amplitude at pin 7

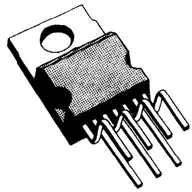
APPLICATION CIRCUIT



TDA8175

TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- POWER AMPLIFIER
- FLYBACK GENERATOR
- AUTOMATIC PUMPING COMPENSATION
- THERMAL PROTECTION
- REFERENCE VOLTAGE



Heptawatt

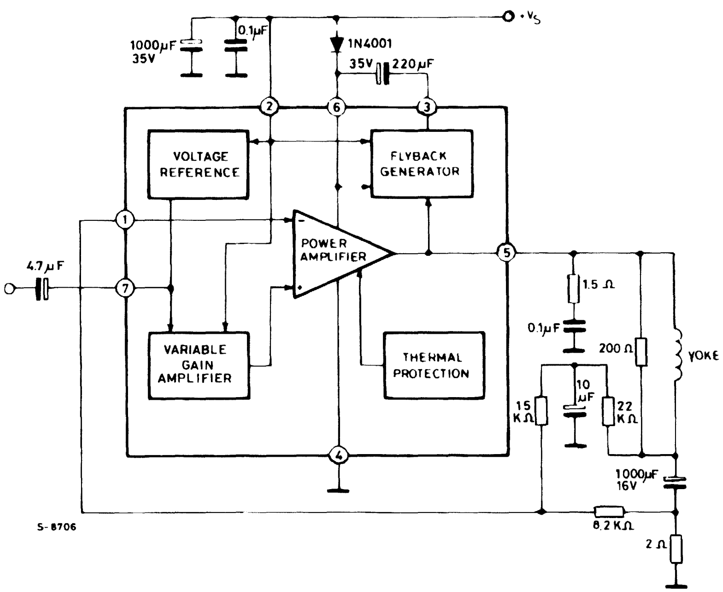
ORDER CODE : TDA8175

DESCRIPTION

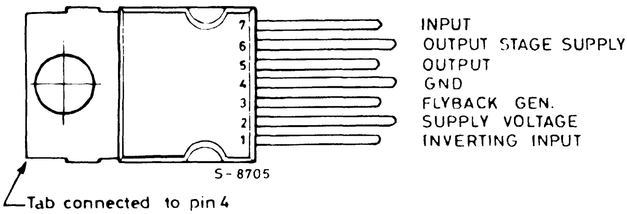
The TDA8175 is a monolithic integrated circuit in HEPTAWATT package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes.

It is intended for use in Color and B & W television sets as well as in monitors and displays.

BLOCK DIAGRAM



CONNECTION DIAGRAM (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	35	V
V_5, V_6	Flyback Peak Voltage	60	V
V_3	Voltage at Pin 3	$+ V_s$	
V_1, V_7	Amplifier Input Voltage	$+ V_s$	
I_o	Output Peak Current (non repetitive, t = 2 ms)	2.5	A
I_o	Output Peak Current at f = 50 or 60 Hz, t ≤ 10 µs	3	A
I_o	Output Peak Current at f = 50 or 60 Hz, t > 10 µs	2	A
I_3	Pin 3 DC Current at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current at f = 50 or 60 Hz, $t_{fly} \leq 1.5$ ms	3	A
P_{tot}	Total Power Dissipation at T_{case} = 70 °C	20	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j-case}$	Thermal Resistance Junction-case	Max	4	°C/W

ELECTRICAL CHARACTERISTICS (V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_2	Pin 2 Quiescent Current			18	36	mA
I_6	Pin 6 Quiescent Current			16	36	mA
I_1	Amplifier Input Bias Current	V_1 = 1 V		– 0.1	– 1	µA
V_3	Pin 3 Saturation to GND	I_3 = 20 mA		1	1.5	V
V_5	Quiescent Output Voltage	V_s = 35V R_a = 39 kΩ		19		V
V_5	Output Saturation Voltage to GND	I_5 = 1.2 A I_5 = 0.7 A		1 0.7	1.4 1	V V
V_5	Output Saturation Voltage to Supply	– I_5 = 1.2 A – I_5 = 0.7 A		1.6 1.3	2.2 1.8	V V
V_o	Ramp Amplitude Versus Voltage Supply	22 < V_s < 30 V		4		%/V
G	AC Gain	V_s = 26 V	0.54	0.61	0.67	V
V_o	DC Output Voltage Accuracy			8		%
V_7	Internal Bias			2.7		V
R_7	Input Resistance			50		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

THERMAL PROTECTION

The thermal protection circuit intervenes when the die temperature reaches 150 °C and turn off the output power device.

PUMPING COMPENSATION

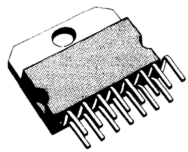
The device incorporates a special preamplifier, the gain of which varies with changes in supply voltage. This function allows perfect compensation of height variations caused by changes in brightness.

SGS-THOMSON MICROELECTRONICS

TDA8176

TV VERTICAL DEFLECTION SYSTEM FOR TV AND MONITORS

- SYNCHRONIZATION CIRCUIT
- OSCILLATOR AND RAMP GENERATOR
- HIGH POWER GAIN AMPLIFIER
- FLYBACK GENERATOR
- VOLTAGE REGULATOR



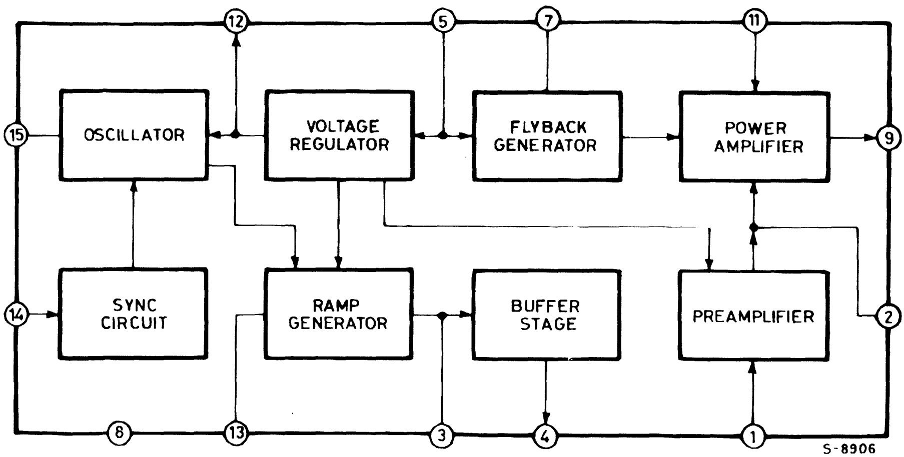
MULTIWATT 15

ORDER CODE : TDA8176

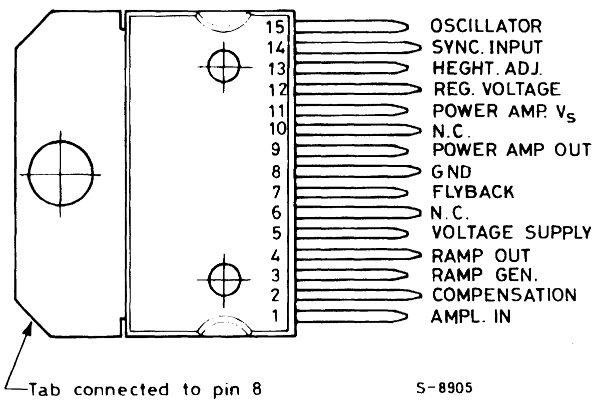
DESCRIPTION

The TDA8176 is a monolithic integrated circuit in Multiwatt 15 package. It is intended for use in color TV sets and monitors.

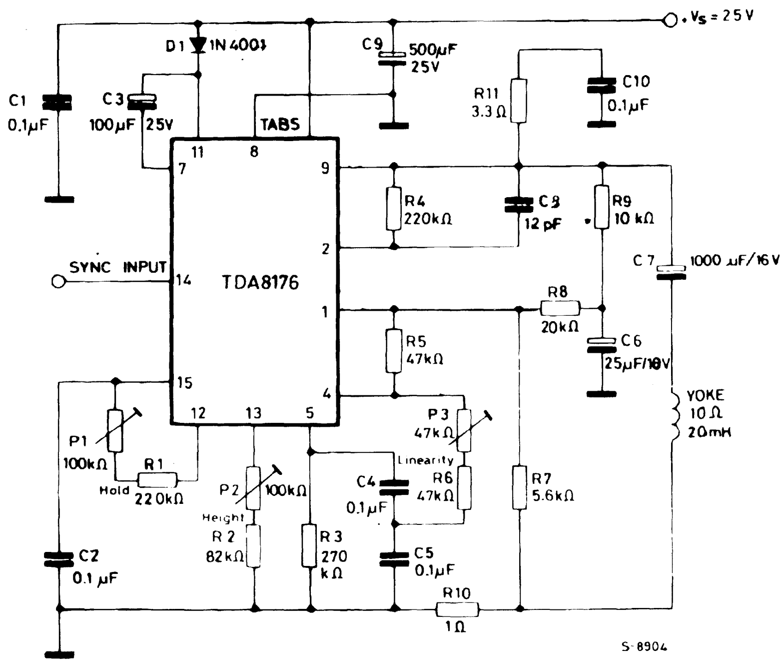
BLOCK DIAGRAM



CONNECTION DIAGRAM



AC TEST CIRCUITS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_5	Supply Voltage at Pin 2	35	V
V_4, V_5	Flyback Peak Voltage	60	V
V_{10}	Power Amplifier Input Voltage	+ 10 – 0.5	V V
I_o	Output Peak Current (non repetitive) at t = 2 ms	2	A
I_o	Output Peak Current at f = 50 Hz t ≤ 10 µs	2.5	A
I_o	Output Peak Current at f = 50 Hz t > 10 µs	1.5	A
I_3	Pin 3 DC Current at $V_4 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for f = 50 Hz, $t_{fly} \leq 1.5$ ms	1.8	A
I_8	Pin 8 Current	± 20	mA
P_{tot}	Power Dissipation : at T_{tab} = 90 °C at T_{amb} = 80 °C	20 1.4	W W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	50	°C/W

AC CHARACTERISTICS
(refer to the test circuit, V_s = 25 V ; f = 50 Hz ; T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_s	Supply Current	I_y = 1 App		140		mA
I_{14}	Sync. Input Current (positive or negative)		500			µA
V_9	Flyback Voltage	I_y = 1 App		51		V
V_{15}	Peak to peak Oscillator Sawtooth Voltage			2.4		V
t_{fly}	Flyback Time	I_y = 1 App		0.7		ms
f_o	Free Running Frequency	$(P_1 + R_1)$ = 300 KΩ C_2 = 100 nF		44		Hz
		$(P_1 + R_1)$ = 260 KΩ C_2 = 100 nF		52		Hz
Δf	Synchronization Range	I_8 = 0.5 mA	14			Hz
$\frac{\Delta f}{\Delta V_s}$	Frequency Drift with Supply Voltage	V_s = 10 to 35 V		0.005		Hz/V
$\left\lvert \frac{\Delta f}{\Delta T_{tab}} \right\rvert$	Frequency Drift with Tab Temperature	T_{tab} = 40 to 120 °C		0.01		Hz/°C

ELECTRICAL CHARACTERISTICS

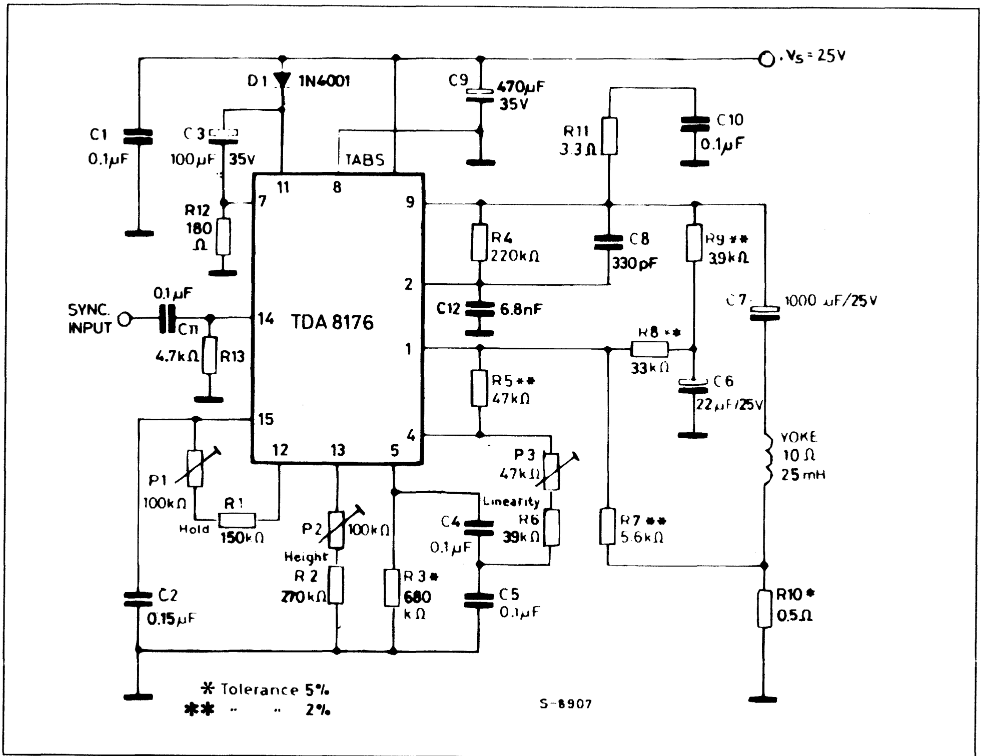
DC CHARACTERISTICS (V_s = 35 V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_5	Pin 5 Quiescent Current	$I_7 = 0$		7	14	mA
I_{11}	Pin 11 Quiescent Current	$I_9 = 0$		8	17	mA
$-I_{15}$	Oscillator Bias Current	$V_{15} = 1$ V		0.1	1	µA
$-I_1$	Amplifier Input Bias Current	$V_1 = 1$ V		0.1	10	µA
$-I_3$	Ramp Generator Bias Current	$V_3 = 0$		0.02	0.3	µA
$-I_3$	Ramp Generator Current	$I_{13} = 20$ µA $V_3 = 0$	18.5	20	21.5	µA
$\frac{\Delta I_3}{I_3}$	Ramp Generator Non-linearity	$\Delta V_{12} = 0$ to 12 V $I_{13} = 20$ µA		0.2	1	%
V_s	Supply Voltage Range		10		35	V
V_4	Pin 4 Saturation Voltage to Ground	$I_4 = 1$ mA		1	1.4	V
V_7	Pin 7 Saturation Voltage to Ground	$I_7 = 10$ mA		300	450	mV
V_9	Quiescent Output Voltage	$V_s = 10$ V $R_1 = 10$ kΩ $R_2 = 10$ kΩ	4.1	4.4	4.75	V
		$V_s = 35$ V $R_1 = 30$ kΩ $R_2 = 10$ kΩ	8.3	8.8	9.45	V
V_{9L}	Output Saturation Voltage to Ground	$-I_9 = 0.1$ A		0.9	1.2	V
		$-I_9 = 0.8$ A		1.9	2.3	V
V_{9H}	Output Saturation Voltage to Supply	$I_9 = 0.1$ A		1.4	2.1	V
		$I_9 = 0.8$ A		2.8	3.2	V
V_{12}	Regulated Voltage at Pin 12		6.1	6.5	6.9	V
V_{13}	Regulated Voltage at Pin 13	$I_{13} = 10$ µA	6.2	6.6	7	V
$\frac{\Delta V_{12}}{\Delta V_s}, \frac{\Delta V_{13}}{\Delta V_s}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_s = 10$ to 35 V		1		mV/V
V_1	Amplifier Input Reference Voltage		2.07	2.2	2.3	V
R_{14}	Pin 8 Input Resistance	$V_{14} \leq 0.4$ V	1			MΩ

TYPICAL PERFORMANCE OF THE CIRCUIT OF FIG. 1

Symbol	Parameter	Value	Unit
V_s	Operating Supply Voltage	25	V
I_s	Supply Current	175	mA
t_{fly}	Flyback Time	1	ms
P_{tot}	TDA8176 Power Dissipation	3.25	W
I_y	Maximum Scanning Current (peak to peak)	1.4	A

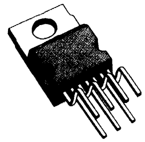
Figure 1 : Typical Application Circuit for large Screen 110° PIL TVC Set (Ry = 10 Ω ; Ly = 25 mH ; Iy = 1.25 App).



TV VERTICAL DEFLECTION BOOSTER

ADVANCE DATA

- POWER AMPLIFIER
- FLYBACK GENERATOR (105V PEAK)
- THERMAL PROTECTION
- REFERENCE VOLTAGE
- CURRENT LIMITED TO GND



Heptawatt

ORDER CODE : TDA8178

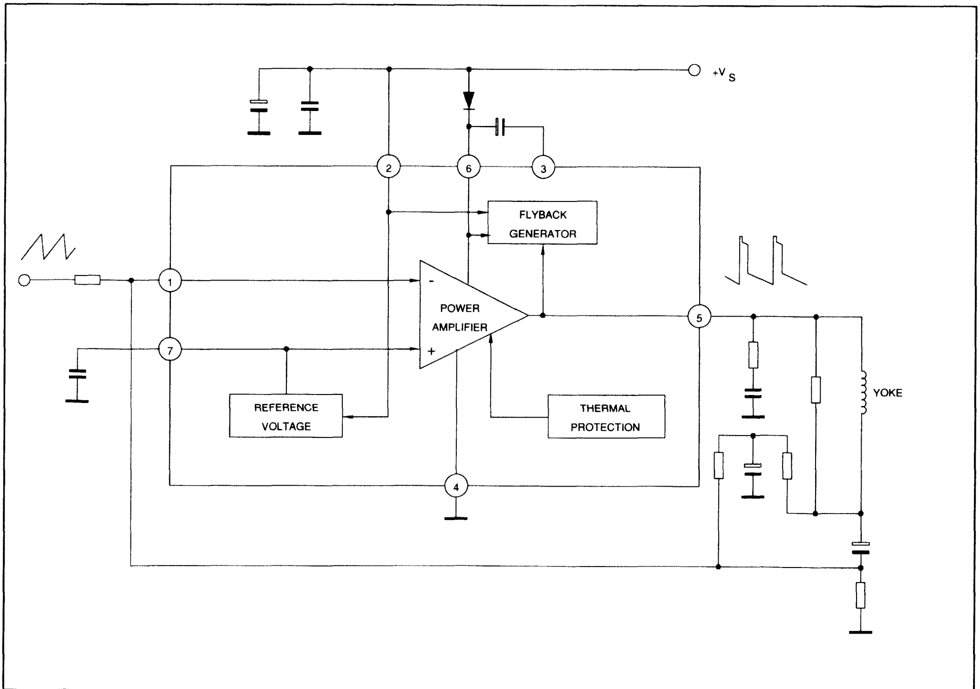
DESCRIPTION

Designed for Monitors and high performance TVs, the TDA8178 vertical deflection booster delivers flyback voltages up to 105V.

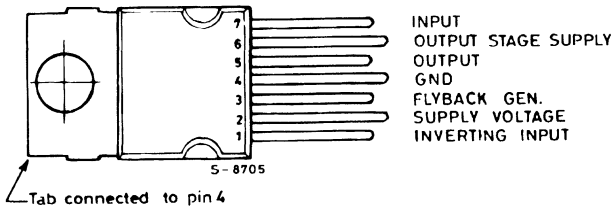
The TDA8178 operates with supplies up to 50V and provides up to 2App output current drive to yoke.

The TDA8178 is offered in HEPTAWATT package.

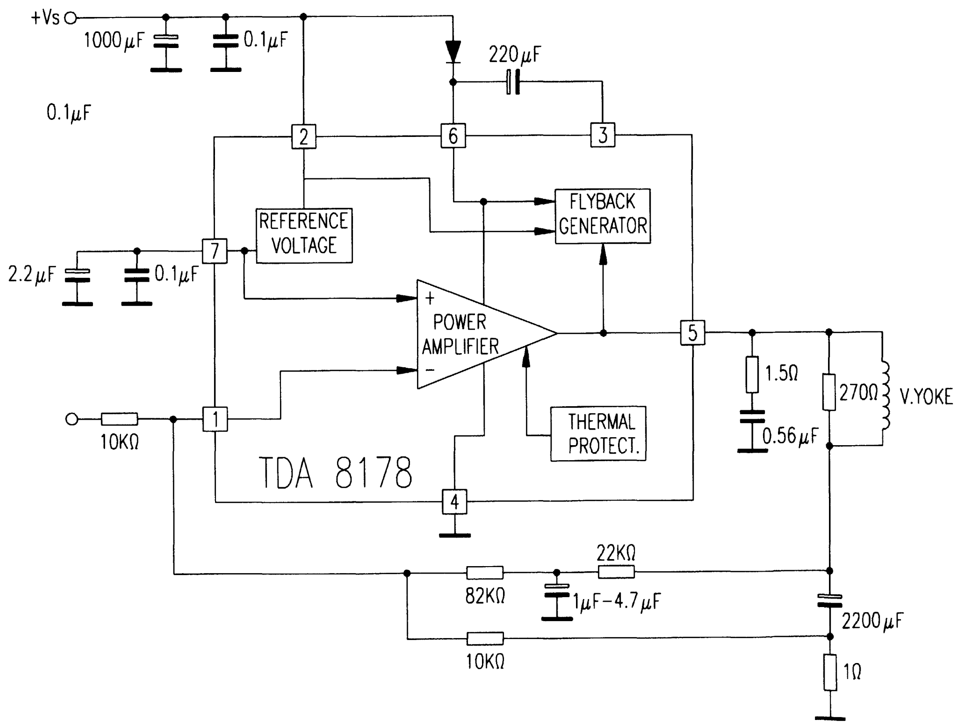
BLOCK DIAGRAM



PIN CONNECTION (top view)



APPLICATION CIRCUIT (V_S = 50V)



ELECTRICAL CHARACTERISTICS
(refer to the test circuits, V_s = 48V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage Range		10		48	V
I_2	Pin 2 Quiescent Current	$I_3 = 0$ $I_5 = 0$		10	20	mA
I_6	Pin 6 Quiescent Current	$I_3 = 0$ $I_5 = 0$		20	40	mA
I_1	Amplifier bias Current	V_1 = 1V		– 0.2	– 1	µA
V_3	Pin 3 Saturation to GND	I_3 = 20mA		1.3	1.8	V
V_5	Quiescent Output Voltage	V_s = 48V R_a = 3.9KΩ		24.2		V
		V_s = 35V R_a = 5.6KΩ		17.5		
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	$- I_5$ = 1A		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_D = 1A		1.5		V
V_{D3-2}	Diode Forward Voltage between Pins 3-2	I_D = 1A		1.5		V
V_7	Internal Reference		2.15	2.2	2.25	V
$\Delta V_7/\Delta V_s$	Reference Voltage Drift Versus V_s	V_s = 10 to 48V		1	2	mV/V
K_T	Reference Voltage Drift Versus T_j	$K_T = \frac{\Delta V_7 . 10^6}{\Delta T_j . V_7}$ T_j = 0 to 125°C		100	150	ppm/°C
R_1	Input Resistance			200		KΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

ABSOLUTE MAXIMUM RATINGS

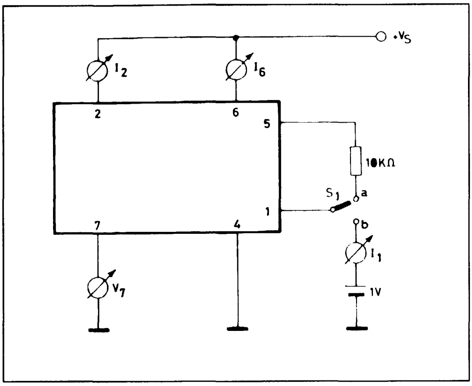
Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 2)	50	V
V_5, V_6	Flyback Peak Voltage	105	V
V_1, V_7	Amplifier Input Voltage	+ V_s	
I_O	Output Peak Current (non repetitive, t = 2ms)	2	A
I_O	Output Peak Current at f = 50 or 60Hz $t \leq 10\mu s$	2	A
I_O	Output Peak Current at f = 50 or 60Hz $t > 10\mu s$	1.8	A
I_3	Pin 3 DC at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq 1.5ms$	1.8	A
P_{tot}	Total Power Dissipation at T_{case} = 70°C	20	W
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}c}$	Junction-case Thermal Resistance	Max	3	°C/W

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_1 ; I_2 ; I_6 ; V_7 ; $\Delta V_7/\Delta V_S$.



S1 : (a) I_2 and I_6 ; (b) I_1.

Figure 1b : Measurement of V_{5H}.

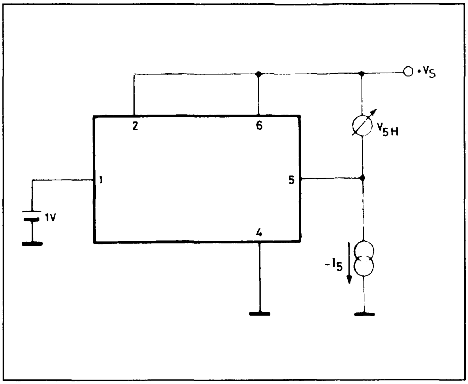
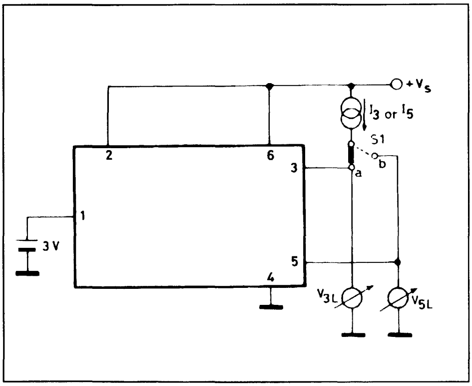


Figure 1c : Measurement of V_{3L}, V_{5L}.



S1 : (a) V_{3L} ; (b) V_{5L}.

Figure 1d : Measurement of V_5.

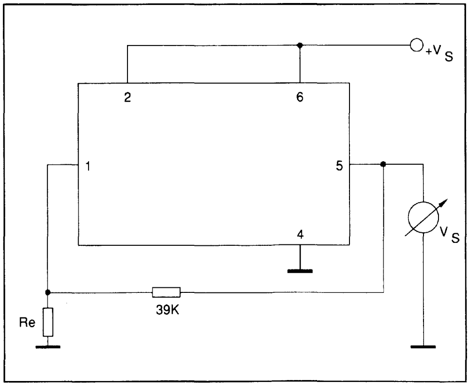
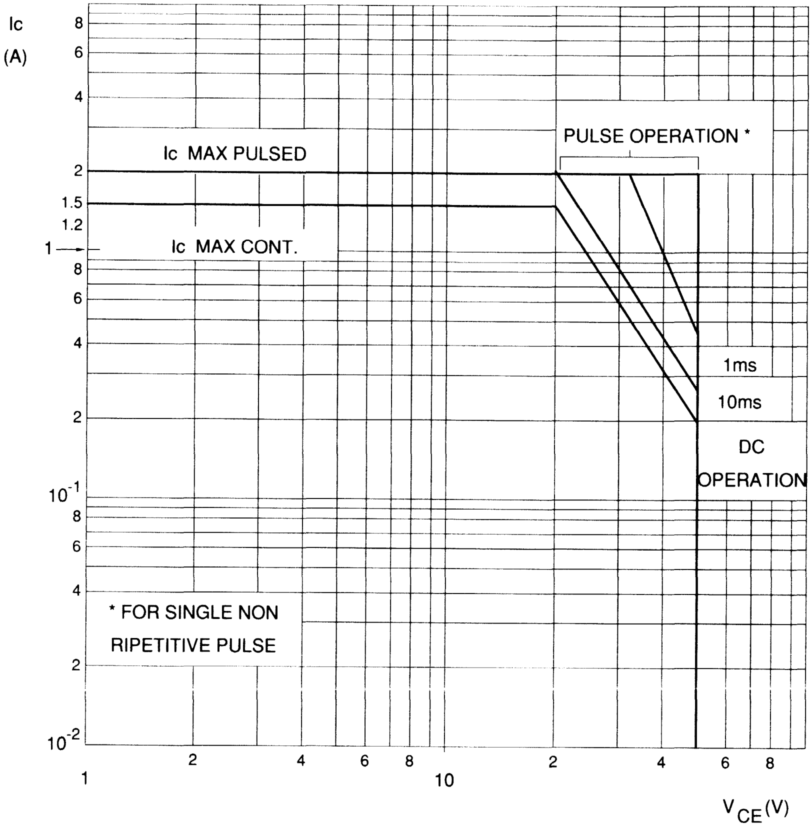


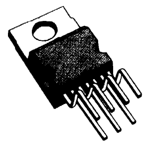
Figure 2 : SOA of Each Output Power Transistor at 25°C amb.



TV VERTICAL DEFLECTION BOOSTER

ADVANCE DATA

- POWER AMPLIFIER
- FLYBACK SUPPLY VOLTAGE SEPARATED
- THERMAL PROTECTION
- REFERENCE VOLTAGE
- CURRENT LIMITED TO GND



Heptawatt

ORDER CODE : TDA8178F

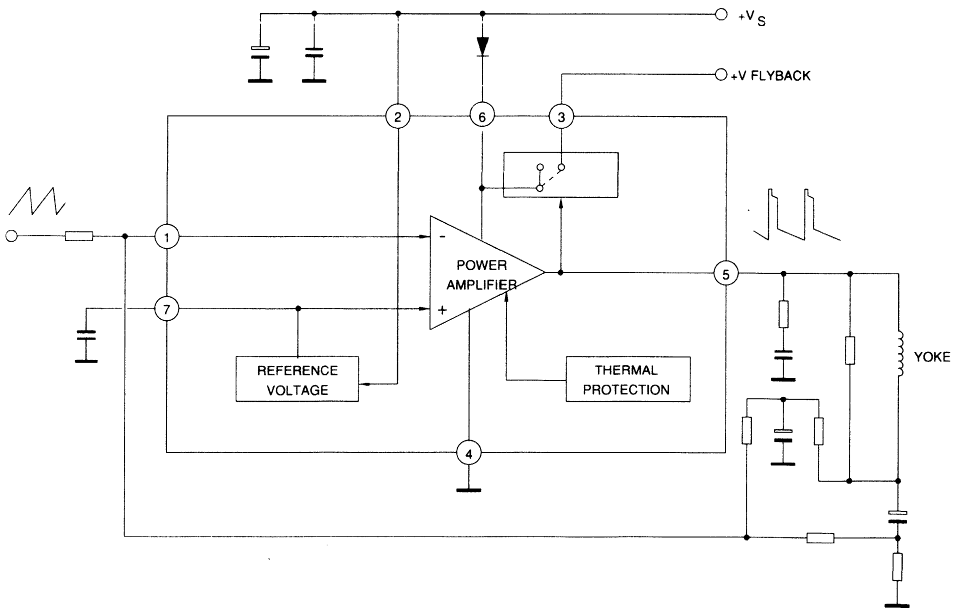
DESCRIPTION

Designed for Monitors and high performance TVs, the TDA8178F vertical deflection booster is able to work with a flyback voltage more than the double of Vs.

The TDA8178F operates with supplies up to 50V, Flyback supply voltage up to 100V and provides up to 2App output current to drive to yoke.

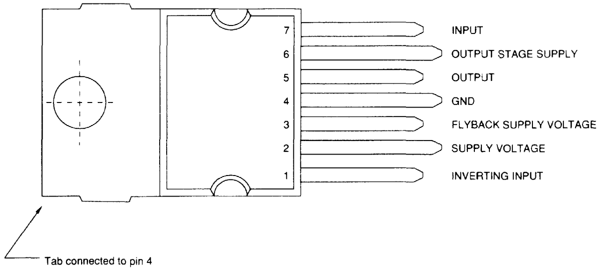
The TDA8178F is offered in HEPTAWATT package.

BLOCK DIAGRAM

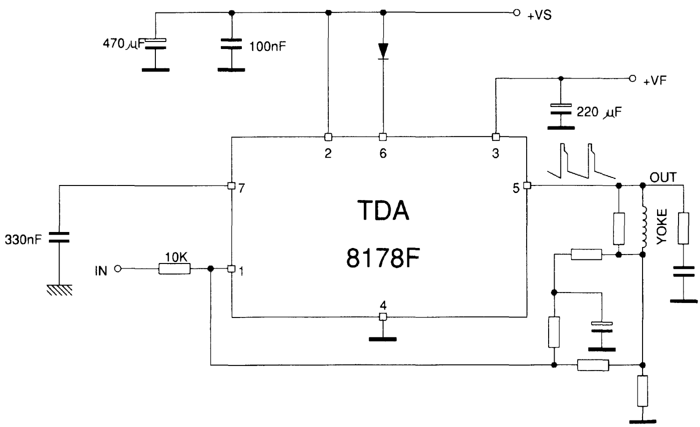


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 2)	50	V
V_f	Flyback Supply Voltage	100	V
V_F-V_S	Difference between Flyback Supply Voltage and Supply Voltage	50	V
V_1, V_7	Amplifier Input Voltage	+ V_s	
I_O	Output Peak Current (non repetitive, t = 2ms)	2	A
I_O	Output Peak Current at f = 50 or 60Hz t ≤ 10μs	2	A
I_O	Output Peak Current at f = 50 or 60Hz t > 10μs	1.8	A
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, t_{fly} ≤ 1.5ms	1.8	A
P_{tot}	Total Power Dissipation at T_{case} = 70°C	20	W
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

THERMAL DATA

$R_{th\ J\text{-}C}$	Thermal Resistance Junction-case Max	3	°C/W

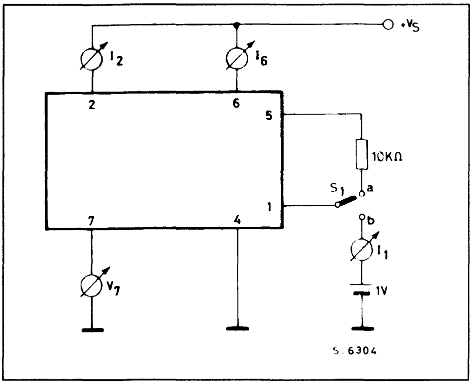
ELECTRICAL CHARACTERISTICS

(refer to the test circuits, V_s = 48V, T_{amb} = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_s	Operating Supply Voltage Range		10		48	V	
I_2	Pin 2 Quiescent Current	I_3 = 0 I_5 = 0		10	20	mA	1a
I_6	Pin 6 Quiescent Current	I_3 = 0 I_5 = 0		20	40	mA	1a
I_1	Amplifier bias Current	V_1 = 1V		– 0.2	– 1	μA	1a
V_5	Quiescent Output Voltage	V_s = 48V R_a = 3.9KΩ		24.2		V	1d
		V_s = 35V R_a = 5.6KΩ		17.5			
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V	1c
V_{5H}	Output Saturation Voltage to Supply	– I_5 = 1A		2.2	2.6	V	1b
$V_{D5\text{-}6}$	Forward Voltage Diode between Pin 5-6	I_D = 1A		1.5		V	
$V_{D3\text{-}6}$	Forward Voltage Diode between Pin 3-6	I_3 = 1A		2		V	
V_7	Internal Reference		2.15	2.2	2.25	V	1a
$\Delta V_7/\Delta V_s$	Reference Voltage Drift Versus V_s	V_s = 15 to 50V		1	2	mV/V	1a
K_T	Reference Voltage Drift Versus T_j	$K_T = \frac{\Delta V_7 . 10^6}{\Delta T_j . V_7}$ Tj = 0 to 125°C		100	150	ppm/°C	1a
R_1	Input Resistance			200		KΩ	
T_j	Junction Temperature for Thermal Shutdown			140		°C	

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_1 ; I_2 ; I_6 ; V_7 ; $\Delta V_7/\Delta V_S$.



S_1 : (a) I_2 and I_6 ; (b) I_1.

Figure 1b : Measurement of V_{5H}.

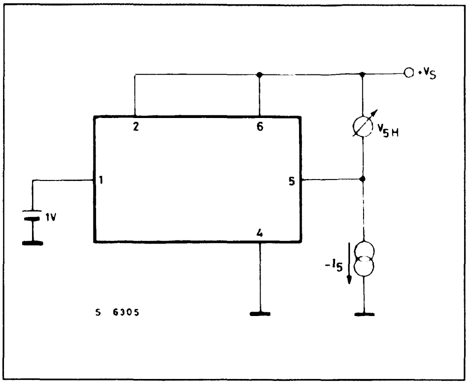


Figure 1c : Measurement of V_{5L}.

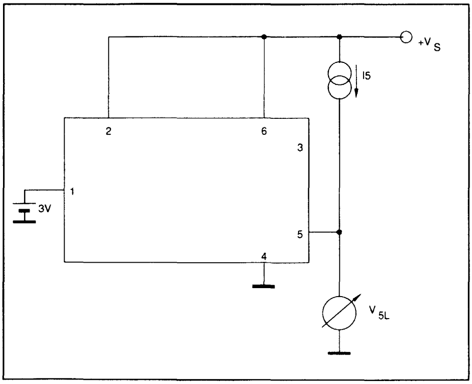


Figure 1d : Measurement of V_5.

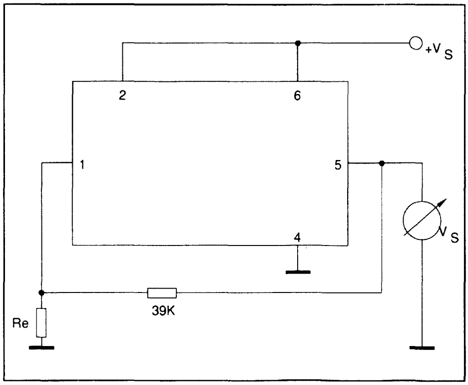


Figure 1e : Measurement of Crossover Distorsion.

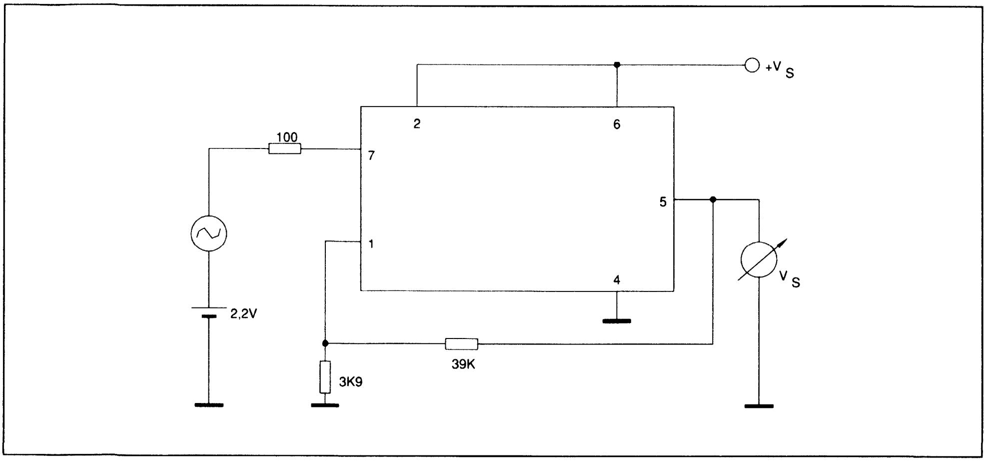
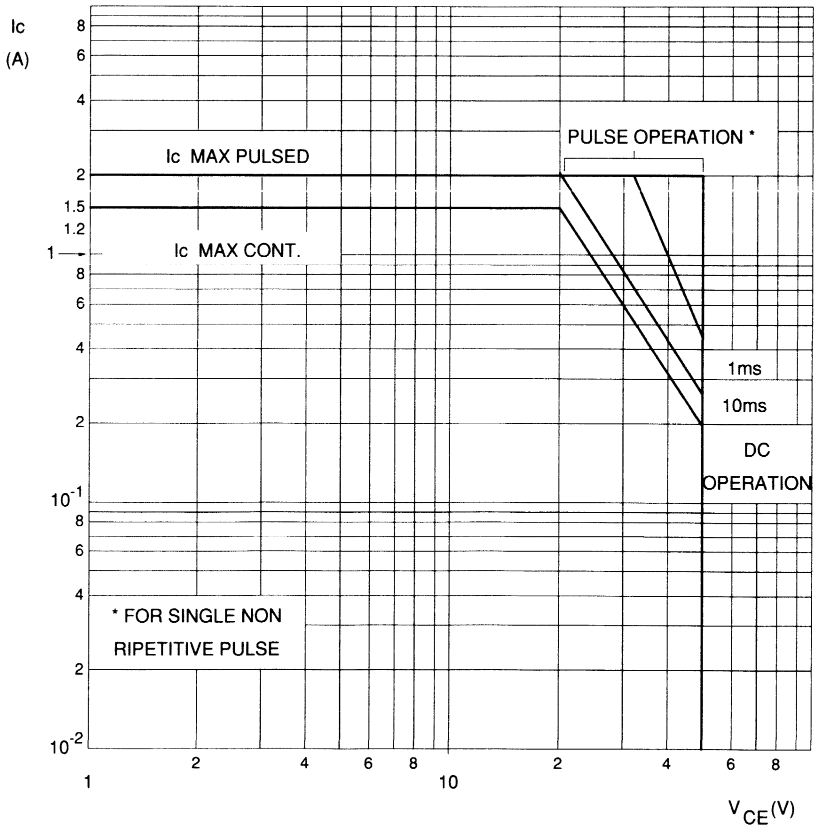


Figure 2 : SOA of Each Output Power Transistor at 25°C amb.



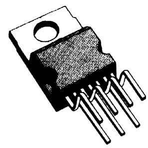
SGS-THOMSON MICROELECTRONICS

TDA8179

TV VERTICAL DEFLECTION BOOSTER

ADVANCE DATA

- POWER AMPLIFIER
- FLYBACK GENERATOR (105V PEAK)
- THERMAL PROTECTION
- CURRENT LIMITED TO GND



HEPTAWATT

ORDER CODE : TDA8179

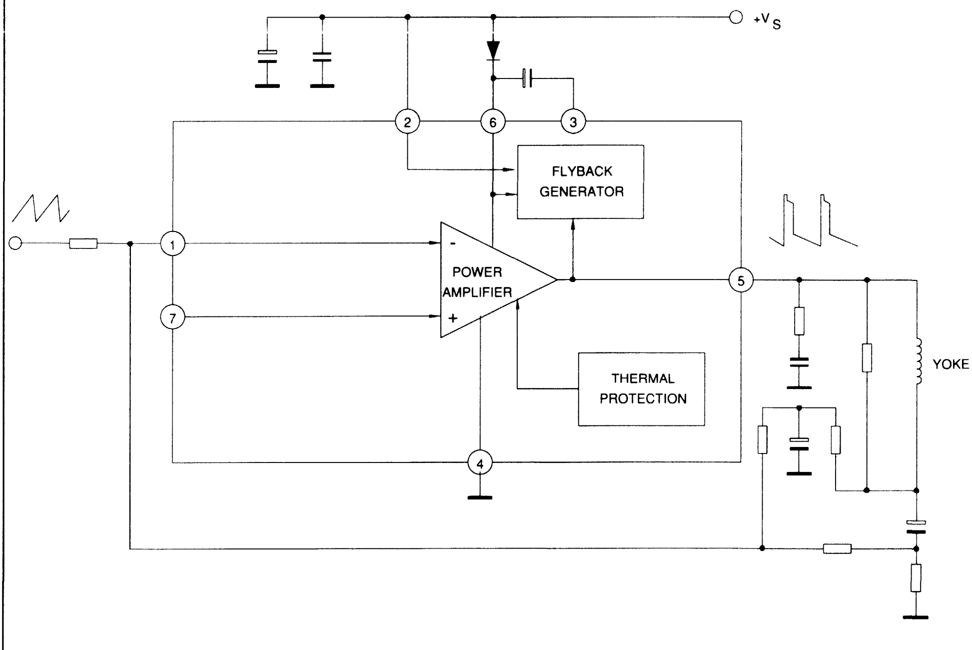
DESCRIPTION

Designed for Monitors and high performance TVs, the TDA8179 vertical deflection booster delivers fly-back voltages up to 105V.

The TDA8179 operates with supplies up to 50V and provides up to 2App output current to drive to yoke.

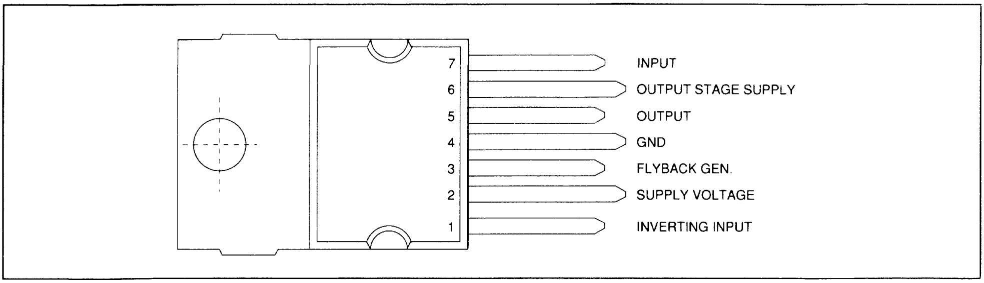
The TDA8179 is offered in HEPTAWATT package.

BLOCK DIAGRAM

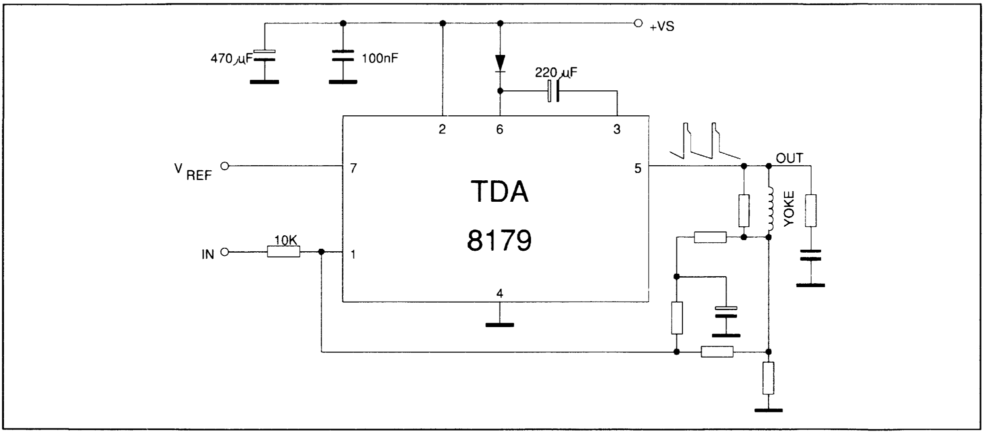


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 2)	50	V
V_5, V_6	Flyback Peak Voltage	105	V
V_1, V_7	Amplifier Input Voltage	+ V_s	
I_O	Output Peak Current (non repetitive, t = 2ms)	2	A
I_O	Output Peak Current at f = 50 or 60Hz t ≤ 10µs	2	A
I_O	Output Peak Current at f = 50 or 60Hz t > 10µs	1.8	A
I_3	Pin 3 DC at $V_5 < V_2$	100	mA
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq$ 1.5ms	1.8	A
P_{tot}	Total Power Dissipation at T_{case} = 70°C	20	W
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

THERMAL DATA

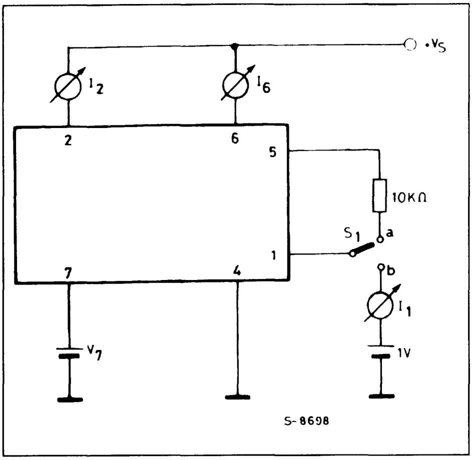
$R_{th\ J\text{-}C}$	Junction-case Thermal Resistance	Max 4	°C/W

ELECTRICAL CHARACTERISTICS
(V_7 = 2.2V, V_s = 48V, T_{amb} = 25°C, unless otherwise specified) (refer to the test circuits)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage Range		10		48	V
I_2	Pin 2 Quiescent Current	I_3 = 0 I_5 = 0		10	20	mA
I_6	Pin 6 Quiescent Current	I_3 = 0 I_5 = 0		20	40	mA
I_1	Amplifier bias Current	V_1 = 1V		– 0.2	– 1	µA
V_{3L}	Scanning Voltage	I_3 = 20mA		1.3	1.8	V
V_5	Quiescent Output Voltage	V_s = 48V R_a = 3.9KΩ		24.2		V
		V_s = 35V R_a = 5.6KΩ		17.5		
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	– I_5 = 1A		2.2	2.8	V
$V_{D5\text{-}6}$	Diode Forward Voltage between Pins 5-6	I_D = 1A		1.5		V
$V_{D3\text{-}2}$	Diode Forward Voltage between Pins 3-2	I_D = 1A		1.5		V
R_1	Input Resistance			200		KΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_1 ; I_2 ; I_6.



S_1 : (a) I_2 and I_6 ; (b) I_1.

Figure 1b : Measurement of V_{5H}.

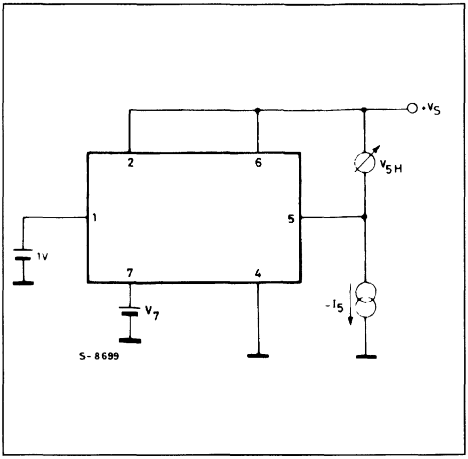
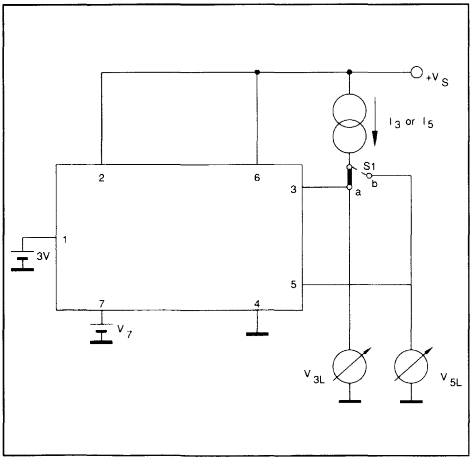


Figure 1c : Measurement of V_{3L} ; V_{5L}.



S1 : (a) V_{3L} ; (b) V_{5L}.

Figure 1d : Measurement of V_5.

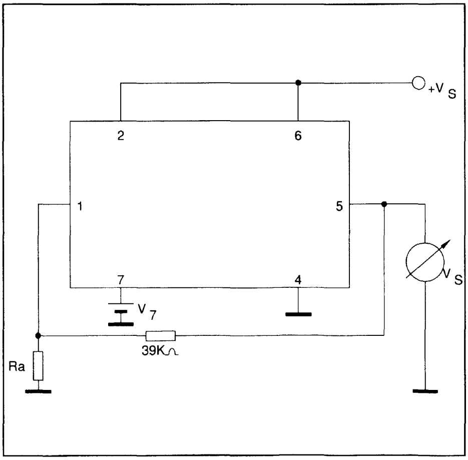
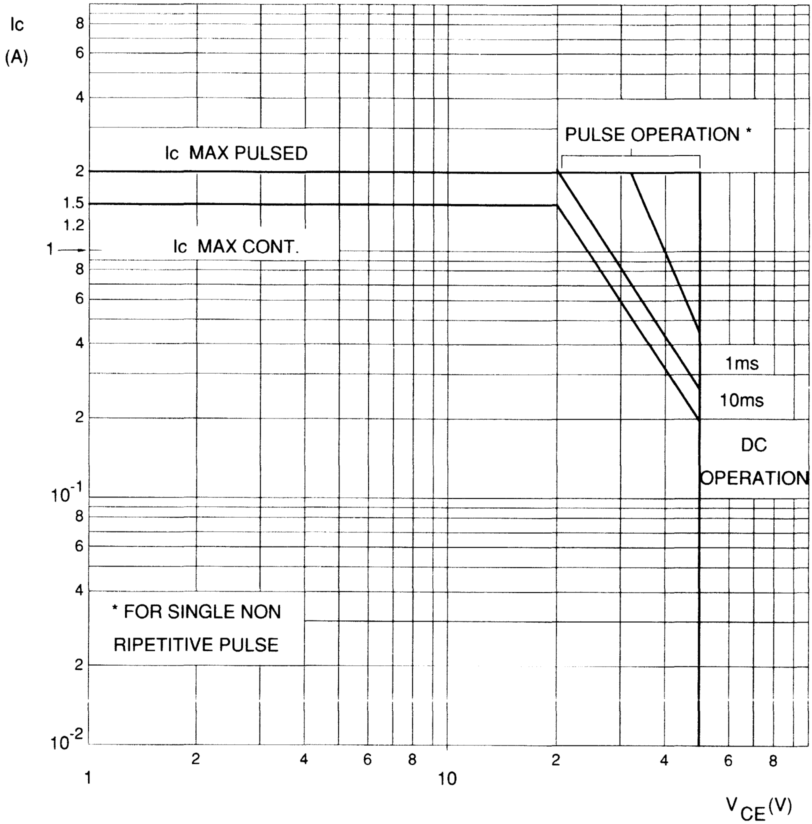


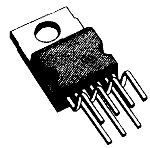
Figure 2 : SOA of Each Output Power Transistor at 25°C amb.



TV VERTICAL DEFLECTION BOOSTER

ADVANCE DATA

- POWER AMPLIFIER
- FLYBACK SUPPLY VOLTAGE SEPARATED
- THERMAL PROTECTION
- CURRENT LIMITED TO GND



HEPTAWATT

ORDER CODE : TDA8179F

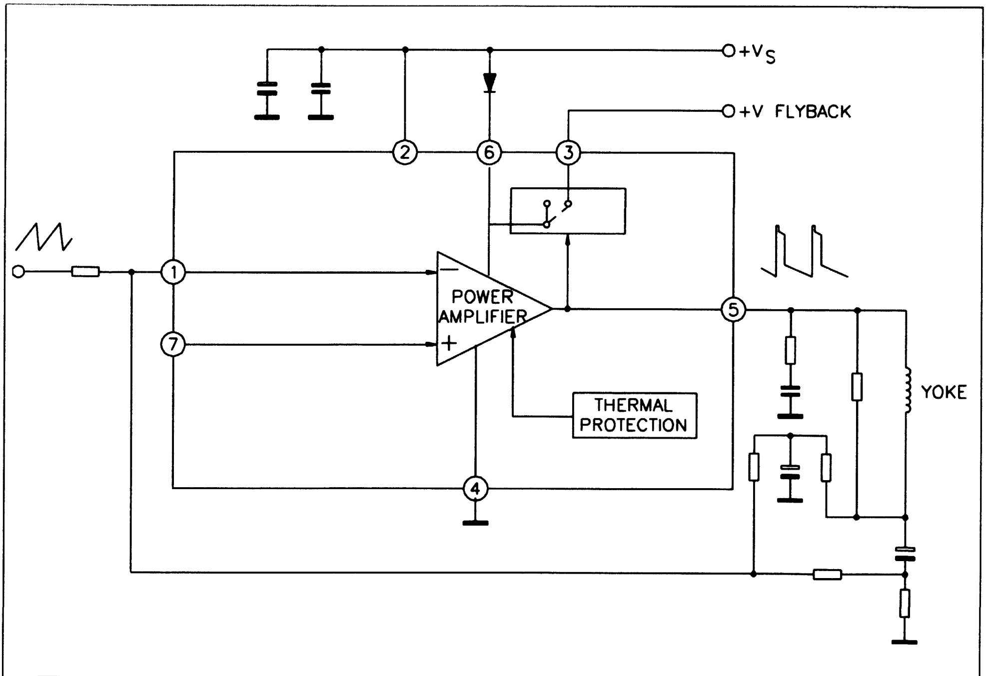
DESCRIPTION

Designed for Monitors and high performance TVs, the TDA8179F vertical deflection booster is able to work with a flyback voltage more than the double at Vs.

The TDA8179F operates with supplies up to 50V, flyback supply voltage up to 100V and provides up to 2App output current to drive to yoke.

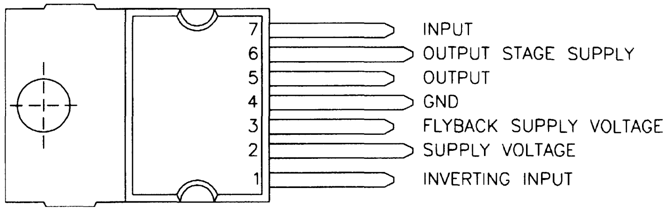
The TDA8179F is offered in HEPTAWATT package.

BLOCK DIAGRAM

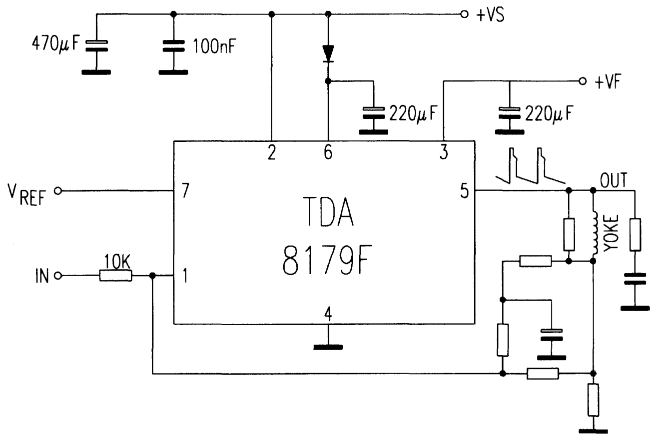


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN CONNECTION (top view)



APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 2)	50	V
V_F	Flyback Supply Voltage	100	V
V_F-V_s	Difference between Flyback Supply Voltage and Supply Voltage	50	V
V_1, V_7	Amplifier Input Voltage	+ V_s	
I_O	Output Peak Current (non repetitive, t = 2ms)	2	A
I_O	Output Peak Current at f = 50 or 60Hz t ≤ 10µs	2	A
I_O	Output Peak Current at f = 50 or 60Hz t > 10µs	1.8	A
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, t_{fly} ≤ 1.5ms	1.8	A
P_{tot}	Total Power Dissipation at T_{case} = 70°C	20	W
T_{stg}	Storage Temperature	– 40 to 150	°C
T_j	Junction Temperature	0 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}c}$	Thermal Resistance Junction-case	Max 3	°C/W

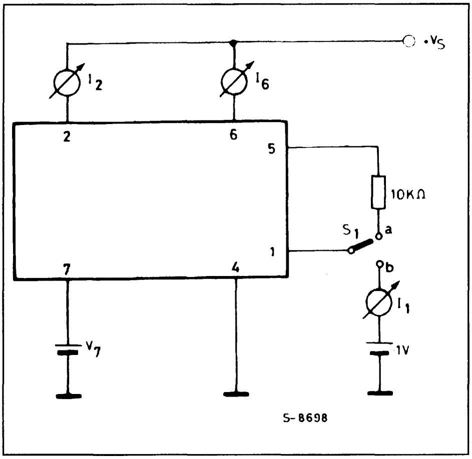
ELECTRICAL CHARACTERISTICS

(V_7 = 2.2V, V_s = 48V, T_{amb} = 25°C, unless otherwise specified, refer to the test circuits)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Operating Supply Voltage Range		10		48	V
I_2	Pin 2 Quiescent Current	I_3 = 0 I_5 = 0		10	20	mA
I_6	Pin 6 Quiescent Current	I_3 = 0 I_5 = 0		20	40	mA
I_1	Amplifier bias Current	V_1 = 1V		– 0.2	– 1	µA
V_5	Quiescent Output Voltage	V_s = 48V R_a = 3.9KΩ		24.2		V
		V_s = 35V R_a = 5.6KΩ		17.5		
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	– I_5 = 1A		2.2	2.6	V
$V_{D5\text{-}6}$	Diode Forward Voltage between Pin 5-6	I_D = 1A		1.5		V
$V_{D3\text{-}6}$	Diode Forward Voltage between Pin 3-6	I_3 = 1A		2		V
R_1	Input Resistance			200		KΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

Figure 1 : DC Test Circuits.

Figure 1a : Measurement of I_1 ; I_2 ; I_6.



S1 : (a) I_2 and I_6 ; (b) I_1.

Figure 1b : Measurement of V_{5H}.

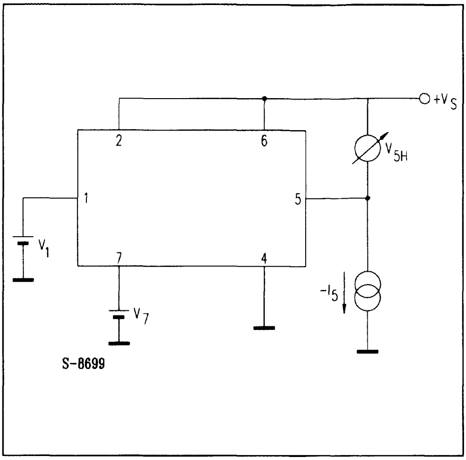


Figure 1c : Measurement of V_{5L}.

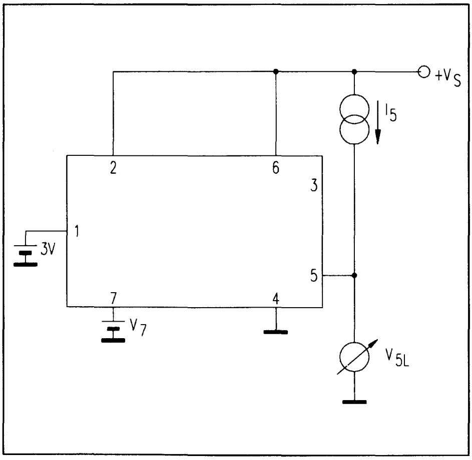


Figure 1d : Measurement of V_5.

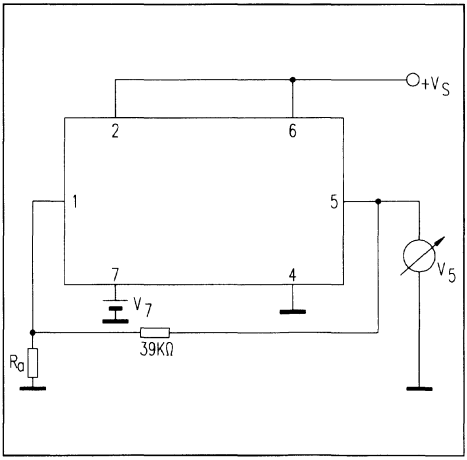
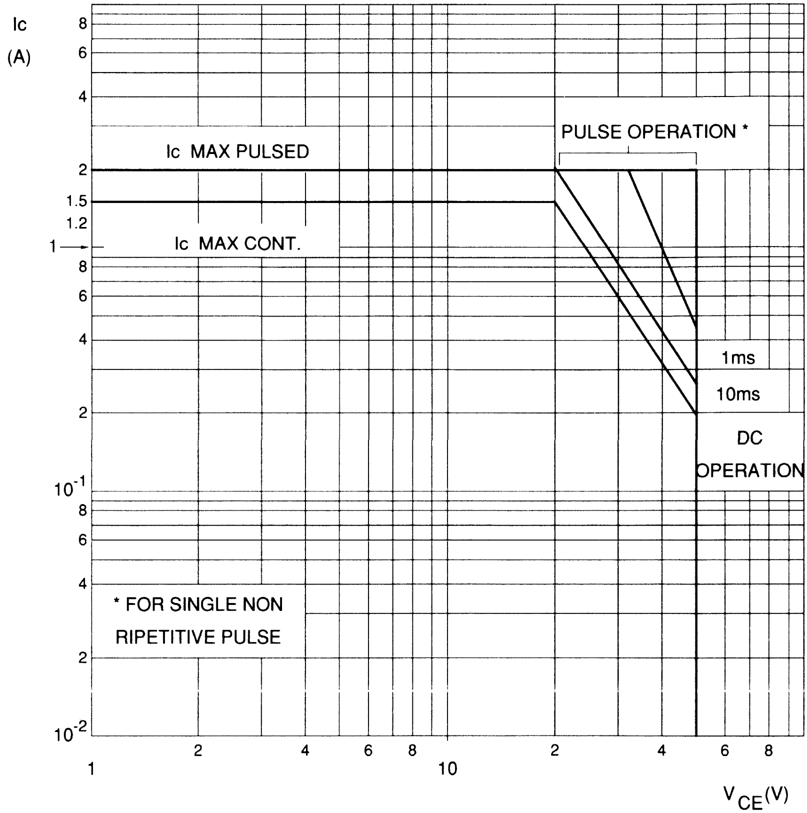


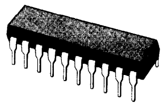
Figure 2 : SOA of Each Output Power Transistor at 25°C amb.



HORIZONTAL AND VERTICAL DEFLECTION

ADVANCE DATA

- 503KHz REFERENCE OSCILLATOR
- 5.5 SUPPLY VOLTAGE INTERNALLY REGULATED
- COUNTDOWN TIMING LOGIC
- ADAPTS AUTOMATICALLY TO 625 LINE 50Hz AND 525 LINE/60Hz STANDARDS
- 50/60Hz IDENTIFICATION OUTPUT
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY-CYCLE
- SUPER-SANDCASTLE DIGITALLY PERFORMED
- CRT PROTECTION



DIP20

DESCRIPTION

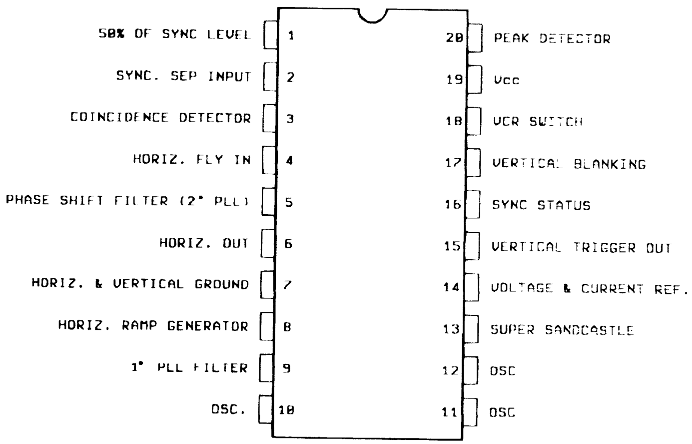
The TDA8181 deflection processor integrates the signal processing functions for horizontal and vertical deflection in TVs and monitors.

It generates drive waveforms for external deflection power stages plus super-sandcastle and separated vertical blanking signal for the chroma processor.

A 5V supply is used and only a series resistor is needed for higher voltage.

An high sensitivity sync separator with 50% sync. Threshold level, PLL and countdown circuitry guarantee high precision and eliminate all frequency adjustments.

PIN CONNECTIONS



TDA8181-1::DIS

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

ELECTRICAL CHARACTERISTICS
(V_S = 5V, V_{CC} = 12V ; T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 19)		4.75	5	5.25	V
I_S	Supply Current (pin 19)		45	60	75	mA
V_{19}	Stabilizied Volt. (pin 19)	With Series Resistor 82Ω	5.3	5.7	6.2	V

SYNC SEPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_2	Peak to Peak Input Signal	Negative Video Signal	0.3	1	4	V

VIDEO IDENTIFICATION AND VCR SWITCH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{18}	VCR Switch Voltage		1.6	2.1	2.4	V
V_3	Threshold Vol. for PLL Gain Switch			2.3		V
I_3	Peak Output Current	Lock Condition		1		mA
$-I_3$	Sink Current			20		μA

OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_O	Free Running Frequency			500		Kz
S_O	Freq. Control Sens.			1		KHz/V
V_9	Control Voltage Range			2.6 to 4		V

SYNC OSCILLATOR PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_9	Control Peak Current			± 0.3		mA
I_9	VCR Control Peak Current			± 0.6		mA
Δf	Catching & Holding Range			± 400		Hz

FLYBACK - OSCILLATOR PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_4	Flyback Thresh. Volt.			1.4		V
V_4	Clamp Voltage			5		V
I_4	Input Current				1	mA
V_5	Control Voltage Range			2.8 to 3.7		V
I_5	Peak Control Current			± 0.5		mA
	Static Control Error			1		%
td	Permiss. Delay between Out Pulse and Flyback	t Flayback 12μsec t out Pulse 29μsec			17	μs

ELECTRICAL CHARACTERISTICS (continued)

SUPER SAND CASTLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_K	Key Pulse Peak Volt.	Res. to V_{CC} 4.7K		10		V
V_L	Line Blanking Voltage		4.25	4.5	4.75	V
V_F	Frame Blanking Volt.		2.38	2.5	2.63	V
t_{Ks}	Phase Relationship between Leading Edge of Key Pulse and the Middle of Video Sync Pulse			2.5		µsec
t_K	Key Pulse Duration			4		µsec
tF	Vertica Blanking Duration			1.4		msec

FRAME

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V15	Saturation Voltage	Pull-up Resistor = 10KΩ		0.3		V
V15	High Level			12		V
tV	Vertical Trigger Output Duration			64		µsec

LINE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
– I6				50		mA
V6	Saturation Voltage	– I6 = 50mA		0.4		V
tL	Output Pulse Duration	(see test circuit)		29		µsec

SYNC STATUS VOLTAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V16	Output Voltage	50Hz		12		V
		60Hz	6.25	7	7.45	V
		UNLOCK			0.3	V

OVERRAL PHASE RELATIONSHIP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
to	Phase Differences between Middle of Flyback and the Middle of Sync. Pulse			2		µsec

VERTICAL BLANKING OUT AND FLY INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V17	Blanking Out Voltage			4		V
tF	Vertical Blank. Duration			1.4		µsec
V17	Flayback Threshould IN			5.7		V
I17	Flayback Curr. IN		0.1			mA

ELECTRICAL CHARACTERISTICS (continued)

VOLTAGE A CURRENT REFERENCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V14	Voltage Reference			3.3		V
I8	Horiz. Sawtooth Output Current	(R14 to GND = 5.6KΩ)		60		μA

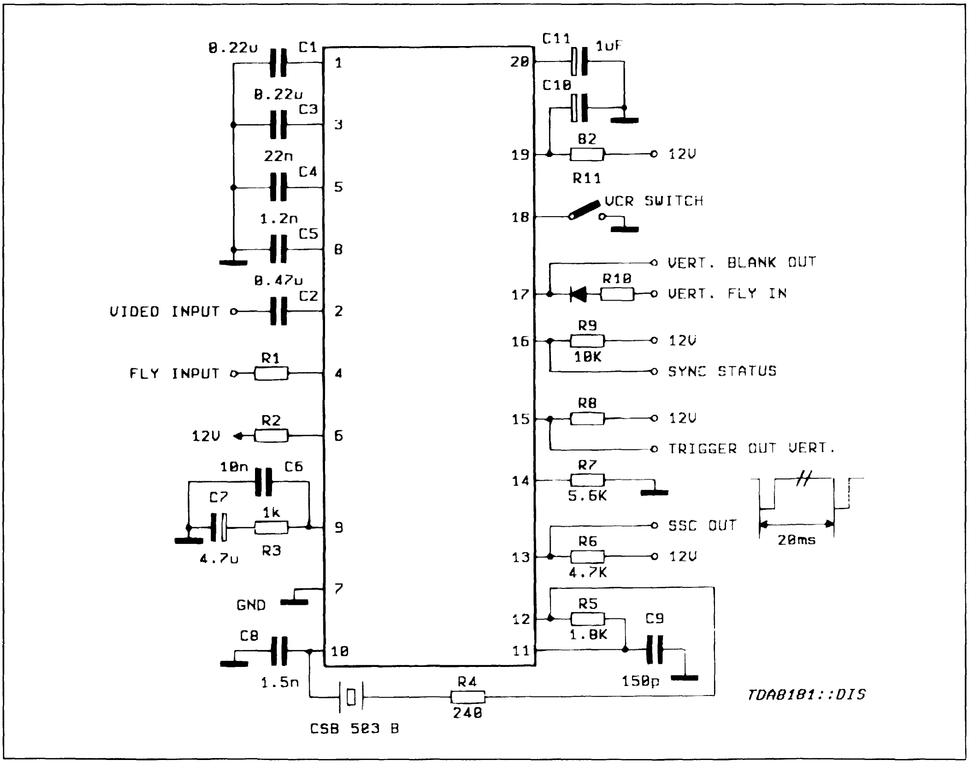
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 19 (without series resistor)	5.25	V
V_{CC}	Voltage at Pins 6, 13, 15, 16	20	V
V_i	Input Signals	5	V
P_{tot}	Total Power Dissipation (T_{amb} = 70°C)	1	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-case	80	°C/W

TEST CIRCUIT

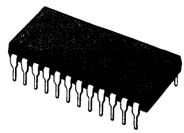


SGS-THOMSON MICROELECTRONICS

TDA8185

HORIZONTAL AND VERTICAL PROCESSOR

- 503 KHz REFERENCE OSCILLATOR
- 5.5 V SUPPLY VOLTAGE INTERNALLY REGULATED
- VERY SOPHISTICATED SYNC. SEPARATOR
- COUNT DOWN TIMING LOGIC
- ADAPTS AUTOMATICALLY TO 625 LINE/50 Hz AND 525 LINE/60 Hz STANDARDS
- 50/60 Hz IDENTIFICATION OUTPUT
- AUTOMATIC VERTICAL AMPLITUDE CORRECTION 50/60 Hz
- CRT PROTECTION CIRCUIT
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY CYCLE



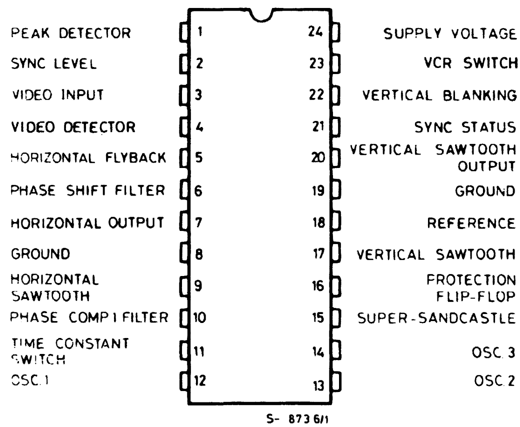
DIP-24

ORDER CODE : TDA8185

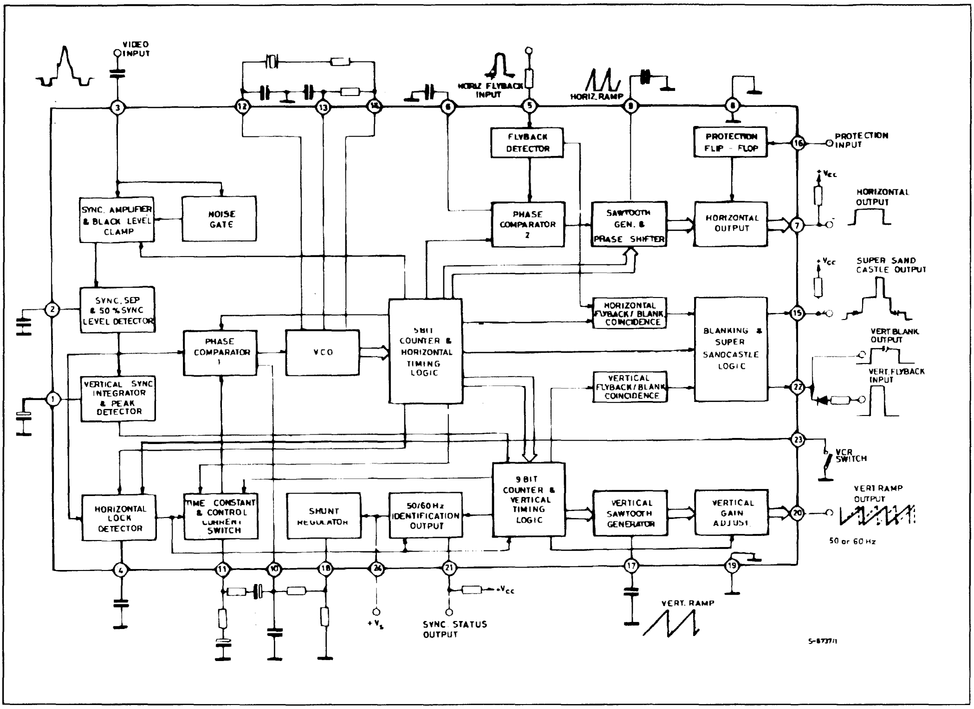
DESCRIPTION

The TDA8185 is a monolithic integrated circuit in 24 pins dual in line plastic package intended for TV signal processing and driving Horizontal and Vertical output stages. It was specially designed for VCR working conditions.

CONNECTION DIAGRAM (top view)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage at Pin 24 (low impedance)	5.25	V
V_{CC}	Voltage at Pins, 7, 15, 21	20	V
V_I	Input Signals	5	V
P_{tot}	Total Power Dissipation (T_{amb} = 70 °C)	1	W
T_j, T_{stg}	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	80	°C

ELECTRICAL CHARACTERISTICS (V_S = 5 V, V_{CC} = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 24)		4.75	5	5.25	V
I_s	Supply Current (pin 24)		30	60	85	mA
V_{24}	Stabilized Voltage at Pin 24			5.6		V

SYNC. SEPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_3	Peak to Peak Input Signal (negative video signal)		0.3	1	4	V

VIDEO IDENTIFICATION AND VCR SWITCH

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{23}	VCR Switch Voltage		1.6	2.1	2.4	V
V_4	Threshold Voltage for Time Constant Switching			2.3		V
I_4	Peak Output Current	Lock		1		mA
$-I_4$	Output Current			25		µA

OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_O	Free Running Frequency			500		kHz
S_O	Frequency Control Sensitivity			2.2		kHz/V
V_{10}	Control Voltage Range			2.6 to 4		V

SYNC–OSCILLATOR PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{10}	Control Peak Curent			± 0.3		mA
I_{10}	VCR Control Peak Current			± 0.6		mA
Δf	Catching and Holding Range			± 40		Hz

FLYBACK – OSCILLATOR PHASE COMPARATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_6	Control Voltage Range			2.8 to 3.7		V
I_5	Flyback Input Current		0.1			mA
	Flyback Input Threshold			5		mA
I_6	Peak Control Current			± 0.5		mA
	Static Control Error			1		%
t_d	Permissible Delay between Output Pulse and Flyback Pulse	$t_{flyback}$ = 12 µs		17		µs

ELECTRICAL CHARACTERISTICS (continued)

COMPOSITE BLANKING AND KEY PULSE (supersandcastle)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_K	Key Pulse Output Peak Voltage			10		V
V_L	Line Blanking Voltage		4.25	4.5	4.75	V
V_F	Frame Blanking Voltage		2.38	2.5	2.63	V
t_{KS}	Phase Relationship between Leading Edge of Key Pulse and Middle of Sync. Pulse			2.4		µs
t_K	Key Pulse Duration			4		µs
t_F	Vertical Blanking Duration			1.4		ms

FRAME

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{20}	Output p.p. Sawtooth Voltage	50 Hz and 60 Hz		2.7		V
V_{20}	Pedestal Voltage			0.3		V

LINE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_7	Output Current			50		mA
V_7	Saturation Voltage	I_7 = 50 mA		0.4		V
t_L	Output Pulse Duration			29		µs

SYNC. STATUS OUTPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{21}	Output Voltage	50 Hz		12		V
		60 Hz		7		V
		Unlock		0.2		V

OVERALL PHASE RELATIONSHIP

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_O	Phase Difference between Middle of Flyback and Middle of Sync. Pulses			2		µs

VERTICAL BLANKING OUT AND FLY. INPUT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{22}	Blanking Output Voltage			4		V
V_{22}	Flyback Threshold Input			5.7		V
I_{22}	Flyback Current Input		0.1			mA

Notes : 1. With t_{fly} = 12 µs and t_l = 29 µs.
2. The TDA8185 may be operated on a 5 V supply directly. A 5.5 V shunt regulator is available internally for operation on higher supply voltage ; in this case an external limiting resistor is required.
Without the external limiting resistor care must be taken to ensure that the supply voltage does not exceed 5.5 V or the regulator will intervene and the decice could be damaged.

Figure 1 : Horizontal and Vertical Deflections for 30AX C.R.T.

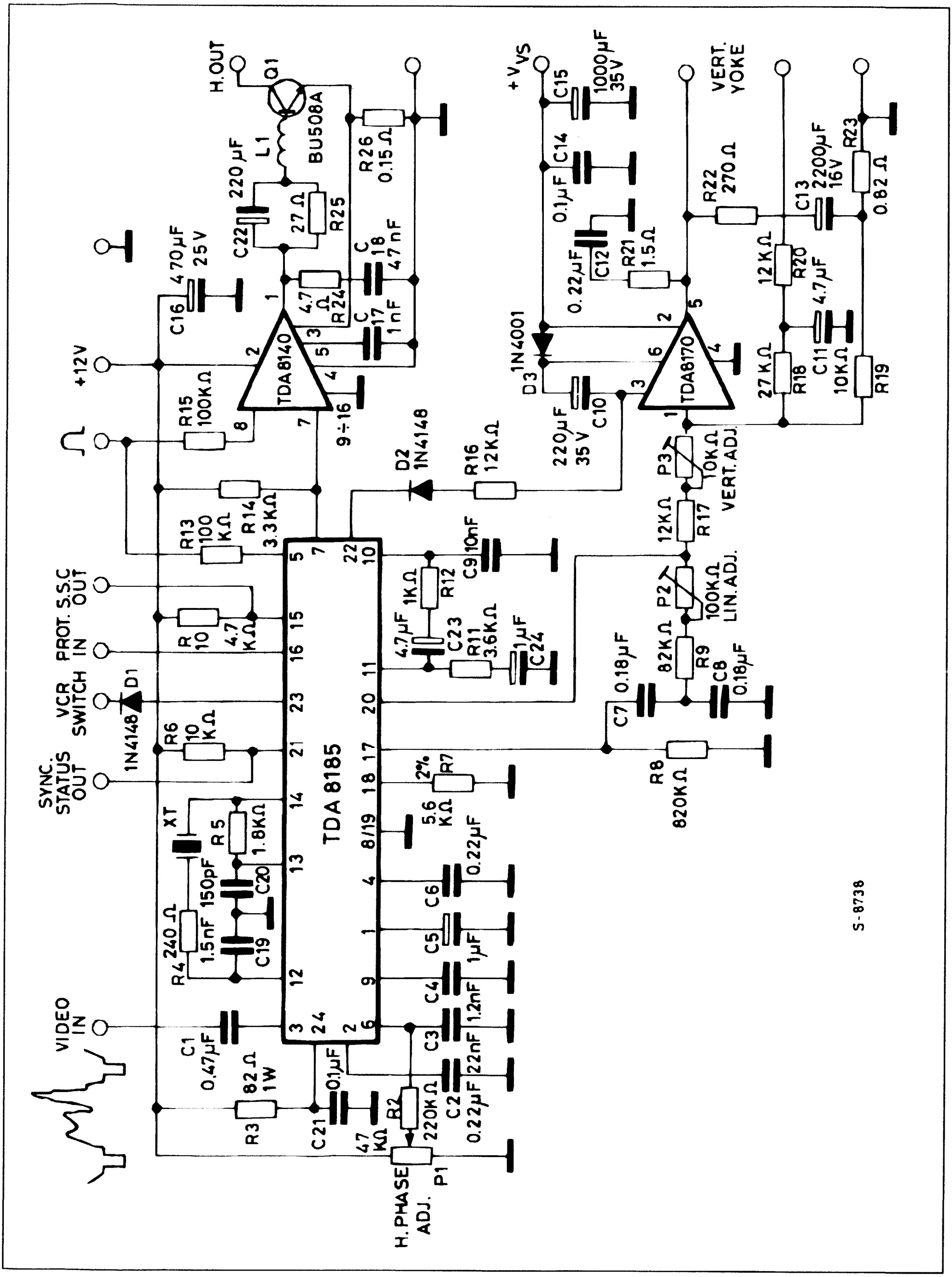


Figure 2 : Horizontal and Vertical Deflection for S4 C.R.T.

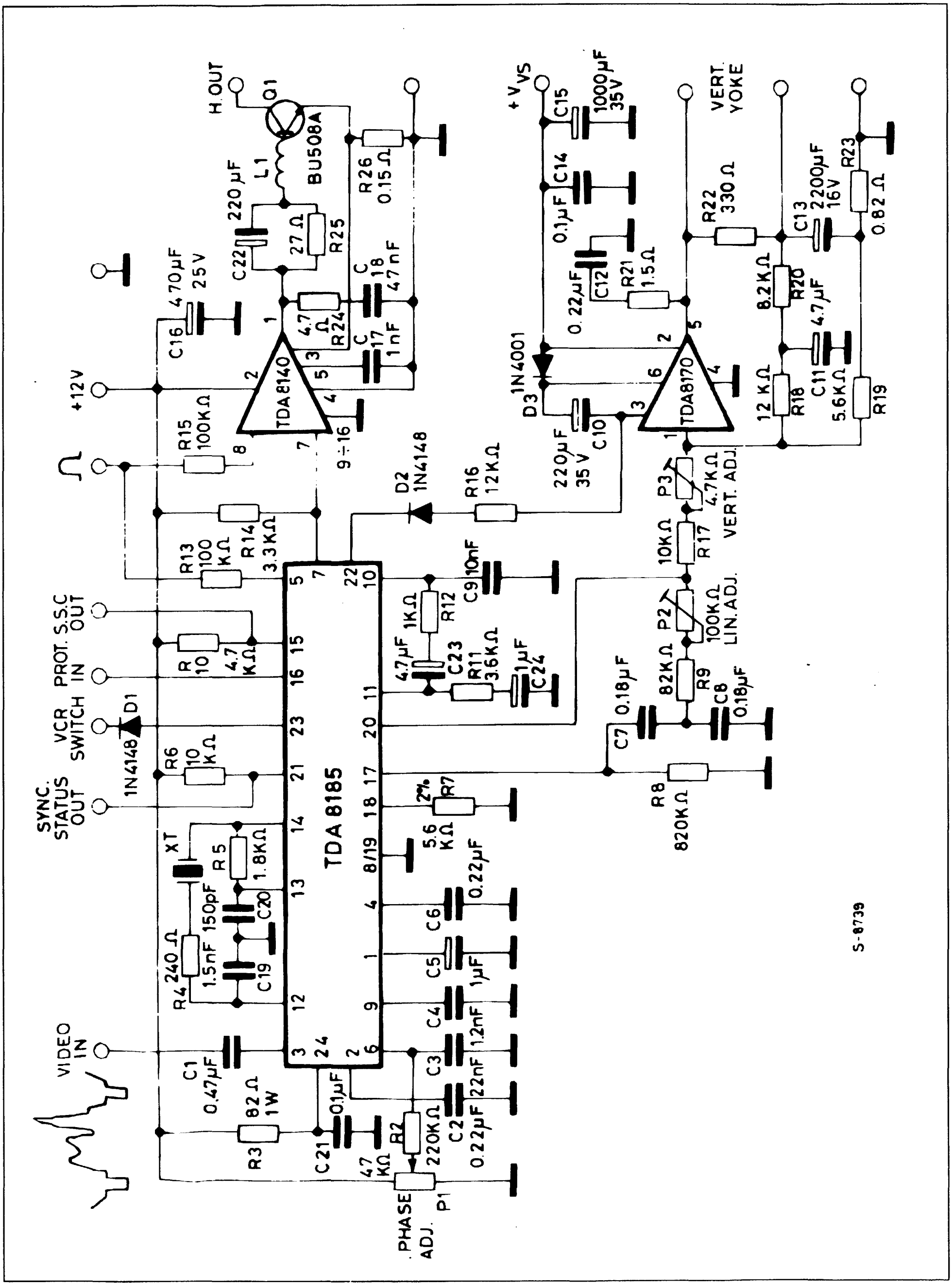
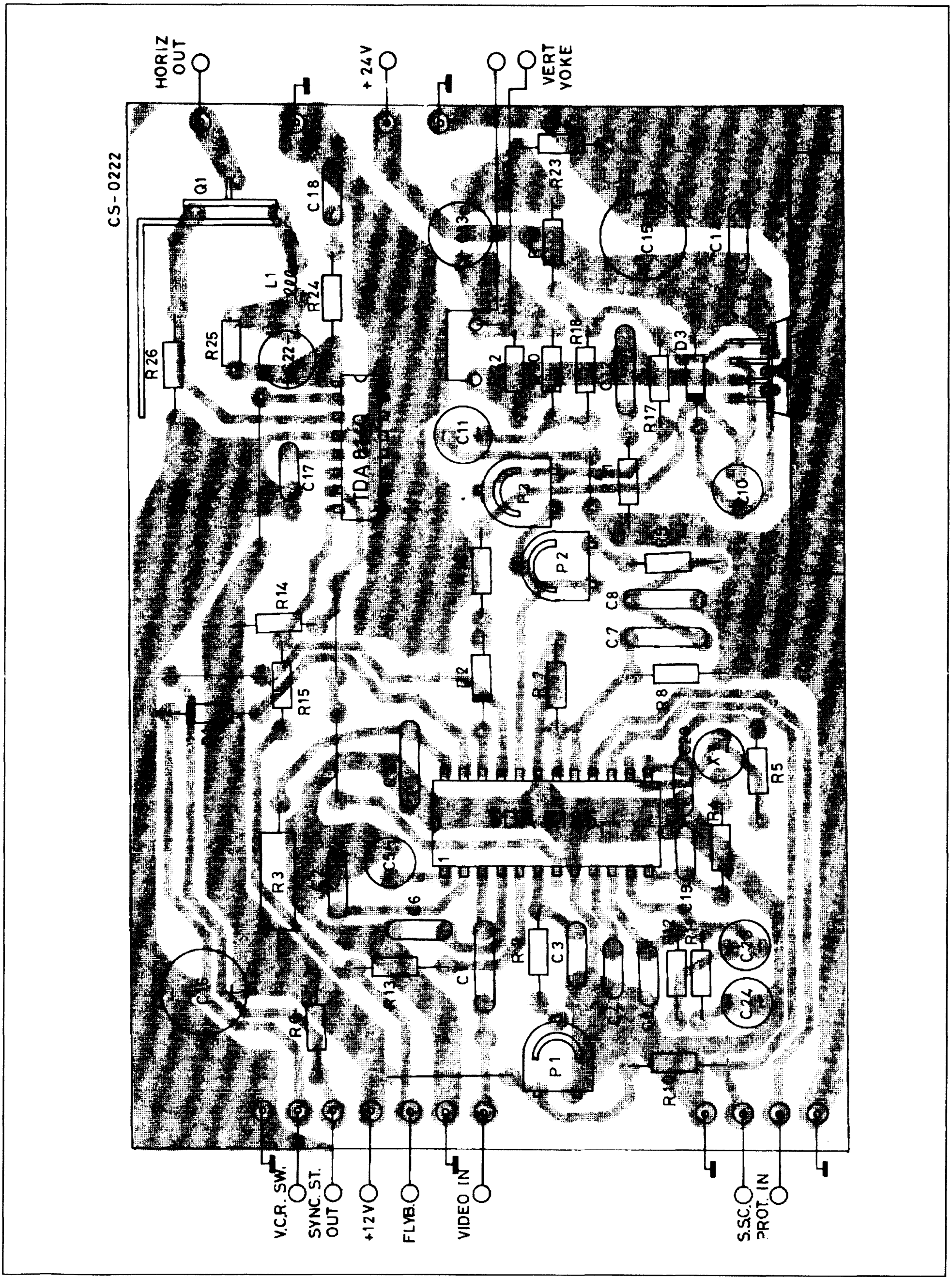


Figure 3 : P.C. Board and Components Layout of the Circuit of Fig. 2 (1:1 scale).



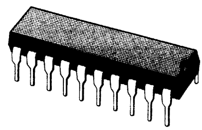
TV SOUND CHANNEL WITH DC CONTROLS

- SEPARATE VCR INPUT AND OUTPUT PINS
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

DESCRIPTION

The TDA8190 is a complete TV sound channel with DC tone and volume controls plus separate VCR input and output connections. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, V_S = 24V) or 1.5W into 8Ω (d = 10%, V_S = 12V). Included in the TDA8190 are : IF amplifier limiter, active low-pass filter, AF pre-amplifier and power amplifier, turn-off muting, mute circuit and thermal protection.

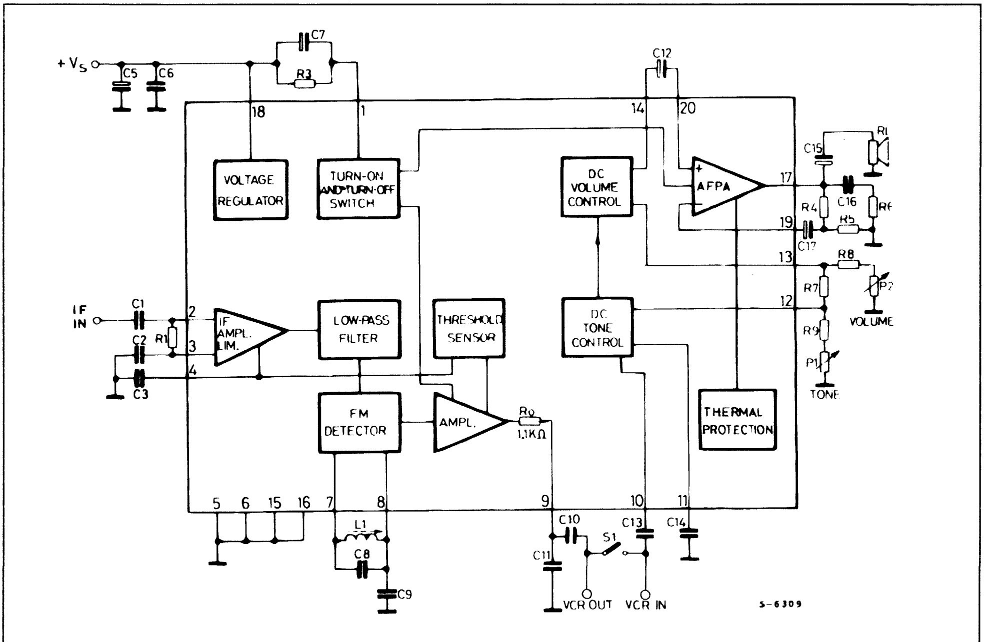
High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.



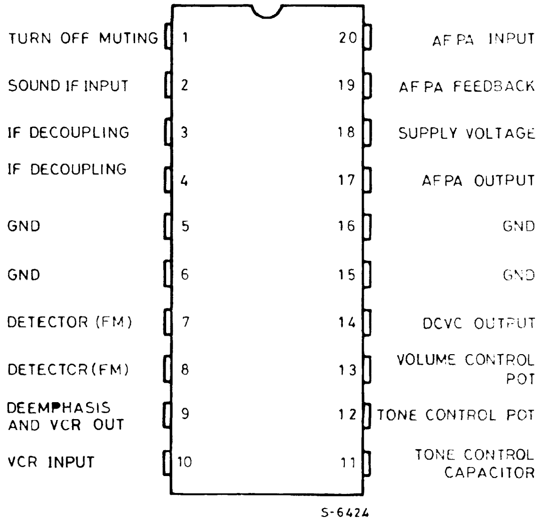
DIP20

ORDER CODE : TDA8190

BLOCK DIAGRAM



CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 18)	28	V
V_l	Voltage at Pin 1	$\pm V_s$	
V_i	Input Voltage (pin 2)	1	V_{pp}
I_o	Output Peak Current (repetitive)	1.5	A
I_o	Output Peak Current (non repetitive)	2	A
I_4	Current (pin 4)	10	mA
P_{tot}	Power Dissipation at T_{pins} = 90 °C at T_{amb} = 70 °C	4.3 1	W W
T_{stg} - T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W*

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_S = 24 V, S1 : on, Δf = ± 25 KHz, V_I = 1mV, P_1 = 12 KΩ, f_o = 4.5 MHz, f_m = 400 Hz, T_{amb} = 25 °C, unless otherwise specified).

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage (pin 18)	P_2 = 12 kΩ	10.8		27	V
V_o	Quiescent Output Voltage (pin 17)		11	12	13	
V_1	Pin 1 DC Voltage	P_2 = 12 kΩ R_1 = 270 kΩ		5.3		V
V_4	Pin 4 DC Voltage	P_2 = 12 kΩ		3.2		V
I_d	Quiescent Drain Current			32		mA

IF AMPLIFIER AND DETECTOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{i\,(threshold)}$	Input Limiting Voltage at Pin 2 (– 3 dB)	V_o = 4 V_{rms}		50	100	µV
V_9	Recovered Audio Voltage (pin 9)	Δf = ± 7.5 kHz P_2 = 12 kΩ	140	200	280	mV
AMR	Amplitude Modulation Rejection (*)	m = 0.3 ; V_i = 1 mV ; V_o = 4 V_{rms}		60		dB
R_i	Input Resistance (pin 2)	Δf = 0 P_2 = 12 kΩ		30		kΩ
C_i	Input Capacitance (pin 2)			6		pF
R_9	Deemphasis Resistance	C_1 = 68 to 888 nF	0.75	1.1	1.5	kΩ

DC VOLUME CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_v	Volume Attenuation (resistance control)	P_2 = 0 Ω P_2 = 4.3 kΩ P_2 = 12 kΩ	20	0 26 88	32	dB dB dB
V_c	Control Voltage	K = 0 dB K = 26 dB K = 88 dB		0 1.3 2.6		V V V
$\frac{\Delta K_v}{\Delta T_{pins}}$	Volume Attenuation Thermal Drift (resistance control)	T_{pins} 25 to 85 °C P_2 = 4.3 kΩ		– 0.05		dB/°C

DC TONE CONTROL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_T	Tone Cut	S1 : Off V_{10} = 200 mV P_1 = 12 kΩ to 100 Ω f_{AF} = 10 kHz		14		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO FREQUENCY AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
P_o	Output Power (d = 10 %)	V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω	3.5	4.1 1.5		W W
B	Frequency Response of Audio Amplifier (– 3 dB)	P_o = 1 W R_L = 16 Ω S1 : Off V_{10} = 200 mV V_o = 4 Vrms @400 Hz	15	50		kHz
SVR	Supply Voltage Rejection	P_2 = 12 kΩ Δf = 0 f_{ripple} = 120 Hz		26		dB

V. C. R.

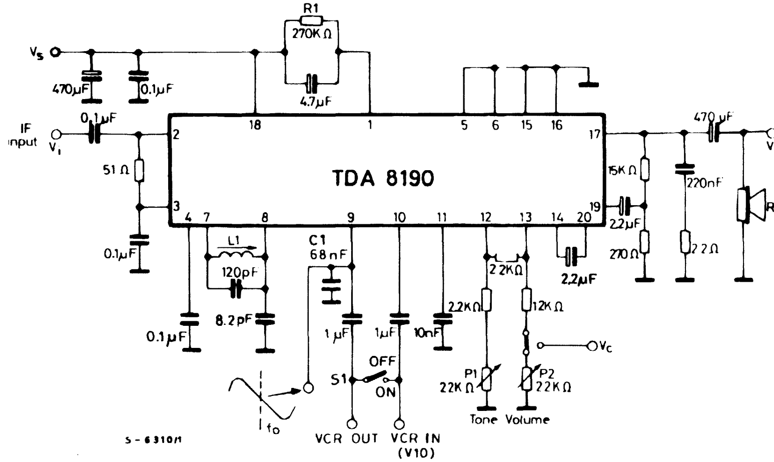
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
d	Total Harmonic Distortion of pin 9 Output Signal	Δf = ± 7.5 kHz V_i = 1 mV		0.5		%
SVR	Supply Voltage Rejection at Output Pin 9	Δf = 0 ; f_{ripple} = 120 Hz P_2 = 12 kΩ		66		dB
$\frac{S+N}{N}$	Signal and Noise to Noise Ratio at Output Pin 9	Δf = 25 kHz $V_i \geq$ 1 mV		70		dB
V_{10}	Input Voltage (playback)	V_o = 4 V_{rms} P_2 = 0 S1 : Off	50	70	100	mV
R_{10}	Input Resistance (playback)	S1 : Off	10			kΩ
	Total Harmonic Distortion for 20 dB Overload of V_{10}	S1 : Off V_{10} = 1 V_{rms} V_o = 4 V_{rms}		0.5	2	%

OVERALL CIRCUIT

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\frac{S+N}{N}$	Signal to Noise Ratio (*)	$V_i \geq$ 1 mV V_o = 4 V_{rms} Δf = 0		70		dB
d	Distortion (*)	P_o = 50 mW Δf = ± 7.5 Hz V_s = 24 V R_L = 16 Ω V_s = 12 V R_L = 8 Ω		 0.5 0.5		 % %
M	Muting (*)	V_o = 4 V_{rms}@ no V_1 ; V_1 = 0	100			dB
Δf	Deviation Sensitivity	P_2 = 0 V_o = 4 V_{rms}		3	6	kHz

* Test Bandwidth = 20KHz.

TEST CIRCUIT



TEST CONDITIONS (unless otherwise specified)

$V_S = 24V$; $Q_o = 60$; $f_o = 4.5MHz$;

$V_{in} = 1mV$; $f_m = 400Hz$; $\Delta f = \pm 25KHz$;

$P_1 = 12K\Omega$; $R_L = \infty$; S1 = on ;

Figure 1 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

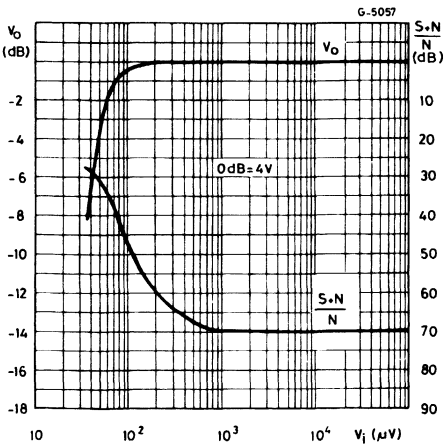


Figure 2 : Output Voltage Alternation vs. DC Volume Control Resistance (a) or Vs. DC Volume Control Voltage (b).

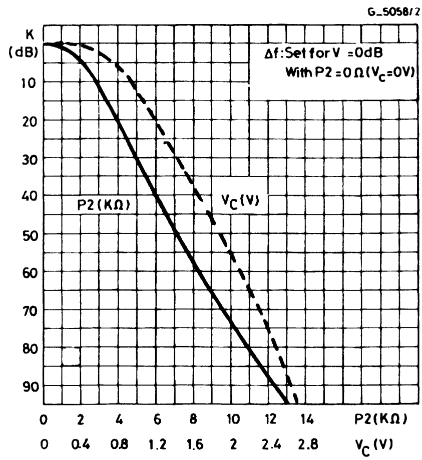


Figure 3 : DC Tone Control Cut of the High Audio Frequencies for some Values of Resistance adjusted by P1.

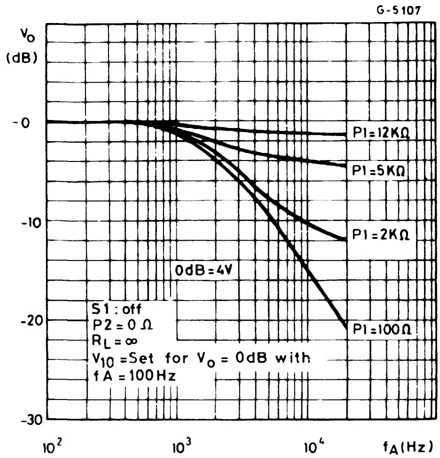


Figure 4 : Amplitude Modulation Rejection vs. Input Signal.

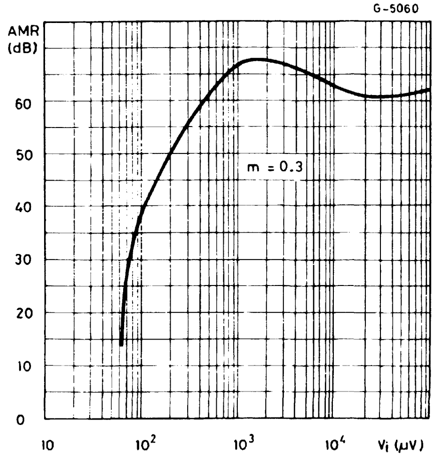


Figure 5 : ΔAMR vs. Timing Frequency Change.

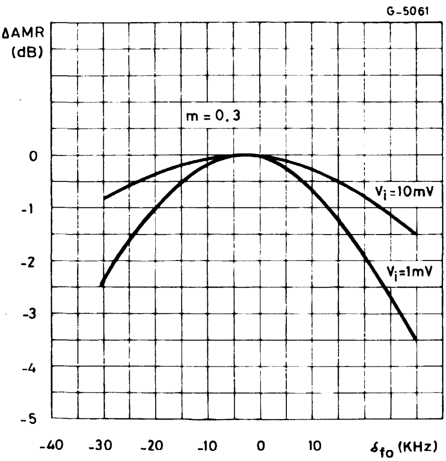


Figure 6 : Recovered udio Voltage vs. Unloaded Q – factor of the Detector Coil.

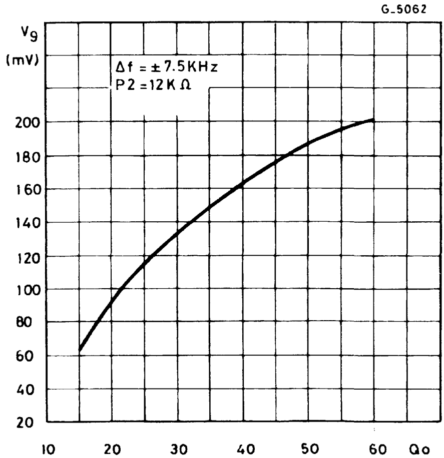


Figure 7 : Distortion vs. UNloaded Q – factor of the Detector Coil.

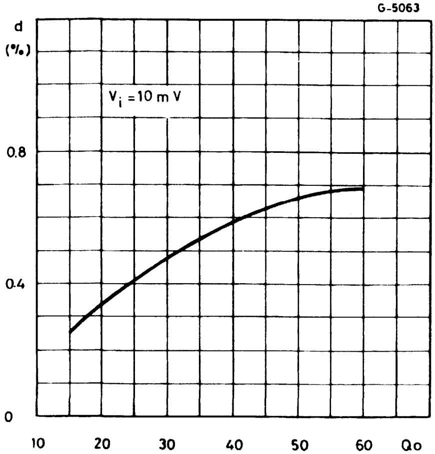


Figure 8 : Distortion vs. Frequency Variation.

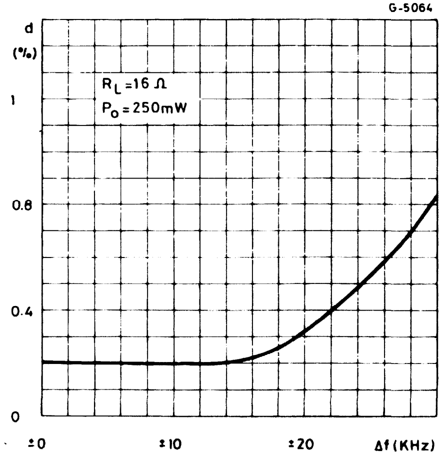


Figure 9 : Distortion vs. Tuning Frequency Change.

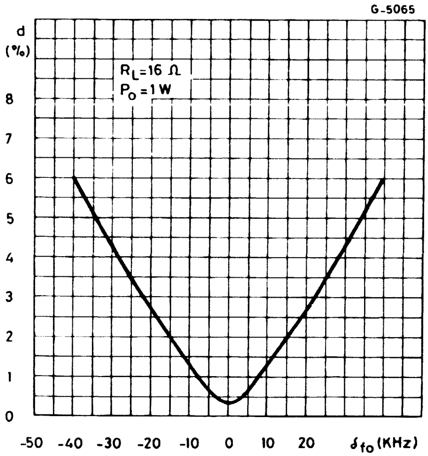


Figure 10 : Distortion vs. Output Power.

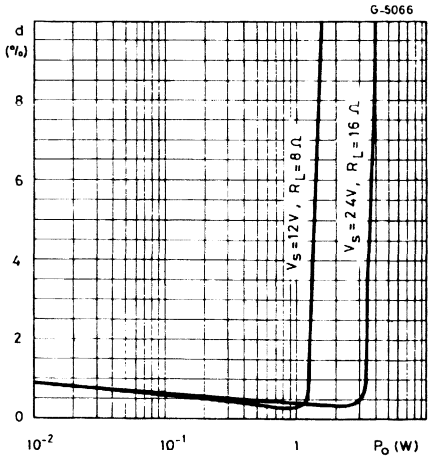


Figure 11 : Audio Amplifier Frequency Response.

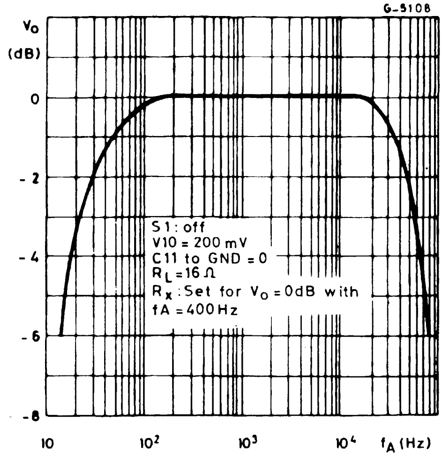


Figure 12 : Output Power vs. Supply Voltage.

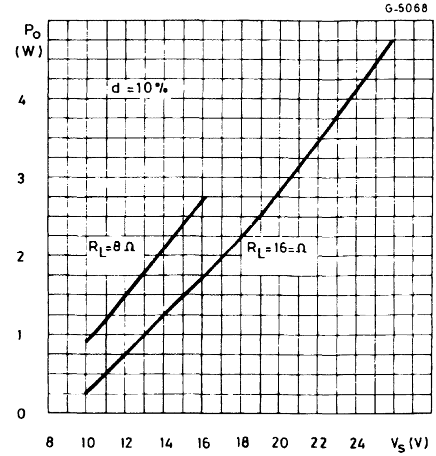


Figure 13 : Power Dissipation vs. Supply Voltage(sine wave operation).

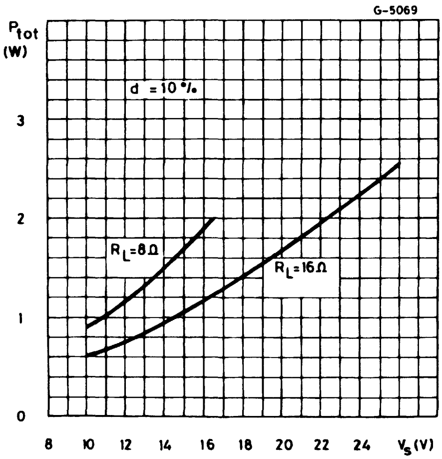


Figure 14 : Power Dissipation and Efficiency vs. Output Power.

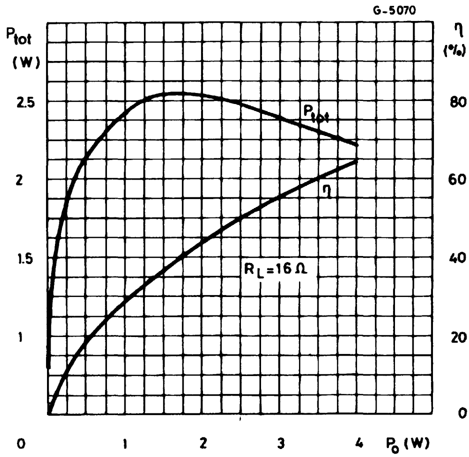
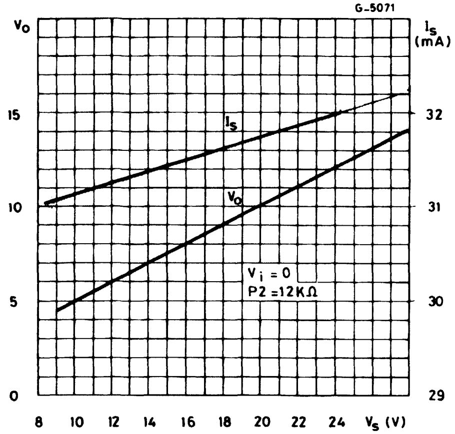


Figure 15 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.



APPLICATION INFORMATION (refer to the block diagram)

IF AMPLIFIER-LIMITER

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50μV.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 is the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50μV. (see VCR facility too).

LOW-PASS FILTER, FM DETECTOR AND AMPLIFIER

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40 dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by :

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve :

$$\frac{f2}{f1} = \sqrt{1 + \frac{C_9}{C_8}}$$

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0 ; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1K, is available the recovered audio signal as auxiliary output.

DC TONE CONTROL

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of P_1.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by :

X_{C11} = 6.8K, typically.

Pin 11 - At this pin is tied the tone capacitor.

Pin 12 - Is the DC Tone Control input.

DC VOLUME CONTROL

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2 ; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

AUDIO FREQUENCY POWER AMPLIFIER AND THERMAL PROTECTION

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio :

$$G_v = 20 \text{ Log } \frac{R5 + R4}{R5} \quad \text{(dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16 load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

TURN-ON AND TURN-OFF SWITCH

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage V_s, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turninig on, pin 1 follows the supply voltage V_s by means of C7 ; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When V_s reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the V_s trend, in series to the voltage V_s V_1 and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1 Vpp of ripple on the supply voltage does not produce any switching..

- Pin 1 is the turn-on and turn-off muting input.

SUPPLY

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

- Pin 18 is the main supply of the device.
- Pin 5 ; pin 6 ; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

APPLICATION INFORMATION (continued)

Components	Units	Appl. 4.5 MHz	Appl. 5.5 MHz	Appl. 6 MHz
L1	µH	10 $Q_o = 60$	12 $Q_o = 80$	10 $Q_o = 70$
C5	pF	120	68	68
C4	pF	9	8.2	6.8
C8	nF	68	47	47
C. F		Murata SFE 4.5 MA	Murata SFE 5.5 MB	Murata SFE 6.0 MB
C1	pF	22	18	18
R2	Ω	1000	560	470
R3	Ω	1000	560	470

Figure 16 : Application Circuit.

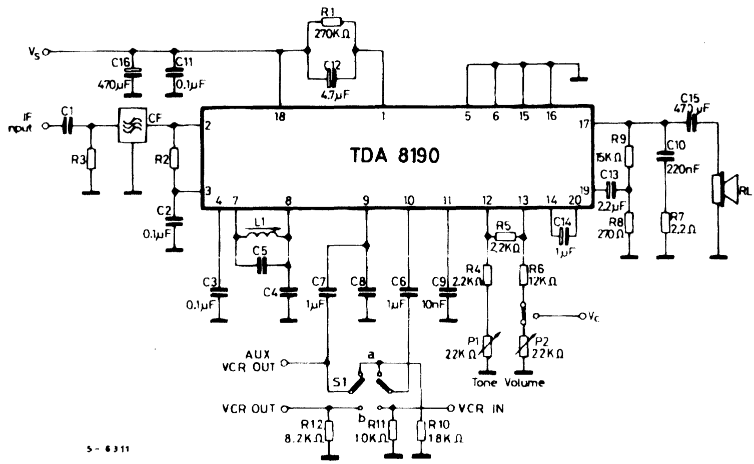
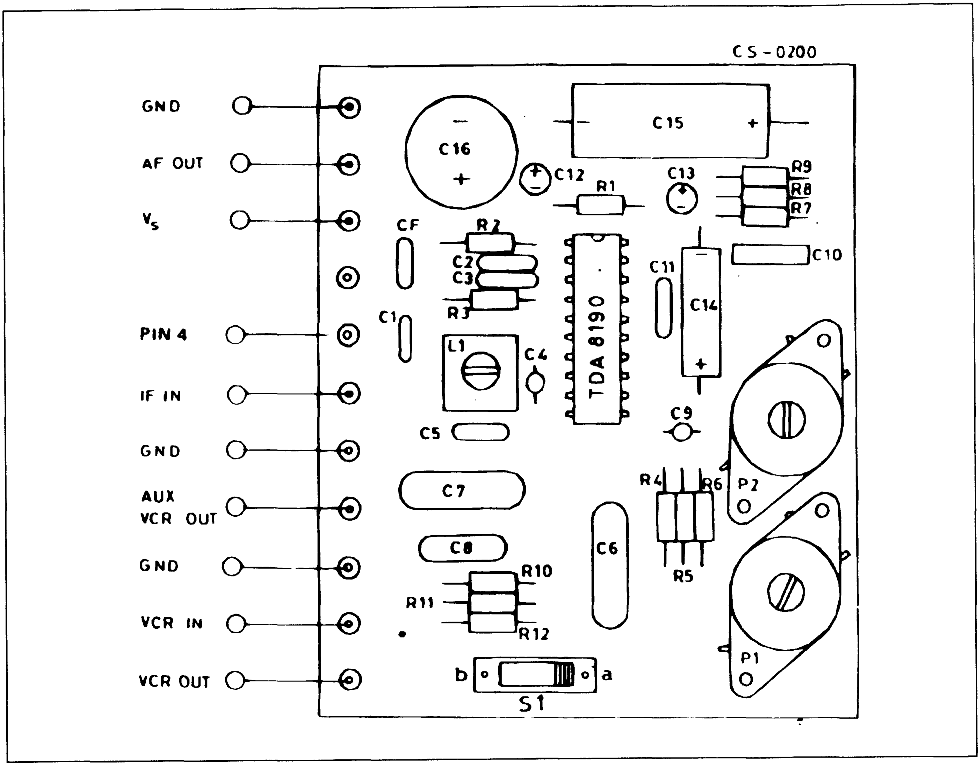


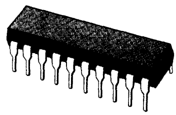
Figure 17 : PC Board and Components Layout of the Circuit of Fig. 16 (1 : 1 scale).



SGS-THOMSON
MICROELECTRONICS

TV SOUND CHANNEL

- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- DC VOLUME CONTROL
- PERITELEVISION FACILITY
- 4W OUTPUT POWER
- LOW DISTORTION
- THERMAL PROTECTION
- TURN-ON AND TURN-OFF MUTING



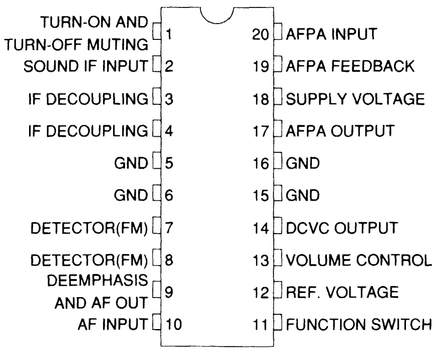
DIP20
(Plastic Package)

ORDER CODE : TDA8191

DESCRIPTION

The TDA8191 is a monolithic integrated circuit that includes all the functions needed for a complete TV sound channel. The TDA8191 is assembled in a 20 pin dual in line power package.

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage (pin 18)	28	V
Vl	Voltage at Pin 1	± Vs	
Vi	Input Voltage (pin 2)	1	V_{PP}
Io	Output Peak Current (repetitive)	1.5	A
Io	Output Peak Current (non repetitive)	2	A
Ptot	Total Power Dissipation at Tpins = 90°C at Tamb = 70°C	4.3 1	W W
Tstg, Tj	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}pins)}$	Junction-pins Thermal Resistance	Max	14	°C/W
$R_{th\ (j\text{-}amb)}$	Junction-ambient Thermal Resistance	Max	80	°C/W

ELECTRICAL CHARACTERISTICS

(Refer to fig. 1 ; Vs = 24V ; RL = 16Ω ; pin 11 floating ; Δf = ± 50KHz ; Vi = 1mV ; fo = 5.5MHz ; fm = 1KHz ; Tamb = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vs	Supply Voltage (pin 18)	Vc = 4.5V	10.8	24	27	V
Vo	Quiescent Output Voltage (pin 17)	Vc = 4.5V	11	12	13	V
V1	Pin 1 DC Voltage	Vc = 4.5V		5.3		V
Id	Quiescent Drain Current	Vc = 4.5V		35		mA
Vi	Input Limiting Voltage at Pin 2 (– 3dB)	Vo = 4VRMS		50	100	µV
V9	Recovered Audio Voltage (pin 9)	Vc = 4.5V Δf = ± 15KHz	200		400	mVRMS
R9	Deemphasis Res.	f = 20Hz to 20KHz	500	700	1000	Ω
AMR	Amplitude Modul. Rejection	m = 0.3 ; Vo = 4VRMS	45	60		dB
Ri	Input Res. (pin 2)	Δf = 0		30		KΩ
Ci	Input Capacitance (pin 2)	Δf = 0 ; Vc = 4.5V		6		pF
V12	DCVC Reference Voltage		5.6		6.2	V
Kv	Volume Attenuation	Vc = 0.5V ; Fig. 2 Vc = 4.5V ; Fig. 2	 80		1.0 	dB dB
$\frac{\Delta Kv}{\Delta Tj}$	Volume Attenuation Thermal Drift	Tj = 300 to 380°K Fig. 3		– 0.05	– 0.1	dB/°C
Po	Output Power (d = 10%)		3.5	4		W
SVR	Supply Voltage Rej. (pin 17) (pin 9)	 Vc = 4.5V fripple = 100Hz	 20 50	 26 60		 dB dB
V11	Function Switch. - Television Broadc. Reproduction - Peritelevision Reproduction		 0 or Pin 11 Floating 8		 2 12	 V V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R11	Input Resistance		10			KΩ
V10	Input Voltage (d ≤ 2%)	Vo = 4VRMS ; V11 = 12V		0.5	2.0	VRMS
R10	Input Resistance	f = 20Hz to 20KHz	10			KΩ
CT	Crosstalk between Pins 9, 10		60			dB
$\frac{S+N}{N}$	Signal to Noise Ratio	Δf = 0 ; Vo = 4VRMS	60	70		dB
d	Distortion (Po = 250mV)				2	%
Δf	Deviation Sens.	Vc = 0.5V ; Vo = 4VRMS ;		± 4	± 10	KHz

Figure 1 : Test Circuit.

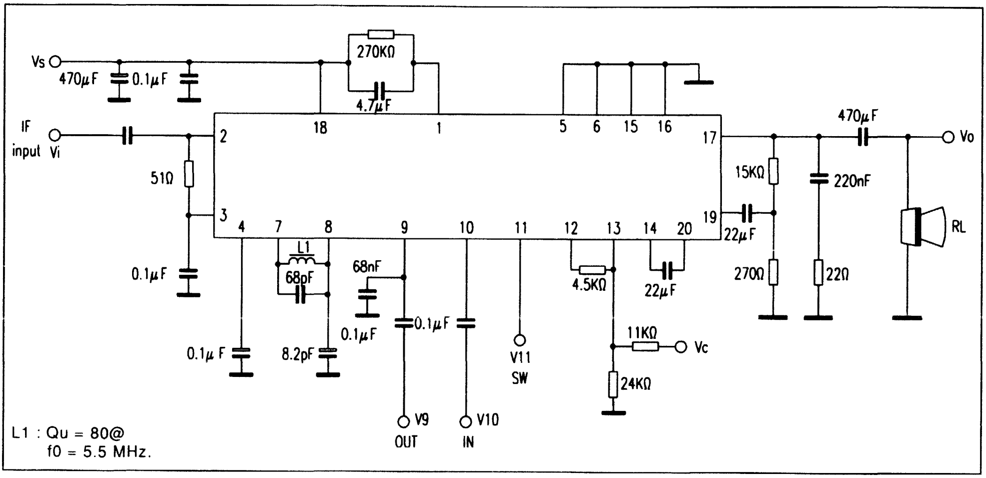


Figure 2 : Volume Attenuation vs. DC Volume Control Voltage.

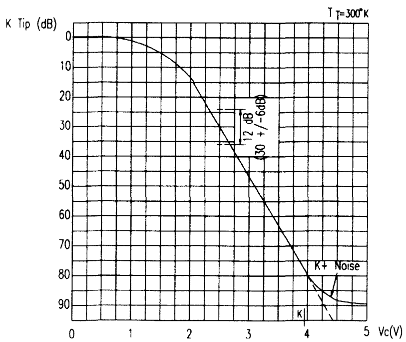
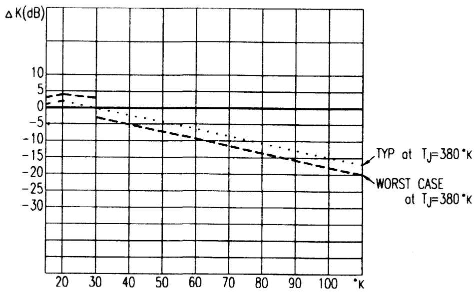
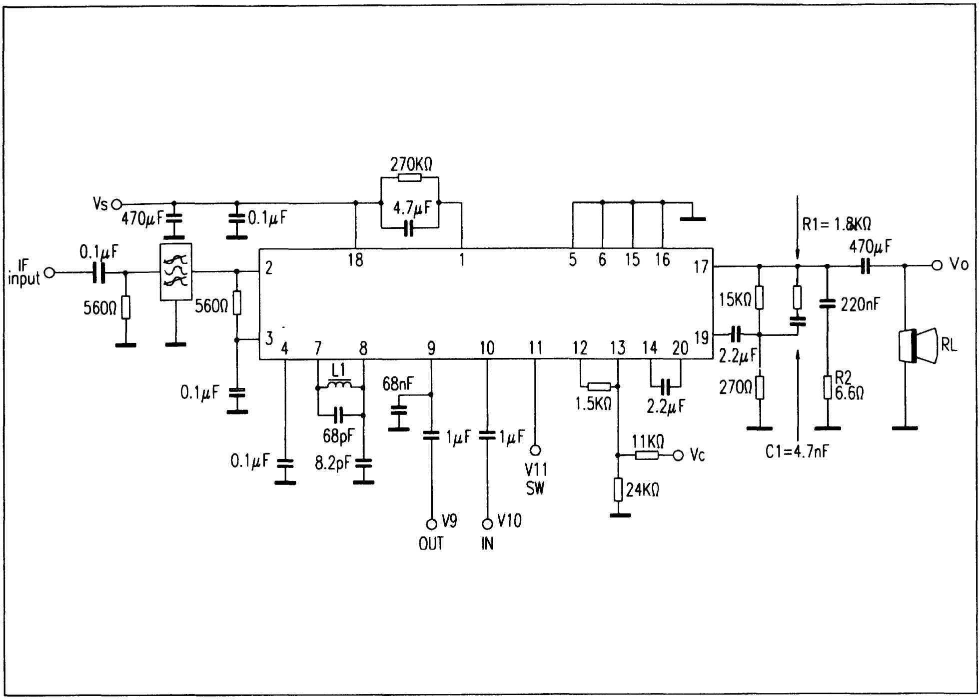


Figure 3 : Volume Attenuation Thermal Drift.



TYPICAL APPLICATION



L1 : Qu = 80e.
fo = 5.5MHz.

Figure 4 : AF Output Amplitude vs. AF Frequency by Using the Changes Shown on Fig. 4.

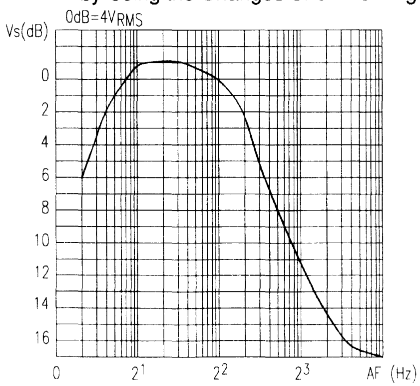


Figure 5 : Relative Audio Output Voltage and Output Noise vs. Input Signal.

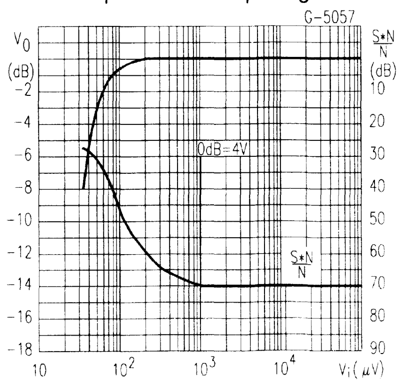


Figure 6 : Distortion vs. Output Power.

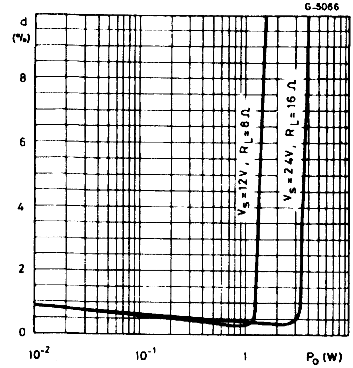


Figure 7 : Audio Amplifier Frequency Response.

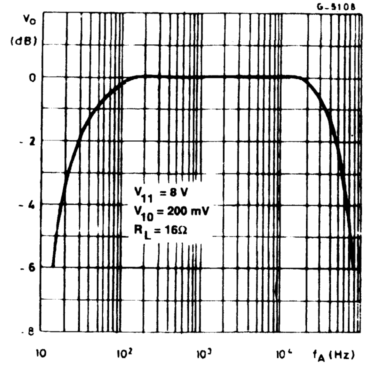


Figure 8 : Output Power vs. Supply Voltage.

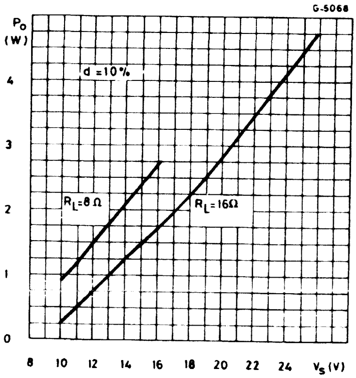


Figure 9 : Power Dissipation vs. Supply Voltage (sine wave operation).

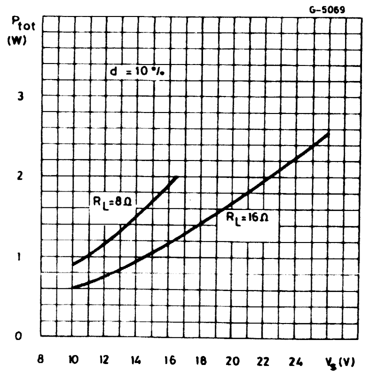


Figure 10 : Power Dissipation and Efficiency vs. Output Power.

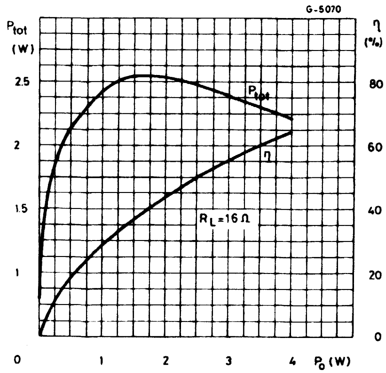
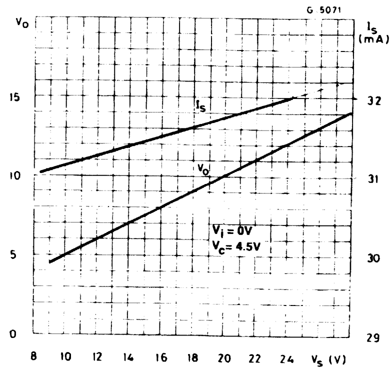


Figure 11 : Quiescent Drain and Quiescent Output Voltage vs. Supply Voltage.

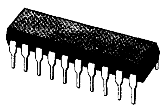


MULTISTANDARD AM AND FM SOUND IF CIRCUIT FOR TV

The TDA8192 integrated circuit performs the following functions :

- A 2-STAGE GAIN CONTROLLED AMPLIFIER, PROVIDING COMPLETE IF GAIN ; (AM SECTION)
- A PEAK DETECTOR AND INTEGRATION WHICH PROVIDES AGC-VOLTAGE ; (AM SECTION)
- A 6-STAGE LIMITING AMPLIFIER FOLLOWED BY A SYNCHRONOUS DEMODULATOR AND DEEMPHASIS NETWORK ; (FM SECTION)
- AN AUDIO PREAMPLIFIER
- A CIRCUIT PROVIDING AM/FM SWITCHING AND MUTE FACILITIES
- AN EXTERNAL AUDIO INPUT CIRCUIT WITH SWITCHING FACILITIES TO DELIVER EITHER THE DEMODULATED IF, OR THE EXTERNAL AUDIO SIGNAL AT THE OUTPUT FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN50 049
- A DC CONTROLLED VOLUME CIRCUIT

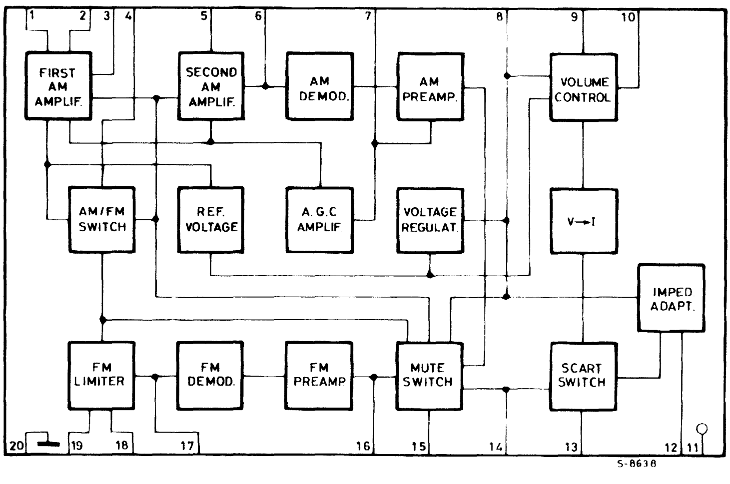
The demodulated IF signal is always available at a low impedance output.



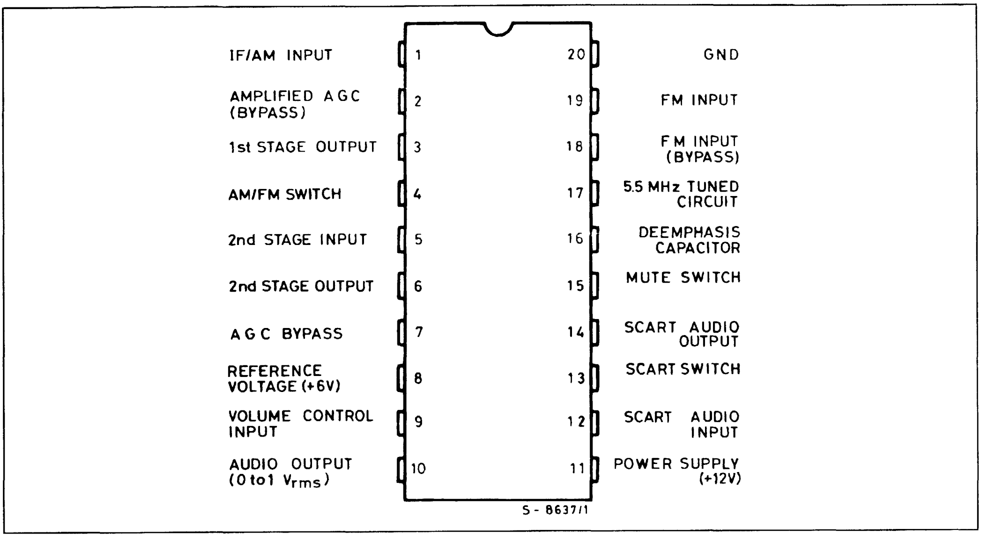
DIP-20

ORDER CODE : TDA8192

BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	16	V
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70°C$	800	mW
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 12V unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_s	Supply Voltage			10.8	12	13.2	V
I_d	Current Drain	$V_i = 0$	AM		30		mA
			FM		30		

ELECTRICAL CHARACTERISTICS (continued)

AM SECTION (f_i = 39.2MHz, V_i = 1mV, m = 0.8, f_m = 1KHz unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input Sensitivity	S/N = 26dB		35		µV
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 0.1mV m = 0.3 V_i = 1mV V_i = 10mV	 50	36 50 56		dB
V_i	AGC Range	ΔV_{OUT} = – 1 to + 1dB		66		dB
V_o	Recovered Audio Signal			1		V
d	Distortion (1)				3	%
d	Distortion (2)				3	%
R_i	Input Resistance between Pins 1 and 2	m = 0	2			KΩ
C_i	Input Capacitance between Pins 1 and 2	m = 0		18		pF

FM SECTION (f_i = 5.5MHz, V_i = 1mV, Δf = ± 50KHz, f_m = 1KHz, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	Input Limiting Voltage	– 3dB Limiting Point		30		µV
AMR	Amplitude Modulation	V_i = 30mV m = 0.3		55		dB
$\frac{S+N}{N}$	Signal to Noise Ratio	V_i = 1mV	60			dB
d	Distortion (3)				1.5	%
d	Distortion (4)			2		%
V_o	Recovered Audio Signal			1		V
R_i	Input Resistance	Δf = 0	2			KΩ
C_i	Input Capacitance	Δf = 0		14		pF
C_T	Crosstalk AM/FM			70		dB

(1) 50% volume setting, V_i = 1mV
(2) 50% volume setting, V_i = 10mV
(3) V_i = 1mV, fm = 100 to 10.000Hz
(4) Vi = 1mV, ± 20KHz offset (detuning of phase shift filter).

AM/FM AND MUTE SWITCHING

Parameter	Min.	Typ.	Max.	Unit
FM "on" (pin. 4)	2.5		V_S	V
AM "on" (pin 4)	0		0.8	V
Mute "on" (pin 15)	0		1	V
Mute "off" (pin 15)	5		V_S	V
Signal Attenuation for Mute "off"	70			dB
Mute Switch Current			50	µA
AM/FM Switch Current	50		250	µA

ELECTRICAL CHARACTERISTICS (continued)

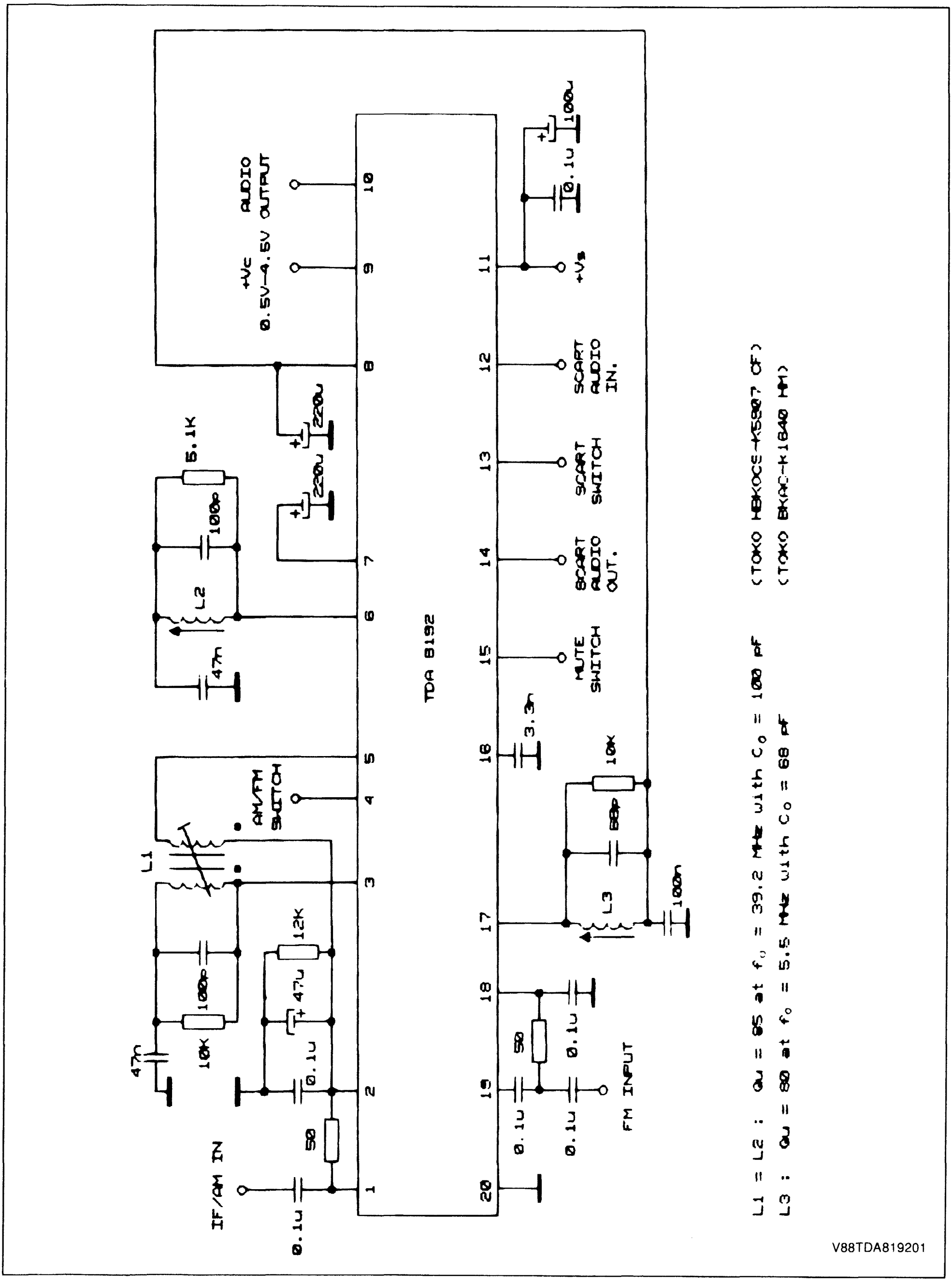
SCART SWITCHING

Parameter	Min.	Typ.	Max.	Unit
Mode Selection Voltage : TV Selected (pin. 13)	0		5	V
Mode Selection Voltage : Scart Selected (pin 13)	8		12	V
Scart Switch Input Resistance	10			KΩ
Scart Audio Input Amplitude (pin 12)		0.5	2	V_{rms}
Crosstalk Between Switched Inputs (TV scart)		80		dB

DC VOLUME CONTROL

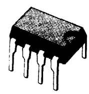
Parameter	Min.	Typ.	Max.	Unit
Audio Output Impedance (pin 10)			1	KΩ
Control Range		90		dB
Output/input Gain for Maximum Gain Control		0		dB
Gain Control Voltage	0.5		4.5	V
Noise Level (DIN 45405)		25		μV_{rms}

TEST CIRCUIT



AUDIO SWITCH AND DC VOLUME CONTROL FOR TV

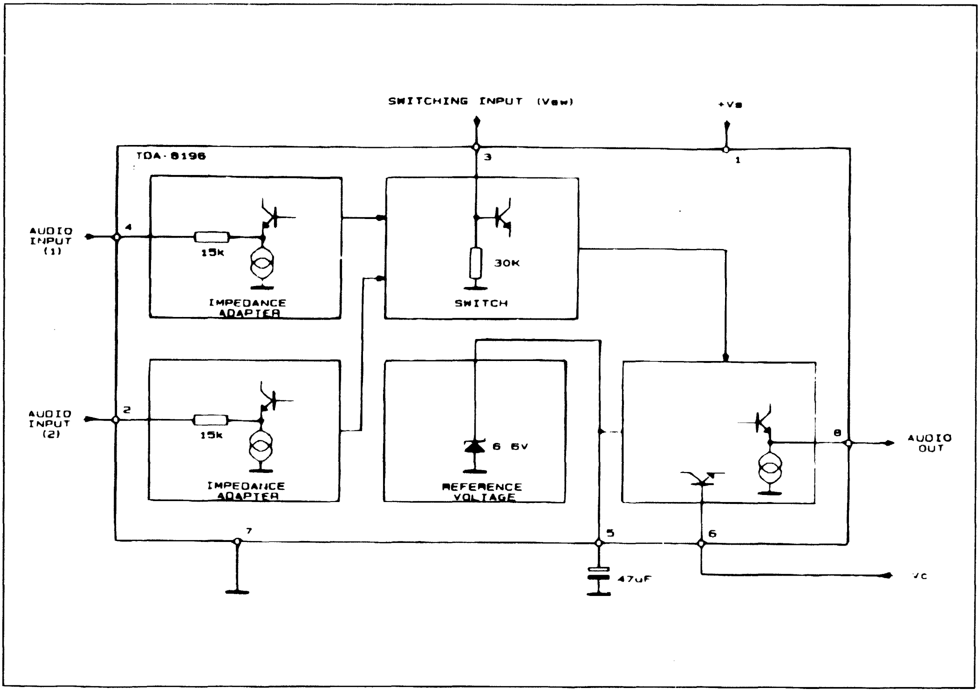
- TWO AUDIO INPUTS CIRCUITS WITH SWITCHING FACILITIES FULLY COMPATIBLE WITH THE SCART EUROPEAN NORM EN 50049
- DC VOLUME CONTROL



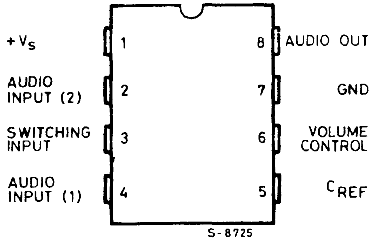
MINIDIP

ORDER CODE : TDA8196

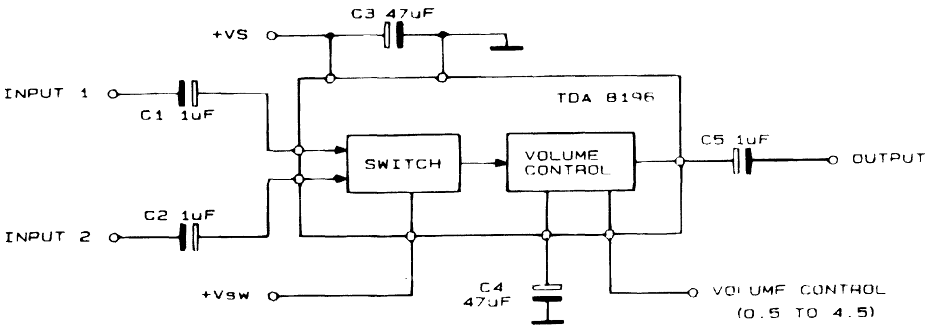
BLOCK DIAGRAM



PIN CONNECTION (top view)



APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_s = 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Pin	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	1		10.8	12	13.2	V
I_S	Supply Current	1	V_i = 0 ; V_c = 0.5V		12		mA
V_r	Reference Voltage	5			6.6		V
V_{sw}	Switching Voltage Audio Input 1 Audio Input 2	3		0 8		5 12	V V
R_{sw}	Switching Input Resistance	3	V_{sw} = 12V	20	30		K_{ohm}
C_{sw}	Switching Input Capacitance	3				10	pF
C_t	Crosstalk Between Switched Inputs		Selective Voltmeter (B_w = 8Hz) ; see fig. 1	70	90		dB
V_i	Audio Input Amplitude (1 or 2)	4 2			0.5	2	V_{rms}
R_i	Audio Input Resistance (1 or 2)	4 2		10	13		K_{ohm}
K_{min}	Output/input Gain for Max Vol				0		dB
R_o	Audio Output Resistance	8			0.2	1	K_{ohm}
K_v	Volume Control Range		Selective Voltmeter (B_w = 8Hz) ; see fig. 2	80	120		dB
V_c	Control Voltage Range $K_v = K_{max}$ (vol. min) $K_v = K_{min}$ (vol. max)	6			0.5 4.5		V
THD	Distortion	8	Vi = $2V_{rms}$ @ V_c = 4.5V		0.4	1	%
En	Output Noise Level	8	DIN 45405 V_c = 0.5V Weighted		20		uV_{rms}
En	Output Noise Level	8	DIN 45405 V_c = 4.5V Unweighted		50	150	uV_{rms}
$\frac{K_v}{\Delta T_a}$	Vol. Attenuation Thermal Drift		T_{amb} = 0 to 70°C K_v = 30dB See fig.3		0.04		$\frac{dB}{°C}$
SVR	Supply Voltage Rejection	8	V_c = 0.5V ; f = 100Hz $V_{ripple} = 1V_{pp}$ Selective Voltmeter (B_w = 8Hz) See fig. 4 and 5		38		dB
V_o	Output DC Shift	8	V_c = 0.5 ÷ 4.5V V_i = $2V_{rms}$		0.25		V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
T_{stg}, T_j	Storage and Junction Temperature	– 55 to 125	°C
T_{amb}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	200	°C/W

TEST CIRCUIT

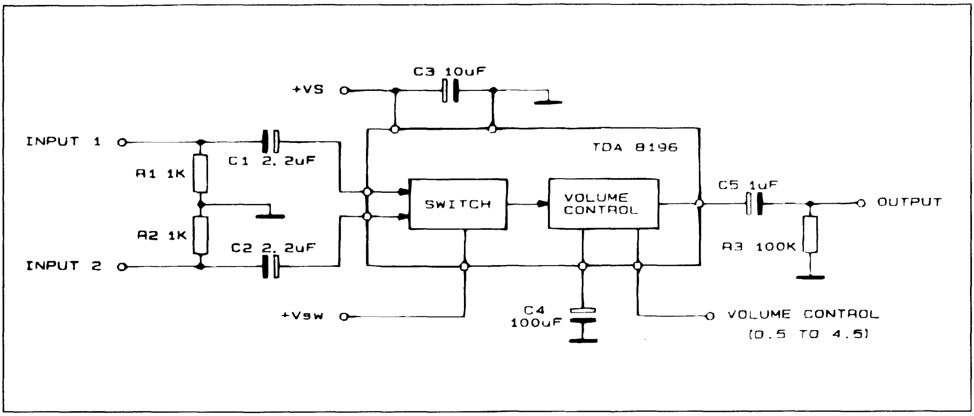


Figure 1 : TDA8196 Crosstalk.

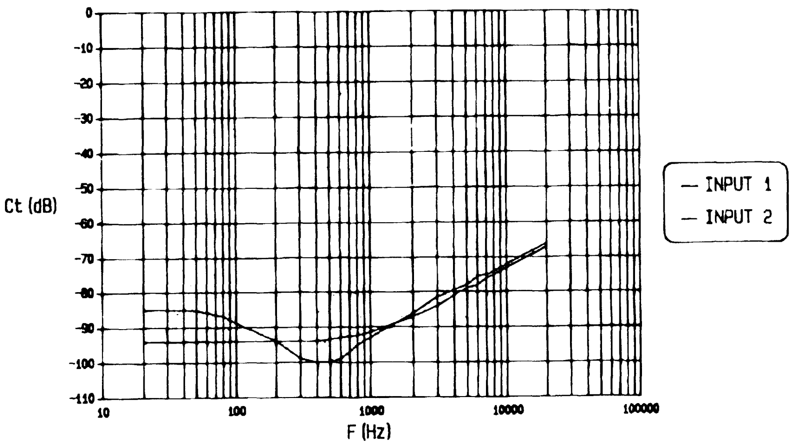


Figure 2 : Output Attenuation versus DC Volume Control Voltage.

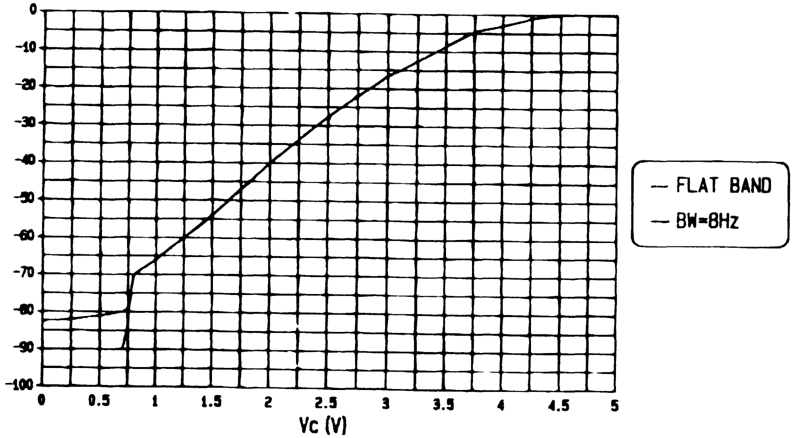


Figure 3 : K_v Drift vs. T_{amb} Variation.

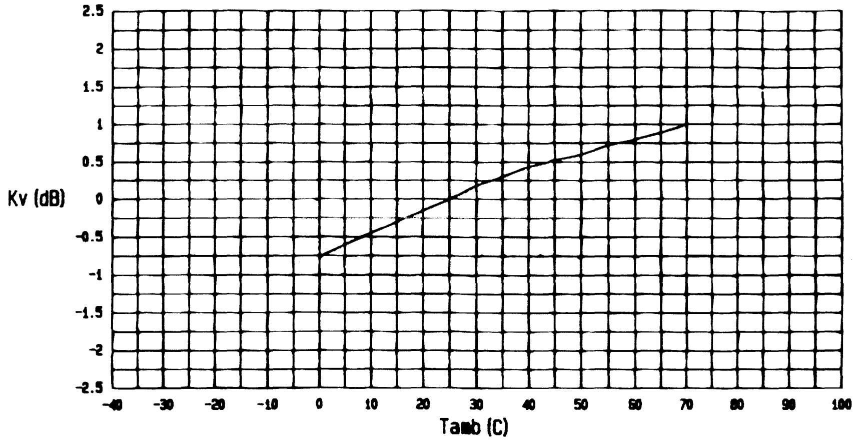


Figure 4 : SVR vs. Ripple Frequency.

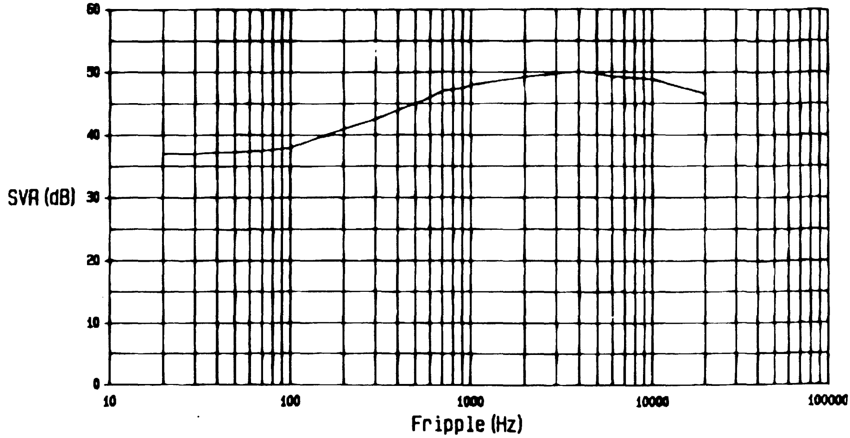
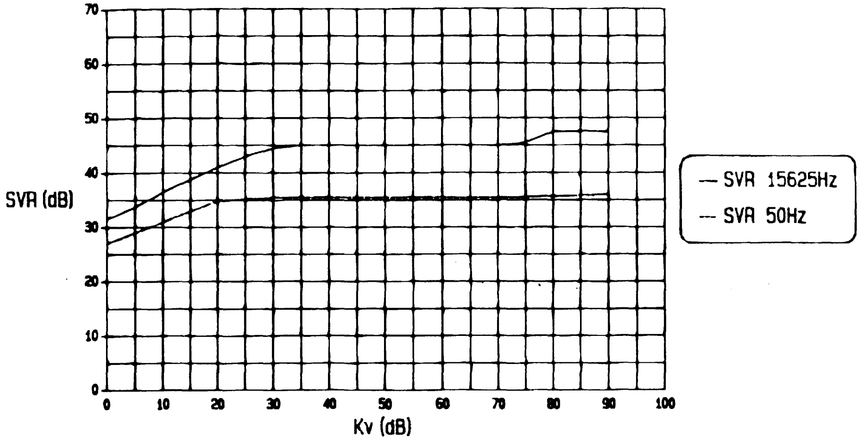


Figure 5 : SVR vs. Volume Attenuation.



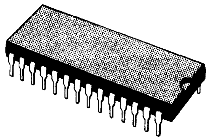
SGS-THOMSON
MICROELECTRONICS

TDA8200

TV STEREO DECODER

ADVANCE DATA

- IDENTIFICATION OF TRANSMISSION MODE (mono/stereo/bilingual)
- DEMATRIXING OF THE STEREO AUDIO SIGNAL, WITH AN INTERNAL PROGRAMMABLE S-BUS NETWORK FOR MINIMAL CROSS-TALK
- DE-EMPHASIS OF THE AUDIO SIGNAL WITHOUT EXTERNAL COMPONENTS
- FILTERS FOR PSEUDOSTEREO AND ENLARGED STEREO BASE SPECIAL EFFECTS
- MONOPHONIC INPUT FOR MULTISTANDARD APPLICATIONS
- STEREO INPUT/OUTPUT FOR VCR
- VOLUME AND BALANCE CONTROL FOR EARPHONE OUTPUT
- ALL FUNCTION PROGRAMMABLE THROUGH USE OF S-BUS



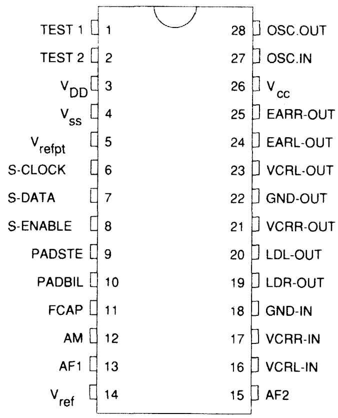
DIP28
(Plastic Package)

ORDER CODE : TDA8200

DESCRIPTION

The TDA8200 combines the functions of audio dematrixing and stereo decoder for the European 2-carrier B/G system ; moreover, the device also includes input and a stereophonic output for reception of the audio signal coming from the SCART connector as well as a monophonic input for MULTISTANDARD applications (e.g., B/G and L).

PIN CONNECTION



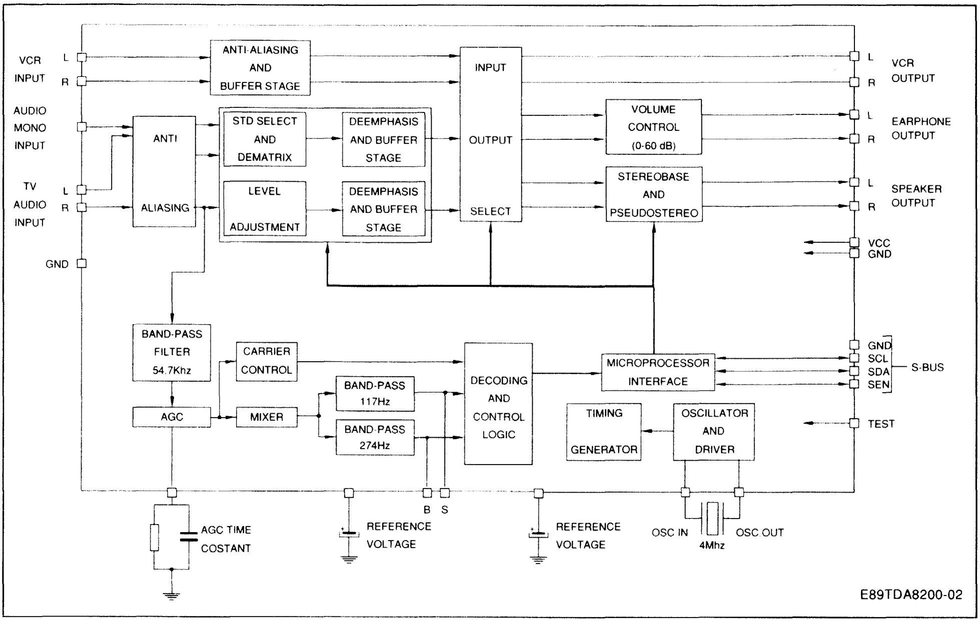
E89TDA8200-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Function
1	Reserved for device testing, normally should be connected to mass.
2	Reserved for device testing, normally should be unconnected.
3	Power Voltage for Digital Part and Pilot Tone Vd = 8.5V
4	Mass for Digital Part and for Pilot Tone
5	Reference Voltage for Pilot Tone
6	SCL Clock Input for S-BUS
7	SDA Data Input for S-BUS
8	SEN Enable Input for S-BUS
9	Stereo Modulating Output (117Hz) for Pilot Tone
10	Bilingual Modulating Output (274Hz) for pilot Tone
11	Time Constant for AGC
12	Monophonic Input for Multistandard "AM"
13	Audio Input Signal from 5.5MHz Demodulator, AF1
14	Reference Voltage for Audio Part
15	Audio Input Signal from 5.74MHz Demodulator, AF2
16	Audio Input Signal from Right Channel of VCRR-IN Videotape Machine
17	Audio Input Signal from Left Channel of VCRL-IN Videotape Machine
18	Mass for Audio Input Signal
19	Audio Output Signal from Right Channel of LDR-OUT Loudspeakers
20	Audio Output Signal from Left Channel of LDL-OUT Loudspeakers
21	Audio Output Signal from Right Channel of VCRR-OUT Videotape Machine
22	Mass for Audio Output Signal
23	Audio Output Signal from Left Channel of VCRL-OUT Videotape Machine
24	Audio Output Signal from Right Channel of EARL-OUT Earphones
25	Audio Output Signal from Left Channel of EARR-OUT Earphones
26	Input Voltage for Analog Part Va = 8.5V
27	Oscillator Input at 4MHz
28	Oscillator Output at 4MHz

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The device is made up of 5 main sections :

1 S-BUS interface

2 Oscillator and power on reset

3 Pilot tone decoder

4 Dematrixing and de-emphasis of the audio signal

5 Reception of the audio signal

1) S-BUS INTERFACE

All of the TDA8200 functions are activated by microprocessors, using a 3-wire serial bus (SCL, SDA, SEN). For further information, see the software section.

2) OSCILLATOR AND POWER ON RESET

OSCILLATOR. The device functions with an external 4MHz crystal quartz connected to pins 27 and 28. A possible alternative is to connect pin 27 to an external 4MHz generator. If the clock frequency does not remain stable, there will be variations in the audio response and pilot tone decoding.

POWER ON RESET. About 120ms after VCC power has reached the required level for correct device operation, the power on reset circuit signals correct operating status, using the RES bit in the RR register. For further information, see the software section.

3) PILOT TONE DECODING

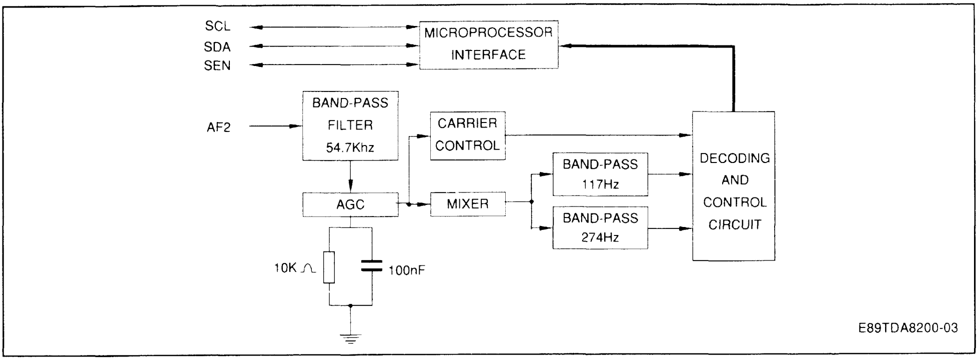
The pilot tone decoding section is used to identify the transmission mode (monophonic, stereophonic or bilingual) in B/G standard.

Figure 1 shows the block diagram for the circuit described hereafter :

The decoding signal goes through the pass-band filter at a frequency of 54.7kHz to the AF2 input in order to eliminate undesirable frequencies.

To guarantee a recognition range from 10 to 300mVeff for a carrier at 54.7kHz, the signal goes throught an AGC circuit the control velocity of which is based on pin 11's capacity. To be able to establish transmission type, the signal is demodulated by the MIXER and filtered into the 117Hz (stereo transmission) and 274Hz (bilingual transmission) fixed frequencies. If, at the output of only one of the two filters, the signal is present, the "DECODING AND CONTROL CIRCUIT" block verifies if the carrier frequency is correct, using the "CARRIER CONTROL" block, and transmits the information to bits B and S of the RR register.

Figure 1 : Pilot Tone Decoder.



4) DEMATRIXING AND DE-EMPHASIS

DEMATRIXING. No external component is used for dematrixing the audio signal, but only a programmable attenuator through S-BUS. Attenuation value must be set in calibration phase for the television set, and loaded every time the TV is turned on by the microprocessor in the R7 and R0 registers of the TDA8200.
Shown below is the dematrixing circuit which differentiates between the STEREO and BILINGUAL signals.

Figure 2 : Stereo Scheme.

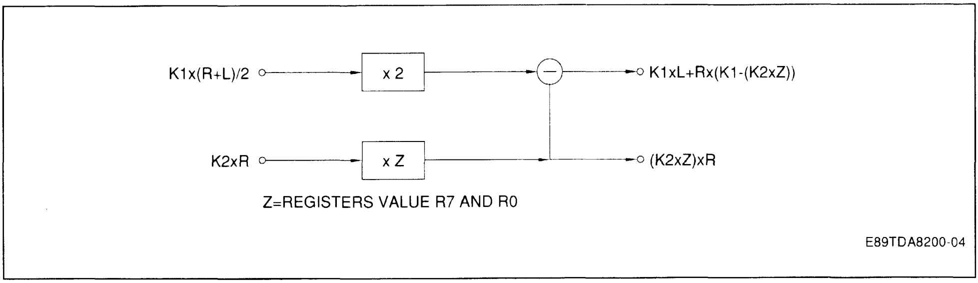
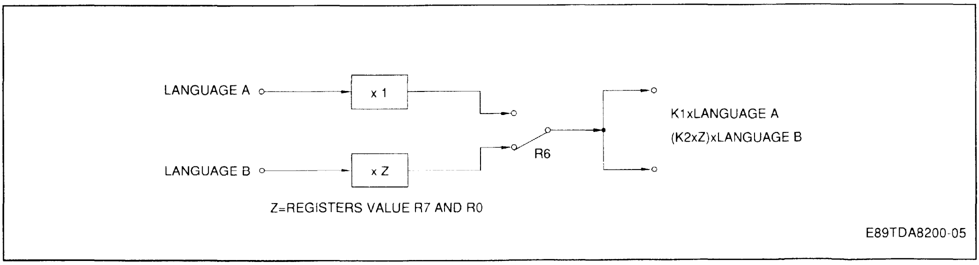


Figure 3 : Bilingual Scheme.



In both circuits, account is taken of the K1 and K2 constants which represent the removal of the AF1 and AF2 signals arriving from the FM demodulator in favor of the real AF1 and AF2 signals transmitted by the generator.

From the output equations can be deduced that, for K1 = K2 x Z, can be obtained, based on precision of Z, the left (L) channel and the correct amplitude of the outputs for the STEREO signal, as well as for the BILINGUAL signals.

As far as the STEREO signal is concerned, a typical value of diaphony between left and right channels of 48dB can be guaranteed by a relationship between K1/K2 of 0.5 to 2, calculated in the following equation :

CT = 20*log[(K1/K2)/2E-9]

In the case of a BILINGUAL signal, a minimal difference in the signal between languages A and B of 0.05dB can be guaranteed by a relationship between K1 and K2 between 0.5 and 2, calculated with the following equation :

K(l-r) = 20*log{(K1/K2)/[(K1/K2)+ 2E-9]}

DE-EMPHASIS.The de-emphasis of the AF1 and AF2 signals coming from the FM demodulator are carried out internally in the device without using external components.

5) AUDIO SIGNAL RECEPTION

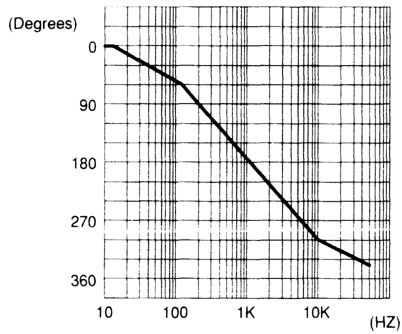
Audio signal reception is made up of three essential parts (see block diagram) :

a) **INPUT OUTPUT SELECT.** This circuit deals with shunting the signal coming from the three inputs (VCR, MONO, TV) into the two outputs (VCR, SPEAKER) in the modes described by the 5 bits S0-S4 in the R6 register. Information on possible configuration is detailed in the software section.

b) **STEREOBASE AND PSEUDOSTEREO.** The special effects function only for the loudspeaker output, and are activated by the PS and ES bits of R6. Operation is as follows :

- **PSEUDOSTEREO**, activated by the PS bit, is used with monophonic signals, and consists in the movement of the right channel phase toward the left, on the basis of the frequency as described in figure 4 below :

Figure 4 : Right Channel Phase.



- **ENLARGED STEREO BASE**, activated by the ES bit, is used for stereophonic signals, and the function is that of making the stereo effect evident, even when the distance between the loudspeakers is reduced. For that purpose, diaphony is introduced in opposition to the right phase and vice versa. The extent of the diaphony to be introduced depends on the distance between the loudspeakers ; in the TDA8200, the diaphony is in the range of 50%.

c) **VOLUME CONTROL.** The earphone output also has a circuit to control and balance volume, carried out by two logarithmic attenuators of 2dB a spet with a maximum attenuation value of 60dB. The attenuation depends on the configuration of the 5 bits, CS1-CS5 of R3 for the left channel and the 5 bits, CD1-CD5 of R4 for the right channel ; the values in dB are shown in table 3 shown in the software section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V28	Analog. Supply Voltage	Max 10	V
Vi	Input Voltage (all input)	– 0.3 to Vs + 0.3	V
Ii	Input Current (all input)	Max 5	mA
Io	Output Current (all output)	Max 10	mA
Tstg	Storage Temperature	– 25 to 125	°C

ELECTRICAL CHARACTERISTICS

Refer to the test circuit, Vs = 8.5V, Tamb = 25°C, without special effects, unless otherwise specified.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Suppply Voltage	8	8.5	9	V
Is	Supply Current		30		mA
SVR	Supply Voltage Rejection (Fripple = 100Hz)		35		dB

AUDIO INPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vin	Voltage Amplitude on all Inputs		1		Vrms
n	Amplitude Ratio between AF1/AF2	0.5		2	
Rin	Resistance on all Audio Inputs	10	40		kΩ

VOLUME CONTROL CHARACTERISTICS

Earphone

Symbol	Parameter	Min.	Typ.	Max.	Unit
KV	Volume Control Range ; Kvmax/Kvmin		60		dB
KVmin	Attenuator Resolution/step		2		dB
Ke	Tracking Error KV = 0 to 60dB		± 1	± 2	dB
KB	Balance Control Range ; KV = 0dB		60		dB

SPECIAL EFFECT CHARACTERISTICS

Pseudostereo

Symbol	Parameter	Min.	Typ.	Max.	Unit
Psh	Phase Shifter Response at : 100HZ 1kHZ 10kHZ		0 180 360		Deg Deg Deg
K(l-r)	Amplitude Tracking Error between Left and Right Channels (KV = 0dB)		± 0.5	± 1	dB

Enlarged Stereo Base

Symbol	Parameter	Min.	Typ.	Max.	Unit
K(l-r)	Amplitude Tracking Error between Left and Right Channel (KV = 0dB)		± 0.5	± 1	dB

DE-EMPHASIS CHARACTERISTICS (active only in AF1/AF2 input)

Symbol	Parameter	Min.	Typ.	Max.	Unit
td	Time Constant	45	50	55	µs

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
Vo	Audio Output Voltage Amplitude (THD ≤ 1%, all outputs)			Vin		Vrms
Kmax	Max Gain at Min. Attenuation (all outputs)		– 1	0	+ 1	dB
K(l-r)	Gain Tolerance between Left and Right Channel at Min. Attenuation (earphone K = 0dB)			± 0.5	± 1	dB
Ro	Resistence on all Audio Output				1	kΩ
R_l	Load Resistance (all outputs) Note : all outputs are short circuit protected.		5			kΩ
C_l	Load Capacitance (all outputs)				2	nF
AT	Muting Attenuation (all outputs)		70	80		dB
En	Output Noise Voltage (CCIR 468-2)					
	VCR Input					
	OUTPUT					
	Earphone	KV = 0dB		100	200	μV
		KV = 40dB		50	100	μV
	Loudspeaker			100	200	μV
	VCR			100	200	μV
	AM Input					
	OUTPUT					
	Earphone	KV = 0dB		100	200	μV
		KV = 40dB		50	100	μV
	Loudspeaker			100	200	μV
	VCR			100	200	μV
	AF1/AF2 Input					
	OUTPUT					
	Earphone	KV = 0dB		200	300	μV
		KV = 40dB		50	100	μV
	Loudspeaker			200	300	μV
	VCR			200	300	μV
S/N	Signal to Noise Ratio (CCIR 468-2)					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	Loudspeaker		75	80		dB
	VCR		75	80		dB
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	Loudspeaker		75	80		dB
	VCR		75	80		dB
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB	70	75		dB
		KV = 40dB	35	45		dB
	Loudspeaker		70	75		dB
	VCR		70	75		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
d	Total Harmonic Distortion					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB		0.2	0.4	%
	Loudspeaker			0.2	0.4	%
	VCR			0.2	0.4	%
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB		0.2	0.4	%
	Loudspeaker			0.2	0.4	%
	VCR			0.2	0.4	%
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Earphone	KV = 0dB		0.2	0.4	%
	Loudspeaker			0.2	0.4	%
	VCR			0.2	0.4	%
CT	Crosstalk between Left and Right Channels					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Stereo :					
	OUTPUT					
	Earphone	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	Loudspeaker		70	80		dB
	VCR		70	80		dB
	AF1/AF2 Input Stereo :					
	OUTPUT					
	Earphone	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	Loudspeaker		70	80		dB
	VCR		70	70		dB
CTb	Bilingual Crosstalk					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Bilingual :					
	OUTPUT					
	Earphone	KV = 0dB	75	85		dB
		KV = 20dB	75	85		dB
	Loudspeaker		75	85		dB
	AF1/AF2 Input Bilingual :					
	OUTPUT					
	Earphone	KV = 0dB	70	80		dB
		KV = 20dB	70	80		dB
	Loudspeaker		70	80		dB
CTI	Crosstalk between VCR and TV Section		70	80		dB

S-BUS CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vil	Input Voltage Low Level	Vss		0.8	V
Vih	Input Voltage High Level	2		VDD	V
Iil-ih	Input Current			1	µA
Iol	Output Low Current Capability (Vol = 0.45V)	5			mA
Ioh	Leakage Output Current (Vo = 5.25V, output off, Vs = 8.5V)			10	µA

ELECTRICAL CHARACTERISTICS (continued)

PILOT TONE CHARACTERISTICS V1 = 50mVrms, m = 0.5, unless otherwise specified

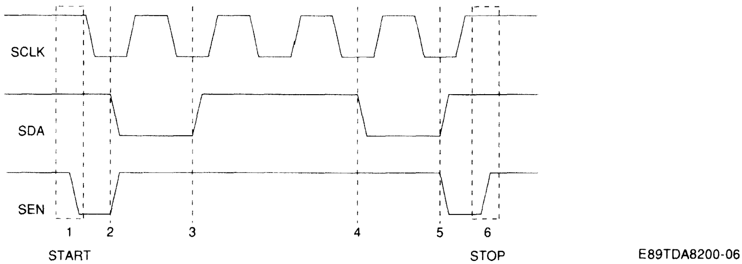
Symbol	Parameter	Min.	Typ.	Max.	Unit
V1	Input Voltage Amplitude (without AM modulation)	10		300	mVrms
dfp	Frequency Range of Carrier to 54687.5Hz		± 1		kHz
dfs	Frequency Range of Stereo Filter (117.4Hz)		± 3		Hz
dfb	Frequency Range of Bilingual Filter (274Hz)		± 6		Hz
dm	Range of AM Modulation Index	40	50	60	%

SOFTWARE INFORMATION

S-BUS DESCRIPTION

Shown below is the timing diagram of the S-BUS protocol :

Figure 5 : S-BUS Timing Diagram.



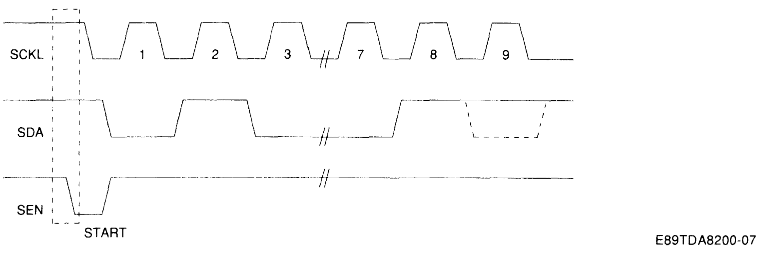
The START/STOP conditions (points 1 and 6) occur only by a transmission of SEN wire (10 and 01 respectively) while the SCL wire is in high state (1).

During transmission, the SDA wire can change only when SCL wire is in low state (points 2, 3, 4, 5). After START condition (point 1), the SEN wire must change to high state (point 2) and it remains in this condition for the whole transmission.

At the end of transmission (point 5), the SDA wire change to high state and in the mean time, the SEN wire must go to low state and then return to high state to generate the STOP condition (point 6).

After the transmission of each byte (composed of 8 bits), there is an ACKNOWLEDGE bit appointed by a high state on SDA wire generated by the transmitter. The device that acknowledges, forces to low state the SDA wire during the time of the acknowledge clock pulse, as described in figure 5 :

Figure 6 : Acknowledge Bit.



In normal conditions, the addressed device must acknowledge after each byte received. If the SDA wire, during the 9th pulse, remains in high state, the master-transmitter can generate the STOP condition to abort the transfer.

Interface between the microprocessor and the TDA8202 occurs through use of the following protocol :

- a start condition (START) see figure 7 and 8
- an address byte, containing the address reserved for the TDA8200 (1000000x) and the bus transmission direction (this information is located in the byte's 8th bit, in which "0" indicates a write, and "1", a read, by the microprocessor). At the end of each byte, the TDA8200 must give the ACKNOWLEDGE signal
- a byte for addressing the registers in write, or the content of register RR in a read
- a third byte containing the information to be written on the register
- a stop condition (STOP)

Figure 7 : Write Protocol Example.

	TDA8200 ADDRESS									REGISTER ADDRESS									DATA ADDRESS		
	MSB	FIRST BYTE						LSB		MSB	SECOND BYTE						LSB		MSB	3RD BYTE	LSB	
S	1	0	0	0	0	0	0	0	ACK	X	X	X	X	X	A3	A2	A1	ACK		ACK	P

Figure 8 : Read Protocol Example.

	TDA8200 ADDRESS									REGISTER RR		
	MSB	FIRST BYTE						LSB		MSB SECOND BYTE LSB		
S	1	0	0	0	0	0	0	1	ACK		ACK	P

Table 1 : TDA8200 Register Address.

Register Name	Address			Content	Type of Operation
	A3	A2	A1		
R0	0	0	0	Dematrixing and Muting	WRITE ONLY
R3	0	1	1	Left Earphone Volume Channel (60dB)	WRITE ONLY
R4	1	0	0	Right Earphone Volume Channel (60dB)	WRITE ONLY
R6	1	1	0	Configuration Switch and Special Effects	WRITE ONLY
R7	1	1	1	Dematrixing	WRITE ONLY
RR				Transmission Conditions and Power on Reset	READ ONLY

REGISTER CONTENTS

RR register : (Transmission conditions and power on reset)

X	X	X	X	X	RES	B	S
MSB							LSB

B = Bilingual transmission (active at "1")
S = Stereo transmission (active at "1")
RES = Power on reset (active at "1")
X = Not used

RES

The RES bit in RR register is set to "1" every time that the supply voltage falls under the minimum level required for the correct operation of TDA8200. In this case the device automatically inserts the muting on the outputs (R0, ML and MV ; R3 and R4 are both at "1"), and resets bits B and S in RR to "0".

The microprocessor must verify this situation and when the RES bit returns to "0", it initializes the registers to the desired audio status.

B and S

B, and S are the bits reserved to identify the transmission type in B/G standard. If both bits are at "0", the transmission is MONO, while if only one bit is at "1", the transmission is STEREO (S at "1") or BILINGUAL (B at "1").

Register R0 : (Dematrixing and muting)

X	X	X	TS	ML	MV	A8	A9
MSB							LSB

Register R7 : (Dematrixing)

A0	A1	A2	A3	A4	A5	A6	A7
MSB							LSB

TS = Testing bit (active at "1")
ML = Loudspeaker muting (active at "1")
MV = VCR muting (active at "1")
A0-A9 = Dematrixing (active at "1")
X = Not used

A0-A9

Bits from A0 to A9 represents the values of the attenuator Z shown in figure 2 and 3. Below is listed the value of every bit when it is in the active state :

$A0 = 2^0$ $A1 = 2^{-1}$ $A2 = 2^{-2}$ $A3 = 2^{-3}$ $A4 = 2^{-4}$

$A5 = 2^{-5}$ $A6 = 2^{-6}$ $A7 = 2^{-7}$ $A8 = 2^{-8}$ $A9 = 2^{-9}$

With the following formula it is possible to calculate the value of the attenuator Z :

$$Z = \sum_{n=0}^{n=9} A^n * 2^n$$

Table 2 : Example Table.

	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	Z
Minimum	0	1	0	0	0	0	0	0	0	0	0.5
Medium	1	0	0	0	0	0	0	0	0	0	1
Maximum	1	1	1	1	1	1	1	1	1	1	2

ML and MV

Bits ML and MV are respectively the mute for the loudspeaker output and VCR output. To have the mute active it is necessary to put the relative bit to the level "1". At the switch on the device automatically sets both bits to "1" putting the outputs in mute ; so it is necessary to set them to "0" after every switch on.

Register R3 : (Left channel earphone volume control)

X	X	X	CS5	CS4	CS3	CS2	CS1
MSB							LSB

CS1-CS5 = Volume control
X = Not used

Register R4 : (Right channel earphone volume control)

X	X	X	CD5	CD4	CD3	CD2	CD1
MSB							LSB

CD1-CD5 = Volume control
X = Not used

In the table below are listed the values of the attenuation in dB depending on the bits set in registers R3 and R4 :

Table 3 : Earphone Volume Table.

Binary Code MSB LSB	Attenuation dB
XXX00000	0
XXX00001	2
XXX00010	4
XXX00011	6
XXX00100	8
XXX00101	10
XXX00110	12
XXX00111	14
XXX01000	16
XXX01001	18
XXX01010	20
XXX01011	22
XXX01100	24
XXX01101	26
XXX01110	28
XXX01111	30
XXX10000	32
XXX10001	34
XXX10010	36
XXX10011	38
XXX10100	40
XXX10101	42
XXX10110	44
XXX10111	46
XXX11000	48
XXX11001	50
XXX11010	52
XXX11011	54
XXX11100	56
XXX11101	58
XXX11110	60
XXX11111	MUTE

Register R6 : Configuration switch and special effects)

X	S4	PS	ES	S3	S2	S1	S0
MSB							LSB

S0-S4 = Configuration switch

PS = Pseudostereo

ES = Enlarged stereo base

X = Not used

S0-S4

Bits from S0 to S4 are used to select the desired audio condition of TDA8200. The following table shows all the possible conditions :

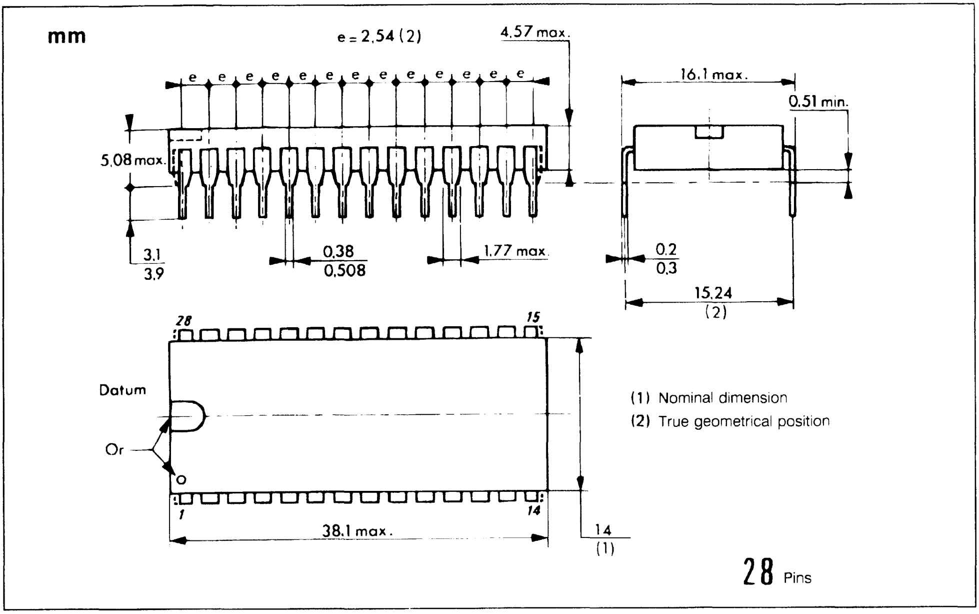
Table 4 : Configuration Switch.

Selection Mode	AM Input	TV Input		VCR Input		VCR Output		Speaker Output		Earph. Output	
S4 S0		AF1	AF2	L	R	L	R	L	R	L	R
00000		$\frac{L+R}{2}$	R	L°	R°	L	R	L°	R°	L°	R°
00001		$\frac{L+R}{2}$	R	1°	2°	L	R	2°	2°	1°	1°
00010		$\frac{L+R}{2}$	R	1°	2°	L	R	1°	1°	2°	2°
00011		$\frac{L+R}{2}$	R			M*	M*	L	R	L	R
00100		$\frac{L+R}{2}$	R			L	R	L	R	L	R
00101		1	2			1	2	2	2	1	1
00110		1	2			1	2	1	1	2	2
00111		1	2			1	1	1	1	1	1
01000		1	2	L°	R°	1	2	L°	R°	L°	R°
01001		1	2	1°	2°	1	2	2°	2°	1°	1°
01010		1	2	1°	2°	1	2	1°	1°	2°	2°
01011		1	2	1°	2°	2	2	2	2	1	1
01100		M		L°	R°	M	M	L°	R°	L°	R°
01101		M		1°	2°	M	M	2°	2°	1°	1°
01110		M		1°	2°	M	M	1°	1°	2°	2°
01111		M				M	M	M	M	M	M
11100	AM			L°	R°	AM	AM	L°	R°	L°	R°
11101	AM			1°	2°	AM	AM	2°	2°	1°	1°
11110	AM			1°	2°	AM	AM	1°	1°	2°	2°
11111	AM					AM	AM	AM	AM	AM	AM
10001		$\frac{L+R}{2}$	R	L°	R°	L°	R°	L	R	L	R
10010		M		L°	R°	L°	R°	M	M	M	M
10011		1	2	L°	R°	L°	R°	1	1	2	2
10100		1	2	L°	R°	L°	R°	2	2	1	1
10101	AM			L°	R°	L°	R°	AM	AM	AM	AM
10110				L°	R°	L°	R°	L°	R°	L°	R°
10111				1°	2°	1°	2°	1°	1°	2°	2°
11000				1°	2°	1°	2°	2°	2°	1°	1°

Where :
M = monophonic standard TV signal B/G
M* = reconstructed monophonic signal starting from L and R
L = left standard TV B/G stereo signal
R = right standard TV B/G stereo signal
1 = bilingual B/G TV standard 1st language
2 = bilingual B/G TV standard 2nd language
L° = VCR stereo left signal
R° = VCR stereo right signal
1° = bilingual VCR 1st language
2° = bilingual VCR 2nd language
AM = monophonic standard L signal

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



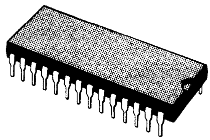
SGS-THOMSON
MICROELECTRONICS

TDA8202

TV STEREO DECODER AND AUDIO PROCESSOR

ADVANCE DATA

- IDENTIFICATION OF TRANSMISSION MODE (mono/stereo/bilingual)
- DEMATRIXING OF THE STEREO AUDIO SIGNAL, WITH AN INTERNAL PROGRAMMABLE S-BUS NETWORK FOR MINIMAL CROSS-TALK
- DE-EMPHASIS OF THE AUDIO SIGNAL WITHOUT EXTERNAL COMPONENTS
- FILTERS FOR PSEUDOSTEREO AND ENLARGED STEREO BASE SPECIAL EFFECTS
- MONOPHONIC INPUT FOR MULTISTANDARD APPLICATIONS
- STEREO INPUT/OUTPUT FOR VCR
- VOLUME AND BALANCE CONTROL FOR LOUDSPEAKER OUTPUT
- ALL FUNCTION PROGRAMMABLE THROUGH USE OF S-BUS



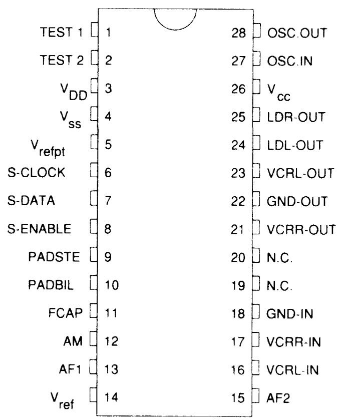
DIP28
(Plastic Package)

ORDER CODE : TDA8202

DESCRIPTION

The TDA8202 combines the functions of audio processor and lowcost stereo decoder for the European 2-carrier B/G system ; moreover, the device also includes input and a stereophonic output for reception of the audio signal coming from the SCART connector as well as a monophonic input for MULTISTANDARD applications (e.g., B/G and L).

PIN CONNECTION



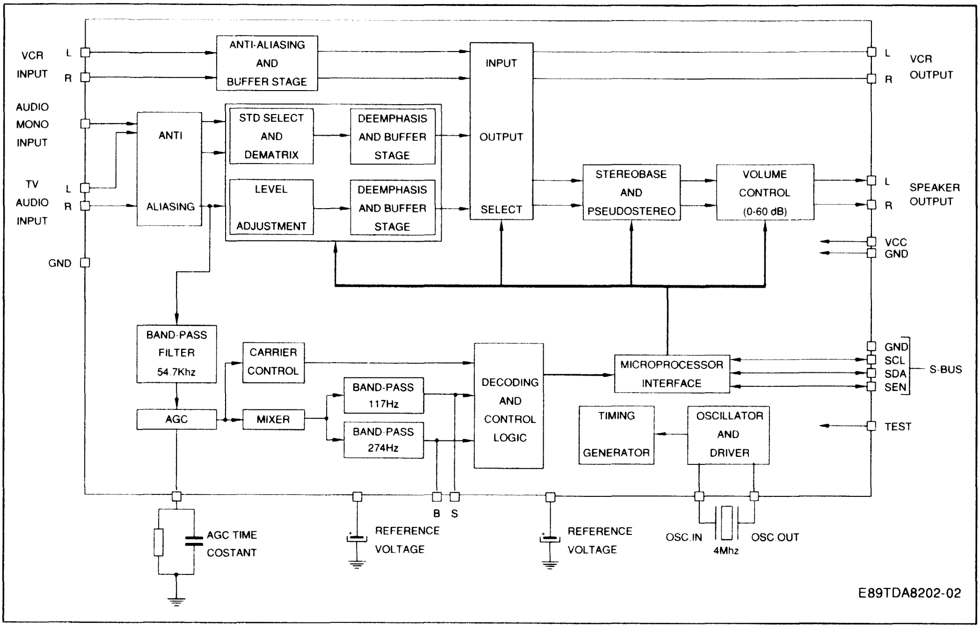
E89TDA8202-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN DESCRIPTION

Pin	Function
1	Reserved for device testing, normally should be connected to mass.
2	Reserved for device testing, normally should be unconnected.
3	Power Voltage for Digital Part and Pilot Tone Vd = 8.5V
4	Mass for Digital Part and for Pilot Tone
5	Reference Voltage for Pilot Tone
6	SCL Clock Input for S-BUS
7	SDA Data Input for S-BUS
8	SEN Enable Input for S-BUS
9	Stereo Modulating Output (117Hz) for Pilot Tone
10	Bilingual Modulating Output (274Hz) for pilot Tone
11	Time Constant for AGC
12	Monophonic Input for Multistandard "AM"
13	Audio Input Signal from 5.5MHz Demodulator, AF1
14	Reference Voltage for Audio Part
15	Audio Input Signal from 5.74MHz Demodulator, AF2
16	Audio Input Signal from Right Channel of VCRR-IN Videotape Machine
17	Audio Input Signal from Left Channel of VCRL-IN Videotape Machine
18	Mass for Audio Input Signal
19	Not Connected
20	Not Connected
21	Audio Output Signal from Right Channel of VCRR-OUT Videotape Machine
22	Mass for Audio Output Signal
23	Audio Output Signal from Left Channel of VCRL-OUT Videotape Machine
24	Audio Output Signal from Right Channel of LDR-OUT Loudspeakers
25	Audio Output Signal from Left Channel of LDL-OUT Loudspeakers
26	Input Voltage for Analog Part Va = 8.5V
27	Oscillator Input at 4MHz
28	Oscillator Output at 4MHz

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The device is made up of 5 main sections :

1 S-BUS interface
2 Oscillator and power on reset
3 Pilot tone decoder
4 Dematrixing and de-emphasis of the audio signal
5 Reception of the audio signal

1) S-BUS INTERFACE

All of the TDA8202 functions are activated by microprocessors, using a 3-wire serial bus (SCL, SDA, SEN). For further information, see the software section.

2) OSCILLATOR AND POWER ON RESET

OSCILLATOR. The device functions with an external 4MHz crystal quartz connected to pins 27 and 28. A possible alternative is to connect pin 27 to an external 4MHz generator. If the clock frequency does not remain stable, there will be variations in the audio response and pilot tone decoding.

POWER ON RESET. About 120ms after V_{CC} power has reached the required level for correct device operation, the power on reset circuit signals correct operating status, using the RES bit in the RR register. For further information, see the software section.

3) PILOT TONE DECODING

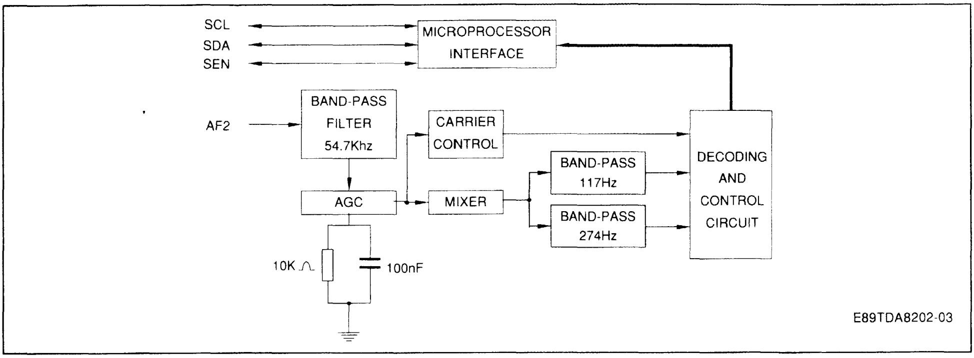
The pilot tone decoding section is used to identify the transmission mode (monophonic, stereophonic or bilingual) in B/G standard.

Figure 1 shows the block diagram for the circuit described hereafter :

The decoding signal goes through the pass-band filter at a frequency of 54.7kHz to the AF2 input in order to eliminate undesirable frequencies.

To guarantee a recognition range from 10 to 300mVeff for a carrier at 54.7kHz, the signal goes throught an AGC circuit the control velocity of which is based on pin 11's capacity. To be able to esta-blish transmission type, the signal is demodulated by the MIXER and filtered into the 117Hz (stereo transmission) and 274Hz (bilingual transmission) fixed frequencies. If, at the output of only one of the two filters, the signal is present, the "DECODING AND CONTROL CIRCUIT" block verifies if the carrier frequency is correct, using the "CARRIER CONTROL" block, and transmits the information to bits B and S of the RR register.

Figure 1 : Pilot Tone Decoder.



4) DEMATRIXING AND DE-EMPHASIS

DEMATRIXING. No external component is used for dematrixing the audio signal, but only a programmable attenuator throught S-BUS. Attenuation value must be set in calibration phase for the television set, and loaded every time the TV is turned on by the microprocessor in the R7 and R0 registers of the TDA8202.

Shown below is the dematrixing circuit which differentiates between the STEREO and BILINGUAL signals.

Figure 2 : Stereo Scheme.

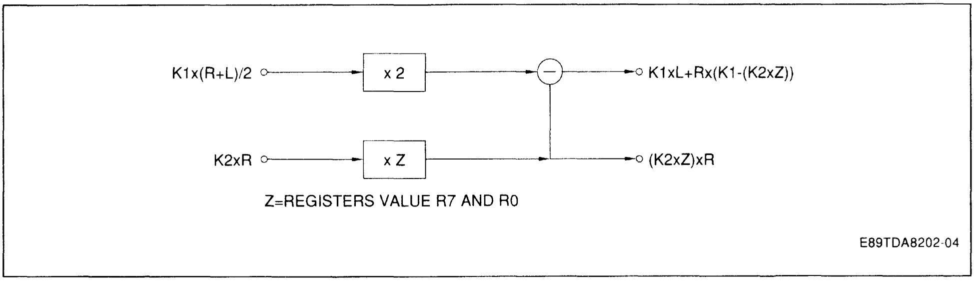
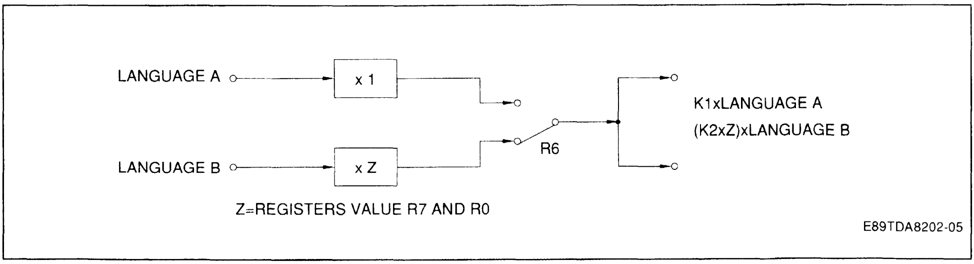


Figure 3 : Bilingual Scheme.



In both circuits, account is taken of the K1 and K2 constants which represent the removal of the AF1 and AF2 signals arriving from the FM demodulator in favor of the real AF1 and AF2 signals transmitted by the generator.

From the output equations can be deduced that, for K1 = K2x Z, can be obtained, based on precision of Z, the left (L) channel and the correct amplitude of the outputs for the STEREO signal, as well as for the BILINGUAL signals.

As far as the STEREO signal is concerned, a typical value of diaphony between left and right channels of 48dB can be guaranteed by a relationship between K1/K2 of 0.5 to 2, calculated in the following equation :

CT = 20*log[(K1/K2) /2E-9]

In the case of a BILINGUAL signal, a minimal difference in the signal ; between languages A and B of 0.05dB can be guaranteed by a relationship between K1 and K2 between 0.3 and 2, calculated with the following equation :

K(l-r) = 20*log{(K1/K2) /[(K1/K2) + 2E-9]}

DE-EMPHASIS. The de-emphasis of the AF1 and AF2 signals coming from the FM demodulator are carried out internally in the device without using external components.

5) AUDIO SIGNAL RECEPTION

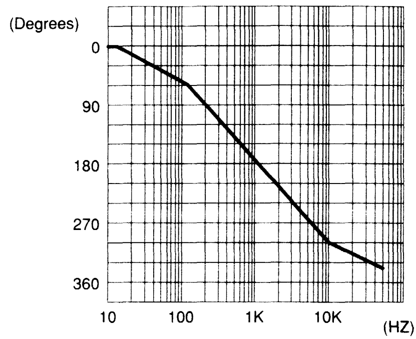
Audio signal reception is made up of three essential parts (see block diagram) :

a) INPUT OUTPUT SELECT. This circuit deals with shunting the signal coming from the three inputs (VCR, MONO, TV) into the two outputs (VCR, SPEAKER) in the modes described by the 5 bits S0-S4 in the R6 register. Information on possible configuration is detailed in the software section.

b) ENLARGED STEREO BASE AND PSEUDO-STEREO. The special effects function only for the loudspeaker output, and are activated by the PS and ES bits of R6. Operation is as follows :

- **PSEUDOSTEREO**, activated by the PS bit, is used with monophonic signals, and consists in the movement of the right channel phase toward the left, on the basis of the frequency as described in figure 4.
- **ENLARGED STEREO BASE**, activated by the ES bit, is used for stereophonic signals, and the function is that of making the stereo effect evident, even when the distance between the loudspeakers is reduced. For that purpose, diaphony is introduced in opposition to the right phase and vice versa. The extent of the diaphony to be introduced depends on the distance between the loudspeakers ; in the TDA8202, the diaphony is in the range of 50%.

Figure 4 : Right Channel Phase.



c) VOLUME CONTROL. The loudspeaker output also has a circuit to control and balance volume, carried out by two logarithmic attenuators of 2dB a spet with a maximum attenuation value of 60dB. The attenuation depends on the configuration of the 5 bits, CS1-CS5 of R3 for the left channel and the 5 bits, CD1-CD5 of R4 for the right channel ; the values in dB are shown in table N. 3 shown in the software section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V28	Analog. Supply Voltage	Max 10	V
Vi	Input Voltage (all input)	– 0.3 to Vs + 0.3	V
Ii	Input Current (all input)	Max 5	mA
Io	Output Current (all output)	Max 10	mA
Tstg	Storage Temperature	– 25 to 125	°C

ELECTRICAL CHARACTERISTICS

Refer to the test circuit, Vs = 8.5V, Tamb = 25°C, without special effects, unless otherwise specified.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Suppply Voltage	8	8.5	9	V
Is	Supply Current		30		mA
SVR	Supply Voltage Rejection (Fripple = 100Hz)		35		dB

AUDIO INPUT CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vin	Voltage Amplitude on all Inputs		1		Vrms
n	Amplitude Ratio between AF1/AF2	0.5		2	
Rin	Resistance on all Audio Inputs	10	40		kΩ

VOLUME CONTROL CHARACTERISTICS

Speaker

Symbol	Parameter	Min.	Typ.	Max.	Unit
KV	Volume Control Range ; Kvmax/Kvmin		60		dB
KVmin	Attenuator Resolution/step		2		dB
Ke	Tracking Error KV = 0 to 60dB		± 1	± 2	dB
KB	Balance Control Range ; KV = 0dB		60		dB

SPECIAL EFFECT CHARACTERISTICS

Pseudostereo

Symbol	Parameter	Min.	Typ.	Max.	Unit
Psh	Phase Shifter Response at : 100HZ 1kHZ 10kHZ		0 180 360		Deg Deg Deg
K(l-r)	Amplitude Tracking Error between Left and Right Channels (KV = 0dB)		± 0.5	± 1	dB

Enlarged Stereo Base

Symbol	Parameter	Min.	Typ.	Max.	Unit
K(l-r)	Amplitude Tracking Error between Left and Right Channel (KV = 0dB)		± 0.5	± 1	dB

DE-EMPHASIS CHARACTERISTICS (active only in AF1/AF2 input)

Symbol	Parameter	Min.	Typ.	Max.	Unit
td	Time Constant	45	50	55	µs

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
Vo	Audio Output Voltage Amplitude (THD ≤ 1%, all outputs)			Vin		Vrms
Kmax	Max Gain at Min. Attenuation (all outputs)		– 1	0	+ 1	dB
K(l-r)	Gain Tolerance between Left and Right Channel at Min. Attenuation (speaker K = 0dB)			± 0.5	± 1	dB
Ro	Resistance on all Audio Output				1	kΩ
R_l	Load Resistance (all outputs) Note : all outputs are short circuit protected.		5			kΩ
C_l	Load Capacitance (all outputs)				2	nF
AT	Muting Attenuation (all outputs)		70	80		dB
En	Output Noise Voltage (CCIR 468-2)					
	VCR Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		100	200	µV
		KV = 40dB		50	100	µV
	VCR			100	200	µV
	AM Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		100	200	µV
		KV = 40dB		50	100	µV
	VCR			100	200	µV
	AF1/AF2 Input					
	OUTPUT					
	Loudspeaker	KV = 0dB		200	300	µV
		KV = 40dB		50	100	µV
	VCR			200	300	µV
S/N	Signal to Noise Ratio (CCIR 468-2)					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	VCR		75	80		dB
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	80		dB
		KV = 40dB	35	45		dB
	VCR		75	80		dB
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	75		dB
		KV = 40dB	35	45		dB
	VCR		70	75		dB

ELECTRICAL CHARACTERISTICS (continued)

AUDIO OUTPUT CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
d	Total Harmonic Distortion					
	VCR Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
	AM Input : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
	AF1/AF2 Input Bilingual : (Vi = 1Vrms, Fi = 1kHz)					
	OUTPUT					
	Loudspeaker	KV = 0dB		0.2	0.4	%
	VCR			0.2	0.4	%
CT	Crosstalk between Left and Right Channel					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Stereo :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	VCR		70	80		dB
	AF1/AF2 Input Stereo :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	60	70		dB
	VCR		70	80		dB
CTb	Bilingual Crosstalk					
	(Vi = 1Vrms, Fi = 50Hz ÷ 15kHz, Bw = 10Hz)					
	VCR Input Bilingual :					
	OUTPUT					
	Loudspeaker	KV = 0dB	75	85		dB
		KV = 20dB	75	85		dB
	AF1/AF2 Input Bilingual :					
	OUTPUT					
	Loudspeaker	KV = 0dB	70	80		dB
		KV = 20dB	70	80		dB
CTI	Crosstalk between VCR and TV Section		70	80		dB

S-BUS CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vil	Input Voltage Low Level	Vss		0.8	V
Vih	Input Voltage High Level	2		VDD	V
Iil-ih	Input Current			1	µA
Iol	Output Low Current Capability (Vol = 0.45V)	5			mA
Ioh	Leakage Output Current (Vo = 5.25V, output off, Vs = 8.5V)			10	µA

ELECTRICAL CHARACTERISTICS (continued)

PILOT TONE CHARACTERISTICS V1 = 50mVrms, m = 0.5, unless otherwise specified.

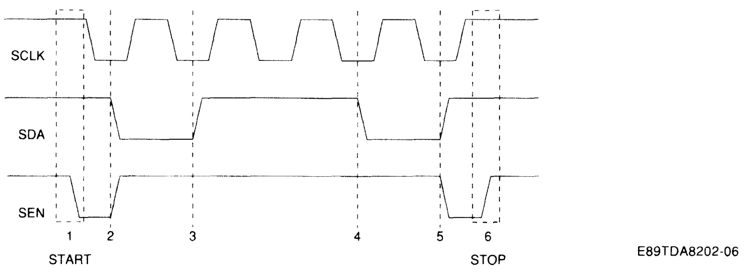
Symbol	Parameter	Min.	Typ.	Max.	Unit
V1	Input Voltage Amplitude (without AM modulation)	10		300	mVrms
dfp	Frequency Range of Carrier to 54687.5Hz		± 1		kHz
dfs	Frequency Range of Stereo Filter (117.4Hz)		± 3		Hz
dft	Frequency Range of Bilingual Filter (274Hz)		± 6		Hz
dm	Range of AM Modulation Index	40	50	60	%

SOFTWARE INFORMATIONS

S-BUS DESCRIPTION

Shown below is the timing diagram of the S-BUS protocol :

Figure 5 : S-BUS Timing Diagram.

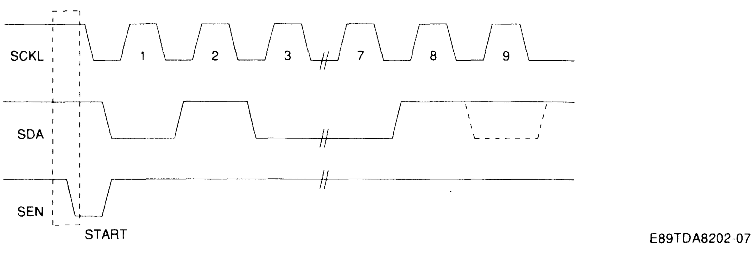


The START/STOP conditions (points 1 and 6) occur only by a transmission of SEN wire (10 and 01 respectively) while the SCL wire is in high state (1).

During transmission, the SDA wire can change only when SCL wire is in low state (points 2, 3, 4, 5). After START condition (point 1), the SEN wire must change to high state (point 2) and it remains in this condition for the whole transmission.
At the end of transmission (point 5), the SDA wire change to high state and in the mean time, the SEN wire must go to low state and then it returns to high state to generate the STOP condition (point 6).

After the transmission of each byte (composed of 8 bits), there is an ACKNOWLEDGE bit appointed by a high state on SDA wire generated by the transmitter. The device that acknowledges, forces to low state the SDA wire during the time of the acknowledge clock pulse, as described in figure 6 :

Figure 6 : Acknowledge Bit.



In normal conditions, the addressed device must acknowledge after each byte received. If the SDA wire, during the 9th pulse, remains in high state, the master-transmitter can generate the STOP condition to abort the transfer.

Interface between the microprocessor and the TDA8202 occurs through use of the following protocol :

- a start condition (START) see figure 7 and 8
- an address byte, containing the address reserved for the TDA8202 (1000000x) and the bus transmission direction (this information is located in the byte's 8th bit, in which "0" indicates a write, and "1", a read, by the microprocessor). At the end of each byte, the TDA8202 must give the ACKNOWLEDGE signal
- a byte for addressing the registers in write, or the content of register RR in a read
- a third byte containing the information to be written on the register
- a stop condition (STOP)

Figure 7 : Write Protocol Example.

TDA8202 ADDRESS — MSB FIRST BYTE LSB; REGISTER ADDRESS — MSB SECOND BYTE LSB; DATA ADDRESS — MSB 3RD BYTE LSB

S	1	0	0	0	0	0	0	0	ACK	X	X	X	X	X	A3	A2	A1	ACK									ACK	P

Figure 8 : Read Protocol Example.

TDA8202 ADDRESS — MSB FIRST BYTE LSB; REGISTER RR — MSB SECOND BYTE LSB

S	1	0	0	0	0	0	0	1	ACK		ACK	P

Table 1 : TDA8202 Register Address.

Register Name	Address			Content	Type of Operation
	A3	A2	A1		
R0	0	0	0	Dematrixing and Muting	WRITE ONLY
R3	0	1	1	Left Speaker Volume Channel (60dB)	WRITE ONLY
R4	1	0	0	Right Speaker Volume Channel (60dB)	WRITE ONLY
R6	1	1	0	Configuration Switch and Special Effects	WRITE ONLY
R7	1	1	1	Dematrixing	WRITE ONLY
RR				Transmission Conditions and Power on Reset	READ ONLY

REGISTER CONTENTS

RR REGISTER : (Transmission conditions and power on reset)

X	X	X	X	X	RES	B	S
MSB							LSB

B = Bilingual transmission (active at "1")
S = Stereo transmission (active at "1")
RES = Power on reset (active at "1")
X = Not used

RES

The RES bit in RR register is set to "1" every time that the supply voltage falls under the minimum level required for the correct operation of TDA8202. In this case the device automatically inserts the muting on the outputs (R0, ML and MV ; R3 and R4 are both at "1"), and resets bits B and S in RR to "0".

The microprocessor must verify this situation and when the RES bit returns to "0", it initializes the registers to the desired audio status.

B and S

B and S are the bits reserved to identify the transmission type in B/G standard. If both bits are at "0", the transmission is MONO, while if only one bit is at "1", the transmission is STEREO (S at "1") or BILINGUAL (B at "1").

REGISTER R0 : (Dematrixing and muting)

X	X	X	TS	X	MV	A8	A9
MSB							LSB

REGISTER R7 : (Dematrixing)

A0	A1	A2	A3	A4	A5	A6	A7
MSB							LSB

TS = Testing bit (active at "1")
MV = VCR muting (active at "1")
A0-A9 = Dematrixing (active at "1")
X = Not used

A0-A9

Bits from A0 to A9 represents the values of the attenuator Z shown in figure 2 and 3. Below is listed the value of every bits when it is in the active state :

A0 = 2^0 A1 = 2^{-1} A2 = 2^{-2} A3 = 2^{-3} A4 = 2^{-4}
A5 = 2^{-5} A6 = 2^{-6} A7 = 2^{-7} A8 = 2^{-8} A9 = 2^{-9}

With the following formula it is possible to calculate the value of the attenuator Z :

$$Z = \sum_{n=0}^{n=9} A^n * 2^n$$

Table 2 : Example Table.

	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	Z
Minimum	0	1	0	0	0	0	0	0	0	0	0.5
Medium	1	0	0	0	0	0	0	0	0	0	1
Maximum	1	1	1	1	1	1	1	1	1	1	2

MV

Bit MV is the mute for the VCR output. To have the mute active it is necessary to put the bit to the level "1". At the switch on the device automatically set bit to "1" putting the output in mute ; so it is necessary to set it to "0" after every, switch on.

REGISTER R3 : (Left channel loudspeaker volume control)

X	X	X	CS5	CS4	CS3	CS2	CS1
MSB							LSB

CS1-CS5 = Volume control
X = Not used

REGISTER R4 : (Right channel loudspeaker volume control)

X	X	X	CD5	CD4	CD3	CD2	CD1
MSB							LSB

CD1-CD5 = Volume control
X = Not used

In the table below are listed the values of the attenuation in dB depending on the bits set in registers R3 and R4 :

Table 3 : Speaker Volume Table.

Binary Code MSB LSB	Attenuation dB
XXX00000	0
XXX00001	2
XXX00010	4
XXX00011	6
XXX00100	8
XXX00101	10
XXX00110	12
XXX00111	14
XXX01000	16
XXX01001	18
XXX01010	20
XXX01011	22
XXX01100	24
XXX01101	26
XXX01110	28
XXX01111	30
XXX10000	32
XXX10001	34
XXX10010	36
XXX10011	38
XXX10100	40
XXX10101	42
XXX10110	44
XXX10111	46
XXX11000	48
XXX11001	50
XXX11010	52
XXX11011	54
XXX11100	56
XXX11101	58
XXX11110	60
XXX11111	MUTE

REGISTER R6 : (Configuration switch and special effects)

X	S4	PS	ES	S3	S2	S1	S0
MSB							LSB

S0-S4 = Configuration switch

PS = Pseudostereo

ES = Enlarged stereo base

X = Not used

S0-S4

Bits from S0 to S4 are used to select the desired audio condition of TDA8202. The following table shows all the possible conditions :

Table 4 : Configuration Switch.

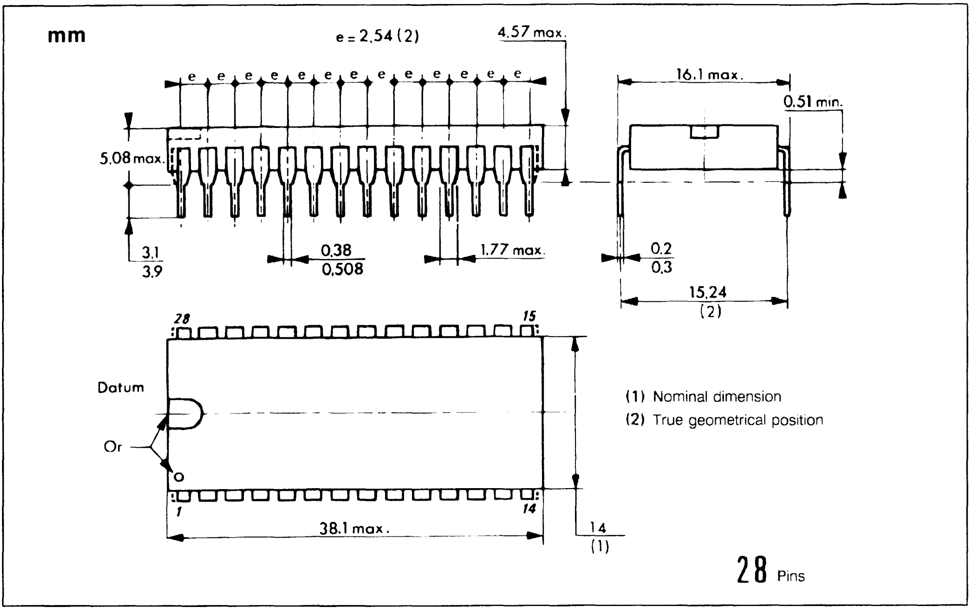
Selection Code	AM Input	TV Input		VCR Input		VCR Output		Speaker Output	
S4 S0		AF1	AF2	L	R	L	R	L	R
00000		$\frac{L+R}{2}$	R	L°	R°	L	R	L°	R°
00001		$\frac{L+R}{2}$	R	1°	2°	L	R	2°	2°
00010		$\frac{L+R}{2}$	R	1°	2°	L	R	1°	1°
00011		$\frac{L+R}{2}$	R			M*	M*	L	R
00100		$\frac{L+R}{2}$	R			L	R	L	R
00101		1	2			1	2	2	2
00110		1	2			1	2	1	1
00111		1	2			1	1	1	1
01000		1	2	L°	R°	1	2	L°	R°
01001		1	2	1°	2°	1	2	2°	2°
01010		1	2	1°	2°	1	2	1°	1°
01011		1	2	1°	2°	2	2	2	2
01100		M		L°	R°	M	M	L°	R°
01101		M		1°	2°	M	M	2°	2°
01110		M		1°	2°	M	M	1°	1°
01111		M				M	M	M	M
11100	AM			L°	R°	AM	AM	L°	R°
11101	AM			1°	2°	AM	AM	2°	2°
11110	AM			1°	2°	AM	AM	1°	1°
11111	AM					AM	AM	AM	AM
10001		$\frac{L+R}{2}$	R	L°	R°	L°	R°	L	R
10010		M		L°	R°	L°	R°	M	M
10011		1	2	L°	R°	L°	R°	1	1
10100		1	2	L°	R°	L°	R°	2	2
10101	AM			L°	R°	L°	R°	AM	AM
10110				L°	R°	L°	R°	L°	R°
10111				1°	2°	1°	2°	1°	1°
11000				1°	2°	1°	2°	2°	2°

Where :

M = monophonic standard TV signal B/G
M* = reconstructed monophonic signal starting from L and R
L = left standard TV B/G stereo signal
R = right standard TV B/G stereo signal
1 = bilingual B/G TV standard 1st language
2 = bilingual B/G TV standard 2nd language
L° = VCR stereo left signal
R° = VCR stereo right signal
1° = bilingual VCR 1st language
2° = bilingual VCR 2nd language
AM = monophonic standard L signal

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP

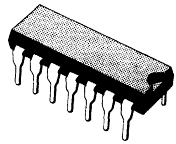


SGS-THOMSON
MICROELECTRONICS

TEA1014

VIDEO AND AUDIO SIGNALS SWITCHING FOR THE PERI-TELEVISION PLUG

- VIDEO CROSSTALK : 60 dB TYPICAL
- LOW IMPEDANCE VIDEO OUTPUT 75 Ω
- SHORT-CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- INTERNAL HORIZONTAL PLL TIME CONSTANT SWITCHING IN CASE OF VIDEO RECORDER RECEPTION



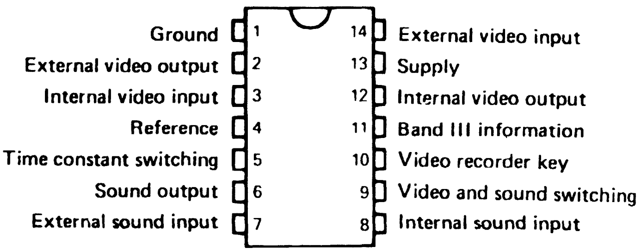
TEA1014
DIP14
(Plastic Package)

DESCRIPTION

This integrated circuit provides all video and sound switching allowing connections between the peri-TV plug and video, sound sections in the TV set.

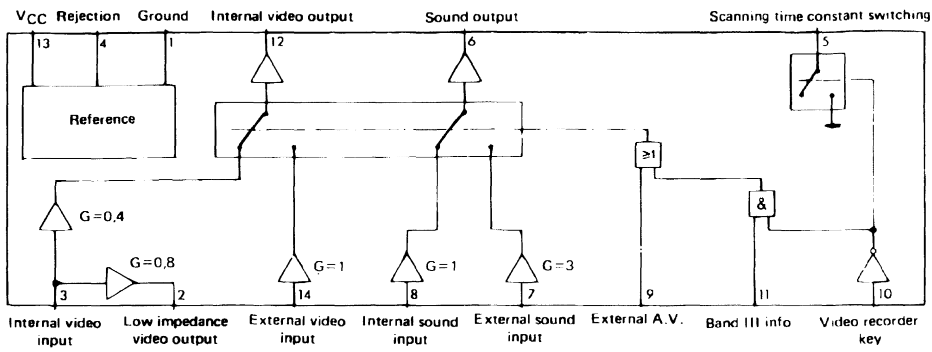
Input and output signal characteristics follow the NFC 92250/EN 50049 norms.

PIN CONNECTIONS



E88TEA1014-01

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The main functions of the I.C. are following :

VIDEO SWITCHING

2 electronically switched inputs :

- one 2.5 Vpp input for internal video.
- one 1 Vpp input for signal coming from the peri-TV plug.

2 outputs :

- 1 Vpp output (low impedance 75 Ω) for peri-TV plug.
- 1 Vpp output low impedance for video section of the TV set.

Each input and output is protected from ground short-circuit. The 75 Ω output is protected through a 75 Ω resistor.

AUDIO SWITCHING

Two electronically switched inputs :

- 300 mV rms input coming from internal audio.
- 100 mV rms input coming from the peri-TV plug
- one low impedance output 300 mV rms.

Inputs and outputs are also protected against ground short-circuit.

SWITCHING LOGIC

The logic takes into account the informations on 3 pins.

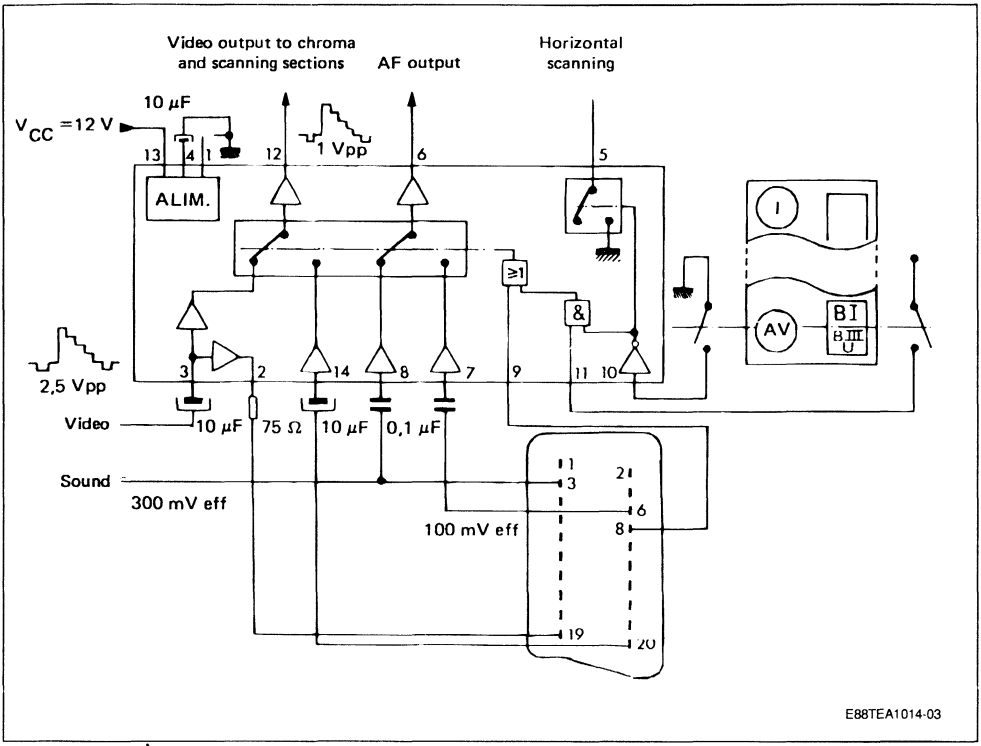
- Internal or external video and sound (pin 8 peri TV plug)
- Band III information
- Video recorder key.

External Video and Audio signals are selected in two cases.

- When there is a voltage information coming from peri-TV plug.
- When the video recorder key is selected (on TV front panel) and programmed on band III.

This I.C. includes an internal switch (open collector transistor) which commutes the time constant of the horizontal PLL circuit in case of video recorder reception.

APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{stg}	Storage Temperature Range	– 40, + 150	°C
T_j	Junction Temperature	+ 150	°C
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C

THERMAL DATA

$R_{th(j-a)}$	Junction Ambient Thermal Resistance	90	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = 12 V ; T_{amb} = + 25 °C (unless otherwise specified)

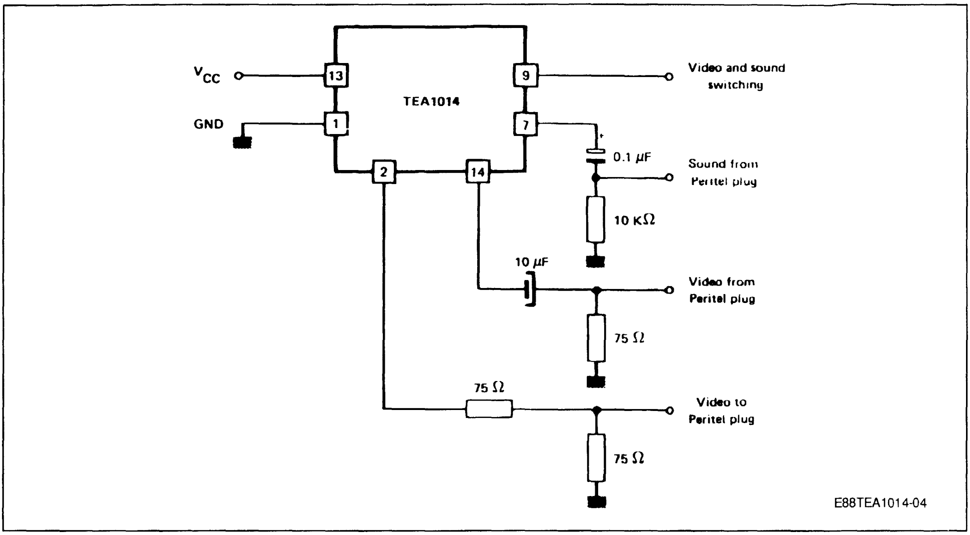
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply Current, with no Load		37	50	mA
	Internal Video Input (coming from picture FI) (pin 3)				
	Video Signal Amplitude (positive video)		2.5	6.8	Vpp
	Input Voltage Range (refered to D. C. input Voltage)	– 2.9		+ 3.9	V
	Input Impedance	5			kΩ
	Input Capacitance			5	pF
	External Video Input (coming from peri-TV plug) (pin 14)				
	Video Signal Amplitude (positive video)		1	2.8	Vpp
	Input Voltage Range (refered to D. C. input Voltage)	– 1.2		+ 1.6	V
	Input Impedance	5			kΩ
	Input Capacitance			5	pF
	TV Video Output (pin 12)				
	Signal Amplitude		1	2.8	Vpp
	Output Voltage Swing (refered to D. C. output Voltage)	– 1.2		+ 1.6	V
	Output Dynamic Impedance			10	Ω
	D. C. Output Voltage (without input signal)		3.5		V
	Loading Resistance	300			Ω
	Video Bandwidth (– 1 dB)	6			MHz
	Gain/internal Video	– 9.5	– 8	– 6.5	dB
	Gain/external Video	– 1.5	0	+ 1.5	dB
	External Video Output (low impedance) (pin 2)				
	Signal Amplitude (on 150 Ω grounded)		2	5.5	Vpp
	Output Voltage Swing	– 2.4		+ 3.1	V
	Dynamic Output Impedance		10		Ω
	D. C. Output Voltage (without input signal)		3.5		V
	Minimum Loading Resistance (electrical performance non specified)	75			Ω
	Gain/internal Video	– 3.5	– 2	– 0.5	dB
	Output Video Signals Characteristics				
	Video Rejection between two Inputs (1 MHz)	– 55			dB
	Differential Group Delay			20	ns
	Linearity Distortion				
	Luma (test line 17)		2		%
	Chroma (test line 331)		2		%
	Intermodulation Luma–chroma (test line 331)		5		%
	Supply Voltage Rejection	45			dB

ELECTRICAL OPERATING CHARACTERISTICS (continued)
V_{CC} = 12 V ; T_{amb} = + 25 °C (unless otherwise specified)

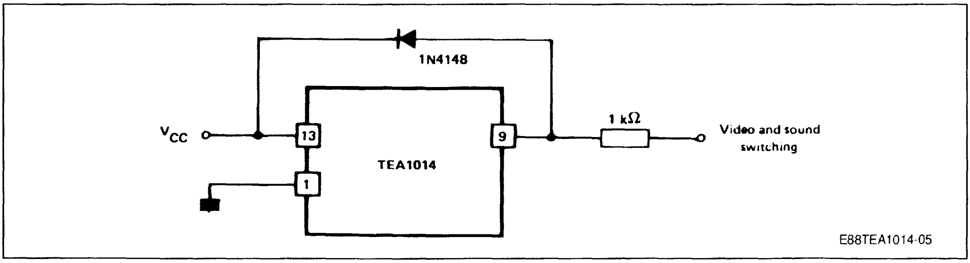
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Internal Sound Input (pin 8)				
	Input Signal		0.3	2	Veff
	Input Impedance		20		kΩ
	External Sound Input (pin 7)				
	Input Signal		0.1	0.7	Veff
	Input Impedance		20		kΩ
	Sound Output (pin 6)				
	Output Signal Amplitude		0.3		Veff
	Output Voltage Swing		2		Veff
	Distortion (V_O = 0.6 V_{eff})			0.5	%
	Bandwidth	16			kHz
	Output Impedance		40		Ω
	Load Impedance	2			kΩ
	Gain/internal Input	– 1.5	0	+ 1.5	dB
	Gain/exteranl Input	8	9.5	11	dB
	Supply Voltage Rejection	60			dB
	Crosstalk	– 60			dB
	Video/sound Crosstalk	– 60			dB
	LOGIC				
	External A. V. Input (peri-TV plug) (pin 9)				
	Unactive Low Level or Unconnected Pin (logic state 0) – (TV receiving)	0		3	V
	Active High Level (logic state 1) (ext. receiving)	9		V_{CC}	V
	Input Impedance		10		kΩ
	"Band III" Input (pin 11)				
	Unactive Low Level or Unconnected Pin (logic state 0)	0		+ 3	V
	Active High Level (logic state 1)	9		V_{CC}	V
	Input Impedance High Level		10		kΩ
	Input Current Low Level			1	µA
	Video–recorder Key Input (pin 10)				
	Unactive High Level or Unconnected Pin (logic state 1)	9		V_{CC}	V
	Active Low Level (logic state 0)	0		3	V
	Input Impedance		10		kΩ
	Open Collector Output (time-constant switching) (pin 5)				
	Leakage Current (open collector)			1	µA
	Maximum Low Level Voltage (I(5) = 4 mA)			1.5	V

SAFETY INFORMATION FOR CRITICAL APPLICATIONS

Typical Connection Between Peritel Plug and TEA2014.

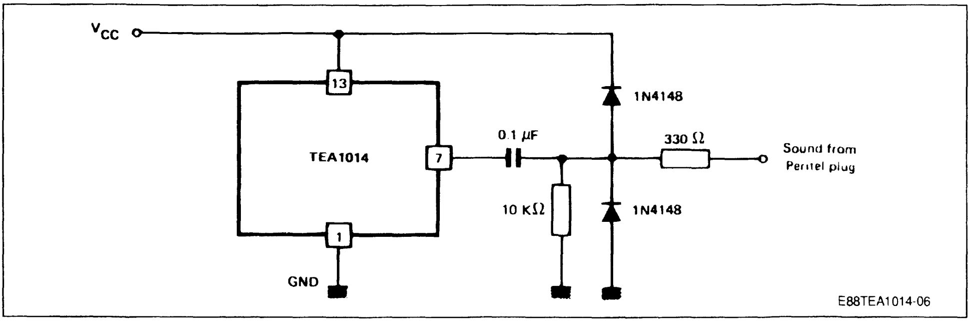


Voltage on pin 9 must not exceed the V_{CC} voltage on pin 13. In case of risk of over voltage, use the protection as described as below :



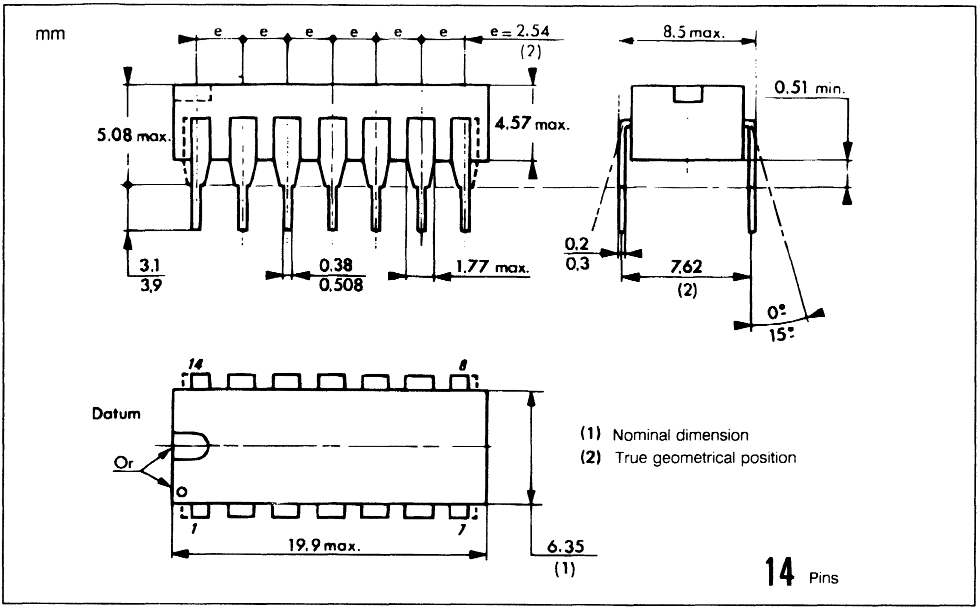
All connections to Peritel plug are terminated by low impedance loads (75 W), except the external sound input.

In case of risk of electrostatic discharge, use the protection as described as below.



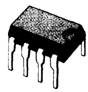
PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP



VIDEO SWITCH

- 1 VIDEO OUTPUT 75 Ω - 1 V_{PP} NOT SWITCHED
- 1 SWITCHED VIDEO OUTPUT 2 V_{PP}
- VIDEO CROSSTALK : 50 dB TYPICAL
- SHORT CIRCUIT PROTECTION OF INPUTS AND OUTPUTS
- CLAMPED VIDEO INPUTS

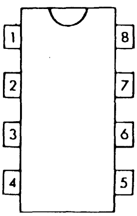


TEA2014A
DIP8
(Plastic package)

DESCRIPTION

This integrated circuit provides all video switching allowing connections between the peri TV plug and video sections in the TV set. The TEA2014A is supplied in a DIL8.

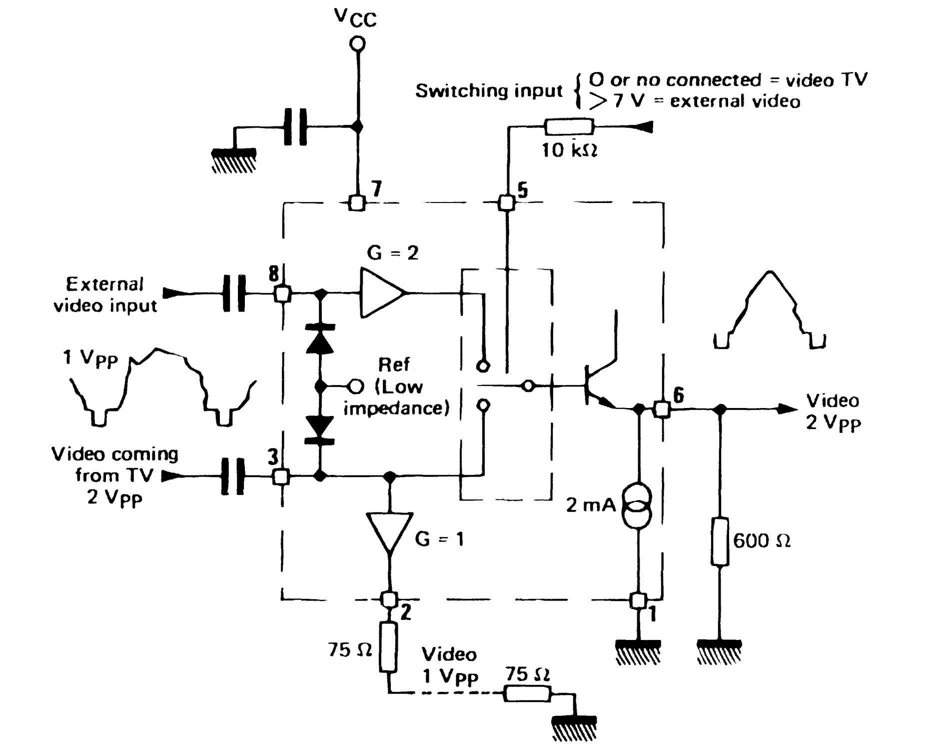
PIN CONNECTIONS



E88TEA2014A-01

1 - Ground
2 - 75 Ω video output
3 - Internal video input
4 - Not to be used
5 - Switching input
6 - Switched video output
7 - Supply voltage
8 - External video input

TYPICAL APPLICATION AND TEST CIRCUIT



We advice to protect the 75 Ω output through a 75 Ω resistor for supply voltage higher than 9 V. E88TEA2014A-02

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_{oper}	Operating Temperature with Load > 150 Ω on PIN 2 with Load = 75 Ω on PIN 2	 0, + 100 0, + 70	°C
T_j	Junction Temperature	– 40, + 150	°C
T_{stg}	Storage Temperature	– 40, + 150	°C
–	Minimum DC Load Resistor PIN 6 Minimum DC Load Resistor PIN 2	600 75	Ω Ω

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	90 Typ	°C/W

ELECTRICAL CHARACTERISTICS

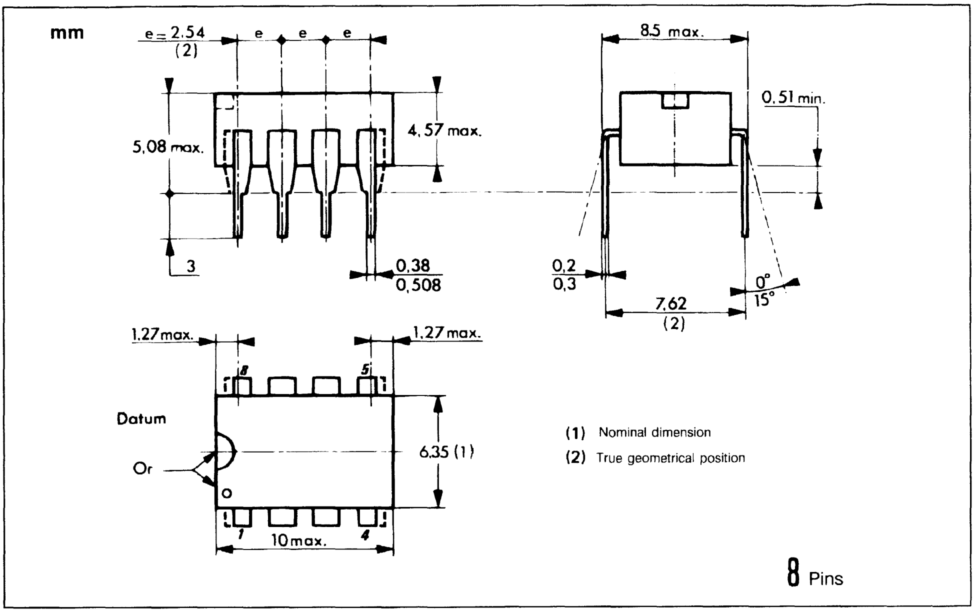
T_{amb} = + 25 °C, V_{CC} = 9 V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	8	–	14	V
I_{CC}	Supply Current (no load on pin 2 and pin 6)	–	–	20	mA
I_{CC}	Supply Current (with 75 Ω pin 2.1, with 600 Ω between pin 6.1)	–	75	–	mA
P_{tot}	Total Power Dissipation with Load	–	450	–	mW
	INPUTS (pin 8 and pin 3)				
–	Internal Video Input Swing from Picture IF (positive Video)	–	–	4.5	Vpp
–	Internal Video Input Impedance (positive video)	50	–	–	kΩ
–	Internal Video Input Bias Current (positive video)	6	25	40	μA
–	External Video Input Swing (positive video)	–	–	2	Vpp
–	External Video Input Impedance (positive video)	50	–	–	kΩ
	SWITCHED OUTPUT (pin 6) - R_{LOAD} = 600 Ω				
–	Video Output Swing	4.5	–	–	Vpp
–	Video Output Dynamic Impedance	–	–	25	Ω
–	Video DC Output Voltage (sync. pulse level note 1)	1.7	2	2.4	V
–	Video Bandwith Pin 6 – from Internal Input pin 3 (– 1 dB)	6	–	–	MHz
–	Video Bandwith Pin 6 – from External Input Pin 8 (– 3 dB)	6	–	–	MHz
–	Output Gain Pin 6 – Pin 8	+ 5	+ 6	+ 7	dB
–	Output Gain Pin 6 – Pin 3	– 1	– 0.5	0	dB
	EXTERNAL OUTPUT (pin 2) - R_{LOAD} = 75 Ω				
–	Video Output Swing	2.2	–	–	Vpp
–	Video Output Dynamic Impedance	–	10	–	Ω
–	Video DC Output Voltage (sync. pulse level , note 1)	1.7	2	2.4	V
–	Video Bandwidth (– 1dB)	6	–	–	MHz
–	Video Output Gain (pin 2 – pin 3)	– 1.8	– 1	– 0.4	dB
	SWITCHING INPUT (pin 5)				
–	Switching Input Unactive Low Level or Unconnected Pin (TV receiving)	0	–	3	V
–	Switching Input Active Level (ext. receiving)	7	–	V_{CC}	V
–	Switching Input Impedance	10	–	–	kΩ
	OTHER DYNAMIC FEATURES				
–	Video rejection Between Two Inputs 1MHz 1kHz	 – – 50	 – 50 –	 – –	 dB dB
–	Linearity Distortion Luma (test line 17) Chroma (test line 331) Intermodulation Luma – Chroma (test line 331)	 – – –	 2 2 5	 – – –	 % % %
–	Supply Voltage Rejection (1 kHz)	40	50	–	dB

Note : 1. Use a video signal with a synchro pulse in order to make the clamp work in a correct way. (75 Ω to the ground and 10 μF in series).

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP

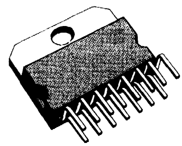


SGS-THOMSON
MICROELECTRONICS

TEA2017

HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT FRAME YOKE DRIVE ±1.5A DRIVING CURRENT
- LINE DARLINGTON DRIVING CAPABILITY
- BUILT-IN FRAME SEPARATOR WITHOUT EXTERNAL COMPONENTS
- MUTING OUTPUT
- INTEGRATED FLYBACK GENERATOR
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- VERY FEW EXTERNAL COMPONENTS
- HIGH DISSIPATION POWER PACKAGE



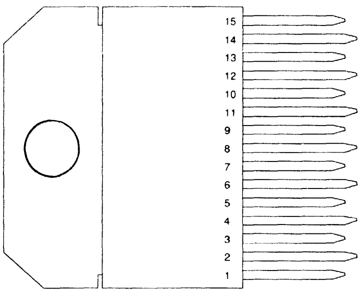
TEA2017
SIP 15
(Plastic Package)

DESCRIPTION

The TEA2017 is an horizontal and vertical deflection circuit. It is particulary intended for black and white TV and display video units but it can also be used in low cost color TV applications. The TEA2017 provides a low cost deflection system.

PIN CONNECTIONS

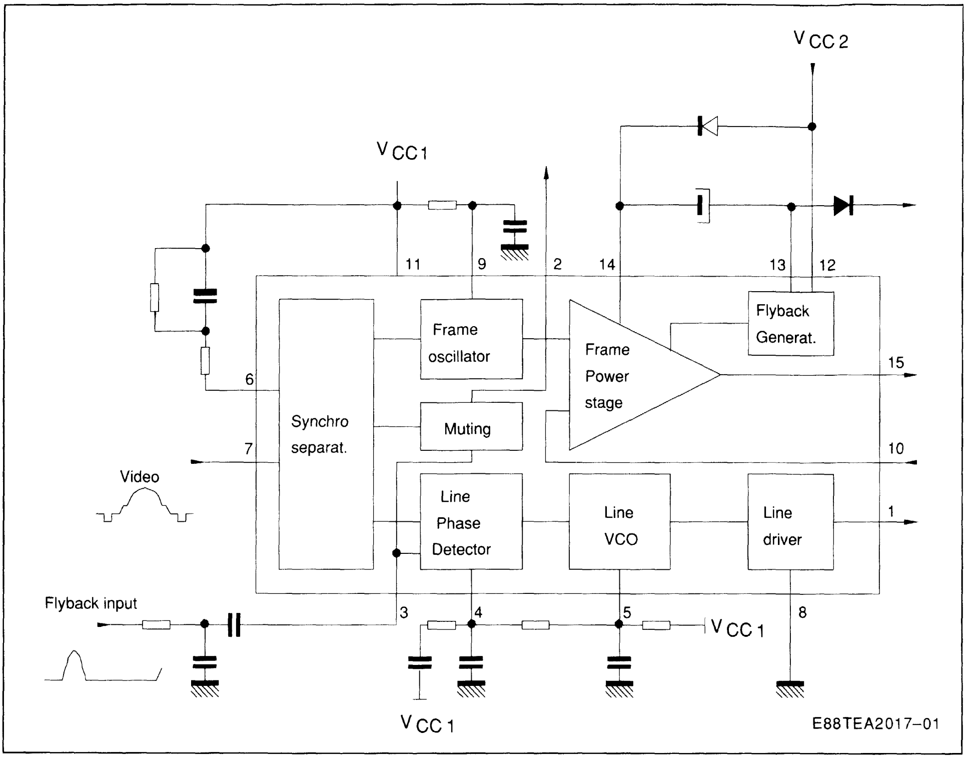
1 Line Output
2 Muting Output
3 Line Flyback Input
4 Phase Detector
5 Line Oscillator
6 Synchro Separator
7 Video Input
8 Ground



9 Frame Oscillator
10 Power Amplifier Negative Input
11 V_{CC1}
12 Flyback Generator Supply
13 Flyback Generator
14 Frame Power Supply
15 Frame Output

E88TEA2017-02

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATNGS

Symbol	Parameter	Value	Unit
VCC1	Supply Voltage	20	V
V12	Flyback Generator Supply Voltage	30	V
V14	Frame Power Supply Voltage	60	V
I15	Frame Output Current	± 1.5	A
V1	Line Output Voltage (external)	60	V
Ip1	Line Output Peak Current	0.8	A
Ic1	Line Output Continuous Current	0.4	A
Tstg	Storage Temperature	– 40 to 150	°C
Tj	Max Operating Junction Temperature	150	°C

THERMAL DATA

Rth (j-c)	Max Junction-case Thermal Resistance	3	°C/W
Rth (j-a)	Typical Junction-ambient Thermal Resis.	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS

(Tamb = 25°C ; VCC1 = 10V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply Pin 11				
ICC1 VCC1	Supply Current Supply Voltage	 8	15 	 20	mA V
	Video Input Pin 7				
V7	Input Threshold Voltage (I7 = – 1µA) Video Input Signal (see figure application n°1)	 0.4	4 	 4	V Vpp
	Line Flyback Input Pin 3				
V3 Z3	Bias Voltage Input Impedance	 4.5	2.7 6	 8	V KΩ
	Phase Comparator Pin 4				
I4 I4R LI4 	Output Current During Synchro Pulse Current Ratio (positive/negative) Leakage Current Control Range Voltage Control Sensibility (see figure application n°1) Pull in Range (see figure application n°1)	 0.9 – 1 2.5 	± 600 1.0 750 ± 800	 1.1 + 1 7 	µA µA V Hz/µs Hz
	Line Oscillator Pin 5				
LT5 HT5 BI5 DR5 FLP1 FLP2 0T5 $\frac{\Delta T}{\Delta V}$	Low Threshold Voltage High Threshold Voltage Bias Current Discharge Impedance Free Running Line Period R = 12KΩ Tied to VCC1 C = 6.8nF Tied to Ground Free Running Line Period R = 12.3KΩ C = 2.2nF Oscillator Threshold for Line Output Pulse Triggering Supply Voltage Influence on Free-running Period	 61.5 	3.2 6.6 50 800 64 27 5 0.051	 66.5 	V V nA Ω µs µs V µs/V

ELECTRICAL CHARACTERISTICS
(Tamb = 25°C ; VCC1 = 10V ; V14 = 30V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Line Output — Pin 1				
LV1	Saturation Voltage to Ground (I1 = 200mA)		1.1	1.5	V
CPW	Output Pulse Width (line period = 64µs)	20	22	24	µs
	Muting — Pin 2				
	(see figure application n°1) Output Voltage : Without Video Signal		8		V
	With Video Signal		0.7	1.2	V
	Frame Oscillator — Pin 9				
LT9	Low Threshold Voltage	1.8	2	2.3	V
HT9	High Threshold Voltage	2.6	3.1	3.6	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance		500		Ω
FFP1	Free Running Frame Period R = 845KΩ Tied to VCC1 C = 180nF Tied to Ground	21.4	22.5	25	ms
FFP2	Free Running Frame Period R = 425KΩ C = 220nF		14.3		ms
MFP	Minimum Frame Period (I7 = – 100µA) with the Same RC	14.6	17	19	ms
FG	Frame Sawtooth Gain between Pin 9 and non-inverting Input of the Frame Amplifier (internal)		– 0.4		
	Frame Power Supply — Pin 14				
V14	Operating Voltage (with flyback generator)	10		58	V
I14	Supply Current (V14 = 30V)		16	25	mA
	Flyback Generator Supply — Pin 12				
V12	Operating Voltage	10		30	V
	Frame Output				
	Saturation Voltage to Ground				
LV15A	I15 = 0.1A		60		mV
LV15B	I15 = 1A		0.4	0.8	V
	Saturation Voltage to VCC2				
HV15A	I15 = – 0.1A		1.3		V
HV15B	I15 = – 1A		1.7	2.4	V
	Saturation Voltage to VCC2 in Flyback Mode (V15 > V14)				
FV15A	I15 = 0.1A		1.7		V
FV15B	I15 = 1A		2.6	4	V
	Flyback Generator — Pin 12 And 13				
	* Flyback Transistor on (output = high state)				
F2DA	V3/2 With $I_{3 \to 2}$ = 0.1A		1.6		V
F2DB	$I_{3 \to 2}$ = 1A		3	4	V
FSVA	V2/3 With $I_{2 \to 3}$ = 0.1A		0.9		V
FSVB	$I_{2 \to 3}$ = 1A		2	4	V
	* Flyback Transistor off (output = V14 – 8V) V12 = V14 = 30V				
FCI	Leakage Current Pin 12			100	µA

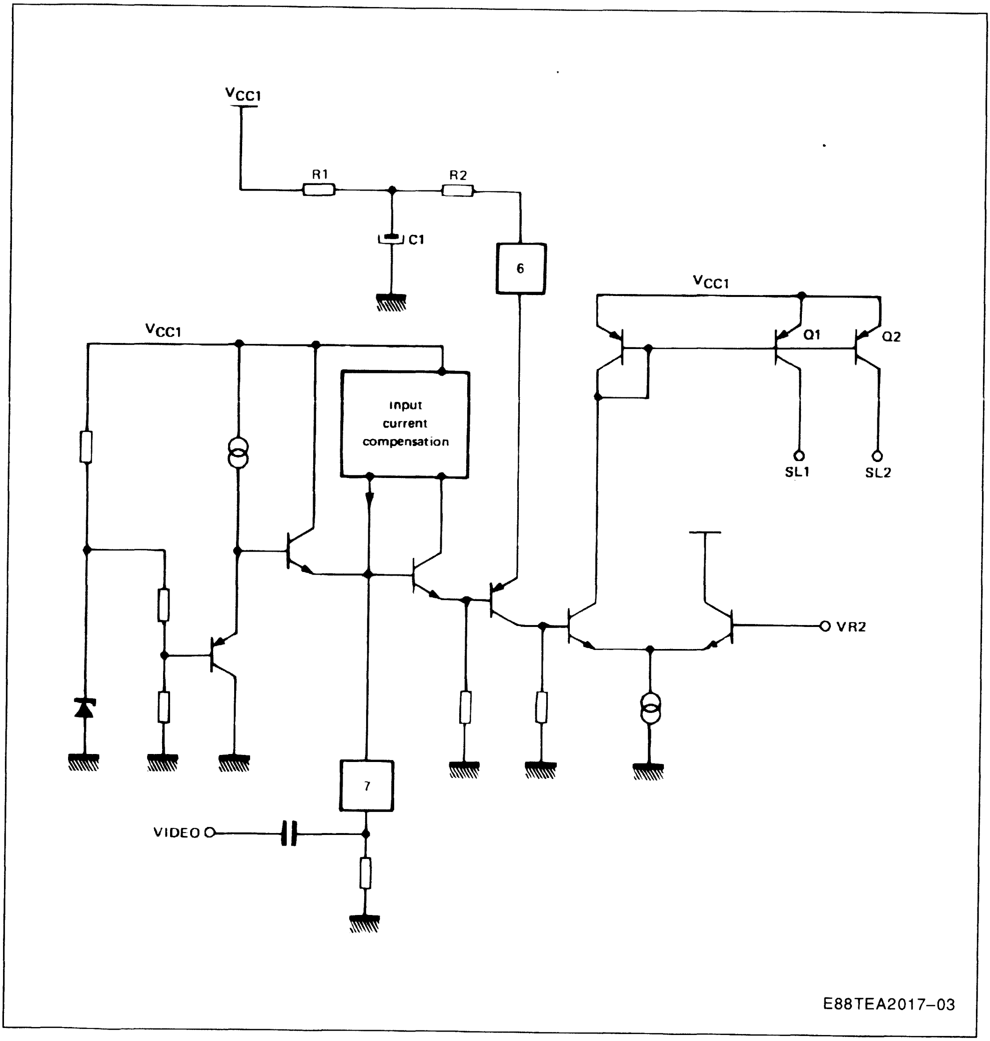
GENERAL DESCRIPTION

The TEA2017 performs all of the video and power functions required to provide signals for the direct drive of a line darlington and the frame yoke.

It contains :

- A synchronizing separator with the slice level of synchro separation determined by the external components.
- An integrated frame synchronizing separator without external components.
- A saw tooth generator for the frame with synchronization allowed during the last fourth of the free run period.
- A power amplifier for direct drive of the frame yoke with overload, short circuit and thermal protections.
- A line phase detector and a voltage control oscillator.
- An open collector output for the direct drive of a line darlington.
- A muting output.

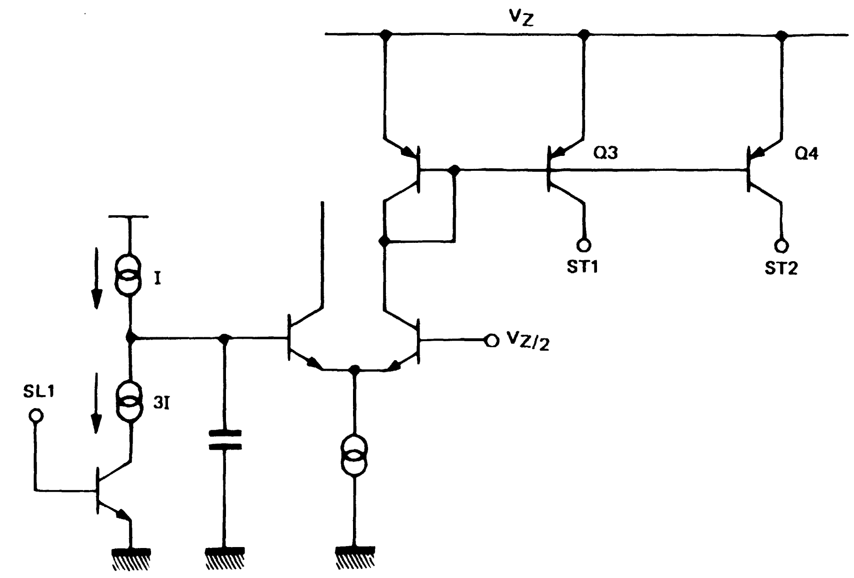
SYNCHRONIZATION SEPARATOR CIRCUIT



The sync-tip DC level on pin 7 is clamped to 3.8V. The slice level of sync-separation present on capacitor C1 depends on the value of resistor R1 and R2.

When the video signal on pin 7 decreases under the capacitor voltage the transistors Q1 and Q2 provide current for the other parts of the circuit.

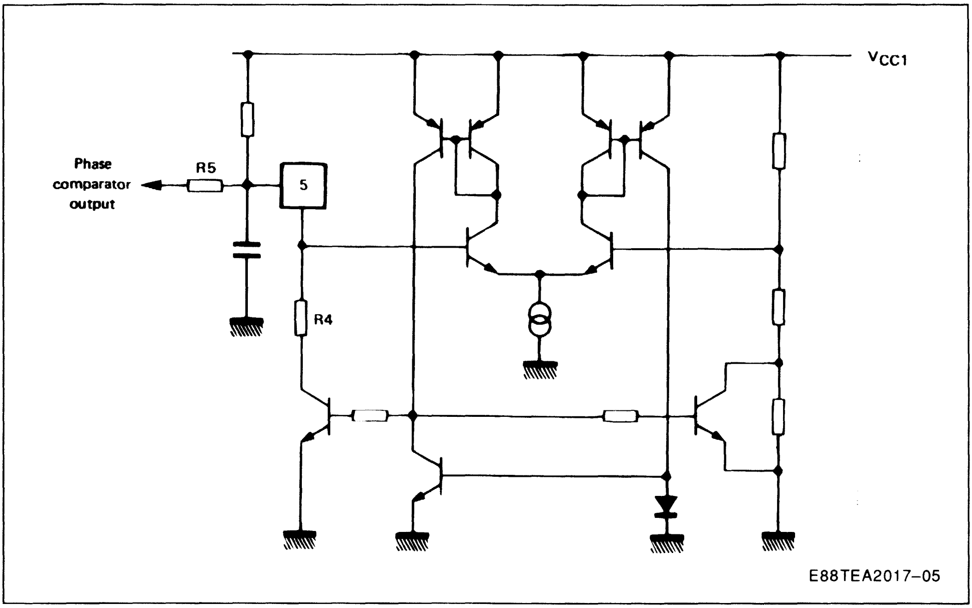
FRAME SEPARATOR



E88TEA2017-04

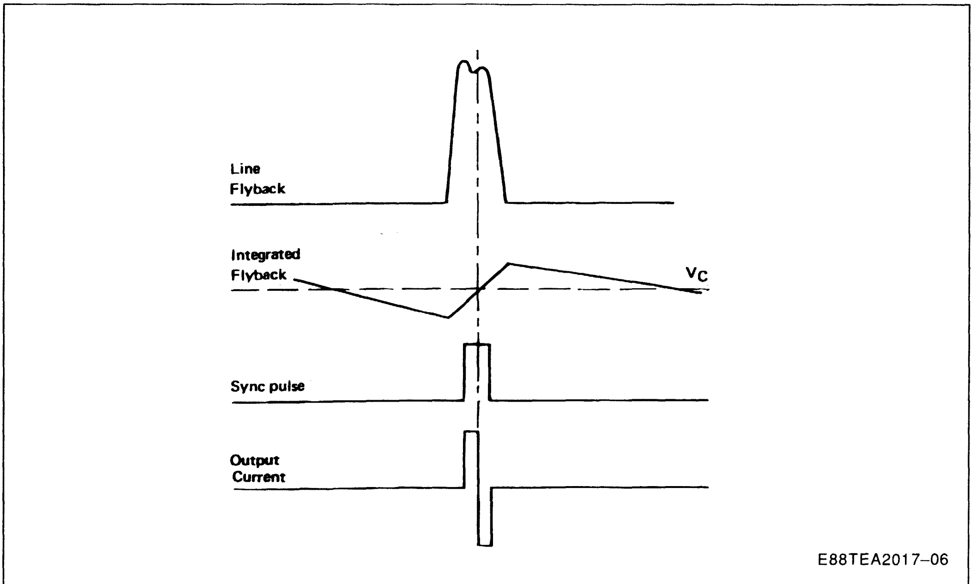
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

LINE OSCILLATOR

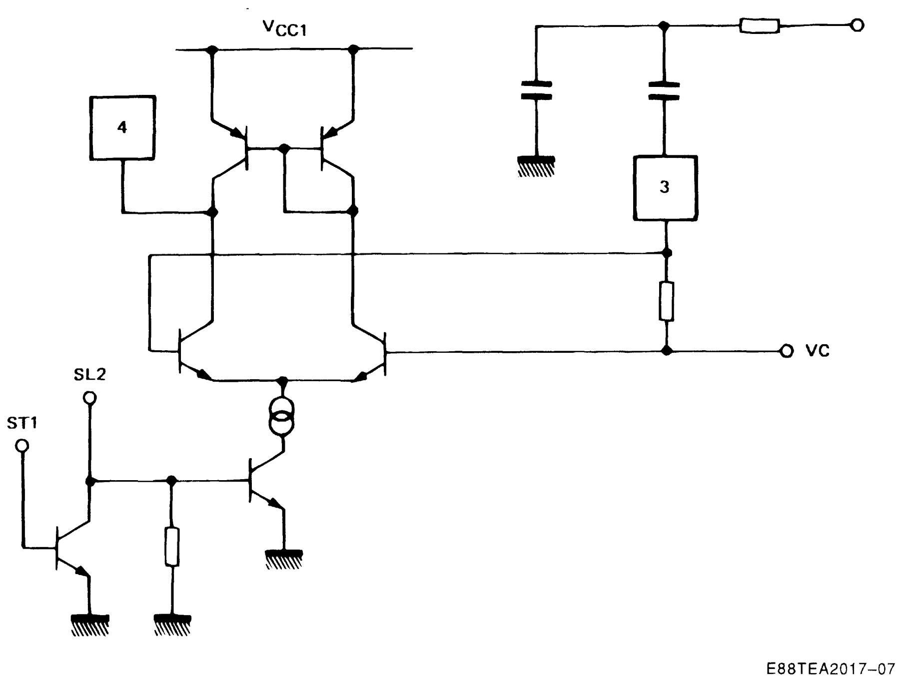


The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The voltage control is applied on resistor R5.

PHASE COMPARATOR



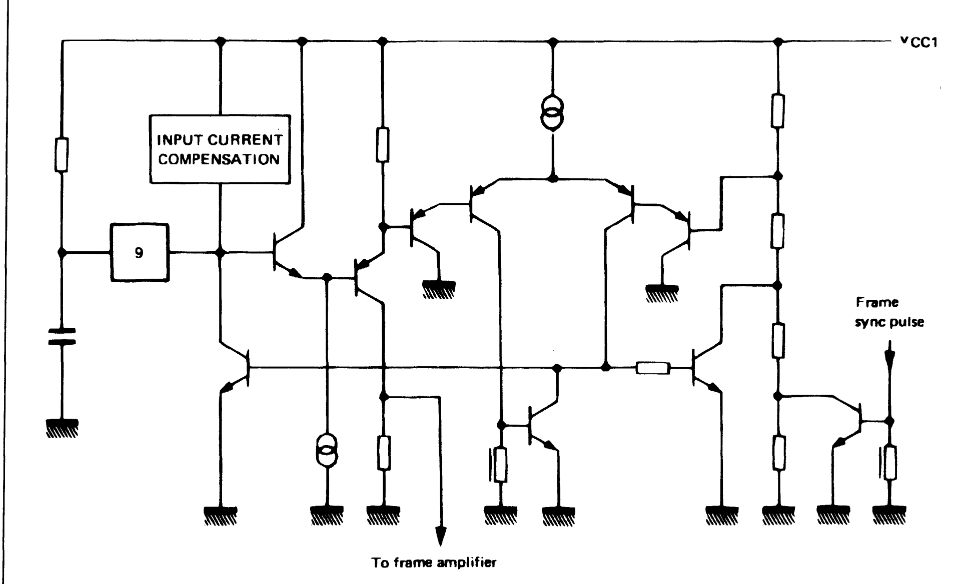
The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 3 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 3 superior to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternately negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.



LINE OUTPUT (PIN 1)

It is an open collector output which is able to drive pulse current of 500mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

FRAME OSCILLATOR



The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last fourth of the free run period. The input current during the charge of the capacitor is less than 100nA.

FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

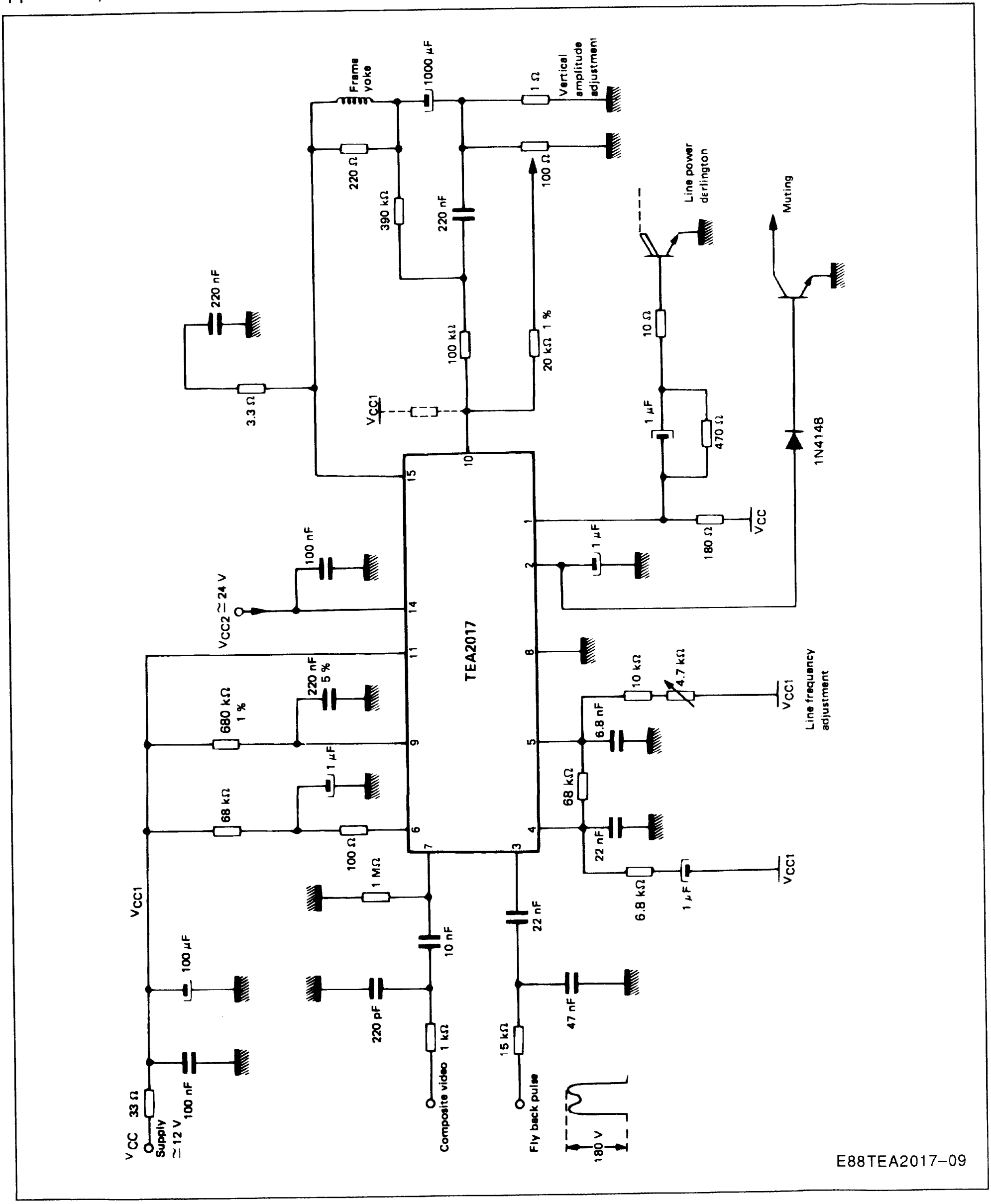
Its positive input is directly connected to the invert of the frame saw tooth.

MUTING OUTPUT

It delivers voltage pulse during the line fly-back if there is no video signal on the input. The output impedance is 1kΩ.

APPLICATION N°1 (without internal flyback generator)

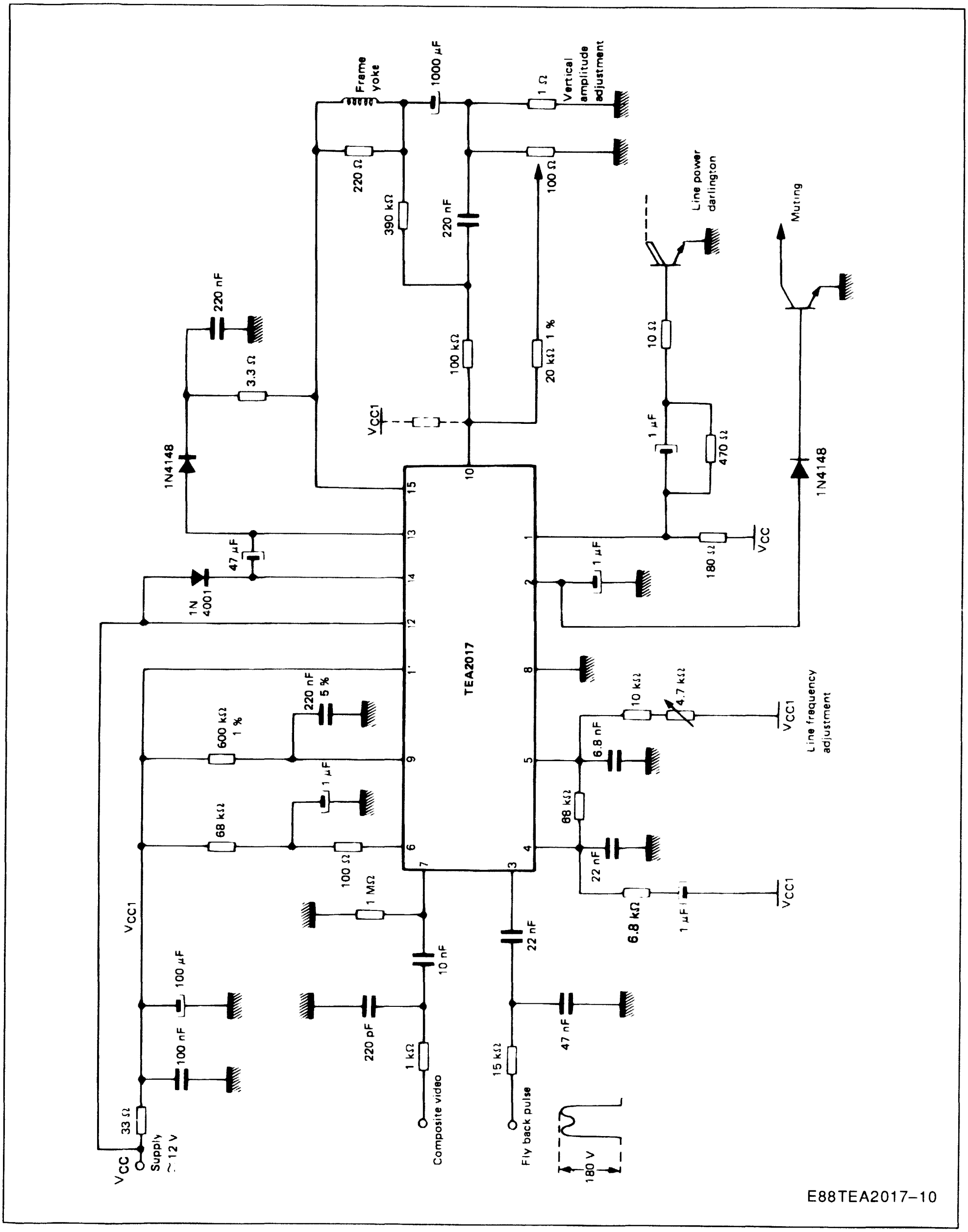
TYPICAL BLACK–WHITE TV APPLICATION FOR 14" – 110° SCREEN (with yoke L = 27 mH, R = 15Ω, Ipp = 0.5A)



V_{CC2} : Power stage supply from high voltage transformer.
V_{CC1} must be perfectly filtered.

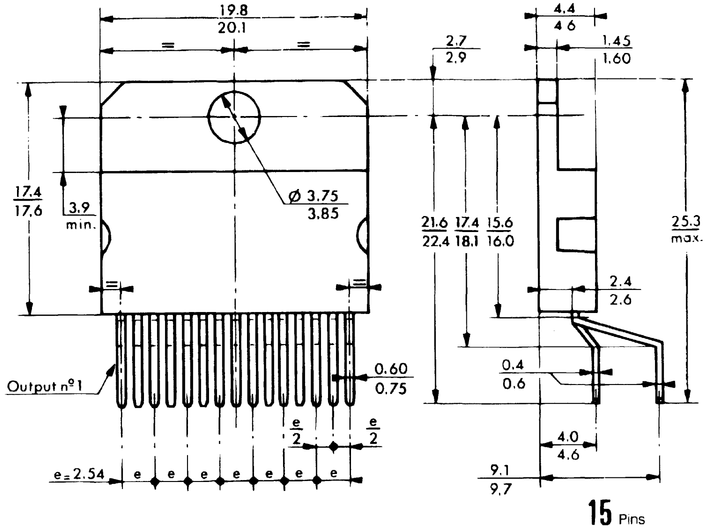
APPLICATION N°2 (with internal flyback generator)

TYPICAL BLACK–WHITE TV APPLICATION FOR 14" – 110° SCREEN (with yoke L = 27 mH, R = 15Ω, Ipp = 0.5A)



PACKAGE MECHANICAL DATA

15 PINS – PLASTIC SIP



CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP to 0.5 A
- CURRENT LIMITATION
- DEMAGNETIZATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (< 1.6 mA)
- THERMAL PROTECTION

DESCRIPTION

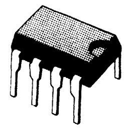
The TEA2018A is an 8-pin mini-dip low cost integrated circuit designed for the control of switch mode power supplies.

Due to its current mode regulation, the TEA2018A facilitates design of power supplies with following features :

- High stability regulation loop
- Automatic input voltage feed-forward in discontinuous mode fly-back
- Automatic pulse-by-pulse current limitation

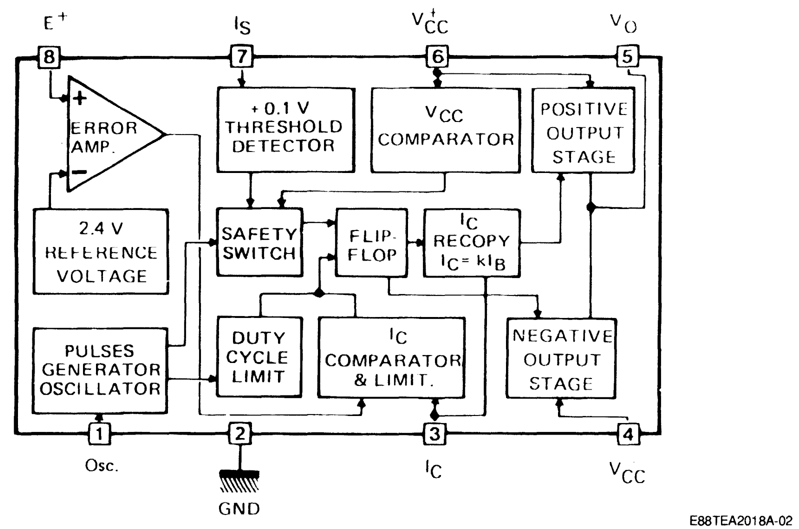
Typical applications : Video Display Units, TV sets, typewriters, microcomputers and industrial applications

Where synchronization is required, use the TEA2019.

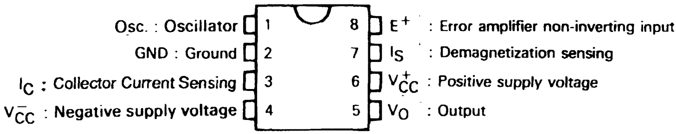


TEA2018A
DIP8
(Plastic Package)

BLOCK DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Positive Supply Voltage	15	V
V_{CC}^{-}	Negative Supply Voltage	– 5	V
I_O(peak)	Peak Output Current (duty cycle < 5 %)	± 1	A
I_I	Input Current (pin 3)	± 5	mA
T_j	Junction Temperature	+ 150	°C
T_{oper}	Operating Ambient Temperature Range	– 20 to 70	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25 °C, potentials referenced to ground (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}^+	Positive Supply Voltage	6.6	8	15	V
V_{CC}^-	Negative Supply Voltage	– 1	– 3	– 5	V
$V_{CC(start)}$	Minimum positive supply voltage required for starting (V_{CC}^+ rising)		6	6.6	V
$V_{CC(stop)}$	Minimum positive voltage below wich device stops operating (V_{CC}^+ falling)	4.2	4.9	5.6	V
ΔV_{CC}^+	Hysteresis on V_{CC}^+ Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Standby Supply Current before starting [$V_{CC}^+ < V_{CC(start)}$]		1	1.6	mA
$V_{th(IC)}$	Current Limitation Threshold Voltage (pin 3)	– 1100	– 1000	– 880	mV
$R_{(Ic)}$	Collector Current Sensing Input Resistance		1000		Ω
I_S	Demagnetization Sensing Threshold	75	100	125	mV
	Demagnetization Sensing Input Current (pin 7 grounded)		1		µA
τ_{max}	Maximum Duty Cycle	60	70		%
A_V	Error Amplifier Gain		50		
I_I^+	Error Amplifier Input Current (non–inverting input)		2		µA
$V_{(ref)}$	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{(ref)}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
$\frac{\Delta f_{osc}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V_{CC}^+ = + 8 V)		0.05		%/°C
$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V_{CC}^+ (+ 8 V < V_{CC}^+ < + 14 V)		0.5		%/V
t_{on}(min)	Minimum Conducting Time (C_t = 1 nF)		2		µs

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}^+	Positive Supply Voltage		8		V
V_{CC}^-	Negative Supply Voltage		– 3		V
I_O	Output Current			0.5	A

GENERAL DESCRIPTION

OPERATING PRINCIPLES (figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator sawtooth which acts as clock signal. The period T_{osc} is given by :

$$T_{osc} = 0.66\ C_t\ (R_t + 2000)$$

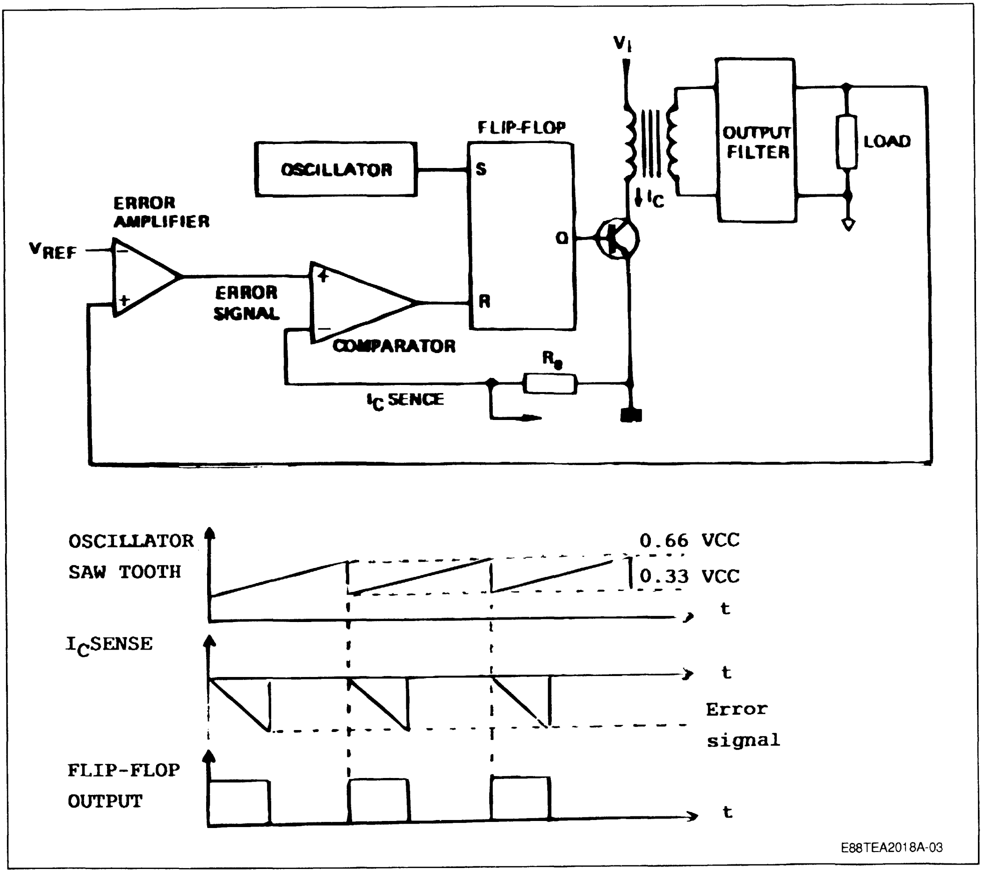
(T_{osc} in seconds, C_t in Farad, R_t in Ohm)

The end of the conduction time is determined by a signal issued from comparing the following signals :

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor,

b) the output of the error amplifier.

Figure 1 : Current Mode Control.



BASE DRIVE

- Fast turn-on
On each period, a current pulse ensures fast transistor switch-on.
This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.
- Proportional base drive
In order to save power, the positive base current after the starting pulse becomes an image of the collector current.

The ratio $\frac{I_C}{I_B}$ is programmed as follows (figure 2) :

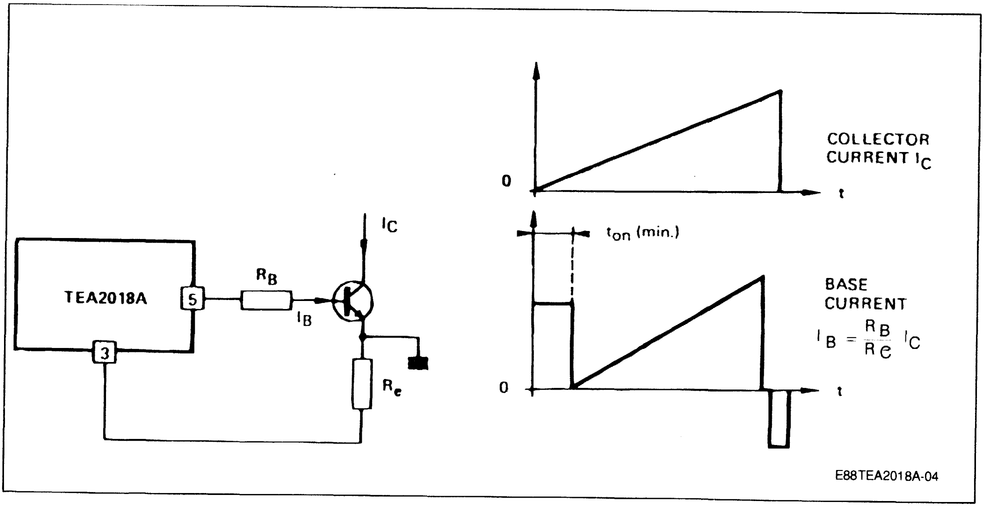
$$\frac{I_C}{I_B} = \frac{R_B}{R_e}$$

- Efficient and fast switch-off
When the positive base drive is removed, 500 ns (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

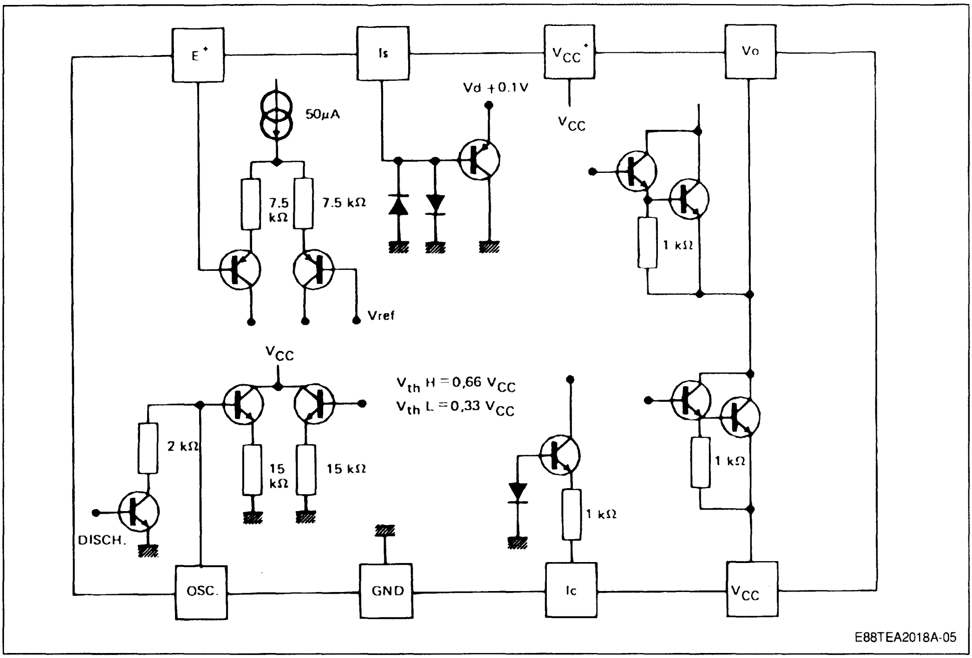
SAFETY FUNCTIONS

- Overload & short-circuit protection
When the voltage applied to pin 3 exceeds the current limitation threshold voltage [$V_{th}(I_c)$], the output flip-flop is reset and the transistor is turned off.
The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 3 at the maximum allowable collector current.
- Demagnetization sensing
This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.
When not used, pin 7 must be grounded.
- $t_{on(max)}$
Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70 % of the period.
- $t_{on(min)}$
A minimum conducting time is ensured during each period (see figure 2)
- Supply voltage monitoring
The TEA2018A will stop operating if V_{CC}^{+} on pin 6 falls below the threshold level V_{CC}^{+} (stop).

Figure 2.



SCHEMATICS OF INPUTS AND OUTPUTS



STARTING PROCESS (figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.

This current charges the power supply voltage capacitor of the device.

No output pulses are available before the voltage on pin 6 has reached the threshold level [$V^{+}_{CC(start)}$, V^{+}_{CC} rising].

During this time the TEA2018A draws only 1 mA (typically). When the voltage on pin 6 reaches this threshold, base drive pulses appear.

The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1 V (typically) (ΔV^{+}_{CC}) is implemented to avoid the device from stopping.

Figure 3 : Normal TEA2018A Start-up Sequence.

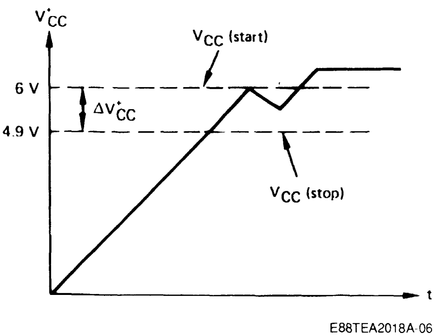
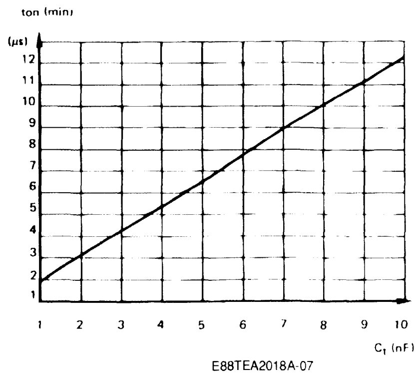
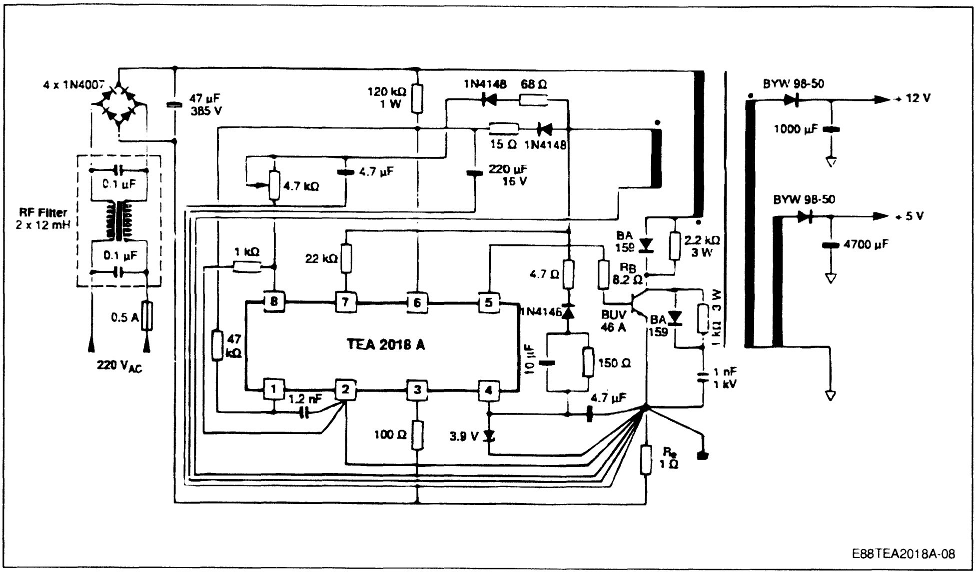


Figure 4 : t_{on}(min) Versus C_t.



TYPICAL APPLICATION



MONITOR APPLICATION

- Maximum power ≈ 30 W
- Operating frequency ≈ 30 KHz
- $I_{nominal}$: 0.75 A
- I_{limit} : 1 A

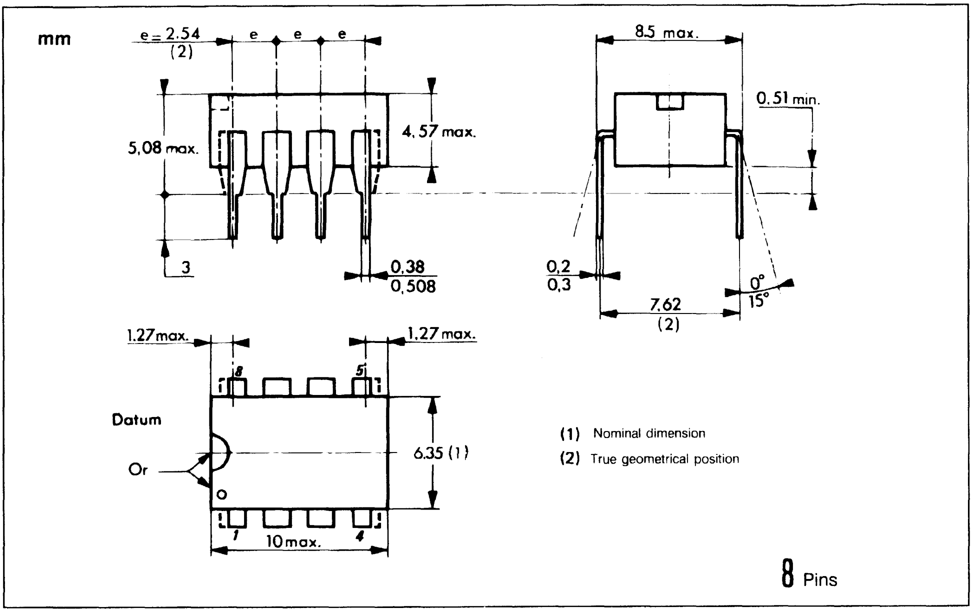
$$R_e = \frac{1\ V}{1\ A} = 1\ \Omega$$

$$R_B = 8.2\ \Omega \Rightarrow \frac{I_C}{I_B} = 8.2$$

Note : Primary Ground.
Secondary Ground.

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP



SGS-THOMSON
MICROELECTRONICS

TEA2019

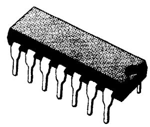
CURRENT MODE SWITCHING POWER SUPPLY CONTROL CIRCUIT

- DIRECT DRIVE OF THE EXTERNAL SWITCHING TRANSISTOR
- POSITIVE AND NEGATIVE OUTPUT CURRENTS UP TO 0.5A
- CURRENT LIMITATION
- DEMAGNETIZATION AND POWER TRANSISTOR SATURATION SENSING
- FULL OVERLOAD AND SHORT-CIRCUIT PROTECTION
- PROPORTIONAL BASE CURRENT DRIVING
- LOW STANDBY CURRENT BEFORE STARTING (< 1.6mA)
- SYNCHRONIZATION CAPABILITY WITH INTERNAL PLL
- THERMAL PROTECTION

Due to its current mode regulation, the TEA2019 facilitates design of power supplies with following features :

- High stability regulation loop.
- Automatic input voltage feed-forward in discontinuous mode fly-back.
- Automatic pulse-by-pulse current limitation.

Typical applications : Video Display Units, TV sets, typewriters, micro-computers and industrial applications.



TEA2019
DIP 14
(Plastic package)

DESCRIPTION

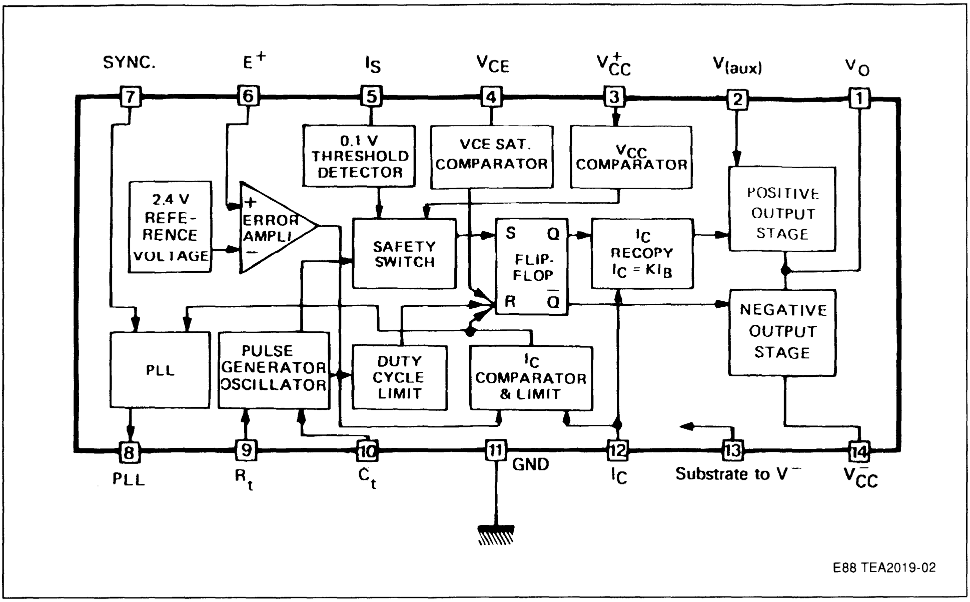
The TEA2019 is an 14-pin mini-dip low cost integrated circuit designed for the control of switch mode power supplies. It has the same basic functions as the TEA2018A but with synchronization capability by internal PLL. It is particularly suitable for applications where oscillator synchronization is required.

PIN CONNECTIONS

V_O	Output	1	14	V_{CC}^{-}	Negative supply (output stage)
$V_{(aux)}$	Auxiliary output supply	2	13	Subst.	Substrate
V_{CC}^{+}	Positive supply voltage	3	12	I_C	I_C sample (negative)
V_{CE}	Saturation sensing	4	11	GND	Ground
I_S	Demagnetization sensing	5	10	C_t	Oscillator capacitor
E^{+}	Error amplifier non-inverting input	6	9	R_t	Oscillator reference current
Sync	Synchronization input	7	8	PLL	PLL input

E88 TEA2019-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}^{+}	Positive Supply Voltage	15	V
$V_{(aux)}$	Auxiliary Output Supply Voltage	15	V
V_{CC}^{-}	Negative Supply Voltage	– 5	V
I_O (peak)	Peak Output Current (duty cycle < 5%)	± 1	A
I_I	Input Current Pins 4-5	± 5	mA
T_j	Junction Temperature	150	°C
T_{oper}	Operating Ambient Temperature Range	– 20 to 70	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = + 25°C, potentials referenced to ground (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}^{+}	Positive Supply Voltage	6.6	8	15	V
V_{CC}^{-}	Negative Supply Voltage	– 1	– 3	– 5	V
$V_{CC(start)}$	Minimum positive supply voltage required for starting (V_{CC}^{+} rising)		6	6.6	V
$V_{CC(stop)}$	Minimum positive voltage below which device stops operating (V_{CC}^{+} falling)	4.2	4.9	5.6	V
ΔV_{CC}^{+}	Hysteresis on V_{CC}^{+} Threshold	0.7	1.1	1.6	V
$I_{CC(sb)}$	Standby Supply Current Before Starting [$V_{CC}^{+} < V_{CC(start)}$]		1	1.6	mA
$V_{th}(I_C)$	Current Limitation Threshold Voltage (pin 12)	– 1100	– 1000	– 880	mV
$R_{(Ic)}$	Collector Current Sensing Input Resistance		1000		Ω
I_S	Demagnetization Sensing Threshold	75	100	125	mV
	Demagnetization Sensing Input Current (pin 5 grounded)		1		µA
τ_{max}	Maximum Duty Cycle	70	80		%
A_V	Error Amplifier Gain		50		
I_I^{+}	Error Amplifier Input Current (non-inverting input) (pin 6)		2		µA
$V_{(ref)}$	Internal Reference Voltage	2.3	2.4	2.5	V
$\frac{\Delta V_{(ref)}}{\Delta T}$	Reference Voltage Temperature Drift		10^{-4}		V/°C
$\frac{\Delta f_{osc}}{\Delta T}$	Oscillator Frequency Drift with Temperature (V_{CC}^{+} = + 8V)		0.05		%/°C
$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	Oscillator Frequency Drift with V_{CC}^{+} (+ 8V < V_{CC}^{+} < + 14V)		0.5		%/V
t_{on}(min)	Minimum Conducting Time (C_t = 1nF)		2		µs

SYNCHRONIZATION INPUT (pin 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{7pp}	Peak to Peak Sawtooth Voltage		0.5	2.5	V
$R_{(7)}$	Input Impedance		20		kΩ

PLL CHARACTERISTICS

C_t = 1.5nF, R_t = 68kΩ, $R_{(8-9)}$ = 50kΩ, + I_B/– I_B = 1.25, V_{7pp} = 0.5V, $t_{storage}$ of the switching transistor = 1.5µs (see typical application)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frequency Sensitivity		100		Hz/µA
ΔT	Capture Range (T_o = 64µs)		± 8		µs

SATURATION SENSING (pin 4)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{(4)}$	Input Threshold		3.2		V
$I_{(4)}$	Input Current (V_4 > 3.2V)	50			µA
	Input Internal Resistance		1		kΩ

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}^{+}	Positive Supply Voltage		8		V
V_{CC}^{-}	Negative Supply Voltage		3		V
I_O	Output Current			0.5	A

GENERAL DESCRIPTION

OPERATING PRINCIPLES (figure 1)

On every period, the beginning of the conduction time of the transistor is triggered by the fall of the oscillator saw-tooth which acts as clock signal. The period T_{osc} is given by :

$T_{osc} \approx 0.66\ C_t\ (R_t + 2000)$

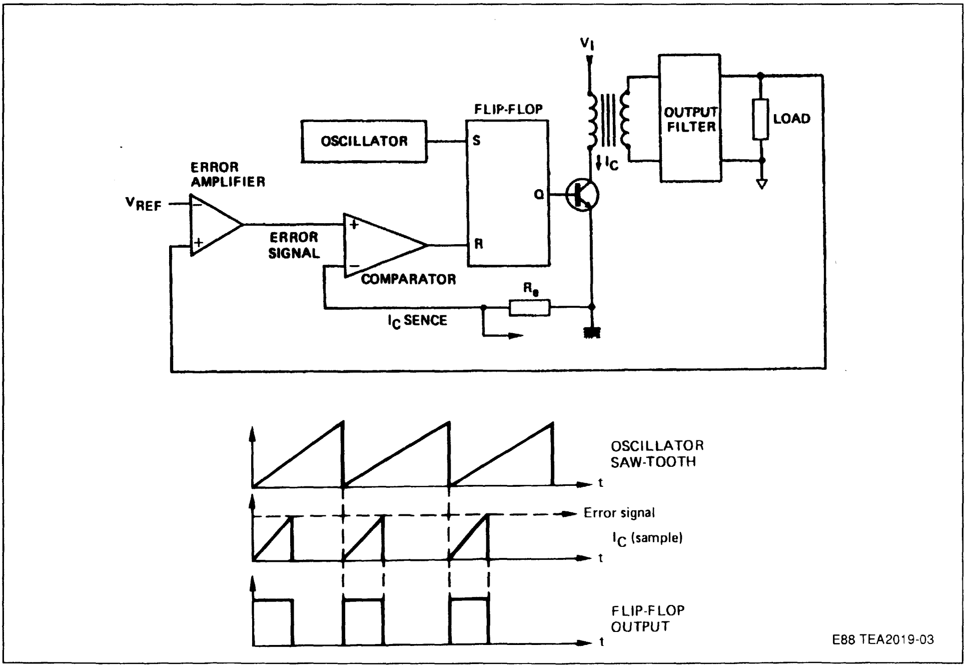
(T_{osc} in seconds, C_t in Farad, R_t in Ohm)

The end of the conduction time is determined by a signal issued from comparing the following signals.

a) the sawtooth waveform representing the collector current of the switching transistor, sampled across the emitter shunt resistor.

b) the output of the error amplifier.

Figure 1 : Current Mode Control.



SGS-THOMSON MICROELECTRONICS

BASE DRIVE

- **Fast turn-on**

On each period, a current pulse ensures fast transistor switch-on.
This pulse performs also the $t_{on(min)}$ function at the beginning of the conduction.

- **Proportional base drive**

In order to save power, the positive base current after the starting pulse becomes an image of the collector current.

The ratio $\frac{I_C}{I_B}$ is programmed as follows (figure 2).

$$\frac{I_C}{I_B} = \frac{R_B}{R_E}$$

- **Efficient and fast switch-off**

When the positive base drive is removed, 500ns (typically) will elapse before the application of negative current therefore allowing a safe and rapid collector current fall.

SAFETY FUNCTIONS

- **Overload & short-circuit protection**

When the voltage applied to pin 12 exceeds the current limitation thershold voltage [$V_{th(Ic)}$], the output flip-flop is reset and the transistor is turned off.

The shunt resistor R_e must be calculated so as to obtain the current limitation threshold on pin 12 at the maximum allowable collector current.

- **Demagnetization sensing**

This function disables any new conduction cycle of the transistor as long as the core is not completely demagnetized.

When not used, pin 5 must be grounded.

- **$t_{on(max)}$**

Outside the regulation area and in the absence of current limitation, the maximum conduction time is set at about 70% of the period.

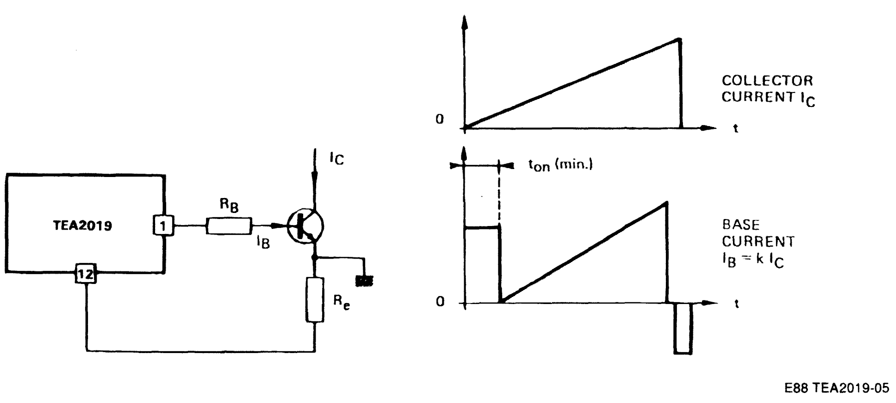
- **$t_{on(min)}$**

A minimum conducting time is ensured during each period (see figure 2).

- **Supply voltage monitoring**

The TEA2019 will stop operating if V^+_{CC} on pin 3 falls below the threshold level $V_{CC(stop)}$.

Figure 2.



STARTING PROCESS (figure 3)

Prior to starting, a low current is drawn from the high voltage source through a high value resistor.

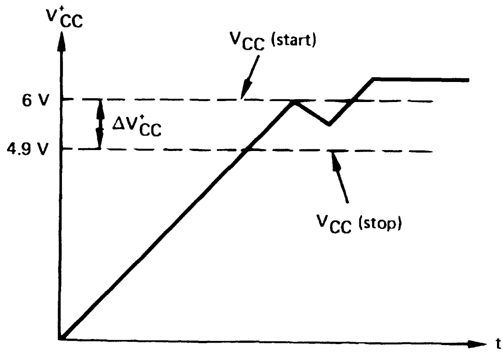
This current charges the power supply storage capacitor of the device.

No output pulses are available before the voltage on pin 3 has reached the threshold level [$V_{CC(start)}$, V^{+}_{CC} rising].

During this time the TEA2019 draws only 1mA (typically). When the voltage on pin 3 reaches this threshold base drive pulses appear.

The energy drawn by these pulses tends to discharge the power supply storage capacitor. However a hysteresis of about 1.1V (typically) (ΔV_{CC}) is implemented to avoid the device from stopping.

Figure 2 : Normal TEA2019 Start up Sequence.



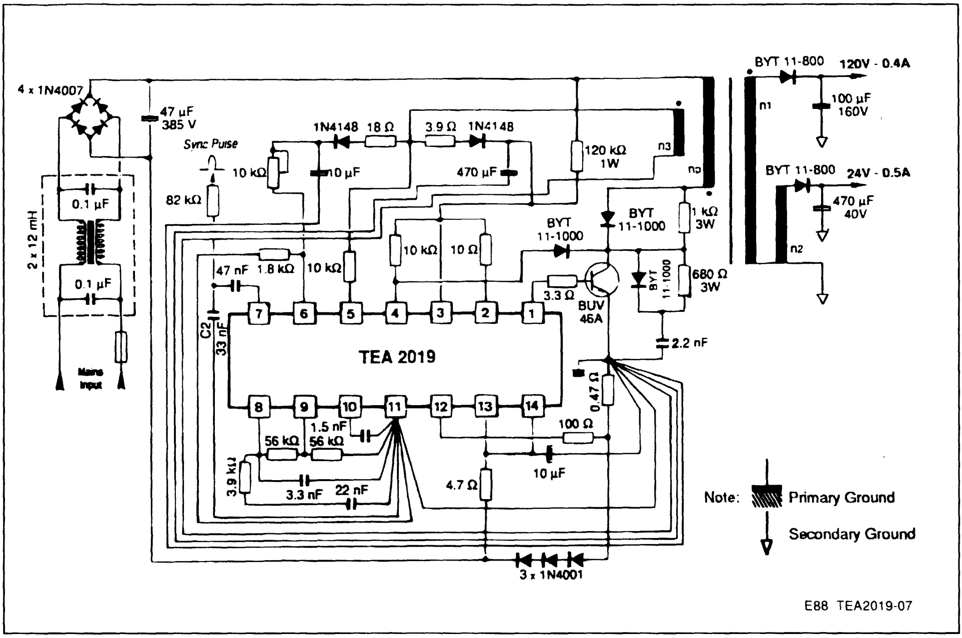
The TEA2019 has some additional capabilities compared to the TEA2018A :

- The oscillator charge current is supplied through an internal current generator, programmed externally - instead of using an external charging resistor. The sawtooth so obtained is linear.
- The oscillator can be synchronized through an internal PLL circuit. This feature provides synchronization between the external sync pulse and the end of the switching transistor current. The sync pulse can be for example the fly-back pulse of a TV horizontal sweep circuit. As indicated in the application diagram, this pulse is applied first to a R.C. network to obtain a low voltage sawtooth and then to pin 7 of the circuit. The PLL output (pin 8) supplies a correction current to pin 9 through an external resistor, so as to maintain the oscillator at the correct frequency.
- In the TEA2019, the power supply of the positive output stage is separated from the main power supply, so that it can be supplied from a lower voltage in order to reduce the I.C. power dissipation.

  For low power applications, the circuit can be normally supplied by connecting pins 2 and 3 together.
- In order to protect the substrate (pin 13) from the parasitic voltage peaks produced by negative output current peaks at pin 14, the substrate (pin 13) is internally separated from the negative supply (pin 14). They must be externally connected together.
- The switching transistor saturation voltage can be monitored at pin 4. To achieve this, a high voltage diode must be connected between the collector of the switching transistor and pin 4. Also a resistor must be connected from pin 4 to V^{+}_{CC} (see application diagram). This arrangement is useful when the chosen value of base current is very low and as a consequence the saturation voltage will be high. In this event, when $V_{CE(sat)}$ increases above 2.5V, the base current is interrupted before the normal end of the period.

  Remark : the TEA2019 can also operate without this protection.

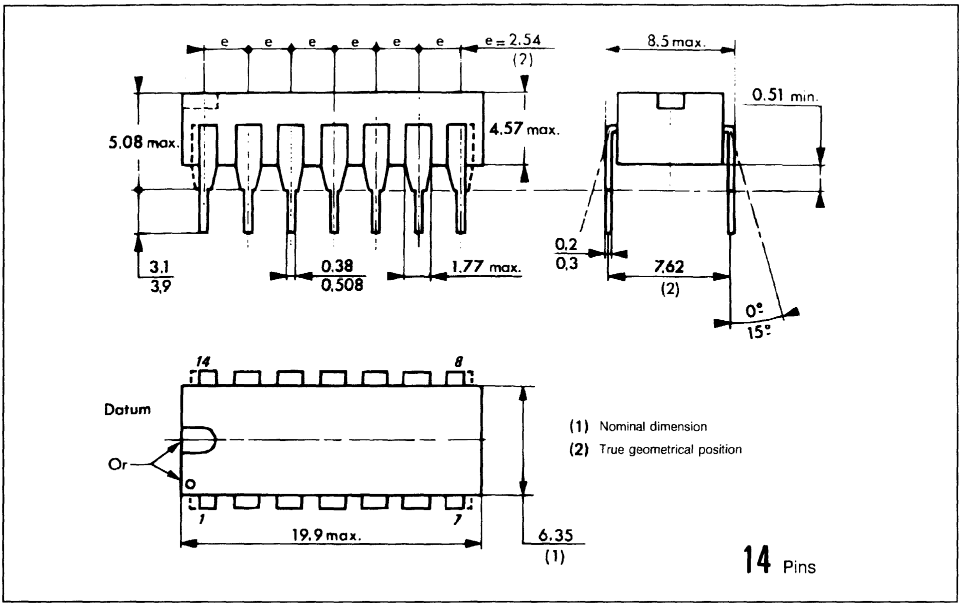
TYPICAL APPLICATION



- P_{MAX} = 60W
- Free-running Frequency : 15kHz
- $155V_{RMS} \leq V_{AC} \leq 250V_{RMS}$
- Outputs :
  - 120V ± 3%, 0.4A
  - 24V ± 3%, 0.5A
- V_{CE} Monitoring

PACKAGE MECHANICAL DATA

14 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TEA2026C

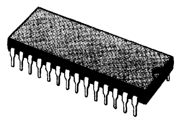
COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION :

- CERAMIC 500 KHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60 Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR
- FRAME PHASE MODULATOR FOR THYRISTOR

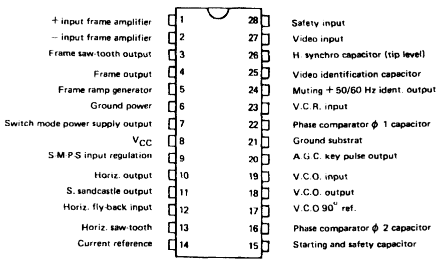
SMPS CONTROL :

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- LINE FREQUENCY OPERATION
- SECURITY CIRCUIT AND START-UP PROCESSOR
- SWITCHING POWER TRANSISTOR IS TURNED OFF BY LINE FLY BACK SIGNAL



TEA2026C
DIP28
(Plastic Package)

PIN CONNECTIONS

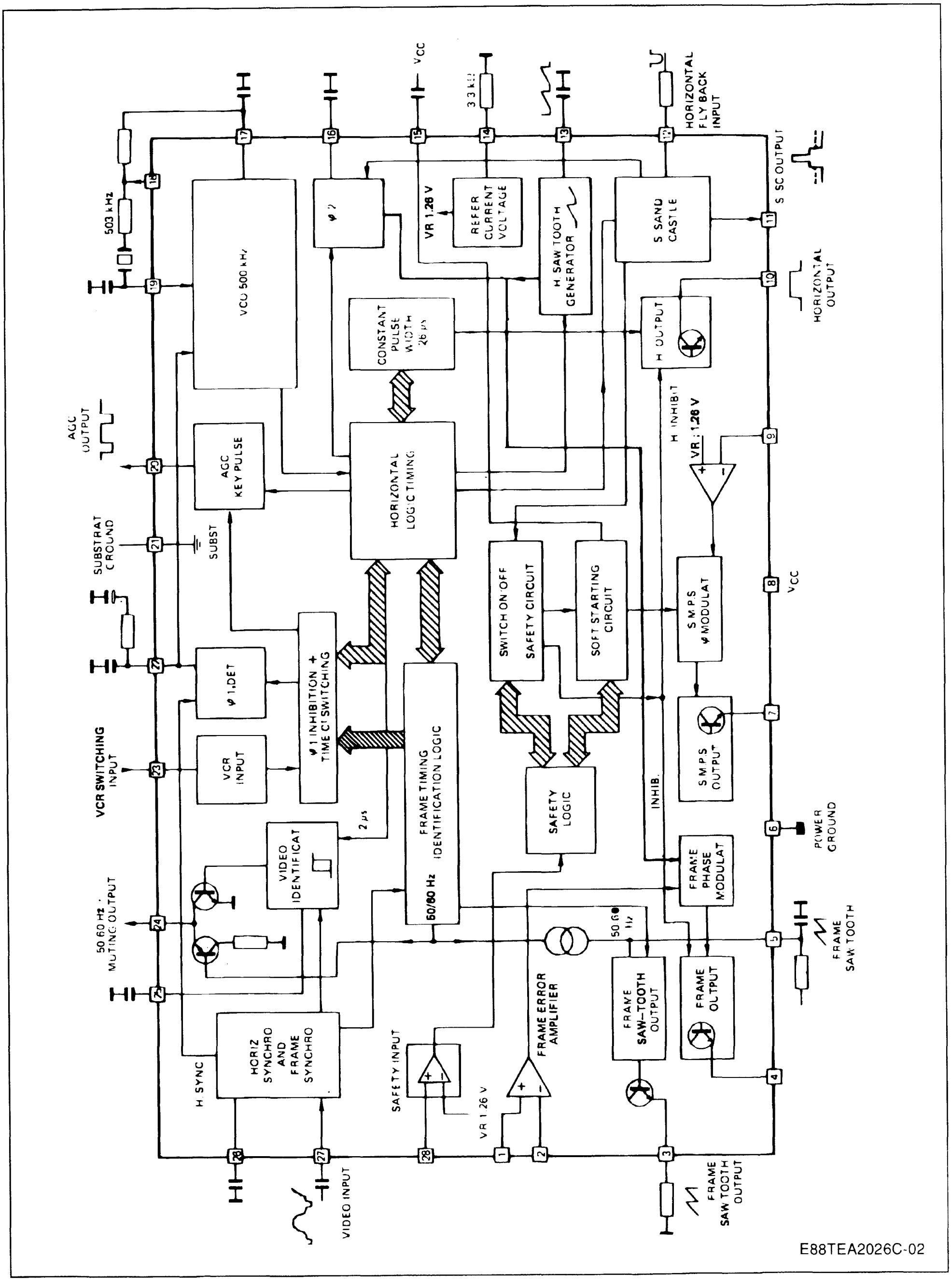


E88TEA2026C-01

DESCRIPTION

The TEA2026C is a complete (horizontal and vertical) deflection processor with secondary step up SMPS control for color TV sets.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(limiting values) - T_{amb} = 25 °C (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Unit
	Supply Voltage (pin 8)		14	V
V_{CC}	Operating Supply Voltage (pin 8)	Starting Threshold	13.2	V
I_{20}	AGC Current (pin 20)		5	mA
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Negative line retrace voltage (pin 12)	– 20		V
I_{12}	Line retrace current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	– 10	40	mA
I_3	Frame Saw–tooth Generator (pin 3)		20	mA
I_4	Frame Output Current (pin 4)		100	mA
I_7	SMPS Output Currrent (pin 7)	– 40	40	mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	
V_1/V_2	Common Mode Range (pins 1–2)		10	V

THERMAL DATA

$R_{th(j-a)}$	Junction Ambient Thermal Resistance	55	°C/W

GENERAL DESCRIPTION

INTRODUCTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500 kHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor : Two applications are possible :
  - D Class Power stage using an external thyristor.
  - B Class Power stage using an external power amplifier with fly-back generator such as the TDA2172.
- Line and frame synchronization separation.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- Automatic 50-60 Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- AGC key pulse output.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500 KHz VCO

The circuit is supplied in a 28 pin DIP case.

V_{CC} = 12 V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Frame synchronization is fully integrated (no external capacitor required).

The frame timing identification logic permits automatic adaptation to 50 - 60 Hz standards or non-interlaced video.

An automatic synchronization window width system provides :

- fast frame capture (6.7 ms wide window),
- good noise immunity (0.4 ms narrow window).

The internal generator starts the discharge of the saw-tooth generator so that it is not disturbed by line fly-back effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32 µs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independant of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500 KHz VCO.

The circuit uses **two phase-locked** loops (PLL) : the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26 µs, independent of V_{CC} and any delay in switching off the scanning transistor.

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2 µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0 V : no video identification
- 6 V : 60 Hz video identification
- 12 V : 50 Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers, and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SCANNING

Frame saw-tooth generator :

The current to charge the capacitor is automatically switched to 60 Hz operation to maintain constant amplitude.

Frame phase modulator (with two differentiel inputs) :

The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.

This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance and can therefore be used in class B operation with a power amplifier circuit.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26 V and a phase modulator operating at the line frequency. The power transistor is turned off by the line fly-back.

The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage exceeding 1.26 V the three outputs are simultaneously cut off until this voltage drops below the 1.26 V threshold again. In this case the switch mode power supply is restarted by the "soft start" system.

If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits V_{CC} must be lower than 3.5 V.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up, the horizontal and vertical scanning functions come into operation at V_{CC} = 6 V. The power supply then comes into operation progressively, only when φ 2 is normally locked.

On shutting down, (with V_{CC} < 5.25 V) the three functions are inhibited simultaneously after the first line fly-back.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C - V_{CC} = 12 V (unless otherwise noted)-Pulse Duration at 50 % of the Ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8 ; frame, line and SMPS output without load)		50	80	mA
	Synch. Separator (pins 26-27)				
	Positive video input AC coupled (ouput impedance of signal source < 200 Ω)	0.2	1.8	3	Vpp
$-I_{27}$	Negative Clamping Current (during synch. pulse)	– 25	– 40	– 55	µA
I_{27}	Clamping Current	3	6	9	µA
	Pin for Slicing Level 0.2 V < V_{27pp} < 2 V, (50 % of sync. amplitude)				
$-I_{26}$	Positive Current	0	– 750	– 1000	µA
I_{26}	Negative Current	17	25	36	µA
	Pulse for keyed AGC (pin 20)				
	Negative (function : without video signal : low level, with video signal : key pulses)				
I_{20}	Output Current			5	mA
V_{20}	Output Saturation Voltage (I_{20} = 5 mA)		0.25	0.4	V
t_k	Pulse Width (synchro pulse is always inside the key pulse)	6.5	8	8.5	µs
	VCO (pins 17-18 and 19)				
	Frequency Control Range after Line Divider (ceramic resonator : 503 kHz)		15.30 to 16.10		kHz
	Phase Comparator φ 1 (pin 22)				
	Output Current Low Loop Gain	± 0.35	± 0.5	± 0.65	mA
	High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
	VCR Switching (pin 23)				
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0.V_{CC} = 12 V)	– 0.03	– 0.25	– 1	mA
	Video Identification (pin 24)				
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3 mA)		0.2	0.6	V
	Output Voltage (with 60 Hz video signal, I_{24} = 2.5 mA)	5	6.5	7.5	V
	Ouput Voltage (with 50 Hz video signal, I_{24} = 10 µA)	11	11.5		V
	Video Identification (pin 25)				
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4.5	5	V
L_{HYS}	Hysteresis	150	240	400	mV
	H–ramp Generator (pin 13)				
I_{ch13}	Charge Current	185	200	215	µA
V_{l13}	Base Voltage of Saw–tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7		mA
	Super Sandcastle (pin 11)				
	Output Voltages				
V_{B11}	Burst Key Pulse Level (I_{11} = – 5 mA)	9			V
V_{L11}	Line Blanking Pulse Level (I_{11} = – 5 mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level (and frame out of function)-(I_{11} = – 5 mA)	2	2.5	3	V
T_{B11}	Delay between Midle of Synch. Pulse (pin 27) and Leading Edge of Burst Key Pulse	2.3		3	µs
	Duration of Burst Key Pulse	3.7	4	5	µs
T_{O11}	Delay between SSC Cutting Level at Pin 12 and Line Blanking Pulse			0.35	µs
	Frame Blanking Time (start with reset of frame divider)		24		Line

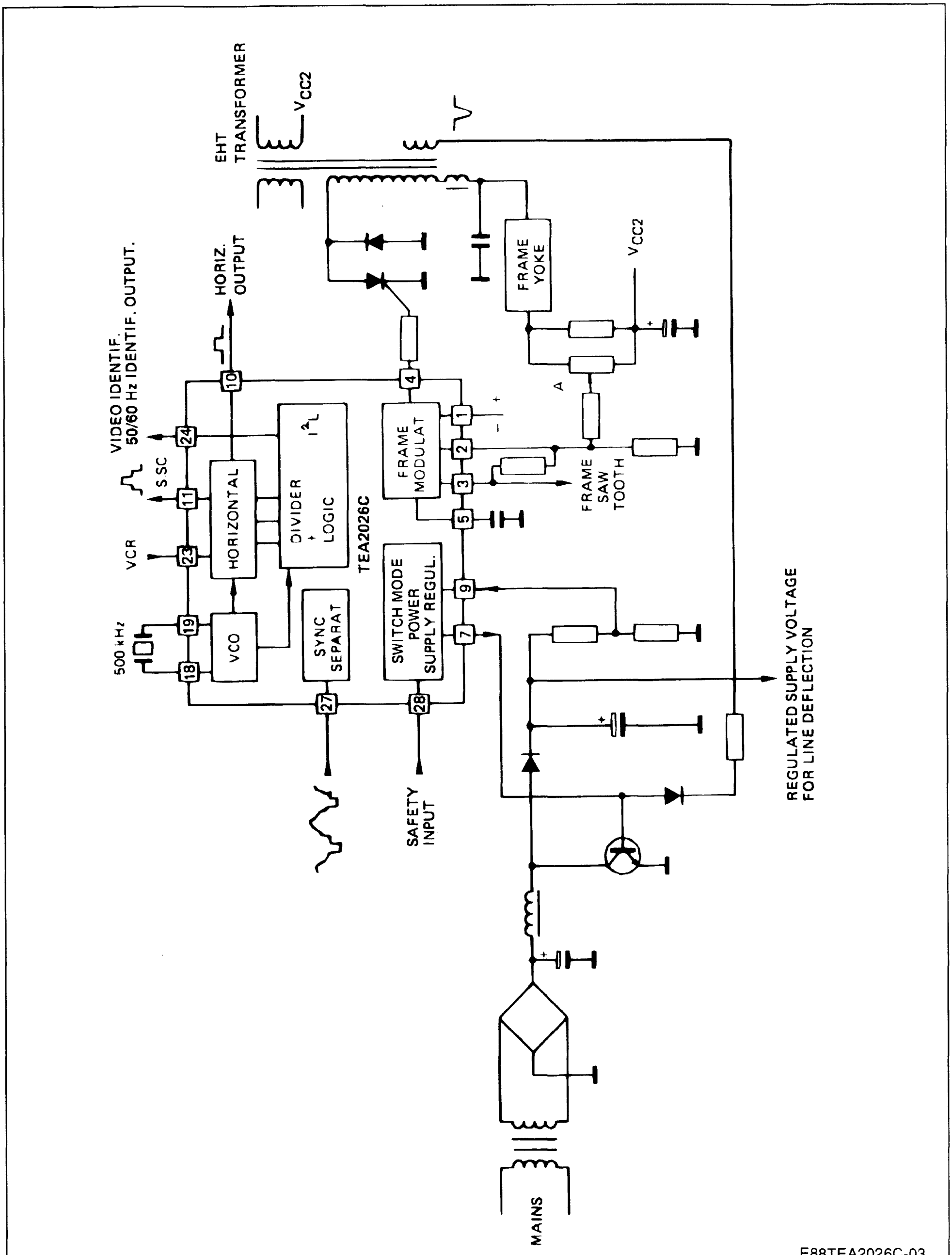
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Negative Line Fly Back Input (pin 12)				
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking	11	11.5	12	V
$V_{\varphi 12}$	Threshold for PLL2	– 1			V
I_{12}	Input Current 11V < V_{12}			– 200	µA
I_{12}	Input Current 1.3 V < V_{12} < 11 V	– 3		+ 3	µA
I_{12}	Input Current 0 V < V_{12} < 1.3 V	0		– 80	µA
I_{12}	Input Current – 1 V < V_{12} < 0 V	0	– 1	– 2	mA
	Line Blanking Trigger			80	µA
	Phase Comparator φ 2 (pin 16)				
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay between the edges of φ 1 and φ 2 (f_{VCO} = 500 kHz)	1.5	2	2.8	µs
	Line Output (open collector, (f_{VCO} = 500 kHz))-(pin 10)				
	Output Voltage (I_{10max} = 20 mA)		1	1.5	V
t_{10}	Output Pulse Duration (when fly–back pulse is in time with t_{10})	24	26	30	µs
Δ_t	φ 2 Phase Range	15	16	19	µs
	Frame Logic				
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50 Hz Window	309		315	Line
	60 Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
	Frame Saw-tooth Generator (pins 3-5)				
	Typical Saw–tooth Amplitude (with external RC)		2.5		Vpp
$I_5(60)$	Internal Current Generator (60 Hz on)	12	14	16	µA
	Discharging Time (with C = 0.47 µF, ΔV < 4 V)	10		60	µs
V_s	Starting Level (0 < I_s < 10 mA)	1	1.26	1.4	V
	Frame Feedback Inputs (pins 1-2)				
$I_{1,2}$	Positive and Negative Input Current			10	µA
	(V_1 – V_2 > 25 mA for frame blanking safety)				
	Frame Output (pin 4)				
	Output Voltage (0 mA < $\|I_4\|$ < 80 mA)	10			V
	t_{ON} max (f_{VCO} = 500 KHz)	36	40	41	µs
	Output Phase Range	0		t_{ON}max	
	SMPS Control Input (pin 9)				
I_9	Input Current (V_9 = V_{ref14})			2	µA
	SMPS Output (pin 7)				
	In all Case, End of SMPS Pulse (pin 7) and Leading Edge of Line Fly–back (pin 12) in Phase				
V_7	Output Voltage (0 < I_7 < 20 mA)	10			V
t_7	t_{ON}max (f_{VCO} = 500 kHz)	30	32	34	µs
	Nominal Time (V_9 = V_{ref14})		10		µs
	Output Phase Range	0		t_{ON} max	
	Safety Input (pin 28)				
V_{28}	Threshold Voltage (V_{ref14})	1.15	1.26	1.37	V
	Input Current (if V_{ref} ≤ V_{28} < 5 V then SMPS, line and frame are switched off during the next line retrace)			3	µA

ELECTRICAL CHARACTERISTICS (continued)

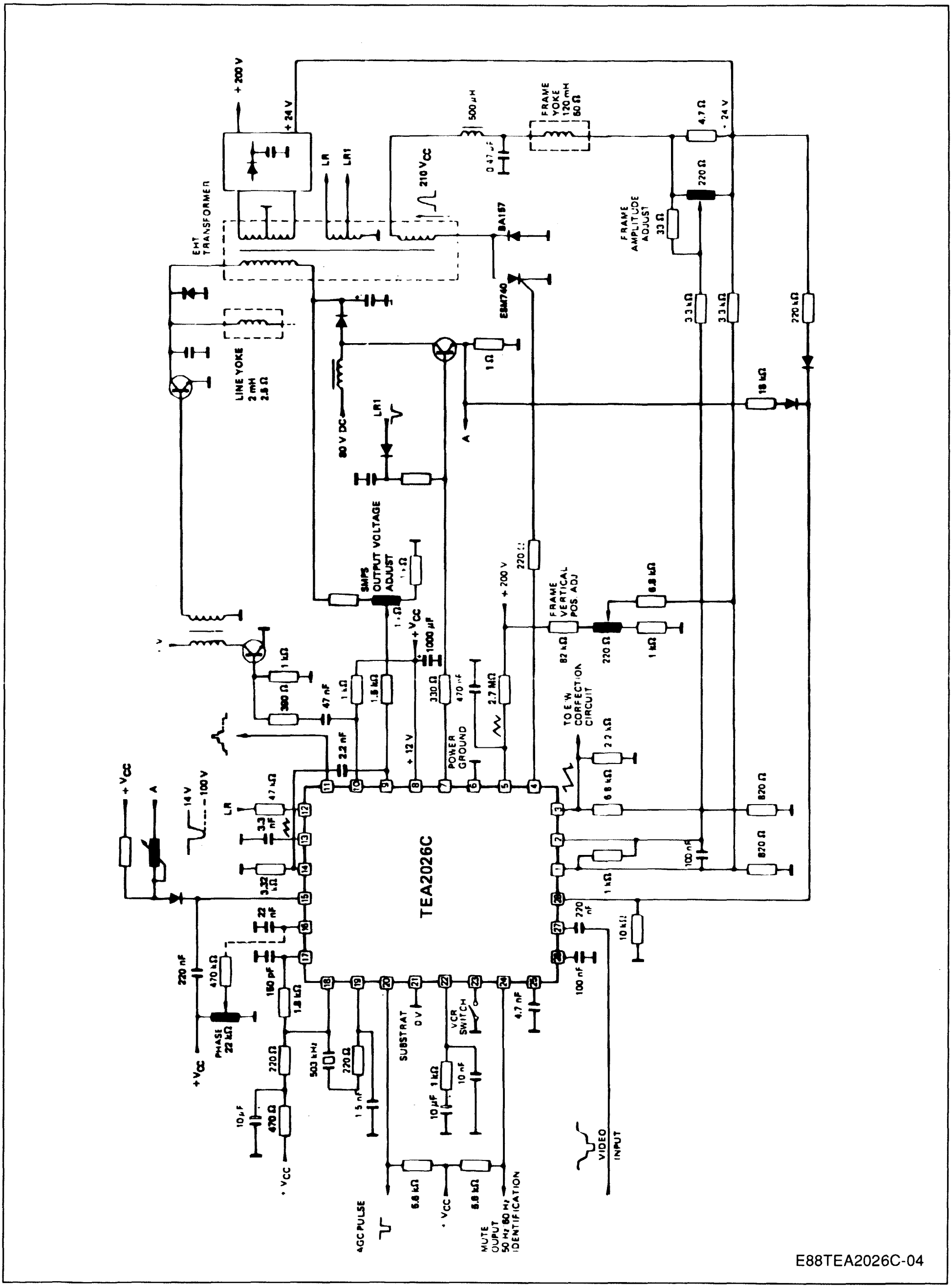
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Switch–on, Switch–off Processing (pin 15)				
I_{ch15}	Charging Current (t_c = 4 µs, T = 64 µs)	70		130	µA
$\frac{I_{ch15}}{I_{dis15}}$	Ratio Charging/discharging	0.8	1	1.2	
	Starting Supply Voltage (pin 8)				
V_{CC}	SMPS*, Frame and Line Starting (pin 7, 10, 4)	5.25		6.5	V
V_{CC}	SMPS Stopping During Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
V_{Hyst}	Hysteresis between Switching-on and Switching-off Level * Progressive Starting by Decreasing V_{15}				mV
	Current Reference (pin 14)				
V_{ref14}	Voltage Reference (with R_{14} = 3.32 KΩ ± 1 %)	1.2	1.26	1.35	V

SIMPLIFIED APPLICATION DIAGRAM



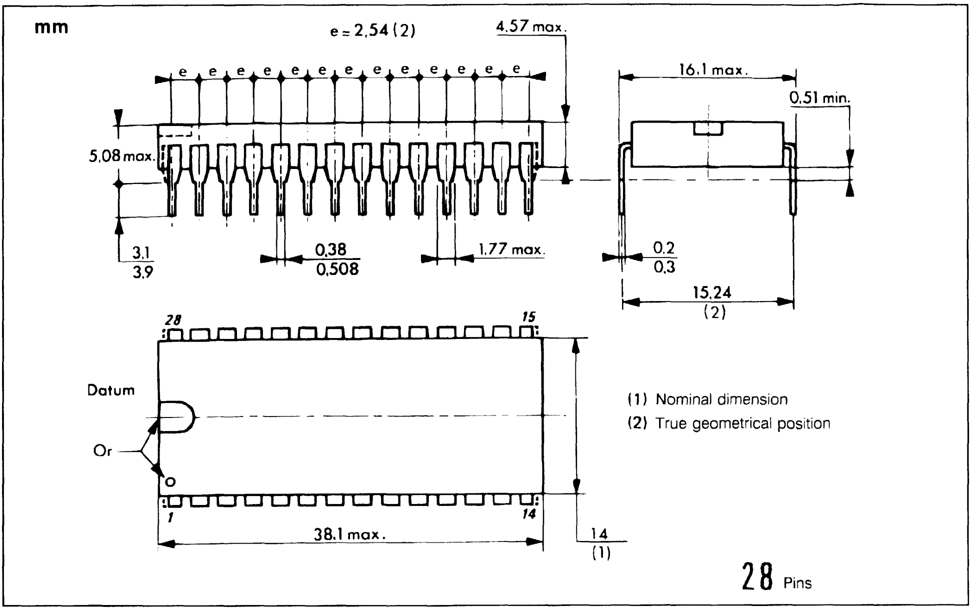
E88TEA2026C-03

APPLICATION CIRCUIT (with thyristor frame power)



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

TEA2028B

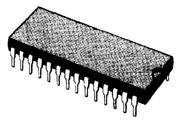
COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION :
- CERAMIC 500kHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT REFERENCE
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- FRAME BLANKING WITH SAFETY CIRCUIT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR

SMPS CONTROL :
- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START-UP PROCESSOR
- OUTPUT PULSES ARE SENT TO THE PRIMARY SMPS IC (TEA2260 or TEA2164) THROUGH A LOW COST SYNCHRO PULSE TRANSFORMER

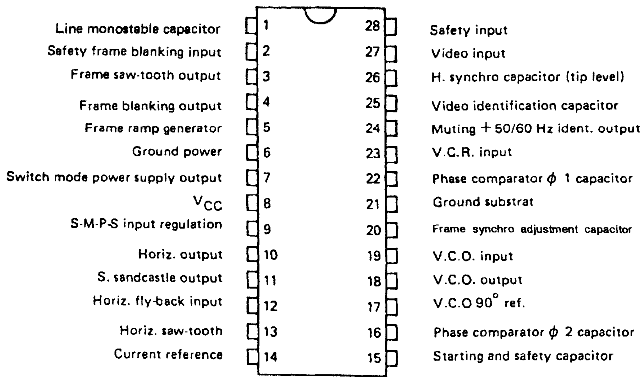
DESCRIPTION

The TEA2028B is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.



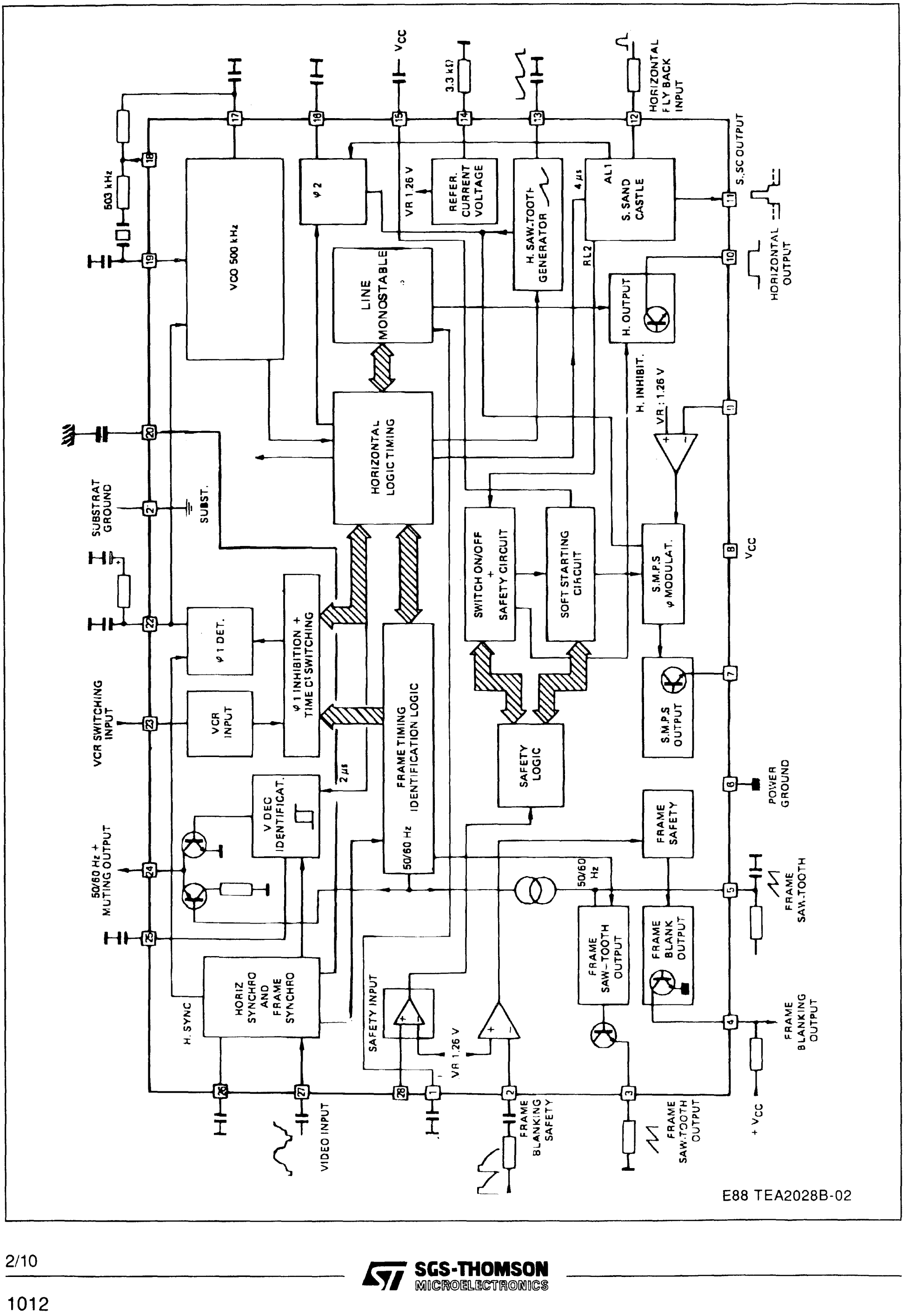
TEA2028B
DIP28
(Plastic Package)

PIN CONNECTIONS



E88 TEA2028B-01

BLOCK DIAGRAM



E88 TEA2028B-02

ABSOLUTE MAXIMUM RATINGS (limiting values)

(T_{amb} = 25 °C unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage (pin 8)		14	V
V_{CC}	Operating Supply Voltage (pin 8)	Starting threshold	13.2	V
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Positive voltage (pin 12)	– 5		V
I_{12}	Line retrace current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	– 10	40	mA
I_3	Frame Saw-tooth Generator (pin 3)		20	mA
I_4	Frame Blanking Input Current (pin 4)		100	mA
I_7	SMPS Output Current (pin 7)	– 40		mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	55	°C/W

GENERAL DESCRIPTION

INTRODUCTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500kHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor.
  - B Class Power stage using an external power amplifier with fly back generator such as the TDA8170.
- Secondary switch mode power regulation.
- The SMPS output synchronize a primary I.C. (TEA2260 or TEA2164) at the mains part.
- This concept allows ACTIVE STANDBY facilities.
- Line and frame synchronization separation.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- Automatic 50-60Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator.
- Frame blanking output.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500KHz VCO.

The circuit is supplied in a 28 pin DIP case.

V_{CC} = 12V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.

The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Time constant of Frame Separator can be adjusted by adding a capacitor pin 20.

The frame timing identification logic permits automatic adaptatio to 50 - 60Hz standards or non-interlaced video.

An automatic synchronization window width system provides :

- fast frame capture (6.7ms wide window),
- good noise immunity (0.4ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly-back effects.

Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32µs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500KHz VCO.

The circuit uses two phase-locked loops (PLL) :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 29µs (with C(pin 1) = 3.3nF), independent of V_{CC} and delay in switching off the scanning transistor.

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0V : no video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly-back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame blanking time (start with reset of frame divider) is 21 lines.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SAW-TOOTH GENERATOR.

The current to charge the capacitor is automatically switched to 60Hz operation to maintain constant amplitude.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary I.C. (TEA2260 or TEA2164) via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage below 1.26V the two outputs are simultaneously cut off until this voltage reaches the 1.26V threshold again. In this case the switch mode power supply is restarted by the "soft start" system.

If this cycle is repeated three times, the two outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be lower than 3.5V.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up the horizontal scanning function comes into operation at V_{CC} = 6V. The power supply then comes into operation progressively.

On shutting down, the two functions are interrupted simultaneously after the first line fly back.

FRAME BLANKING SAFETY (pin 2)

The frame blanking safety checks the normal of frame scanning.

In case of any problem pin 4 and pin 11 is at a high level (frame blanking) in order to protect the tube.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8) (frame, line and SMPS output without load)		50	80	mA
	Sync Separator (pins 26-27)				
	Positive Video Input AC Coupled (output impedance of signal source < 200Ω)	0.2	1.8	3	V_{pp}
$-I_{27}$	Negative Clamping Current (during sync pulse)	– 25	– 40	–55	µA
I_{27}	Clamping Current	3	6	9	µA
	Pin for slicing level 0.2V < V_{27pp} < 2V (50% of sync amplitude)				
$-I_{26}$	Negative Current	0	– 750	– 1000	µA
I_{26}	Positive Current	17	25	36	µA
	Frame Synchro adjustment (pin 20) (V_{20} = 2.5V)				
I_{20H}	Output Current (V_{27} = 12V)		7.2		µA
I_{20L}	Output Current (V_{27} = 0V)		– 2.8		µA
	VCO (pins 17-18 and 19)				
	Frequency control range after line divider (ceramic resonator : 503kHz)		15.30 to 16.10		kHz
	Phase Comparator φ 1 (pin 22)				
	Output Current Low Loop Gain	± 0.35	± 0.50	± 0.65	mA
	High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
	VCR Switching (pin 23)				
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0, V_{CC} = 12V)	– 0.030	– 0.25	– 1	mA
	Video Identification (pin 24)				
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3mA)		0.2	0.6	V
	Output Voltage (with 60Hz video signal, I_{24} = 2.5mA)	5	6.5	7.5	V
	Output Voltage (with 50Hz video signal, I_{24} = 10µA)	11.0	11.5		V
	Video Identification (pin 25)				
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4.5	5	V
L_{HYS}	Hysteresis		350		mV
	H-ramp Generator (pin 13)				
I_{ch13}	Charge Current	185	200	215	µA
V_{l13}	Base Voltage of Saw-tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7.0		mA
	Super Sandcastle (pin 11) Output Voltages				
V_{B11}	Burst key pulse level (I_{11} = – 5mA)	9			V
V_{L11}	Line Blanking Pulse Level (I_{11} = – 5mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level (and frame out of function) (I_{11} = – 5mA)	2	2.5	3	V
	Super Sandcastle				
T_{B11}	Delay between middle of synch pulse (pin 27) and leading edge of burst key pulse	2.3		3.0	µs
	Duration of burst key pulse	3.7	4	5	µs
T_{O11}	Delay Between SSC Cutting Level at Pin 12 and Line Blanking Pulse			0.35	µs
	Frame Blanking Time (start with reset of frame divider)		21		Line

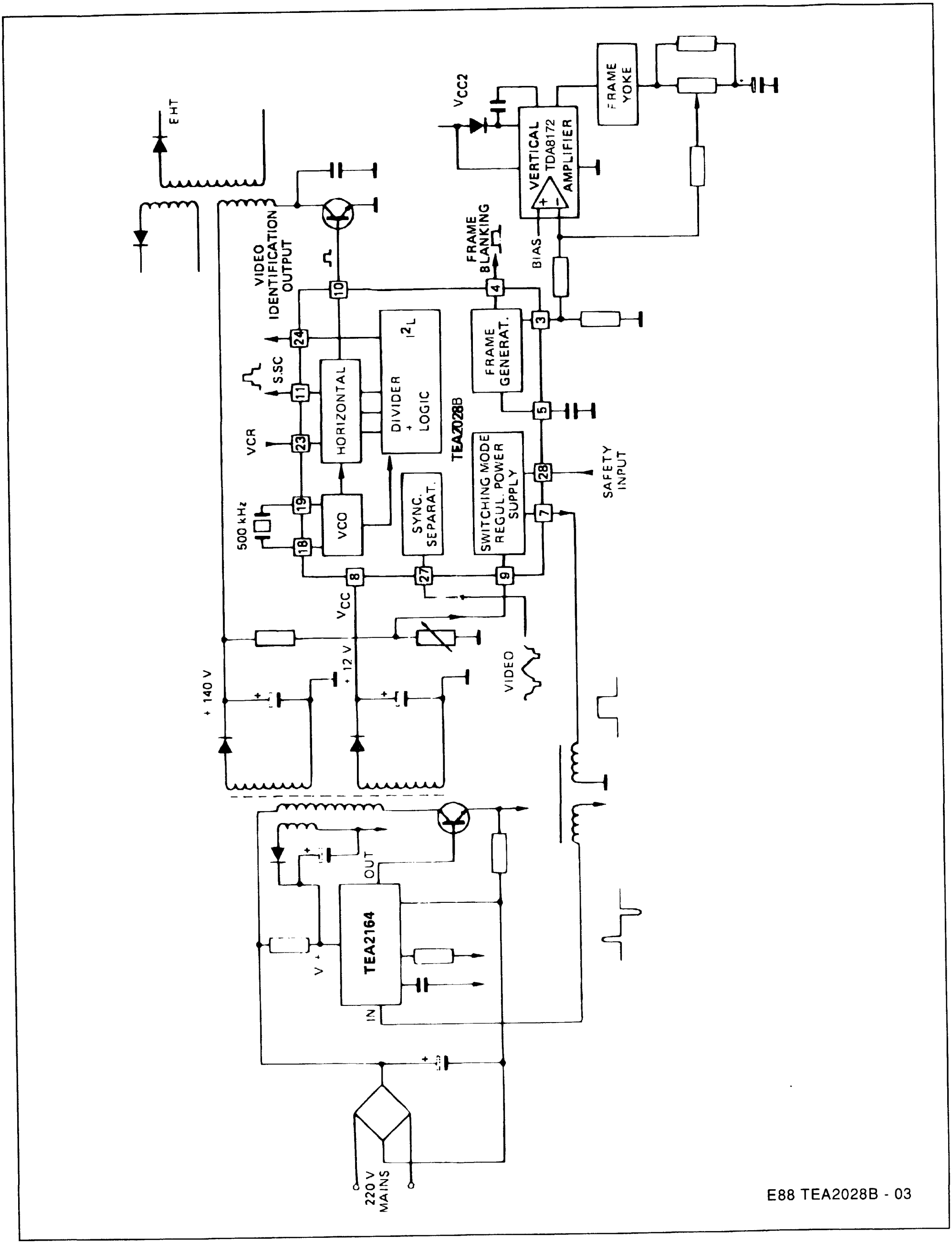
ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Positive Line Fly Back Input (pin 12)				
	Delay between middle of synch pulse and middle of line retrace	2.1	2.6	3.1	µs
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking		0.3		V
$V_{\varphi 12}$	Threshold for PLL2		3		V
I_{12}	Input Current $-0.4\ V < V_{12} < V_{bl12}$		− 20		µA
I_{12}	Input Current $V_{bl12} < V_{12} < V_{\varphi 12}$		− 10		µA
I_{12}	Input Current $V_{\varphi 12} < V_{12} < V_{CC}$	0		1	µA
	Phase Comparator φ 2 (pin 16)				
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay Between the Edges of φ 1 and φ 2 (f_{VCO} = 500kHz)		2.3		µs
	Line Output (open collector, F_{vco} = 500KHz) (pin 10)				
	Output Voltage (I_{10max} = 20mA)		1	1.5	V
t_{10}	Output Pulse Duration (when fly-back pulse is with in time t_{10}) (with C (pin 1) = 3.3nF)	27.5	29	30.5	µs
Δt	φ 2 Phase Range	15	16	19	µs
	Frame Logic				
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50 Hz Window	309		315	Line
	60 Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
	Frame Saw-tooth generator (pins 3-5)				
$I_5(60)$	Internal Current Generator (60Hz on)	12	14	16	µA
	Discharging Current	18	55		mA
V_s	Starting Level ($0 < I_s < 10mA$)	1	1.26	1.4	V
	Frame Blanking Safety Input (pin 2)				
	Threshold Voltage (negative going pulse)	1.15	1.26	1.37	V
	Frame Blanking Output (open collector) - (pin 4)				
	Output Saturation Voltage (I_4 = 5mA)			0.4	V
	Output Current (low level)			10	mA
	Blanking Time		21		Line
	SMPS Control Input (pin 9)				
I_9	Input Current ($V_9 = V_{ref\ 14}$)			2	µA
	SMPS Output (pin 7)				
	No relation between end of SMPS pulse (pin 7) and leading edge of line fly back (pin 12)				
V_7	Output Voltage ($0 < I_7 < 20mA$)	10			V
t_7	t_{ON} max (f_{VCO} = 500kHz)	26	30	31	µs
	Output Phase Range	0		t_{ON} max	
	Safety Input (pin 28)				
V_{28}	Threshold Voltage ($V_{28} = V_{ref\ 14}$)	1.20	1.26	1.5	V
	Input Current (if $V_{28} < V_{ref\ 14}$ then SMPS and line are switched off during the next line retrace)			3	µA
	Switch-on, Switch-off Processing (pin 15)				
I_{ch15}	Charging Current (t_c = 4µs, T = 64µs)	70		130	µA
$\frac{I_{ch15}}{I_{dis15}}$	Ratio charging/discharging	0.8	1	1.2	

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Starting Supply Voltage (pin 8)				
V_{CC}	SMPS* and Line Starting (pin 7 and pin 10)	5.25		6.5	V
V_{CC}	SMPS Stopping During Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
V_{Hyst}	Hysteresis between Switching-on and Switching-off Level		450		mV
	* Progressive Starting by Decreasing V15				
	Current Reference (pin 14)				
$V_{ref\ 14}$	Voltage Reference (R_{14} = 3.32KΩ ± 1%)	1.2	1.26	1.35	V

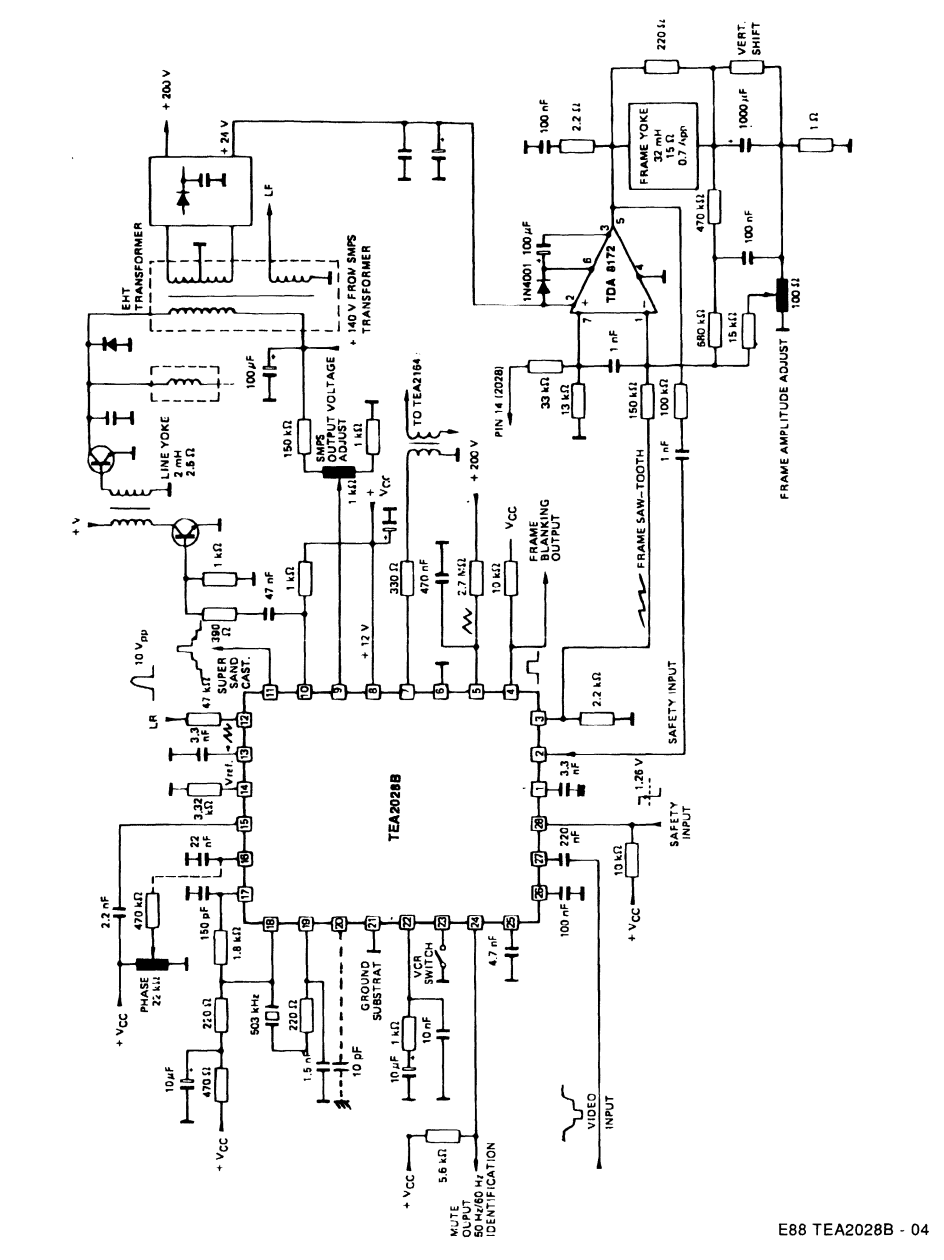
APPLICATION WITH TDA8172 FOR B CLASS FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION



E88 TEA2028B - 03

APPLICATION CIRCUIT

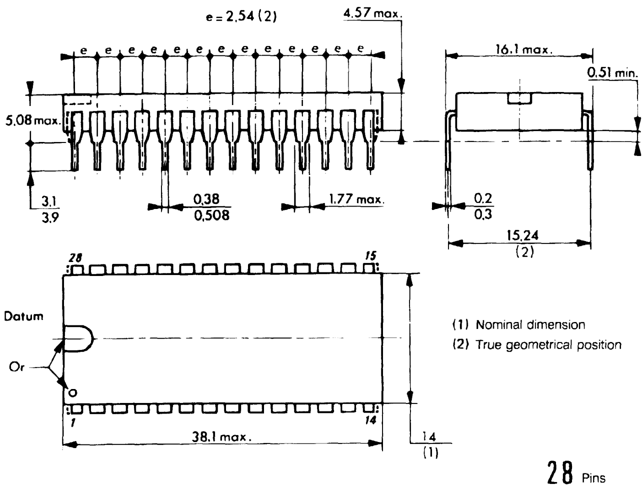
(with B class frame power)



E88 TEA2028B - 04

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



SGS-THOMSON
MICROELECTRONICS

TEA2029C

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

DEFLECTION :

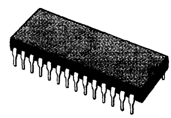
- CERAMIC 500KHz RESONATOR FREQUENCY REFERENCE
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- HIGH PERFORMANCE SYNCHRONIZATION
- SUPER SANDCASTLE OUTPUT
- VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL
- SPECIAL PATENTED FRAME SYNCHRO DEVICE FOR VCR OPERATION
- FRAME SAW-TOOTH GENERATOR
- FRAME PHASE MODULATOR FOR THYRISTOR

SMPS CONTROL :

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START UP PROCESSOR
- OUTPUT PULSES ARE SENT TO THE PRIMARY SMPS IC (TEA2164) THROUGH A LOW COST SYNCHRO PULSE TRANSFORMER

DESCRIPTION

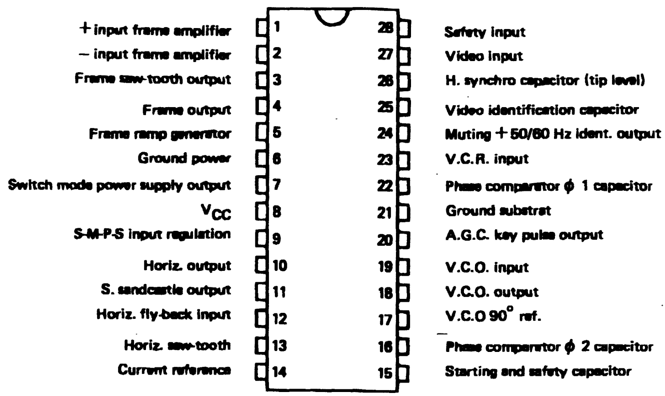
The TEA2029C is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.



DIP 28
(Plastic Package)

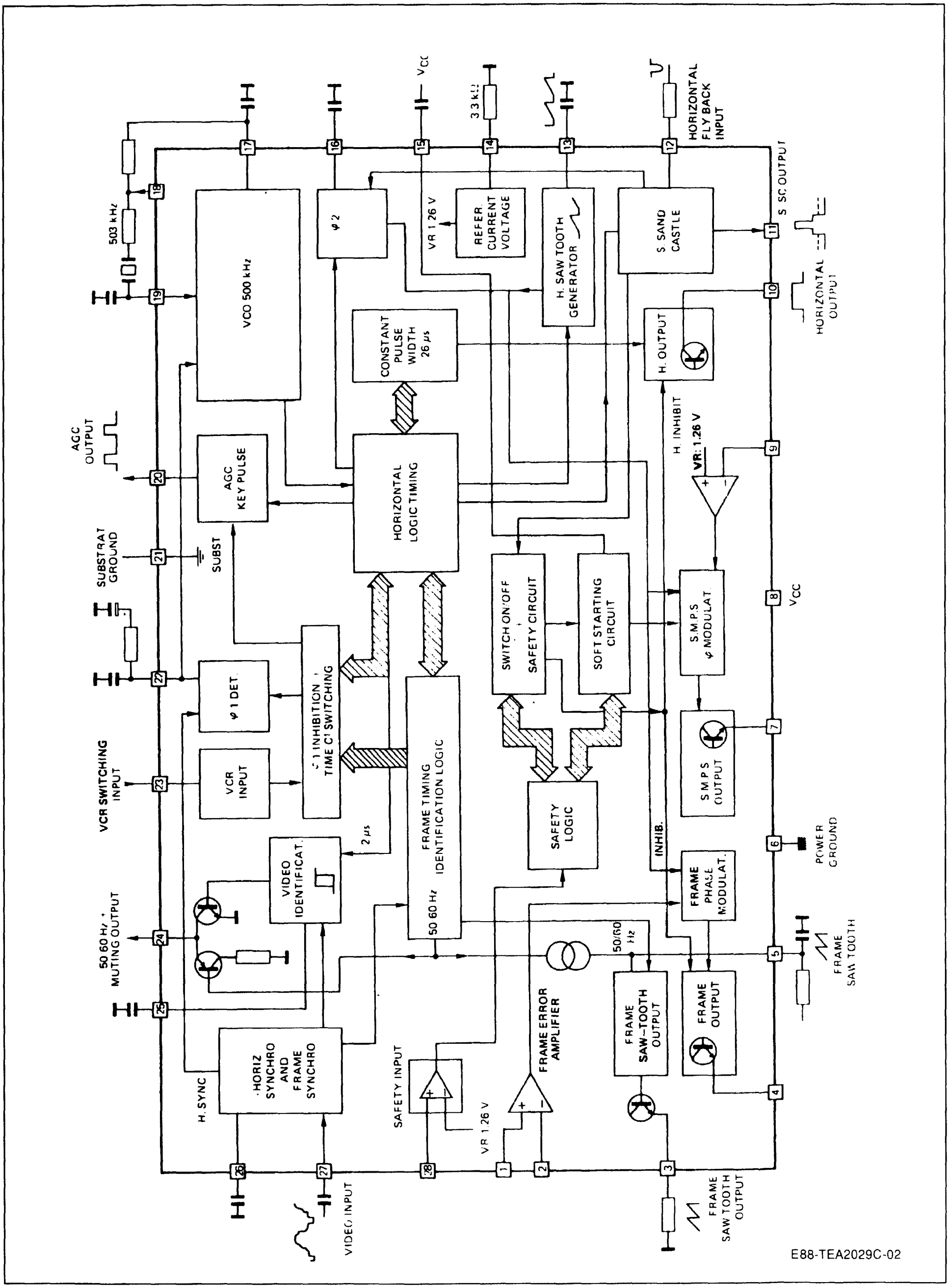
ORDER CODE : TEA2029C

PIN CONNECTIONS



E88 TEA2029C-01

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (limiting values) T_{amb} = 25°C (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
	Supply Voltage (pin 8)		14	V
VCC	Operating Supply Voltage (pin 8)	Starting threshold	13.2	V
I_{20}	AGC Current (pin 20)		5	mA
I_{24}	Video Identification Current (pin 24)		10	mA
V_{12}	Negative Line Retrace Voltage (pin 12)	– 20		V
I_{12}	Line Retrace Current (pin 12)		+ 10	mA
I_{10}	Line Output Current (pin 10)	– 10	40	mA
I_3	Frame Saw-tooth Generator (pin 3)		20	mA
I_4	Frame Output Current (pin 4)		100	mA
I_7	SMPS Output Current (pin 7)	– 40	40	mA
I_{28}	Safety Input Current (pin 28)		5	mA
V_{28}	Safety Input Voltage (pin 28)		V_{CC}	
V_1/V_2	Common Mode Range (pins 1-2)		10	V

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	55	°C/W

GENERAL DESCRIPTION

This integrated circuit uses I^2L bipolar technology and combines analog signal processing with digital processing.

Timing signals are obtained from a voltage-controlled oscillator (VCO) operating at 500KHz by means of a cheap ceramic resonator. This avoids the frequency adjustment normally required with line and frame oscillators.

A chain of dividers and appropriate logic circuitry produce very accurately defined sampling pulses and the necessary timing signals.

The principal functions implemented are :

- Horizontal scanning processor.
- Frame scanning processor. Two applications are possible :
  - D Class Power stage using an external thyristor.
  - B Class Power stage using an external power amplifier with fly-back generator such as the TDA8170.
- Secondary switch mode power regulation. The SMPS output synchronize a primary I.C. (TEA2164) at the mains part. This concept allows ACTIVE STANDBY facilities.
- Dual phase-locked loop horizontal scanning.
- High performance frame and line synchronization with interlacing control.
- Video identification circuit.
- Super sandcastle.
- AGC key pulse output.
- Automatic 50-60Hz standard identification.
- VCR input for PLL time constant and frame synchro switching.
- Frame saw-tooth generator and phase modulator.
- Switching mode regulated power supply comprising error amplifier and phase modulator.
- Security circuit and start-up processor.
- 500KHz VCO

The circuit is supplied in a 28 pin DIP case.
V_{CC} = 12V.

SYNCHRONIZATION SEPARATOR

Line synchronization separator is clamped to black level of input video signal with synchronization pulse bottom level measurement.
The synchronization pulses are divided centrally between the black level and the synchronization pulse bottom level, to improve performance on video signals in noise conditions.

FRAME SYNCHRONIZATION

Frame synchronization is fully integrated (no external capacitor required).
The frame timing identification logic permits automatic adaptation to 50 - 60Hz standards or non-interlaced video.

An automatic synchronization window width system provides :

- fast frame capture (6.7ms wide window),
- good noise immunity (0.4ms narrow window).

The internal generator starts the discharge of the saw-tooth generator capacitor so that it is not disturbed by line fly back effects.
Thanks to the logic control, the beginning of the charge phase does not depend on any disturbing effect of the line fly-back.

A 32µs timing is automatically applied on standardized transmissions, for perfect interlacing.

In VCR mode, the discharge time is controlled by an internal monostable independent of the line frequency and gives a direct frame synchronization.

HORIZONTAL SCANNING

The horizontal scanning frequency is obtained from the 500kHz VCO.

The circuit uses two phase-locked loops (PLL) :

the first one controls the frequency, the second one controls the relative phase of the synchronization and line fly-back signals.

The frequency PLL has two switched time constants to provide :

- capture with a short time constant,
- good noise immunity after capture with a long time constant.

The output pulse has a constant duration of 26µs, independent of V_{CC} and any delay in switching off the scanning transistor.

VIDEO IDENTIFICATION

The horizontal synchronization signal is sampled by a 2µs pulse within the synchronization pulse. The signal is integrated by an external capacitor.

The identification function provides three different levels :

- 0V : no video identification
- 6V : 60Hz video identification
- 12V : 50Hz video identification

This information may be used for timing research in the case of frequency or voltage synthetizer type receivers, and for audio muting.

SUPER SANDCASTLE with 3 levels : burst, line fly-back, frame blanking.

In the event of vertical scanning failure, the frame blanking level goes high to protect the tube.

Frame blanking time (start with reset of Frame divider) is 24 lines.

VCR INPUT

This provides for continuous use of the short time constant of the first phase-locked loop (frequency).

In VCR mode, the frame synchronization window widens out to a search window and there is no delay of frame fly-back (direct synchronization).

FRAME SCANNING

FRAME SAW-TOOTH GENERATOR. The current to charge the capacitor is automatically switched to 60Hz operation to maintain constant amplitude.

FRAME PHASE MODULATOR (WITH TWO DIFFERENTIAL INPUTS). The output signal is a pulse at the line frequency, pulse width modulated by the voltage at the differential pre-amplifier input.

This signal is used to control a thyristor which provides the scanning current to the yoke. The saw-tooth output is a low impedance, however, and can therefore be used in class B operation with a power amplifier circuit.

SWITCH MODE POWER SUPPLY (SMPS) SECONDARY TO PRIMARY REGULATION

This power supply uses a differential error amplifier with an internal reference voltage of 1.26V and a phase modulator operating at the line frequency. The power transistor is turned off by the falling edge of the horizontal saw-tooth.

The "soft start" device imposes a very small conduction angle on starting up, this angle progressively increases to its nominal regulation value.

The maximum conduction angle may be monitored by forcing a voltage on pin 15. This pin may also be used for current limitation.

The output pulse is sent to the primary S.M.P.S. I.C. (TEA2164) via a low cost synchro transformer.

SECURITY CIRCUIT AND START UP PROCESSOR

When the security input (pin 28) is at a voltage exceeding 1.26V the three outputs are simultaneously cut off until this voltage drops below the 1.26V threshold again. In this case the switch mode power supply is restarted by the "soft start" system.

If this cycle is repeated three times, the three outputs are cut off definitively. To reset the safety logic circuits, V_{CC} must be zero volt.

This circuit eliminates the risk to switch off the TV receiver in the event of a flash affecting the tube.

On starting up, the horizontal and vertical scanning functions come into operation at V_{CC} = 6V. The power supply then comes into operation progressively.

On shutting down, the three functions are interrupted simultaneously after the first line fly-back.

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25°C V_{CC} = 12V (unless otherwise noted) Pulse duration at 50% of the ampl.

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current (pin 8, frame, line and SMPS output without load)		50	80	mA
	Synch Separator (pins 26-27)				
	Positive Video Input AC Coupled (output impedance of signal source < 200Ω)	0.2	1.8	3	V_{pp}
$-I_{27}$	Negative Clamping Current (during synch, pulse)	– 25	– 40	– 55	µA
I_{27}	Clamping Current	3	6	9	µA
	Pin for slicing level 0.2V < V_{27pp} < 2V (50% of sync amplitude)				
$-I_{26}$	Positive Current	0	– 750	– 1000	µA
I_{26}	Negative Current	17	25	36	µA
	Pulse for keyed AGC (pin 20) Positive (function : without video signal : low level, with video signal : key pulses)				
I_{20}	Output Current			5	mA
V_{20}	Output Saturation Voltage (I_{20} = 5mA)		0.25	0.4	V
t_k	Pulse width (synchro pulse is always inside the key pulse)	6.5	8	8.5	µs
	VCO (pins 17-18 and 19) Frequency control range after line divider (ceramic resonator : 503kHz)	15.30 to 16.10			kHz
	Phase Comparator φ 1 (pin 22)				
	Output Current Low Loop Gain	± 0.35	± 0.50	± 0.65	mA
	High Loop Gain	± 1	± 1.5	± 2	mA
	Window Pulse Width	7	10	13	µs
	VCR Switching (pin 23)				
	Threshold Voltage VCR Operating	1.7	2.2	2.7	V
I_{23}	Input Current (V_{23} = 0 V_{CC} = 12V)	– 0.030	– 0.25	– 1	mA
	Video Identification (pin 24)				
V_{24}	Output Saturation Voltage (without video signal, I_{24} = 3mA)		0.2	0.6	V
	Output Voltage (with 60Hz video signal, I_{24} = 2.5mA)	5	6.5	7.5	V
	Output Voltage (with 50Hz video signal, I_{24} = 10µA)	11	11.5		V
	Video Identification (pin 25)				
I_{25}	Output Current (charging the capacitor)	0.5	0.75	1	mA
t_{25}	Identification Time (charging the capacitor)	1.3	1.7	2.2	µs
V_{25}	Threshold (voltage changing from lower to higher value)	4	4..5	5	V
L_{HYS}	Hysteresis	150	240	400	mV

ELECTRICAL OPERATING CHARACTERISTICS (continued)

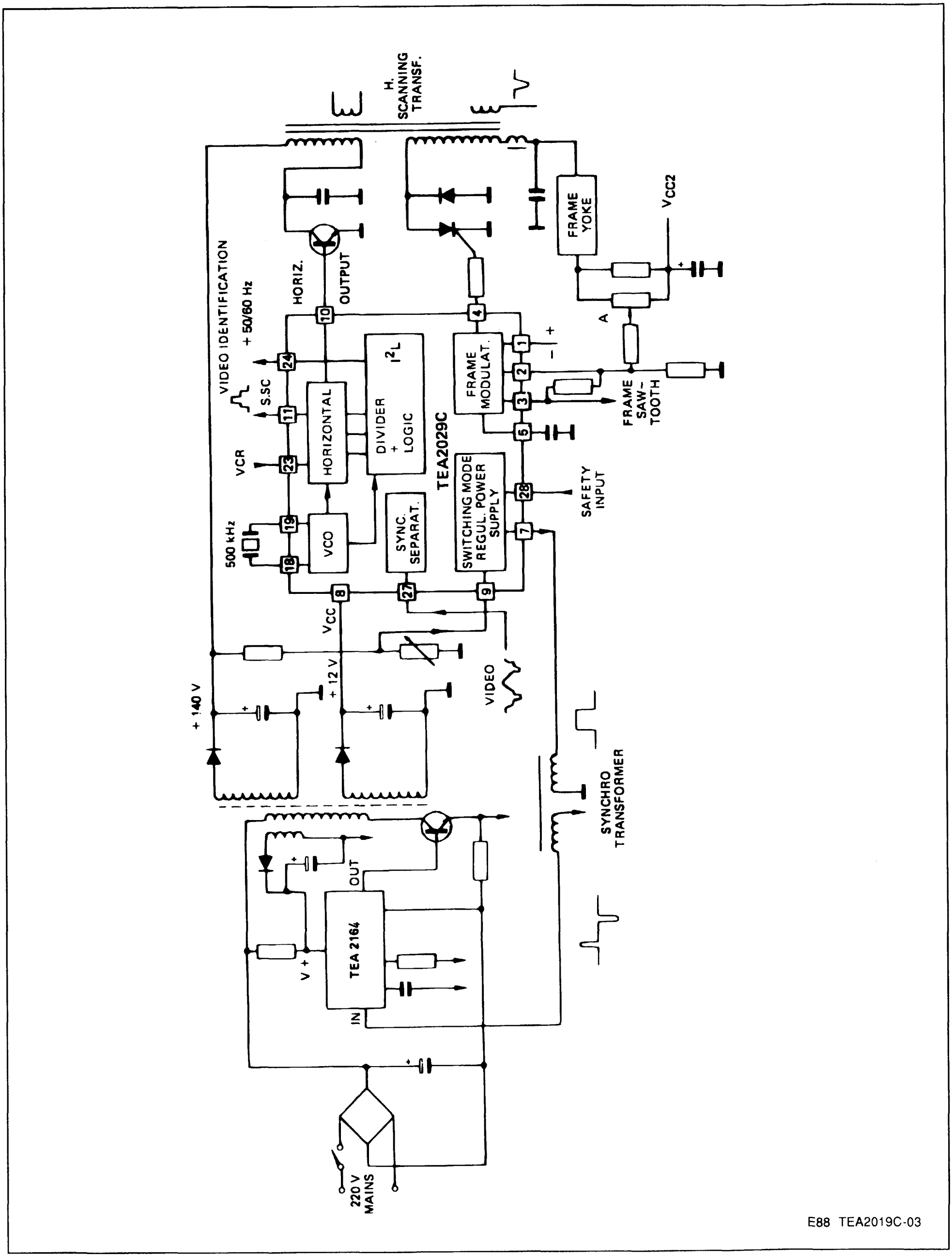
Symbol	Parameter	Min.	Typ.	Max.	Unit
	H-ramp Generator (pin 13)				
I_{ch13}	Charge Current	185	200	215	µA
V_{l13}	Base Voltage of Saw-tooth			0.5	V
I_{dis13}	Discharge Current	3.5	7		mA
	Super Sandcastle (pin 11)				
	Output Voltages				
V_{B11}	Burst Key Pulse level (I_{11} = – 5mA)	9			V
V_{L11}	Line Blanking Pulse Level (I_{11} = – 5mA)	4	4.5	5	V
V_{BT11}	Frame Blanking Pulse Level (and frame out of function) (I_{11} = – 5mA)	2	2.5	3	V
	Super Sandcastle (continued)				
T_{B11}	Delay Between Middle of Synch Pulse (pin 27) and Leading Edge of Burst Key Pulse	2.3		3	µs
	Duration of Burst Key Pulse	3.7	4	5	µs
T_{O11}	Delay Between SSC Cutting Level at Pin 12 and Line Blanking Pulse			0.35	µs
	Negative Line Fly Back Input (pin 12)				
	Threshold for SMPS Safety	1.1			V
V_{bl12}	Threshold for Blanking	11	11.5	12	V
$V_{\varphi12}$	Threshold for PLL2	– 1			V
I_{12}	Input Current 11V < V_{12}			– 200	µA
I_{12}	Input Current 1. 3V < V_{12} < 11V	– 3		3	µA
I_{12}	Input Current 0V < V_{12} < 1.3V	0		– 80	µA
I_{12}	Input Current – 1V < V_{12} < 0V	0	– 1	– 2	mA
	Line Blanking Trigger			80	µA
	Phase Comparator φ 2 (pin 16)				
I_{16}	Charging Current	0.4	0.6	0.8	mA
	Delay Between the Edges of φ 1 and φ 2 (f_{VCO} = 500kHz)	1.5	2	2.8	µs
	Line Output (open collector) (pin 10)				
	Output Voltage ($I_{10\ max}$ = 20mA)		1	1.5	V
T_{10}	Output Pulse Duration (when fly-back pulse is with in time T_{10}) (f_{VCO} = 500kHz)	24	26	30	µs
Δt	φ 2 Phase Range	15	16	19	µs
	Frame Logic				
	Free Running Period (with mute signal)		315		Line
	Search Window	247		361	Line
	50Hz Window	309		315	Line
	60Hz Window	247		276	Line
	VCR Mode Window	247		361	Line
	Frame Saw-tooth generator (pins 3-5)				
	Saw-tooth Amplitude	2	3	4	V_{pp}
$I_5(60)$	Internal Current Generator (60Hz on)	12	14	16	µA
	Discharging Time (with C = 0.47µF, ΔV < 4V)	50		70	µs
V_s	Starting Level (0mA < I_s < 10mA)	1	1.26	14	V
	Saw-tooth Amplitude (I_s = 10mA)	2	3	4	V_{pp}
	Frame Feedback Inputs (pins 1-2)				
$I_{1.2}$	Positive and Negative Input Current ((V_1 – V_2) > 25mV for frame blanking safety)			10	µA

ELECTRICAL OPERATING CHARACTERISTICS (continued)

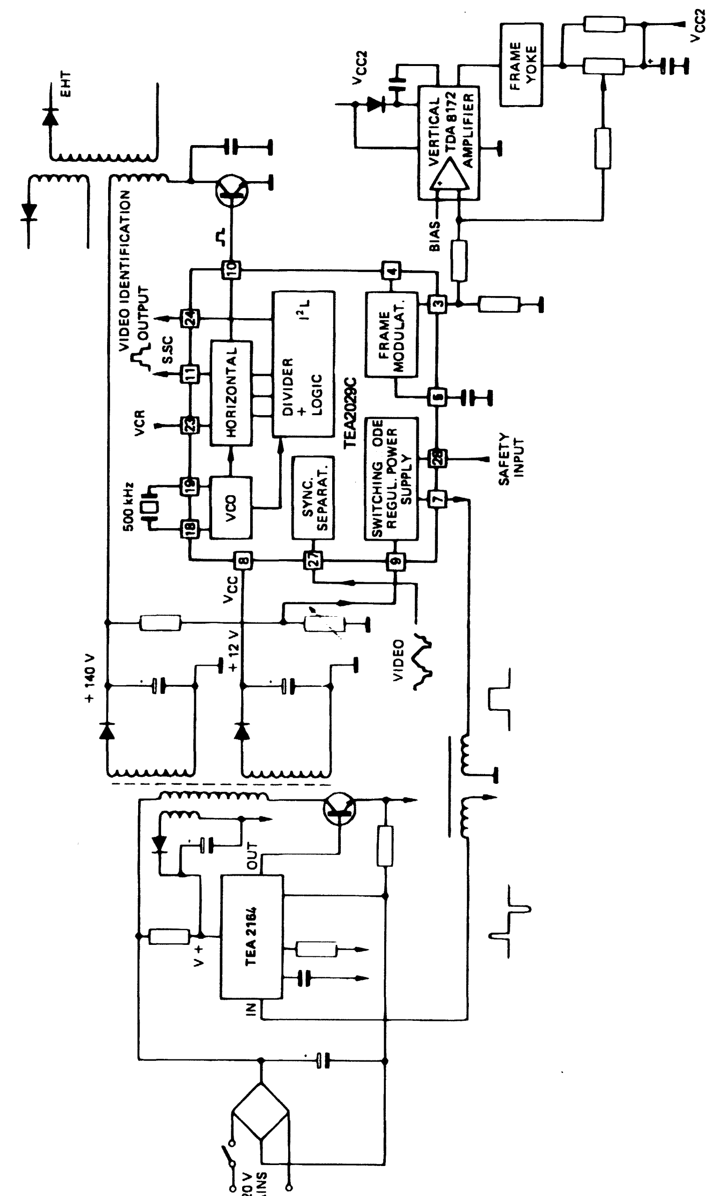
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frame Output (pin 4)				
	Output Voltage (0mA < $\|I_4\|$ < 80mA)	10			V
	T_{ON} max (f_{VCO} = 500kHz)	36	40	41	µs
	Output Phase Range	0		t_{ON} max	
	SMPS Control Input (pin 9)				
I_9	Input Current ($V_9 = V_{ref\ 14}$)			2	µA
	SMPS Output (pin 7) No Relation Between End of SMPS Pulse (pin 7) and Leading Edge of Line Fly Back (pin 12)				
V_7	Output Voltage (0 < I_7 < 20mA)	10			V
T_7	t_{ON} max (f_{VCO} = 500kHz)	30	32	34	µs
	Nominal Time ($V_9 = V_{ref\ 14}$)	26		31	µs
	Output Phase Range	0		t_{ON} max	
	Safety Input (pin 28)				
V_{28}	Threshold Voltage ($V_{28} = V_{ref\ 14}$)	1.15	1.26	1.37	V
	Input Current (if $V_{28} > V_{ref\ 14}$ then SMPS, line and frame are switched off during the next line retrace)			3	µA
	Switch-on, Switch-off Processing (pin 15)				
$I_{ch\ 15}$	Charging Current (t_c = 4µs, T = 64µs)	70		130	µA
$\frac{I_{ch\ 15}}{I_{dis\ 15}}$	Ratio Charging/discharging	0.8	1	1.2	
	Starting Supply Voltage (pin 8)				
V_{CC}	SMPS*, Frame and Line Starting (pins 7, 10 and 4)	5.25		6.5	V
V_{CC}	SMPS Stopping During Line Retrace	5.25		6.5	V
V_{CC}	Frame and Line Stopping	5.25		6.5	V
	Current Reference (pin 14)				
$V_{ref\ 14}$	Voltage Reference	1.2	1.26	1.35	V

* Progressive starting by decreasing V_{15}.

APPLICATION WITH THYRISTOR FOR FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION

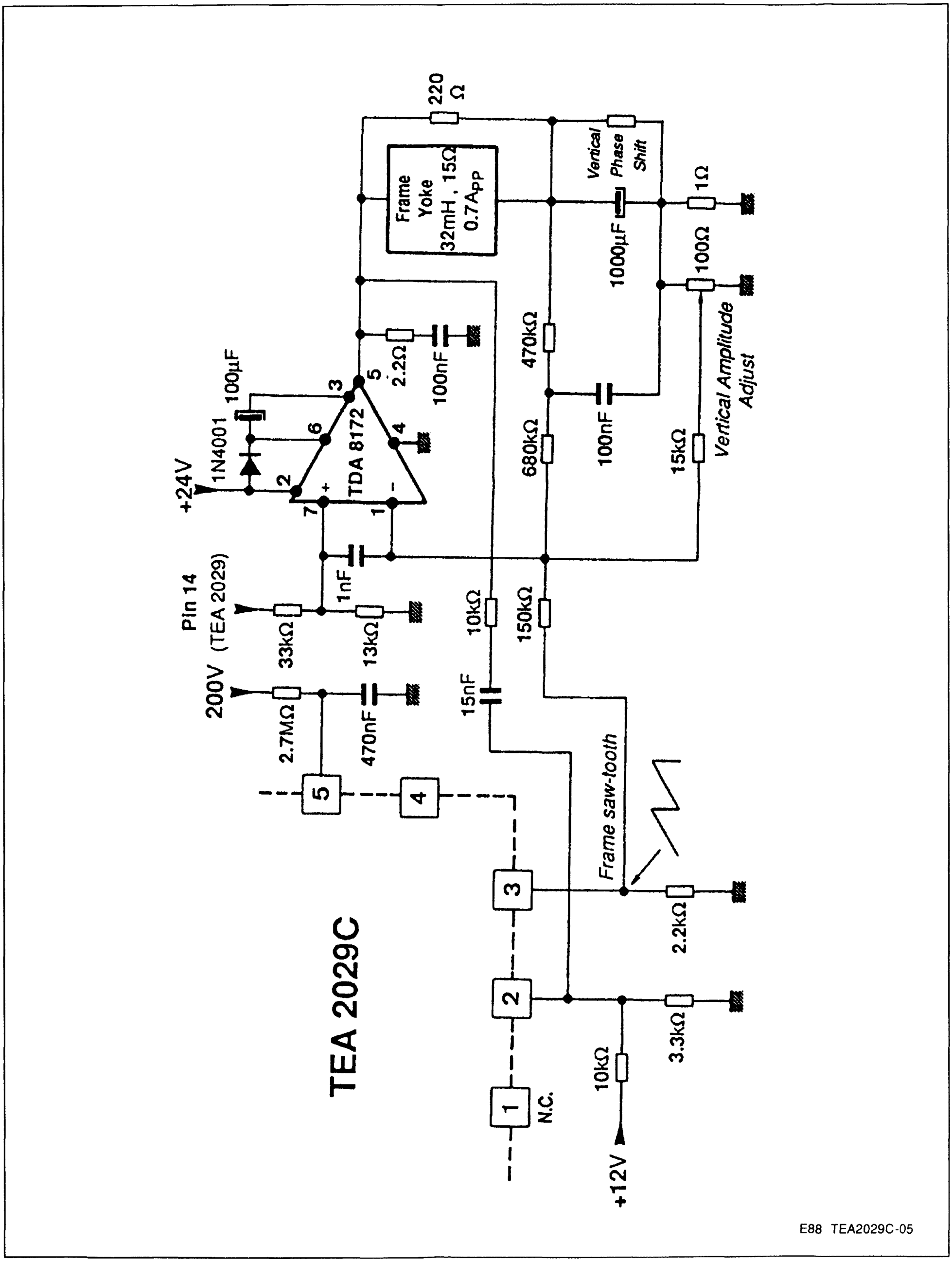


APPLICATION WITH TDA8172 FOR B CLASS FRAME POWER AND TEA2164 FOR SECONDARY SMPS REGULATION

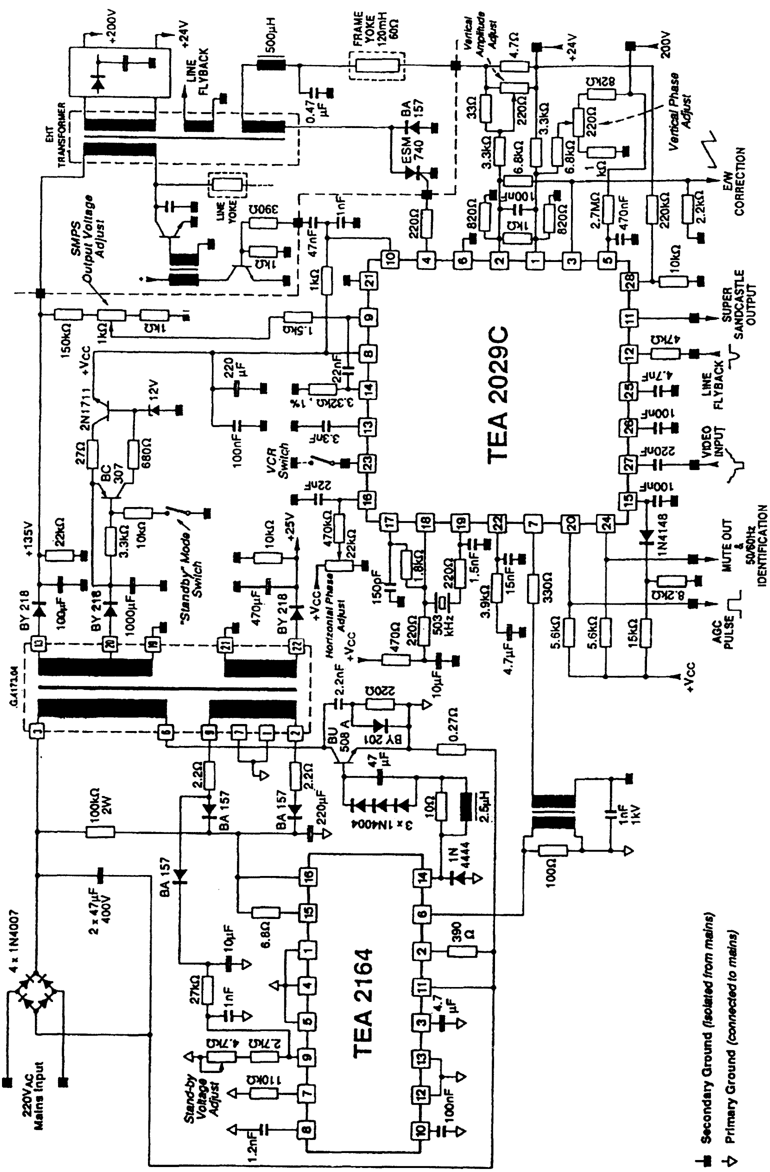


E88 TEA2029C-04

APPLICATION CIRCUIT (WITH B CLASS FRAME POWER)



COMPLETE APPLICATION WITH TEA 2164



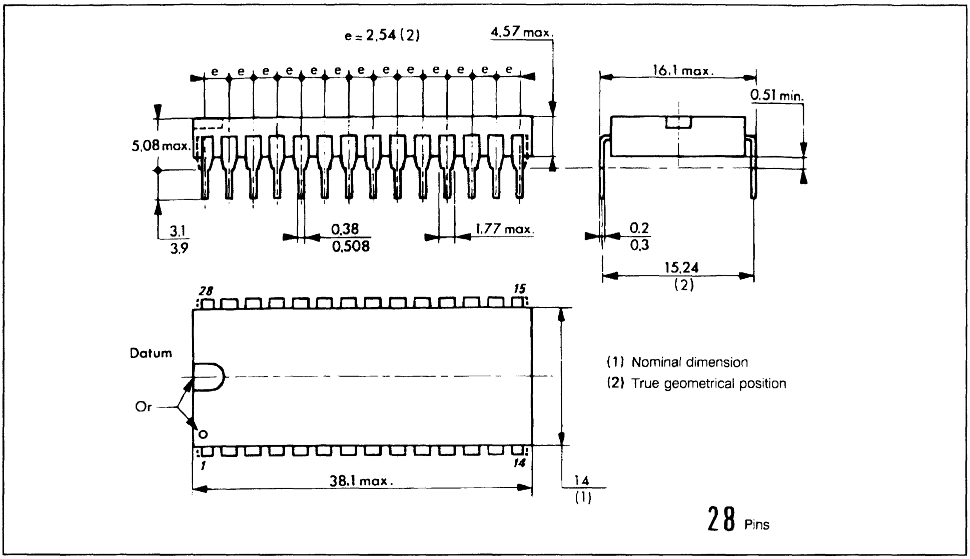
■ Secondary Ground (*isolated from mains*)

∇ Primary Ground (*connected to mains*).

E88 TEA2029C-07

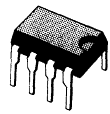
PACKAGE MECHANICAL DATA

28 Pins – Plastic DIP



COLOR TV EAST - WEST CORRECTION

- BUILD IN FRAME PARABOLA FROM EXTERNAL SAW-TOOTH
- PARABOLA CORRECTION ADJUSTMENT
- KEYSTONE CORRECTION ADJUSTMENT
- LINE SIZE ADJUSTMENT
- LINE DYNAMIC CORRECTION POSSIBILITY (beam current)
- D CLASS OUTPUT MODULATOR WITH BUILD IN RECOVERY DIODE
- 50 OR 60Hz OPERATION
- LOW DISSIPATION
- FEW EXTERNAL COMPONENTS



TEA2031A
DIP-8
(Plastic Package)

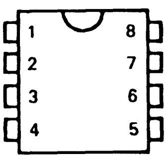
DESCRIPTION

The TEA2031A is intended to ensure frame rate modulated parabolic and keystone corrections to the horizontal deflection circuitry of 110 °color TV sets.

The linear frame saw-tooth is applied to appropriate circuitry from which a corresponding parabolic waveforms is obtained. This waveform is then fed to a comparator together with the linear line saw-tooth for comparison. Comparator's output drives the output power stage which is capable of sinking the external coil currents of up to 0.5A.

An internal recovery diode feeds back to the power supply the coil fly-back current pulses of as high as 0.5A.

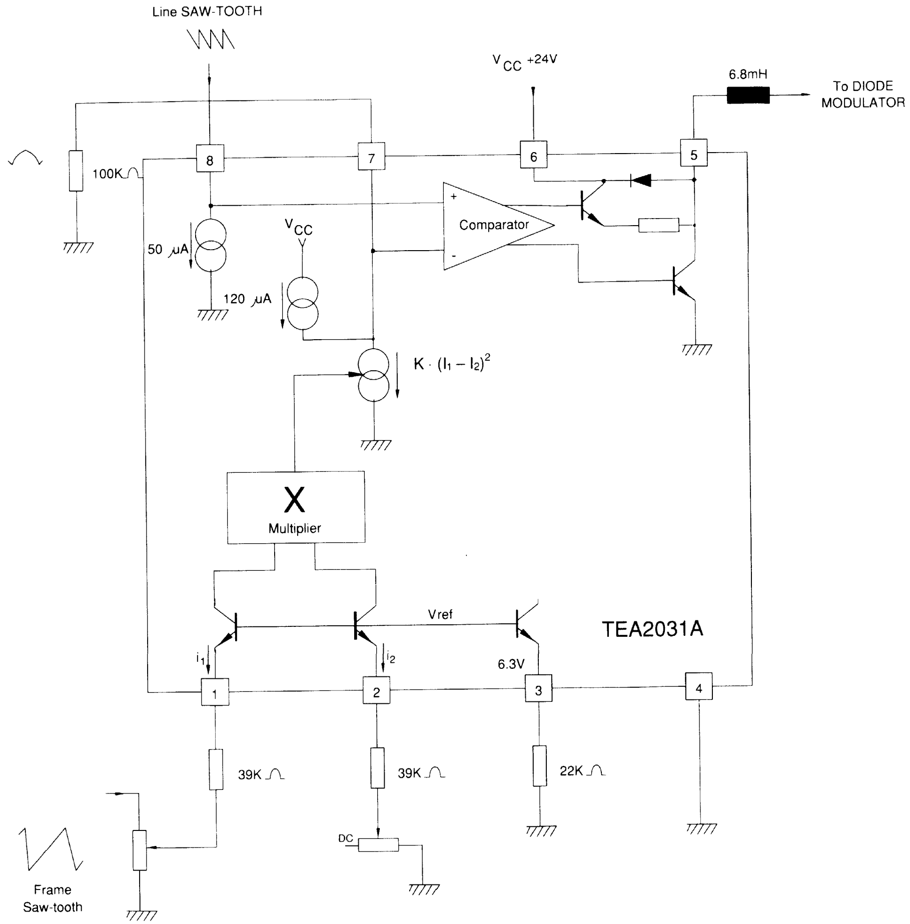
PIN CONNECTIONS



1 - Multiplier Input 1
2 - Multiplier Input 2 } 1 and 2 can be inverted
3 - Current Reference
4 - Ground
5 - Output
6 - VCC Power Supply
7 - Multiplier Output and Comparator Input 1
8 - Comparator Input 2

E88TEA2031A-02

BLOCK DIAGRAM



GENERAL DESCRIPTION

The TEA2031A is intended to provide to 110° color TV sets a parabolic and keystone frame rate modulated correction in addition to the main horizontal scanning.

A stable 6.3V internal reference provides current and voltage references to the whole IC.

Pins 1 and 2 are two symmetrical inputs of an on-chip multiplier circuit and are internally held at 6.3V reference potential level. Current inputs to these pins are drawn from external sources via appropriate resistors. The frame saw-tooth waveform which has a peak-to-peak value of around 3 volts and a mean value of about 2.5 volts, supplies the required current via a series resistor to pin 1. Likewise, the current to pin 2 is drawn through a series resistor from an external dc voltage source. These series resistors can have values of around 40kΩ resulting in input currents of approximately 0.1mA ± modulation current.

Pin 7 should be loaded to ground through a 100kΩ resistor which as a result will produce a parabola of 5 volts peak-to-peak at pin 7. This parabola is symmetrical if the DC current flowing into pin 2 is equal to the mean input current of pin 1. Otherwise, the parabola becomes dissymmetrical and produces a keystone effect correction.

The line saw-tooth at pin 8 is obtained by feeding the line fly-back voltage through an integrator network formed by a diode and a grounded capacitor (see typical application diagram). The DC component of the line saw-tooth is compensated by an internal current sinking source ; so that the mean DC values of line saw-tooth and frame parabola voltages are equal.

Line saw-tooth and frame parabola signals are applied to a comparator whose output is in the form of width modulated pulses. During every pulse duration, the output (pin 5) can sink external coil currents of up to 0.5A associated with diode modulator of the main horizontal scanning circuit.

An internal recovery diode feeds back the fly-back energy of the coil to the power supply. This diode can carry currents of up to 0.5A.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{6-4}	Supply Voltage	35	V
I_{5-4}	Output Sink Current	0.5	A
I_{5-6}	Diode Output Current	0.5	A
I_1 and I_2	Input Current	– 0.5	mA
	Storage Temperature Range	– 20 to 150	°C
I_{5-4}	Non Repetitive Peak Current on Output Transistor	1.5	A
I_{5-6}	Non Repetitive Peak Current on Output Diode	1.5	A

THERMAL DATA T_{amb} = + 50°C

$R_{TH\ (j-a)}$	Thermal Resistance Max Total Dissipated Power	80 0.8	°C/W W

ELECTRICAL OPERATING CHARACTERISTICS

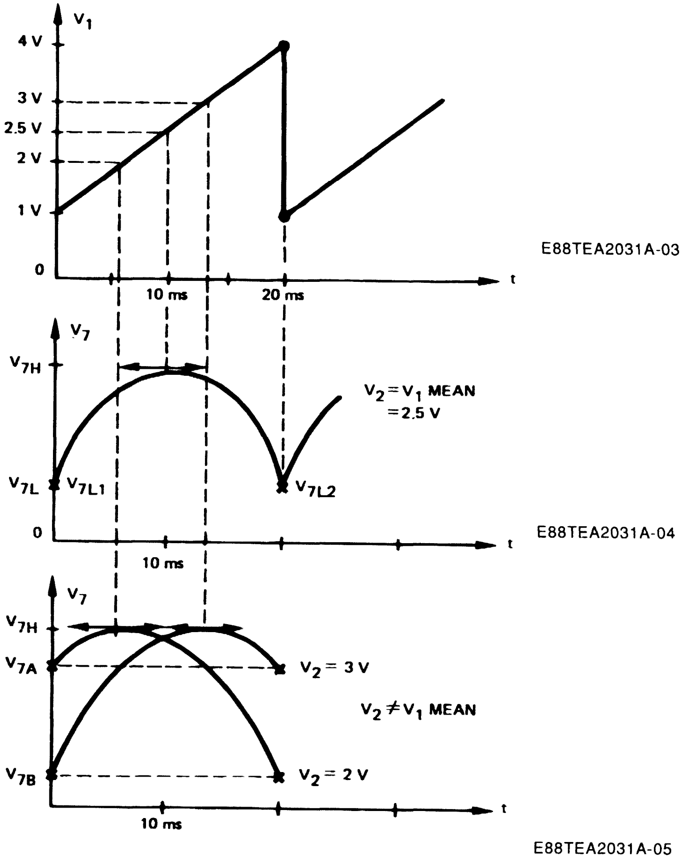
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{6-4}	Supply Voltage	16	24	35	V
I_6	Supply Current ($R_{(3-4)}$ = 22kΩ ; I_{OUT} = 0)		4	6	mA
	No Load Consumption ($R_{(3-4)}$ = 22kΩ ; I_{OUT} = 0 ; $V_{(6-4)}$ = 24V)		100	150	mW
V_{3-4}	V Reference ($R_{(3-4)}$ = 22kΩ)	5.9	6.3	6.7	V
I_1 mean	Frame Saw-tooth Input DC Mean Current R_1 = 39kΩ at 2.5V Mean - saw-tooth Voltage		0.1		mA
I_{1pp}	Frame Saw-tooth Input Peak-to-peak Current R_1 = 39kΩ at 2.5V Mean - saw-tooth Voltage		70		µA
I_2	Keystone Correction Input DC Current If I_1 Mean = I_2 : No Keystone Effect. R_2 = 39kΩ at 2.5V DC ref.		0.1		mA
ΔI_2	Keystone Correction Input DC Current for Maximum Keystone Effect		± 12.5		µA
V_{7H}	Top Parabola Voltage (2V < V_1 = V_2 < 3V)	10		15	V
ΔV_{7H}	Top parabola temperature drift			0.5	mV/°C
Symmetrical parabola for no keystone effect (see figure 2)					
$V_{7H} - V_{7L}$	Parabola Amplitude (V_2 = 2.5V ; V_1 mean = 2.5V, V_{1pp} = 3V)	3.5	5.2	6	V
$\Delta(V_{7H} - V_{7L})$	Parabola amplitude drift versus temperature			1	mV/°C
$\frac{V_{7H} - V_{7L1}}{V_{7H} - V_{7L2}}$	Symmetry	0.8	1	1.2	
Maximum dissymmetrical parabola for maximum keystone effect (see figure 3)					
$V_{7H} - V_{7B}$	Parabola Amplitude (V_2 = 2V or V_2 = 3V ; V_1 mean = 2.5V ; V_{1pp} = 3V)	5.3	8.5	9.2	V
$\frac{V_{7H} - V_{7B}}{V_{7H} - V_{7A}}$	Parabola Amplitude Ratio	2.6		4.1	
Differential Amplifier					
	Input 8 Sink Current Source	0.04		0.06	mA
$\Delta I_8 = F(\theta)$	Input 8 Current Drift Versus Temperature			0.1	%/°C
	Transfer Characteristics (pins 7-8) (F = 1MHz)	5		500	mA/mV
	Input Noise (pins 7-8)			50	µV
	Rise and Fall Time (Iouput = 250mA)	1			A/µs
V_{5-4}	Output Saturation Voltage to Ground (I_5 = 0.5 A)			1.2	V
V_{6-5}	Output Saturation Voltage to V_{CC} (I_5 = 0.1A)			2	V
V_{5-6}	Output Diode Direct Voltage (I_5 = + 0.5A)			1.2	V

PARABOLA OUTPUT

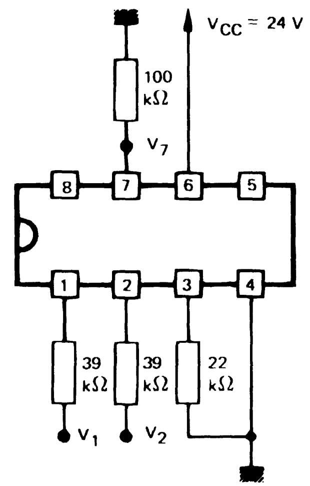
FIGURE 1

FIGURE 2

FIGURE 3

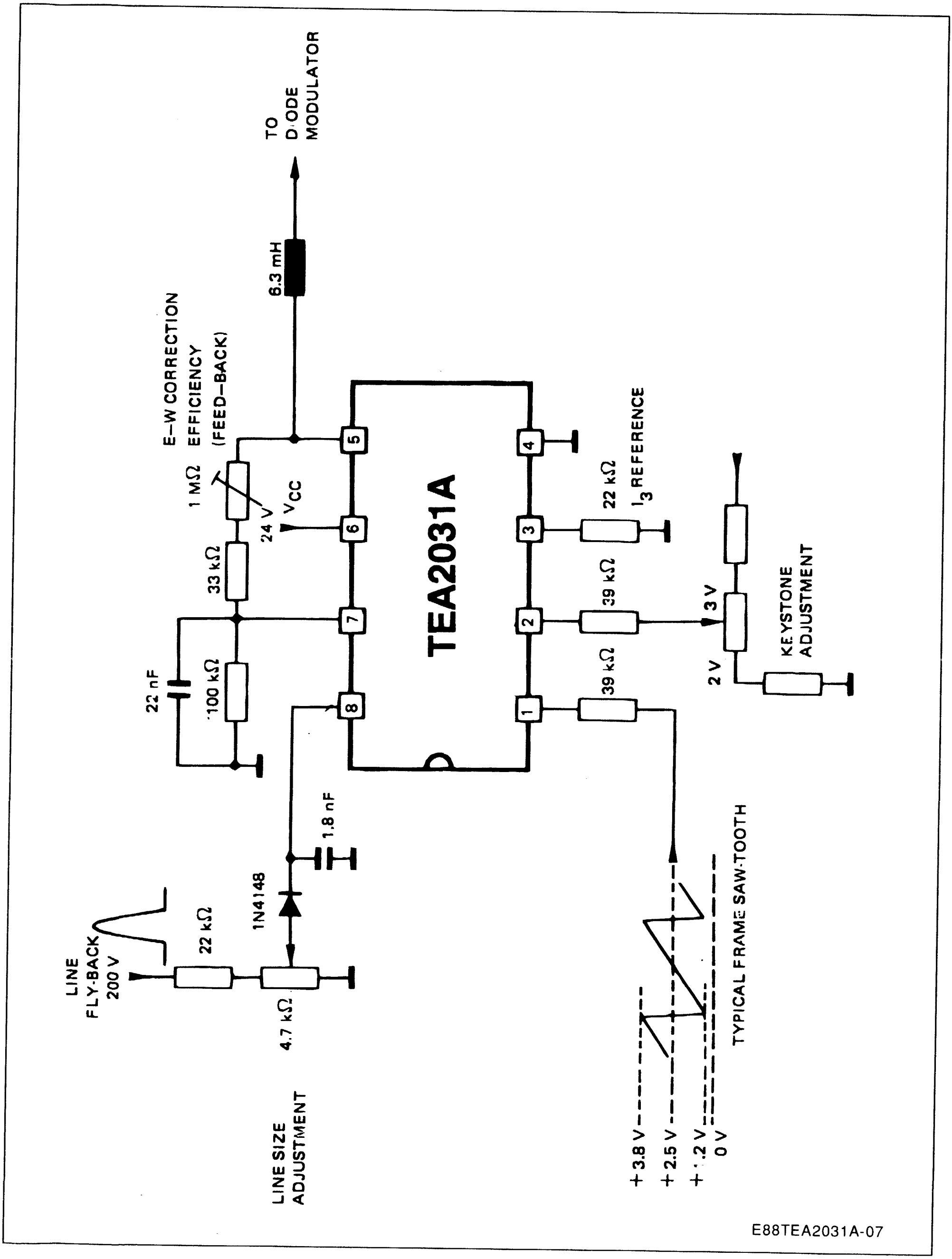


PARABOLA TEST DIAGRAM



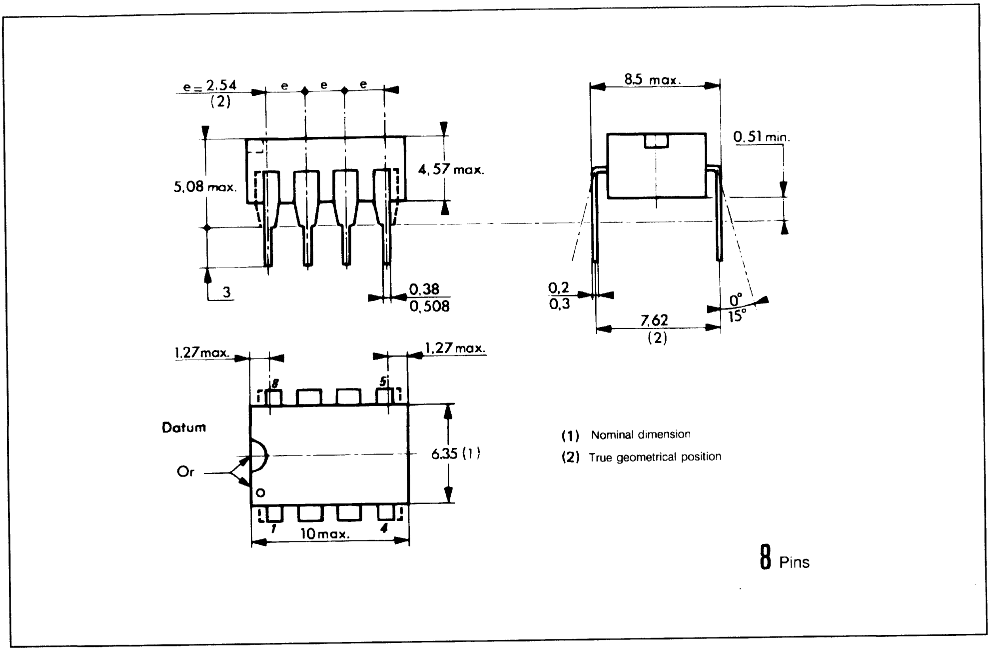
E88TEA2031A-06

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP

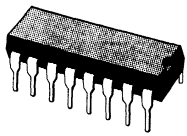


SGS-THOMSON MICROELECTRONICS

TEA2037A

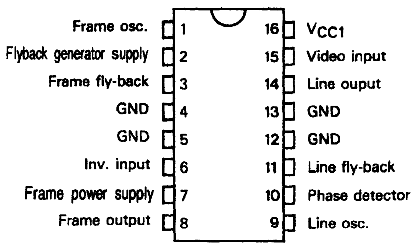
HORIZONTAL AND VERTICAL DEFLECTION MONITOR

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VERY FEW EXTERNAL COMPONENT
- VERY LOW COST POWER PACKAGE



TEA2037A
BATWING DIP 16
(Plastic Package)

PIN CONNECTIONS

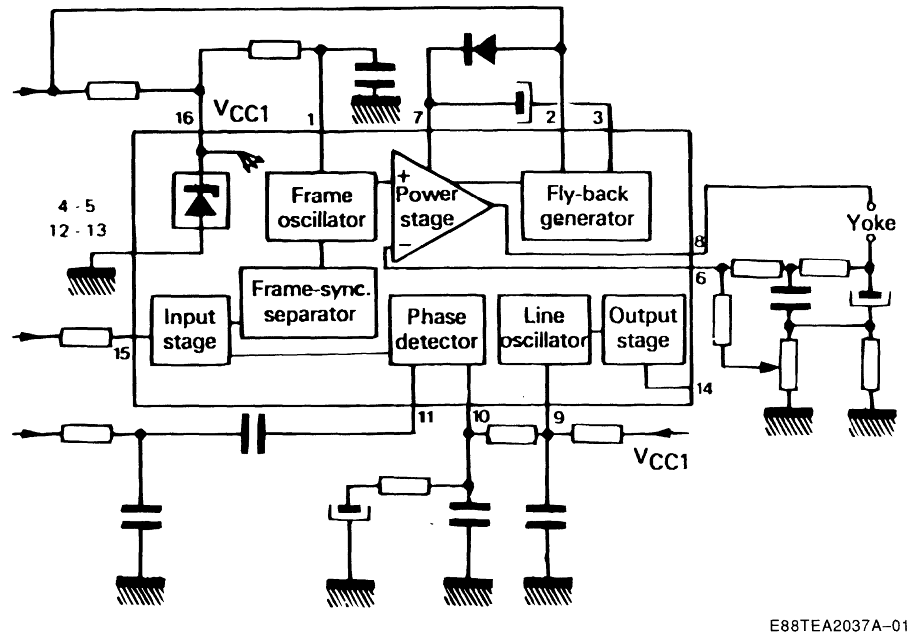


E88TEA2037A-02

DESCRIPTION

The TEA2037A is an horizontal and vertical deflection circuit. It uses the same concept as the TEA2017 but optimised for small screens, for a very low cost solution.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VCC1	Supply Voltage	30	V
V2	Flyback Generator Supply Voltage	35	V
V7	Frame Power Supply Voltage	60	V
I8nr	Frame Output Current (non repetitive)	± 1.5	A
I8	Frame Output Current (continuous)	± 1	A
V14	Line Output Voltage (external)	60	V
Ip14	Line Output Peak Current	0.8	A
IC14	Line Output Continuous Current	0.4	A
Tstg	Storage Temperature	–40, + 150	°C
Tj	Max Operating Junction Temperature	150	°C

THERMAL DATA

Rth (j-c)	Max Junction-case Thermal Resistance	15	°C/W
Rth (j-a)	Typical Junction-ambient Thermal Resistance (soldered on a 35μm thick 45cm2 PC board copper aera)	45	°C/W
T_J	Max Recommended Junction Temperature	120	°C

ELECTRICAL CHARACTERISTICS
(T_{amb} = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply (shunt regulator) Pin 16				
ICC1	Supply Current	10		20	mA
VCC1	Supply Voltage (ICC1 = 15mA)	9	9.8	10.5	V
ΔVCC1	Voltage Variation (ICC1 : 10mA → 20mA)	– 280	50	+ 280	mV
LPS	Starting Threshold for Line Output Pulses			5	V
	Video Input Pin 15				
V15	Reference Voltage (I15 = – 1μA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (when synchronized with TTL signal)	50			μs
	Line Oscillator Pin 9				
LT9	Low Threshold Voltage	2.8	3.2	3.6	V
HT9	High Threshold Voltage	5.4	6.6	7.8	V
BI9	Bias Current		100		nA
DR9	Discharge Impedance	1.0	1.4	1.8	KΩ
FLP1	Free Running Line Period R = 34.9KΩ Tied to VCC1 C = 2.2nF Tied to Ground	62	64	66	μs
FLP2	Free Running Line Period R = 13.7KΩ C = 2.2nF		27		μs
OT9	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application fig.8)		2		Hz/°C
	Line Output Pin 14				
LV14	Saturation Voltage (I14 = 200mA)		1.1	1.6	V
OPW	Output Pulse Width (line period = 64μs)	20	22	24	μs
	Line Flyback Input Pin 11				
V11	Bias Voltage	1.8	2.4	3.2	V
Z11	Input Impedance	4.5	5.8	8	KΩ
	Phase Detector Pin 10				
I10	Output Current During Synchro Pulse	250	450	800	μA
RI10	Current Ratio (positive/negative)	0.95	1	1.05	
LI10	Leakage Current	– 2		+ 2	μA
CV10	Control Range Voltage	2.60		7.10	V

ELECTRICAL CHARACTERISTICS (continued)

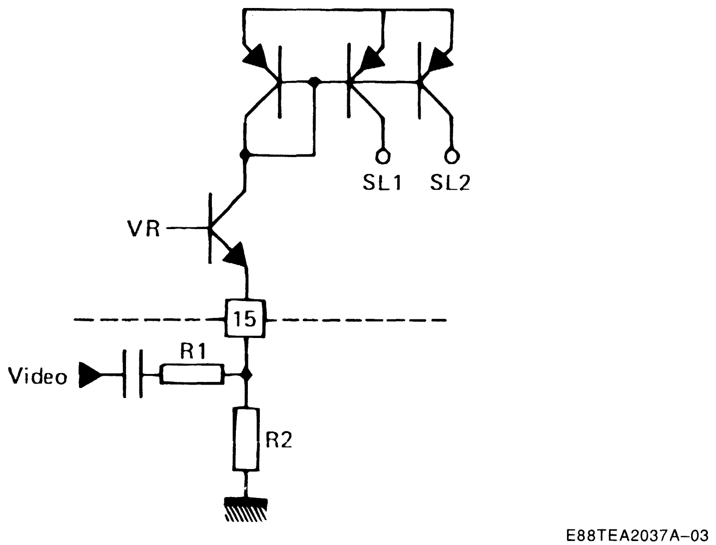
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Frame Oscillator Pin 1				
LT1	Low Threshold Voltage	1.6	2.0	2.3	V
HT1	High Threshold Voltage	2.6	3.1	3.6	V
BI1	Bias Current		30		nA
DR1	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period R = 845KΩ Tied to VCC1 C = 180nF Tied to Ground	20.5	23	25	ms
MFP	Minimum Frame Period (I15 = – 100μA) With the Same RC		12.8		ms
FFP2	Free Running Frame Period R = 408KΩ C = 220nF		14.3		ms
FPR	Frame Period Ratio = $\frac{FFP}{MFP}$	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		– 0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Freq. Drift with Temperature (see application fig.8)		4.10^{-3}		Hz/°C
	Frame Power Supply Pin 7				
V7	Operating Voltage (with flyback Generator)	10		58	V
I7	Supply Current (V7 = 30V)			22	mA
	Flyback Generator Supply Pin 2				
V2	Operating Voltage	10		30	V
	Frame Output Pin 8				
	Saturation Voltage to Ground (V7 = 30V)				
LV8A	I8 = 0.1A		0.06	0.6	V
LV8B	I8 = 1A		0.37	1	V
	Saturation Voltage to V7 (V7 = 30V)				
HV8A	I8 = – 0.1A		1.3	1.6	V
HV8B	I8 = – 1A		1.7	2.4	V
	Saturation Voltage to V7 in Flyback Mode (V8 > V7)				
FV8A	I8 = 0.1A		1.6	2.1	V
FV8B	I8 = 1A		2.5	4.5	V
	Flyback Generator Pin 2 and Pin 3				
	* Flyback Transistor on (output = high state) V2 = 30V				
F2DA	V3/2 with $I_{3 \rightarrow 2}$ = 0.1A		1.5	2.1	V
F2DB	$I_{3 \rightarrow 2}$ = 1A		3.0	4.5	V
FSVA	V2/3 with $I_{2 \rightarrow 3}$ = 0.1A		0.8	1.1	V
FSVB	$I_{2 \rightarrow 3}$ = 1A		2.2	4.5	V
	* Flyback Transistor off (output = V7 – 8V) V7 = V2 = 30V				
FCI	Leakage Current Pin 2			170	μA

The TEA2037A performs all the video and power functions required to provide signals for the direct drive of the line darlington and frame yoke.

It contains :

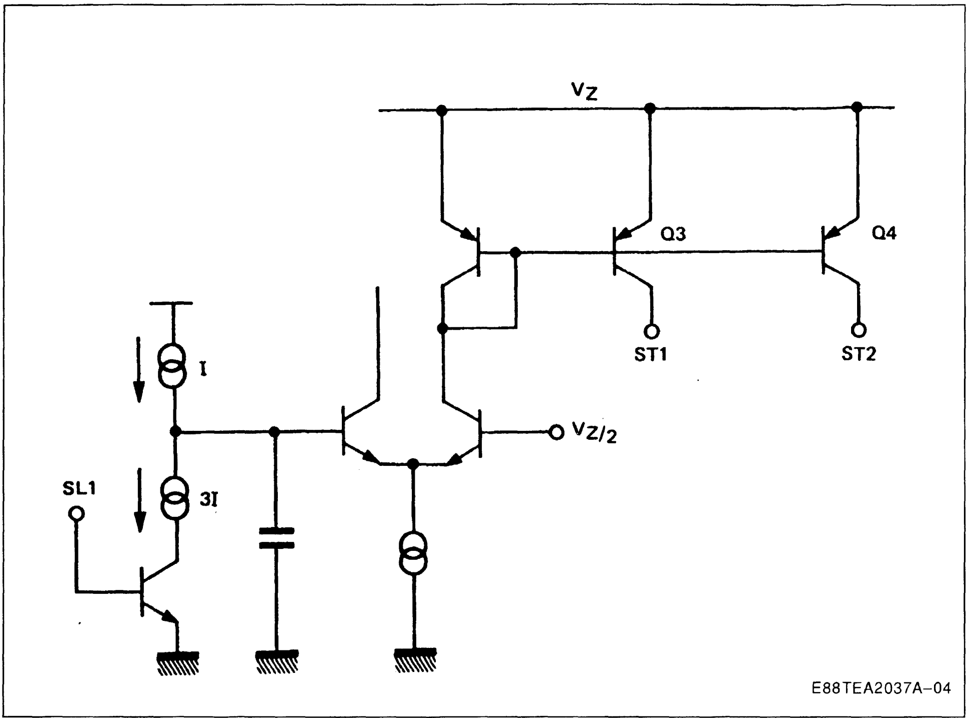
- A shunt regulator
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator

Figure 1 : Synchronization Separator Circuit.



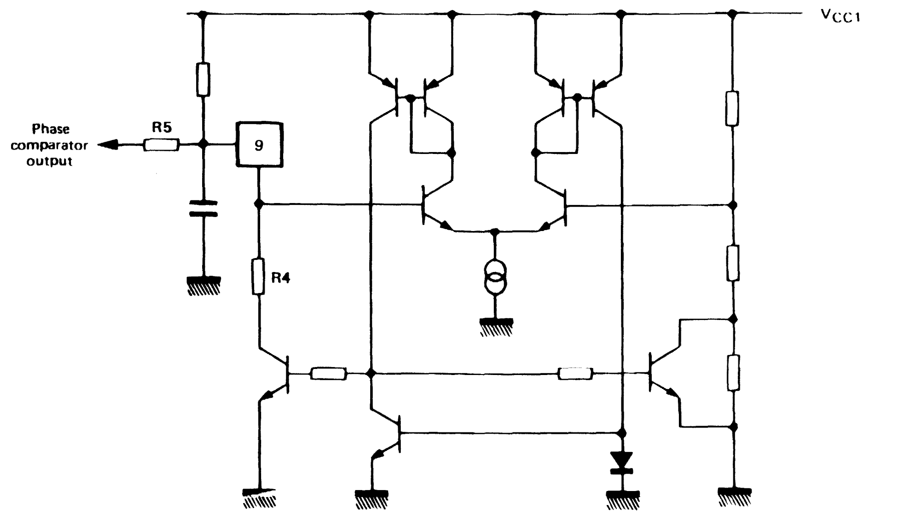
The slice level of sync-separation is fixed by value of the external resistors R_1 and R_2. V_R is an internally fixed voltage.

Figure 2 : Frame Separator.



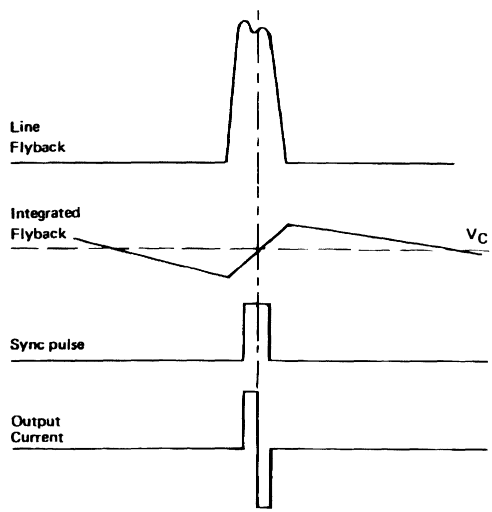
The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q3 and Q4 provide current for the other parts of the circuit.

Figure 3 : Line Oscillator.



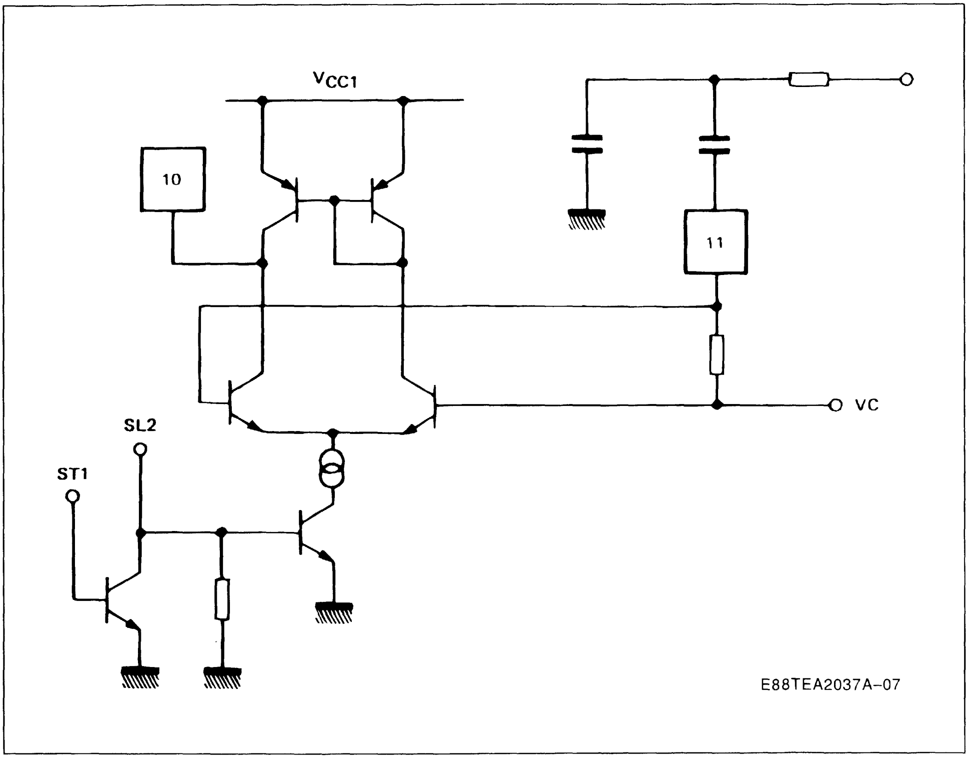
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4 : Phase Comparator.



The sync-pulse drives the current in the comparator. The line flyback integrated by the external network gives on pin 11 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 11 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

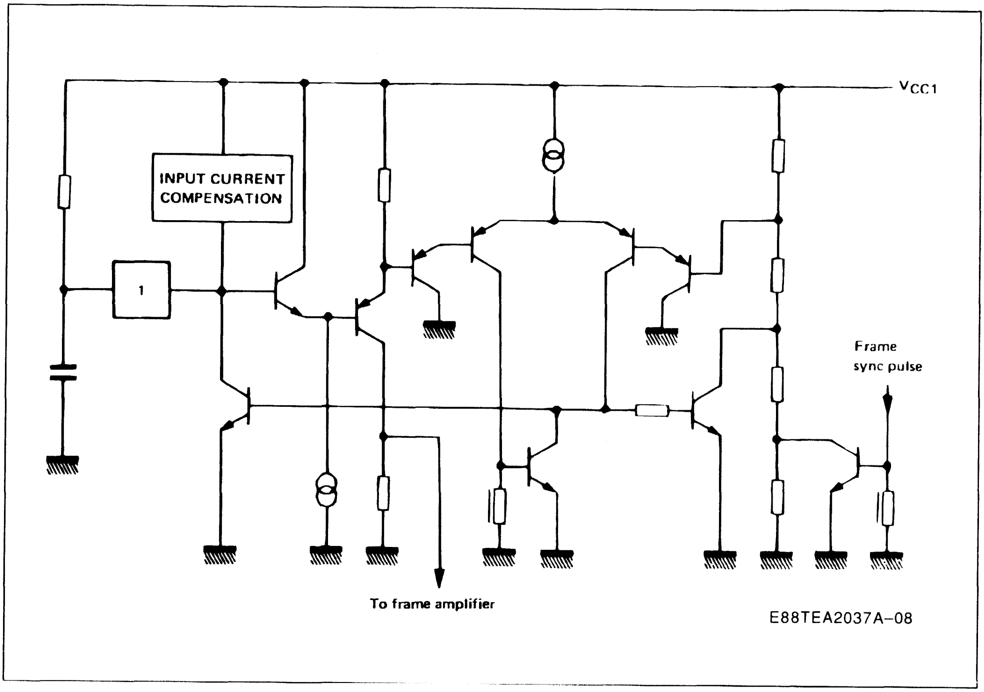
Figure 5.



LINE OUTPUT (PIN 14)

It is an open collector output which is able to drive pulse current of 800mA for a rapid discharging of the darlington base. The output pulse time is 22µs for a 64µs period.

Figure 6 : Frame Oscillator.



The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

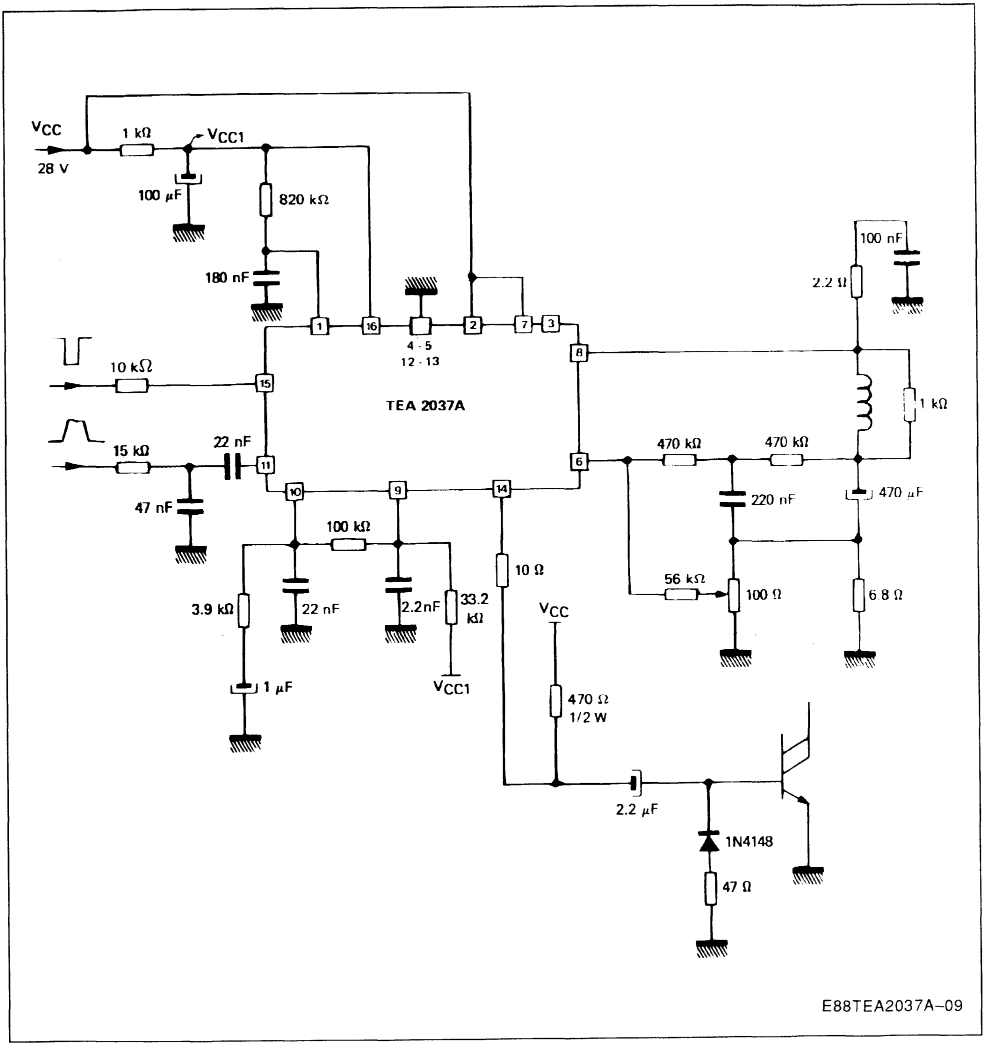
FRAME OUTPUT AMPLIFIER

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected ; it contains also a thermal protection.

TYPICAL APPLICATION FOR DISPLAY UNITS

(without flyback generator and with TTL sync-pulse drive ; yoke : 72mH, 40Ω)

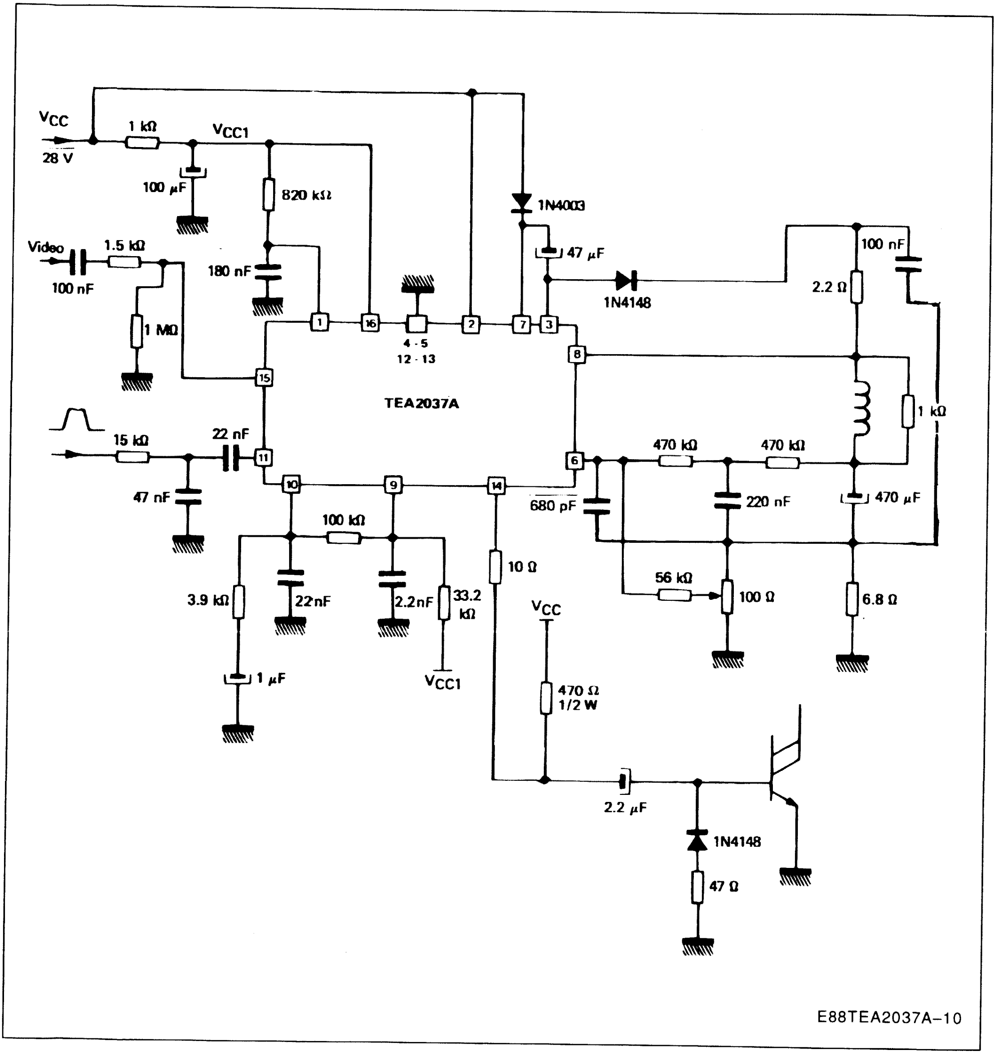
Figure 7.



TYPICAL APPLICATION FOR DISPLAY UNITS

(with flyback generator and video drive ; yoke : 72mH, 40Ω)

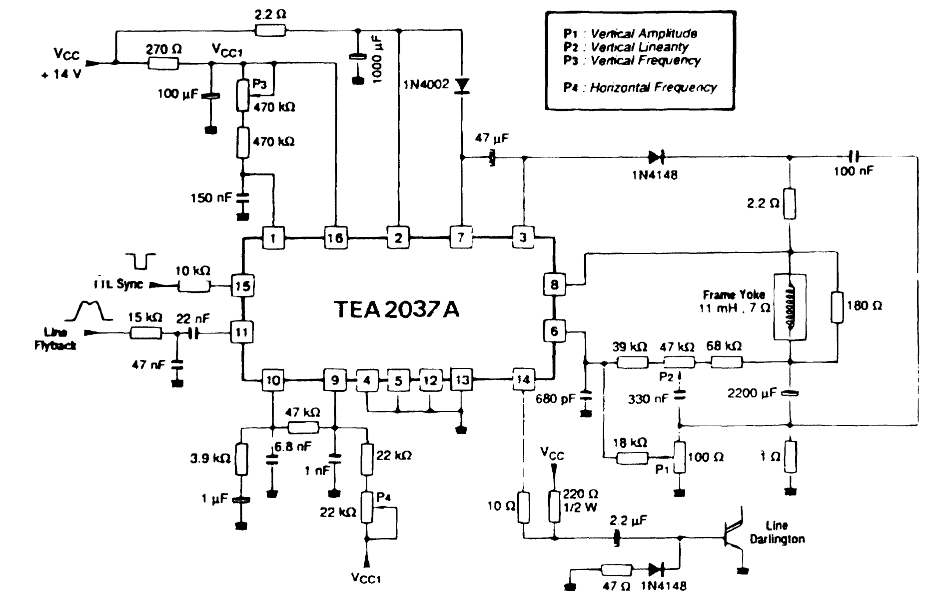
Figure 8.



TYPICAL APPLICATION FOR HIGH FREQUENCY MONITOR

CHARACTERISTICS

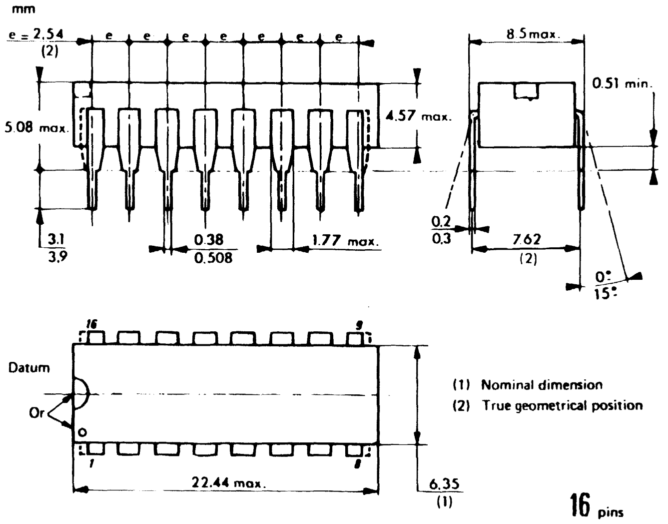
- Screen : 14" Colour
- Frame deflection yoke : 11mH, 7Ω, 750mA peak–to–peak
- V_{CC} = + 14V with flyback generator
- Frame flyback time : 0.6ms
- Vertical frequency : 72Hz
- Vertical free–running period : 16ms (adjustable)
- Horizontal frequency : 35kHz (adjustable)
- Line flyback time : 5.5µs
- Capture range : ± 5µs (@ sync pulse = 4.7µs)
- Input signal : negative TTL sync (line + frame)
- Dissipated power : 1.4W (heatsink required)
- Adjustments :
  - Vertical amplitude
  - Vertical Linearity
  - Vertical frequency
  - Horizontal frequency



E88TEA2037A–11

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP



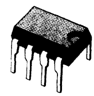
SGS-THOMSON
MICROELECTRONICS

TEA2114

VIDEO SWITCH

ADVANCE DATA

- 2 VIDEO OUTPUTS WHICH CAN DRIVE 150Ω LOAD
- DYNAMIC OUTPUT AMPLITUDE 2 VPP ON EACH OUTPUT
- BANDWIDTH 20MHz
- FULLY PROTECTION AGAINST ESD



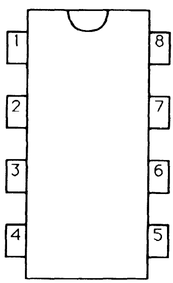
DIP8
(Plastic Package)

ORDER CODE : TEA2114

DESCRIPTION

This integrated circuit provides general video switches. It is particularly intended for switching between the peri TV plug and video section of the sets. Its electrical performances make it suitable for wide bandwidth applications (teletext, D2MAC).

PIN CONNECTIONS

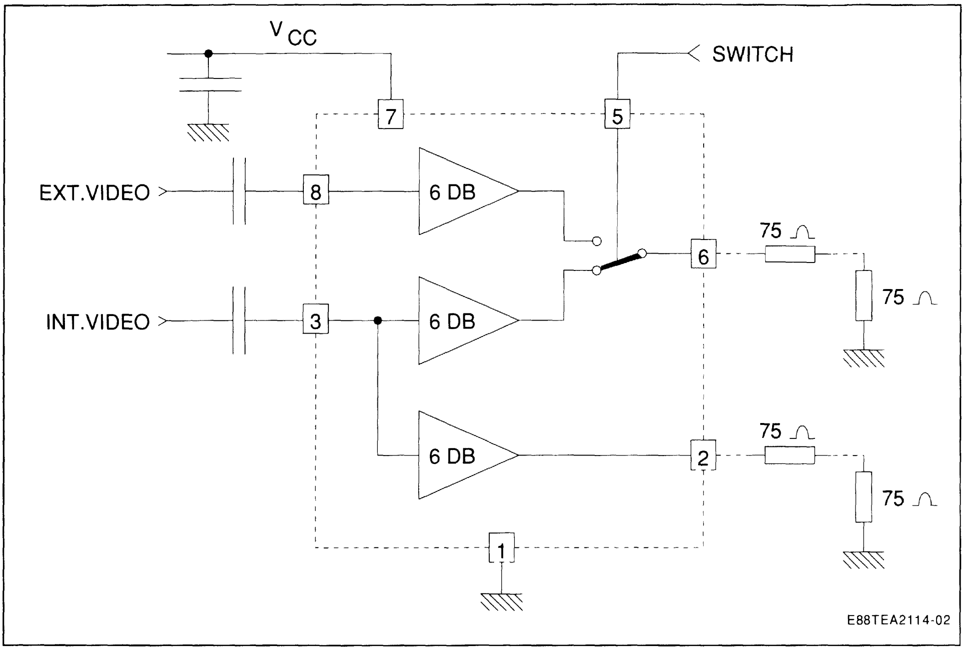


1 - Ground
2 - unswitched video output
3 - Internal video input
4 - Not to be used
5 - Switching input
6 - Switched video output
7 - Supply voltage
8 - External video input

E88TEA2114-01

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
T_j	Junction Temperature	– 40 to + 150	°C
T_{stg}	Storage Temperature	– 40 to + 150	°C

ELECTRICAL CHARACTERISTICS

T_{AMB} = 25°C ; V_{CC} = 8V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	6.5		14.5	V
I_{CC}	Supply Current (no load pin 2 and pin 6)		8	15	mA
I_{CC}	Supply Current (with load 150Ω on pin 2 and pin 6, no video on inputs)		25	35	mA

INPUTS (pin 3 and pin 8)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Video Input Swing	1.5	1.8		V_{PP}
V_{DCIN}	DC Level Input		1.3		V
I_{IN}	Input Bias Current (V_{DC} = V_{DCIN} + 1.5 V_{DC})		3		µA

ELECTRICAL CHARACTERISTICS (continued)

T_{amb} = 25°C ; V_{CC} = 8V (unless otherwise specified)

SWITCHED OUTPUT (pin 6)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Video Output Swing	3	3.6		V_{PP}
	DC Level Output		1.3		V
	Video Gain (pin 6 versus pin 3 or pin 8, measured at 100KHZ, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (pin 6 versus pin 3 or pin 8, 1VPP input signal, load 150Ω)	15	20		MHZ
	Output Impedance (measured pin 6)		15		Ω

EXTERNAL OUTPUT (pin 2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Video Output Swing	3	3.6		V_{PP}
	DC Level Output		1.3		V
	Video Gain (pin 2 versus pin 3, measured at 100KHZ, 1 V_{PP} input signal)	5.5	6	6.5	dB
	Video Bandwidth (pin 2 versus pin 3, 1VPP input signal, load 150Ω)	15	20		MHZ
	Output Impedance (measured pin 2)		15		Ω

SWITCHING INPUT (pin 5)

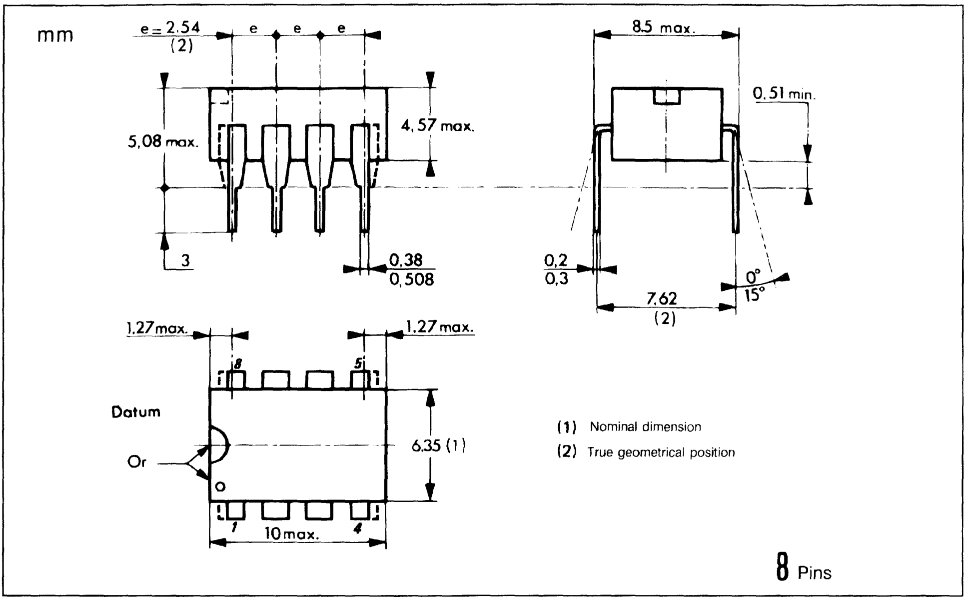
Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output Current Selection Pin			5	μA
	Threshold Voltage		4		V
	Max DC Level			V_{CC}	V

OTHER DYNAMIC FEATURES

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Supply Voltage Rejection (measured pin 2 or pin 6 at 1KHZ)		40		dB
	Crosstalk (between any input, measured at 1MHZ)		– 50		dB

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



SGS-THOMSON
MICROELECTRONICS

TEA2128

COLOR TV SCANNING AND POWER SUPPLY PROCESSOR

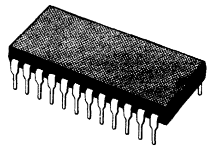
PRODUCT PREVIEW

DEFLECTION :

- DEFLECTION 500K RESONATOR OSCILLATOR
- NO LINE AND FRAME OSCILLATOR ADJUSTMENT
- DUAL PLL FOR LINE DEFLECTION
- SUPER SANDCASTLE OUTPUT
- DIGITAL VIDEO IDENTIFICATION CIRCUIT
- AUTOMATIC 50Hz/60Hz STANDARD IDENTIFICATION
- EXCELLENT INTERLACING CONTROL

SMPS CONTROL :

- ERROR AMPLIFIER AND PHASE MODULATOR
- SYNCHRONIZATION WITH HORIZONTAL DEFLECTION
- SECURITY CIRCUIT AND START-UP PROCESSOR
- MASTER/SLAVE CONCEPT FACILITIES

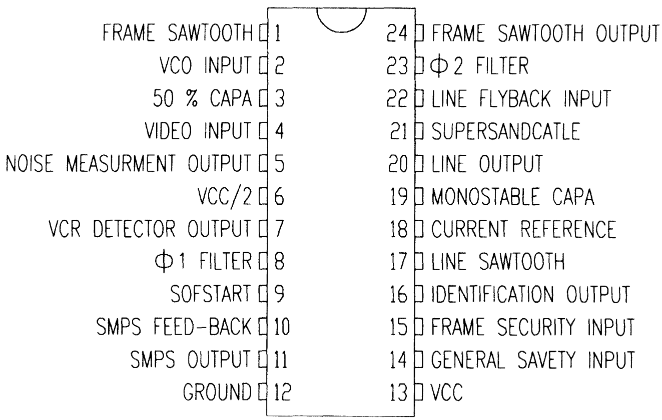


TEA2128
DIP 24S

DESCRIPTION

The TEA2128 is a complete (horizontal and vertical) deflection processor with secondary to primary SMPS control for color TV sets.

PIN CONNECTIONS



E88TEA2128-01

SGS-THOMSON MICROELECTRONICS

TEA2164

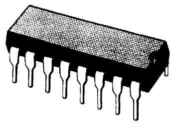
SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

- POSITIVE AND NEGATIVE OUTPUT CURRENT UP TO 1.2A AND – 1.7A
- A TWO LEVEL COLLECTOR CURRENT LIMITATION
- COMPLETE TURN OFF AFTER LONG DURATION OVERLOADS
- UNDER AND OVER VOLTAGE LOCK-OUT
- SOFT START BY PROGRESSIVE CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- BURST MODE OPERATION UNDER STAND-BY CONDITIONS

DESCRIPTION

In a master slave architecture, the TEA2164 control IC achieves the slave function. Primarily designed for TV receivers and monitors applications, this circuit provides an easy synchronization and smart solution for low power stand by operation.
Located at the primary side the TEA2164 Control IC ensures :

- the power supply start-up
- the power supply control under stand-by conditions
- the process of the regulation signals sent by the master circuit located at the secondary side
- direct base drive of the bipolar switching transistor
- the protection of the transistor and the power supply under abnormal conditions.



TEA2164
BATWING DIP 16
(Plastic Package)

PIN CONNECTIONS

Function	Pin	Pin	Function
Ground	1	16	V_{CC} Supply Voltage
Icopy	2	15	Output Stage Positive Supply Voltage
Long Duration Overload Capacitor	3	14	Output (base current)
Substrate	4	13	Substrate
Substrate	5	12	Substrate
Pulse Input	6	11	I_{cMax} Sense
Oscillator Timing Resistor	7	10	Low Frequency Oscillator Capacitor
Oscillator Timing Capacitor	8	9	Feedback Input is Burst Mode

E89TEA2164-03

BLOCK DIAGRAM

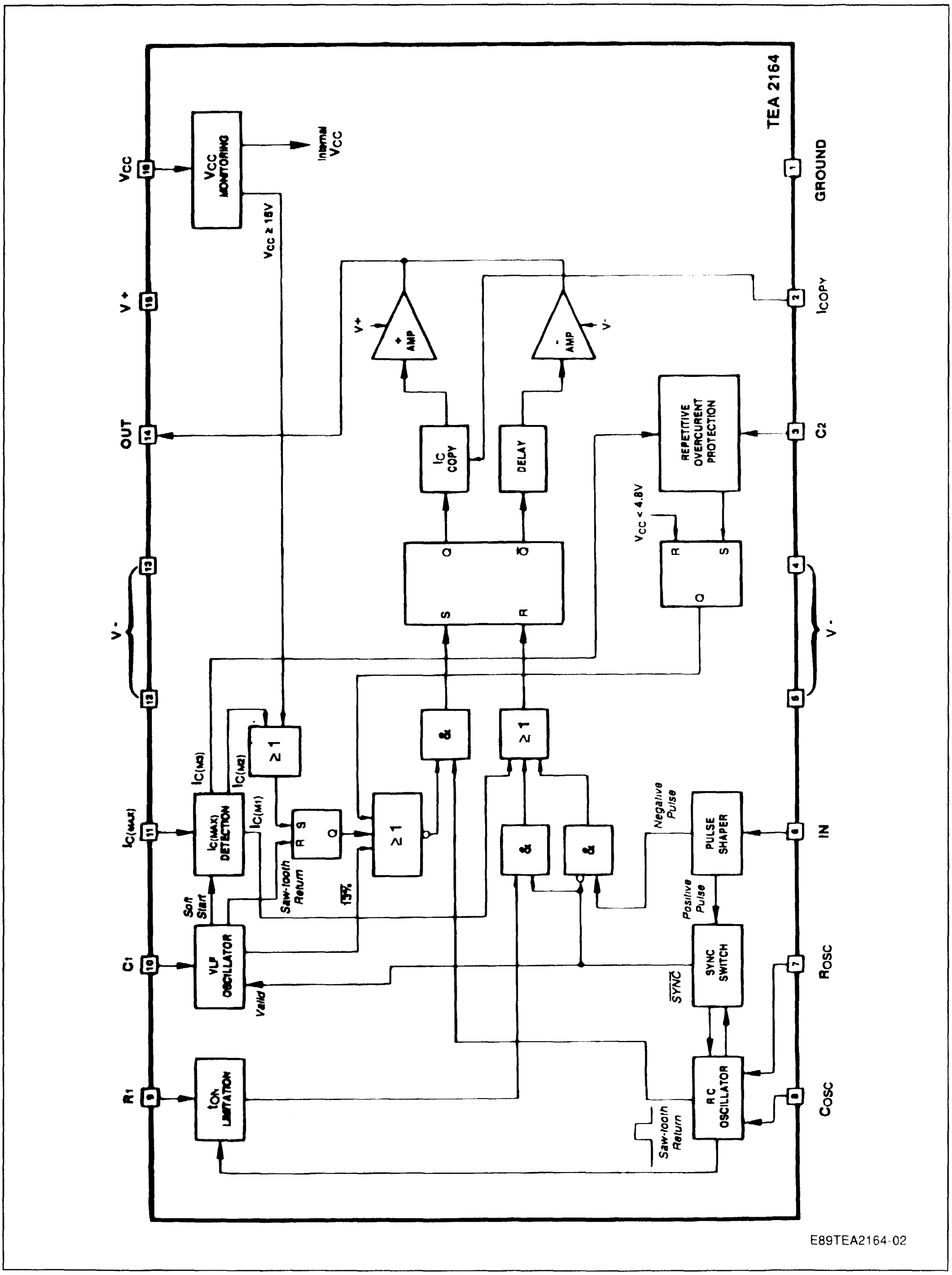
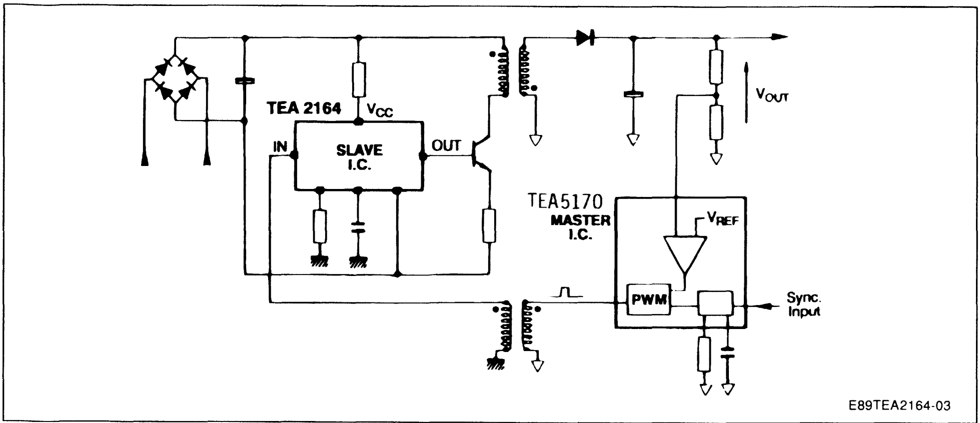


Figure 1 : Simplified Application Diagram.



ABSOLUTE MAXIMUM RATINGS

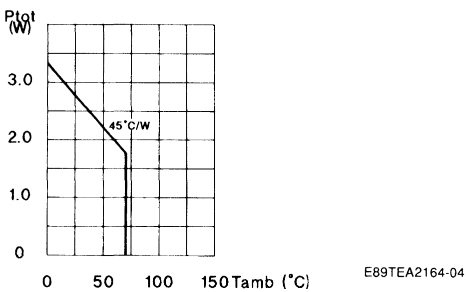
Symbol	Parameter	Value	Unit
V_{CC}	Positive Power Supply V16-V1	18	V
V+	Positive Power Supply of the Output Stage V15-V1	18	V
V–	Negative Power Supply V4, 5, 12, 13-V1	– 5	V
V_{CC} - V– V+ - V–	Total Power Supply V16-V4, 5, 12, 13 or V15-V4, 5, 12, 13	20	V
I_{out+}	Positive Output Current	1.5	A
I_{out-}	Negative Output Current	2	A
T_j	Operating Junction Temperature	150	°C
T_{stag}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

$R_{th(j-c)}$	Junction Case Thermal Resistance	11	°C/W
$R_{th(j-a)}$*	Junction Ambiant Thermal Resistance	45	°C/ W

* Soldered on a 35µm thick 40 cm^3 PC board copper area.

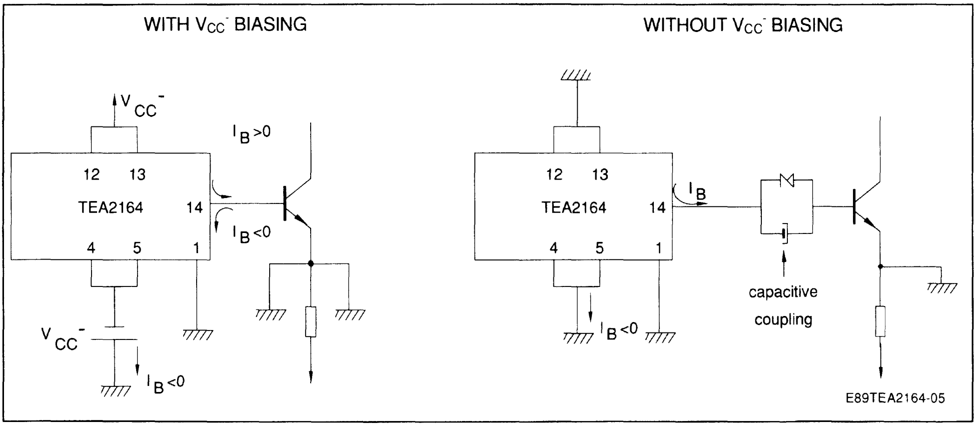
MAXIMUM POWER DISSIPATION



RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Positive Power Supply		10	14	V
$\|V-\|$	Negative Power Supply (absolute value) (note 1)	0		5	V
$V_{CC} - V-$	Total Power Supply			18	V
I_{out+}	Positive Output Current			1.2	A
I_{out-}	Negative Output Current			1.7	A
Fsw	Switching Frequency			50	Khz
Ro	Oscillator Resistor Range	30		150	KΩ
Co	Oscillator Capacitor Range	470		2700	pF
C1	Starting Oscillator Capacitor Range	0.1		4.7	μF
C2	Repetitive Overload Protection Capacitor	1		22	μF
$\|V_{in}\|$	Input Pulses Amplitude (peak) (derivated pulses - time constant = 1 μs)	0.5		1	V
T_{oper}	Operating Ambiant Temperature	– 20		70	°C

Note : 1. The TEA2164 can be used without negative supply voltage, in this case pins 4 - 5 - 12 - 13 must be grounded.



ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, V_{CC-} = 0 V, potentials referenced to ground (pin 1)
(unless otherwise specified)

POWER SUPPLY

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC} (start)	Starting Voltage (V_{CC} increasing)	8	9	9.6	V
V_{CC} (stop)	Stopping Voltage (V_{CC} decreasing)	5	6.2	7.4	V
ΔV_{CC}	Hysteresis (V_{CC} start – V_{CC} stop)	2	2.8	3.5	V
V_{ccmax}	Overvoltage Lock-out	14.8	15.5	16.2	V
$I_{ccstart}$	Starting Positive Supply Voltage	0.5	0.8	1.5	mA

CURRENT LIMITATION AND PROTECTION (pin 11)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$\lvert VCM1 \rvert$	Pulse by Pulse Current Limitation Threshold	720	840	970	mV
$\lvert VCM2 \rvert$	Current Monitoring 2nd Threshold	1200	1350	1500	mV
ΔVCM	$\Delta VCM = \lvert VCM2 \rvert - \lvert VCM1 \rvert$	300	500	700	mV

REPETITIVE OVERCURRENT PROTECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
$\lvert VCM3 \rvert$	Repetitive Overcurrent Threshold (pin 11)	700	900	1100	mV
VCM3-VCM1	(VCM3-VCM1)	– 20	50	130	mV
VC2	Lock-out Voltage on Pin 3	2.4	3	3.6	V
I3 disch	Capacitor C2 Discharge Current (synchronized mode)	10	20	30	µA
I3 ch.	Capacitor C2 Charge Current	50	80	110	µA

OSCILLATOR, MAX DUTY CYCLE, SYNCHRONIZATION

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_o	Oscillator Initial Accuracy RT = 50 K, CT = 1 nF	19.3	21	22.7	µs
$T_{on(max)}$	Maximum Duty Cycle (T_{syn} = 1.05 T_o)	60	70	85	%
$\frac{T_{syn}}{T_o}$	Synchronization Window	1.0		1.5	

OUTPUT STAGE

Symbol	Parameter	Min.	Typ.	Max.	Unit
	I_c Copy Current Gain		1000		
I_{BON}	Base Current Starting Pulse		300		mA

VERY LOW FREQUENCY OSCILLATOR

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Burst Duty Cycle		13		%

1. FIELD OF APPLICATION

The TEA2164 control circuit has been designed primarily for discontinuous mode flyback built with a master-slave architecture, whatever the field of application.

But due to its capability to synchronize the transistor switching-off with an external signal (line flyback) and due to an adapted burst-mode operation for a low power stand-by operation, the TEA2164 offers a smart solution for monitors and TV sets applications.

Power supply main features :
- maximum output power 140W (transistor forced gain : 3.5)
- stand-by mode output power (1W ≤ Psb ≤ 6W ; efficiency > 50%)
- operating frequency up to 50kHz
- power-switch : bipolar transistor

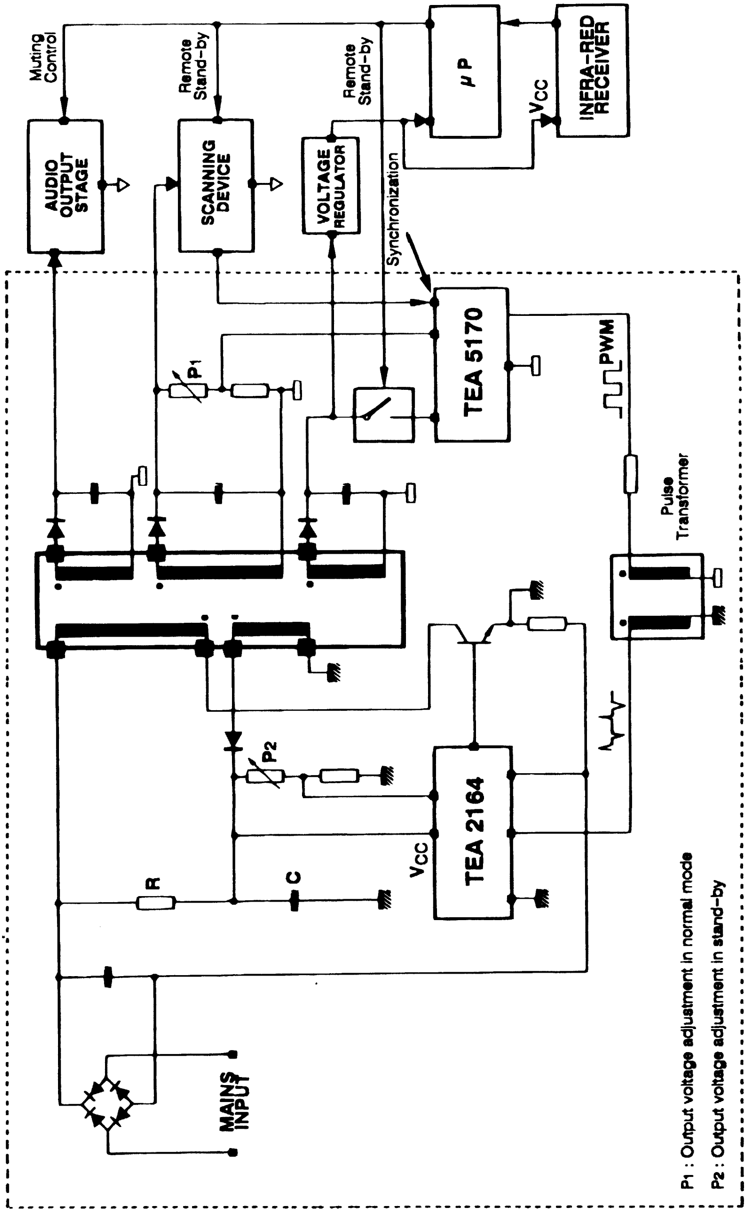
Adapted master-circuit :
Monitor application ——→ TEA5170
Standard TV application ——→ TEA2028B
TEA2029C
TEA5170
Digital TV application ——→ TEA5170

(TEA2028B and TEA2029C are deflection processor with built-in PWM generator).

2. GENERAL DESCRIPTION

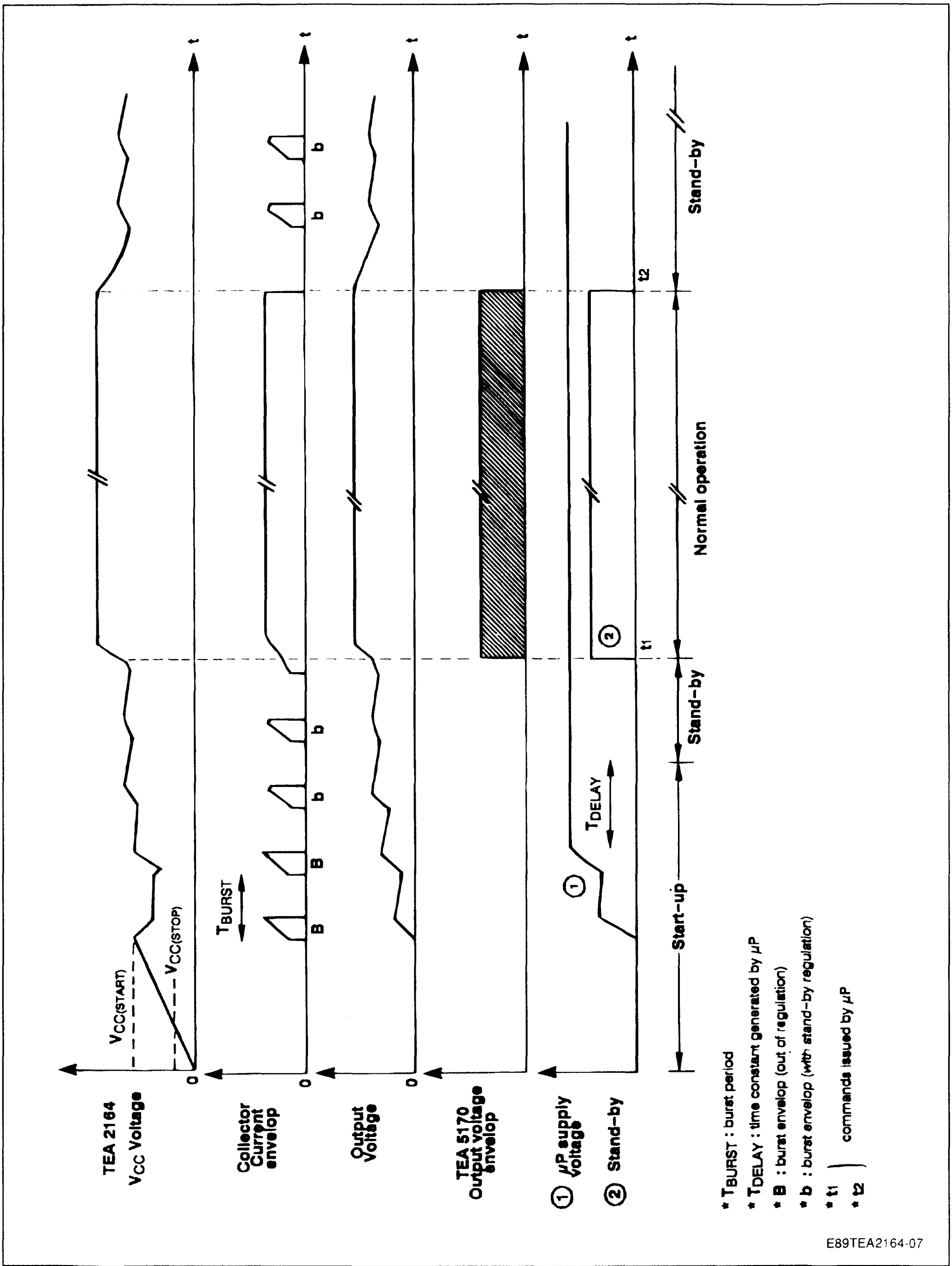
In a master slave architecture, the TEA2164 Control IC, located at the primary side of an off line power supply achieves the slave function ; whereas the master circuit is located at the secondary side. The link between both circuits is realized by a small pulse transformer (fig. 3).

Figure 2 : Master Slave Power Supply Architecture.



E89TEA2164-06

Figure 3 : System Description Waveforms.



In the operation of the master-slave architecture, four majors cases must be considered :

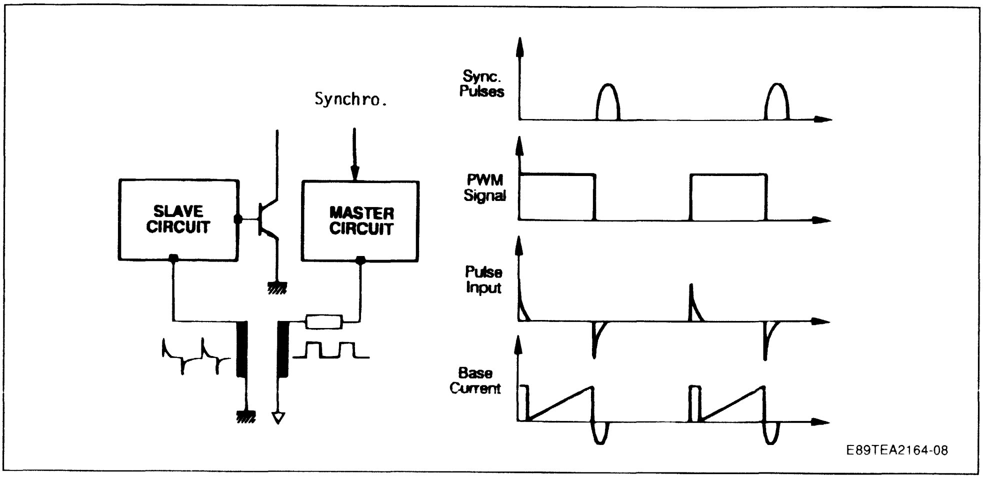
- normal operating
- stand-by mode
- power supply start-up
- abnormal conditions : off load, short circuit, ...

a) Normal operating (master slave mode)

In this configuration, the master circuit generates a pulse width modulated signal issued from the monitoring of the output voltage which needs the best accuracy (in TV applications : the horizontal deflection stage supply voltage). The master circuit power supply can be supplied by another output.

The PWM signal are sent towards the primary side through small differentiating transformer. For the TEA2164 positive pulses are transistor switching-on commands ; and negative pulses are transistor switching-off commands (fig. 4). In this configuration, only by synchronizing the master oscillator, the switching transistor may be synchronized with an external signal.

Figure 4 : Master Slave Mode Wave-forms.



b) Stand by mode

In this configuration the master circuit no longer sends PWM signals, the structure is not synchronized ; and the TEA2164 operates in burst mode. The average power consumption at the secondary side may be very low 1W ≤ P ≤ 6W (as it is consumed in TV set during stand by).

By action on the maximum duty cycle control, a primary loop maintains a semi-regulation of the output voltages. Voltage on feed-back is applied on pin 9.

Burst period is externally programmed by capacitor C1.

Figure 5 : Burst Mode Waveforms.

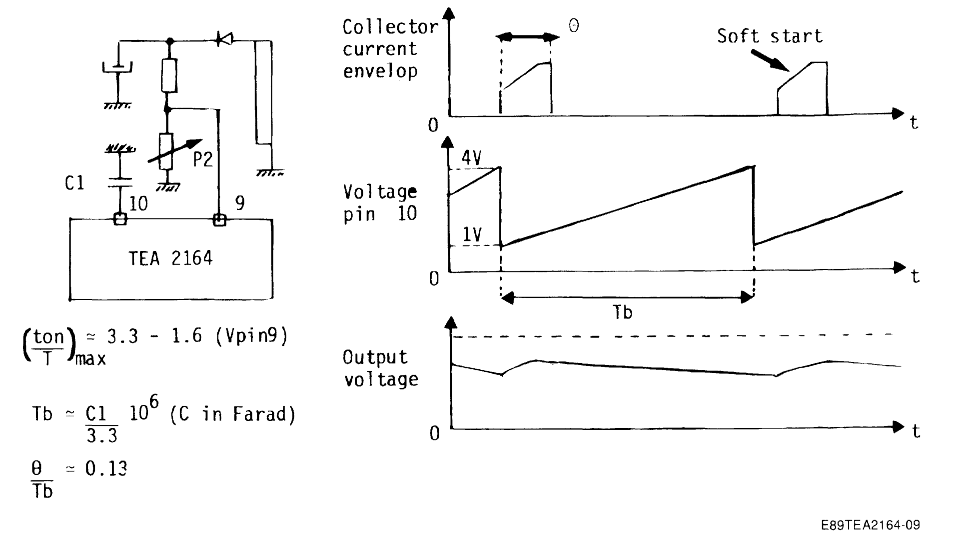
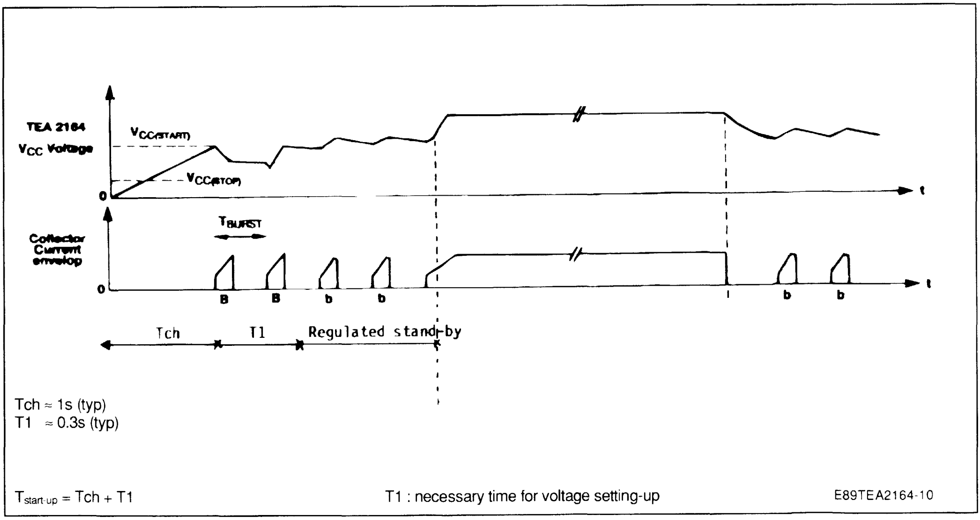


Figure 6 : Power Supply Start-up.



c) Power supply start-up

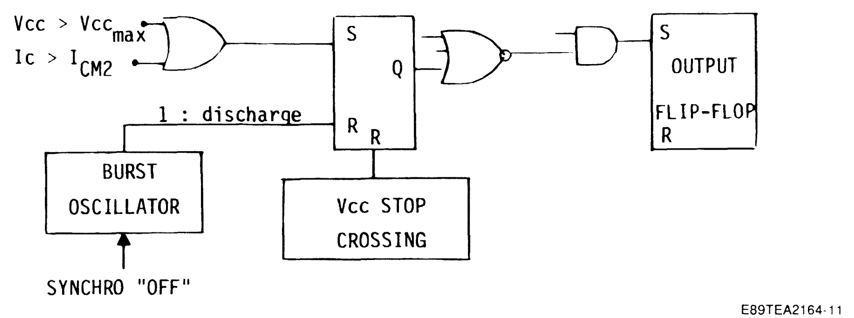
After the mains have been switched-on, the Vcc storage capacitor of the TEA2164 is charged through a high value resistor connected to the rectified high voltage. When Vcc reaches Vcc start threshold (9V typ), the TEA2164 starts operating in burst mode. Since available output power is low in burst mode the output power consumption must remain low before complete setting-up of output voltage. In TV application it can be achieved by maintaining the TV in stand-by mode during start-up (fig. 6).

d) Abnormal conditions : safety functions

Overvoltage protection
When Vcc exceeds Vcc max, an internal flip-flop stops output conduction signals. The circuit will start again after the capacitor C1 discharge ; it means : after loss of synchronization or after Vcc stop crossing (fig. 7).

In flyback converters, this function protects the power supply against output voltage runaway.

Figure 7 : Over Voltage Lock-out.



Under voltage lock-out

The TEA2164 control circuit stops operating when Vcc goes under Vcc stop.

Power limitation, current protection, long duration overload protection

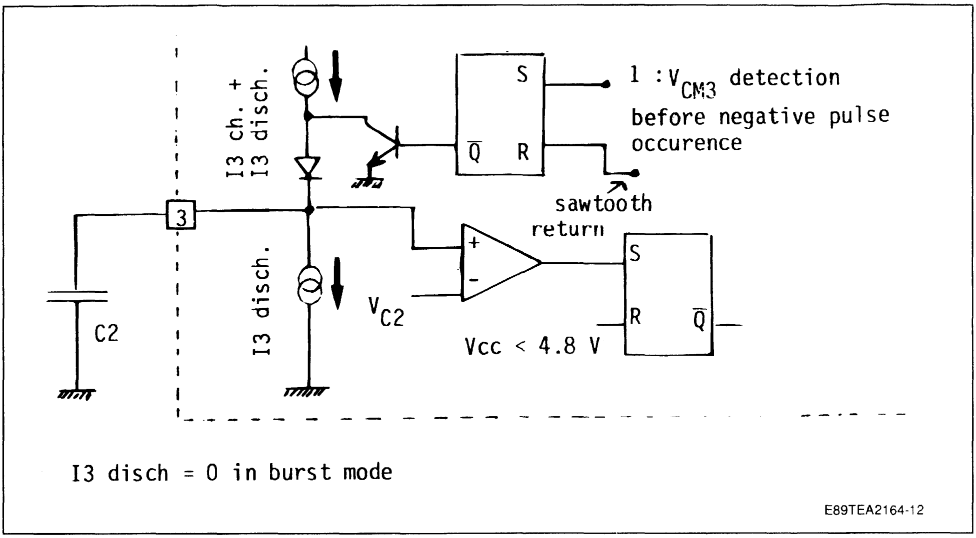
- Output power limitation : by a pulse by pulse col lector current limitation the TEA2164 limits the maximum output power. VCM1 is the corresponding voltage threshold, its detection is memorized up to the next period.

- Current protection (transistor protection)
  Under particular conditions a hard overload or short circuit may induce a flux runaway in spite of the current limitation (VCM1).

  The TEA2164 control circuit features a second current protection, VCM2. When this threshold is reached an internal flip-flop memorizes it and output conduction signals are inhibited. The circuit will send base drives again after capacitor C1 discharge(fi.g 7).

- Long duration overload protection : (fig. 8)
  An overload is detected when the sense-voltage on pin 11 reaches VCM3 before a negative pulse has been applied to pin 6. In this case the capacitor C2 (connected to pin 3) is charged with I3 ch up to the end of the period and discharged with I3 disch until a next VCM3 detector. By this way in case of long duration overload, the capacitor keeps charging at each period and its voltage encreases gradually. When the voltage on pin 3 exceeds VC2, the TEA2164 control circuit stops sending base drives and memorizes this event. No restart is allowed as long as Vpin 3 is higher than VC2 and Vcc higher than 4.8V.

Figure 8 : Long Duration Overload Monitoring Circuit.



*** Remark :**

- The harder is the overload the faster is the protection
- The capacitor keeps charging between two burst after VCM2 detection.

Figure 9 : Long Duration Over-load Detection.

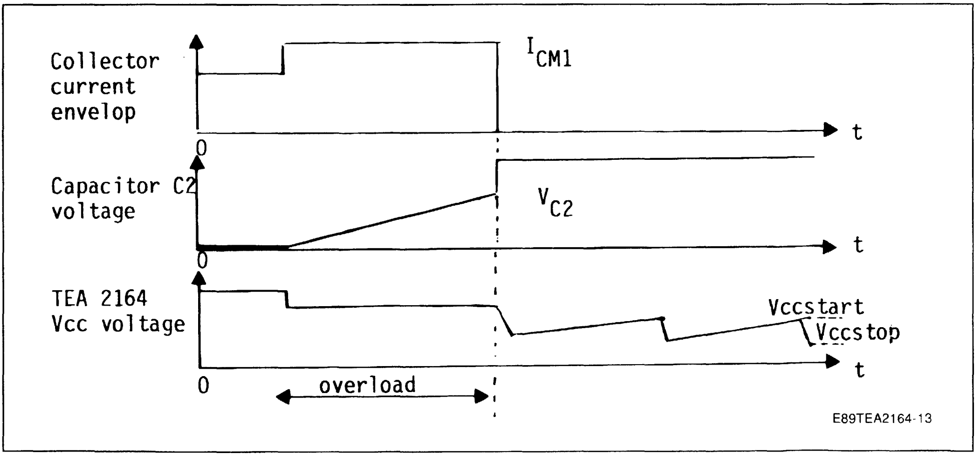
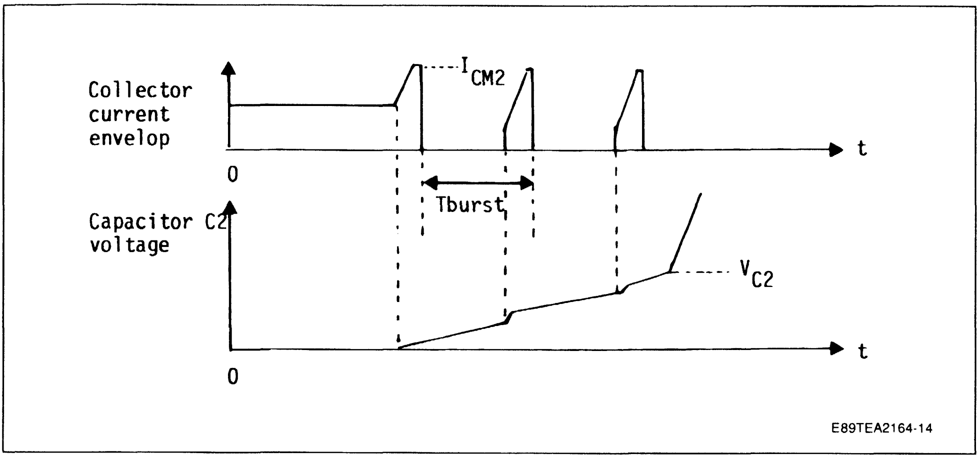


Figure 10 : Repetive Over-current Protection.

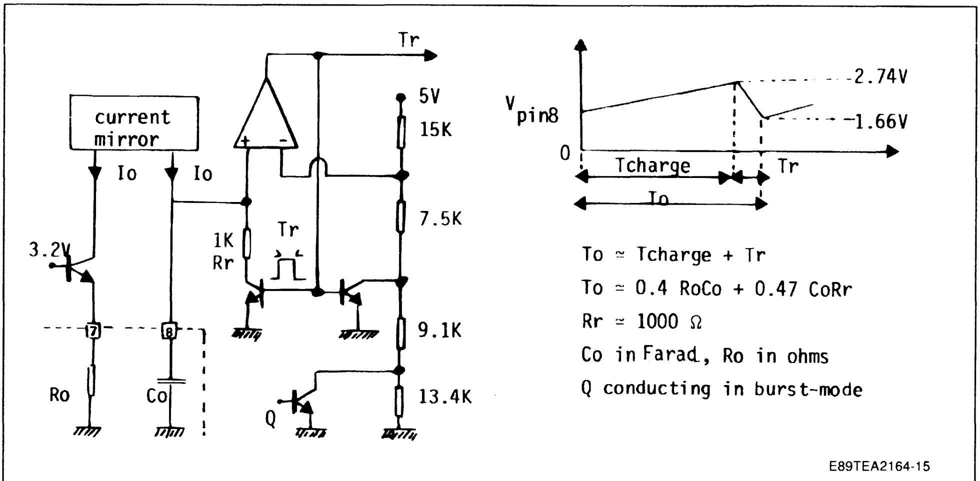


3. SWITCHING OSCILLATOR AND SYNCHRONIZATION

- Switching oscillator

When the TEA2164 control circuit operates in burst mode, the switching frequency is fixed by the free frequency oscillator. The period is determined by two external components Co and Ro.

Figure 11 : Free Frequency Running.



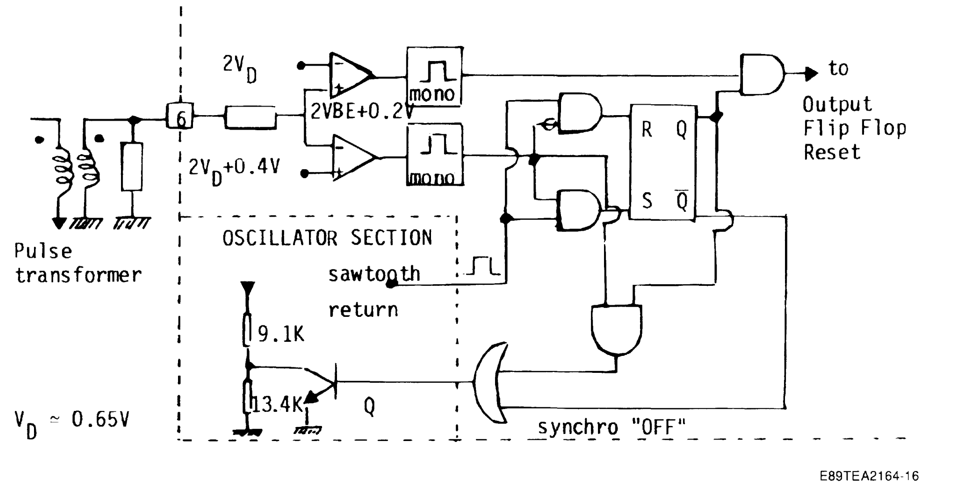
- Synchronization

When the master-circuit starts to send pulses both oscillators are not synchronous. In order to avoid any erratic conduction of the power transistor, the first synchronization will be taken into account when a positive synchronization pulse will arrive simultanously with the sawtooth return of the TEA2164 oscillator.

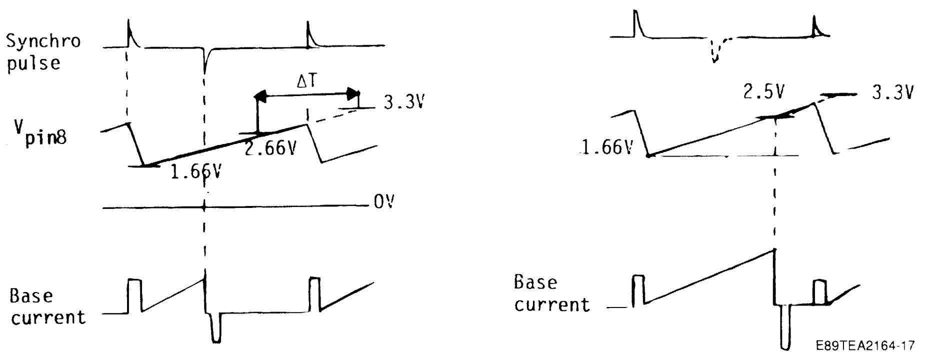
To get synchronization the free frequency must be higher than the synchronization frequency.

$$T_O < T_{sync.} < 1.50\ T_O$$

Figure 12 : Synchronization Pulse Shaper and Synchronization.



- Operation after synchronization

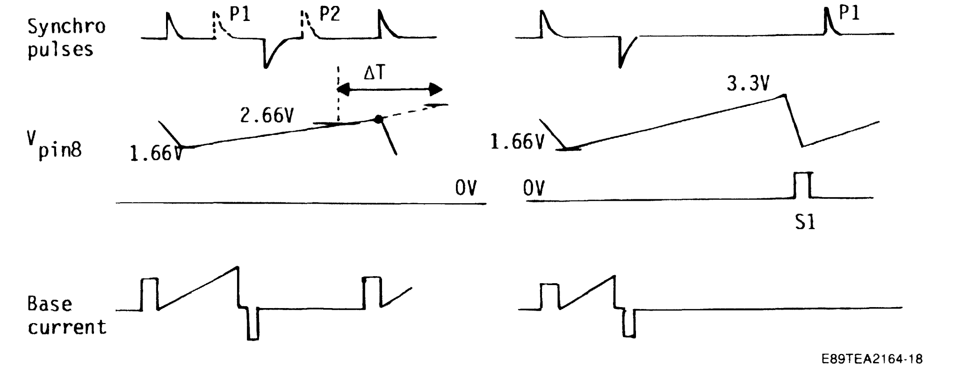


(1) NORMAL OPERATION

ΔT : synchronization window

(2) NEGATIVE PULSE MISSING

Transistor turn-off is ensured by VCM1 current limitation crossing or by an internal ton(max) limitation set by a 2.5V threshold.



(3) ERRATIC POSITIVE PULSES

P1 and P2 are masked due to the synchronization window.

(4) Fsynchro < 0.65 Fo

Signal S1 triggers burst oscillator capacitor discharge. The TEA2164 restarts in burst-mode.

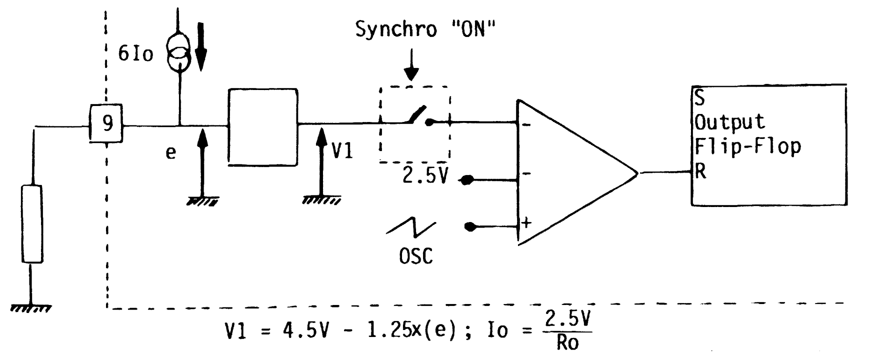
Cases (2) (3) (4) do not occur in normal operating.

4. MAXIMUM DUTY CYCLE LIMITATION

Burst mode : The maximum duty cycle is controlled by the voltage on pin 9 (fig. 13).

Synchronized mode : Normally the maximum duty cycle is set by the master circuit. However the maximum conducting time will never exceed the value given by the comparison of the oscillator wave-form with the 2.5V internal threshold.

Figure 13 : Maximum Duty Cycle Limitation.

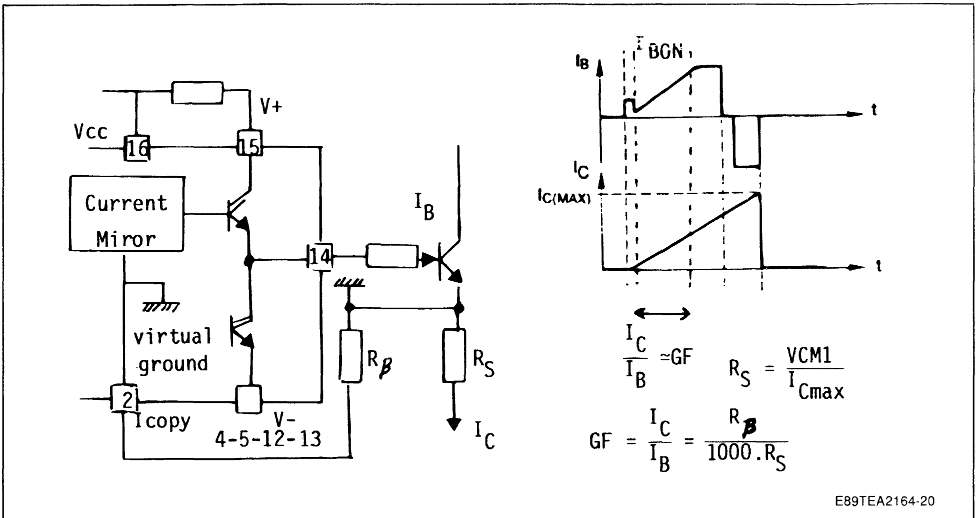


5. OUTPUT STAGE

TEA2164 output stage has been designed to drive switching bipolar transistor.

- Each base drive begins with a positive pulse IBON that realizes an efficient transistor turn-on.
- After the starting pulse IBON, the base current is proportional to the collector current. The current gain is easily fixed by a resistor R (fig. 15).
- A fast and safe transistor turn-off is realized by a fast positive base current cut-off and by applying a negative base drive which draws stored carriers. A typical 0.7s delay prevents from cross-conduction of positive and negative output stages.

Figure 14 : Output Stage Architecture and Base Drive.



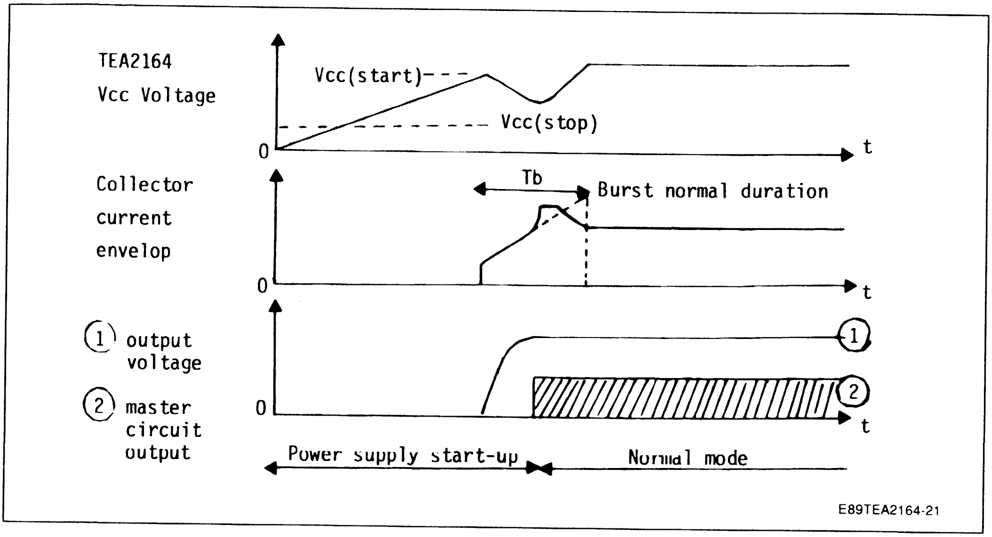
Remark : In order to reduce power dissipation on the positive output stage with the low gain transistors, for high base currents the positive output stage operates in saturated mode (fig. 15). This can be achieved by using a resistor between Vcc and V+.

6. MONITOR APPLICATIONS

In most of monitor applications, the power supply must start-up under full load conditions and the stand-by mode is no longer useful.

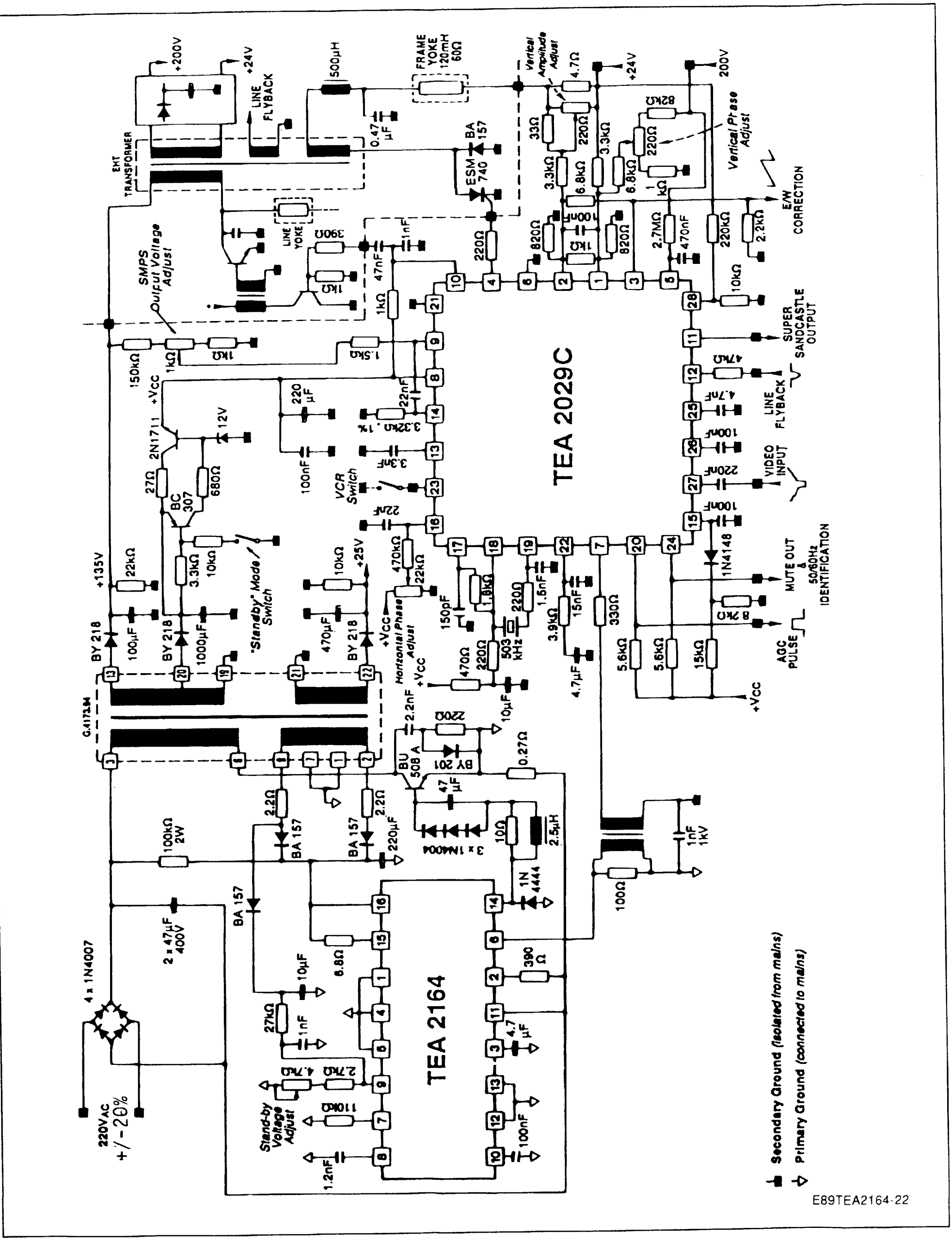
The energy of the starting burst must be high enough to ensure start-up, then the capacitor C1 must be higher in these applications than on TV application (typ. : 1µF).

Figure 15 : Power Supply Start-up and Normal Operation.

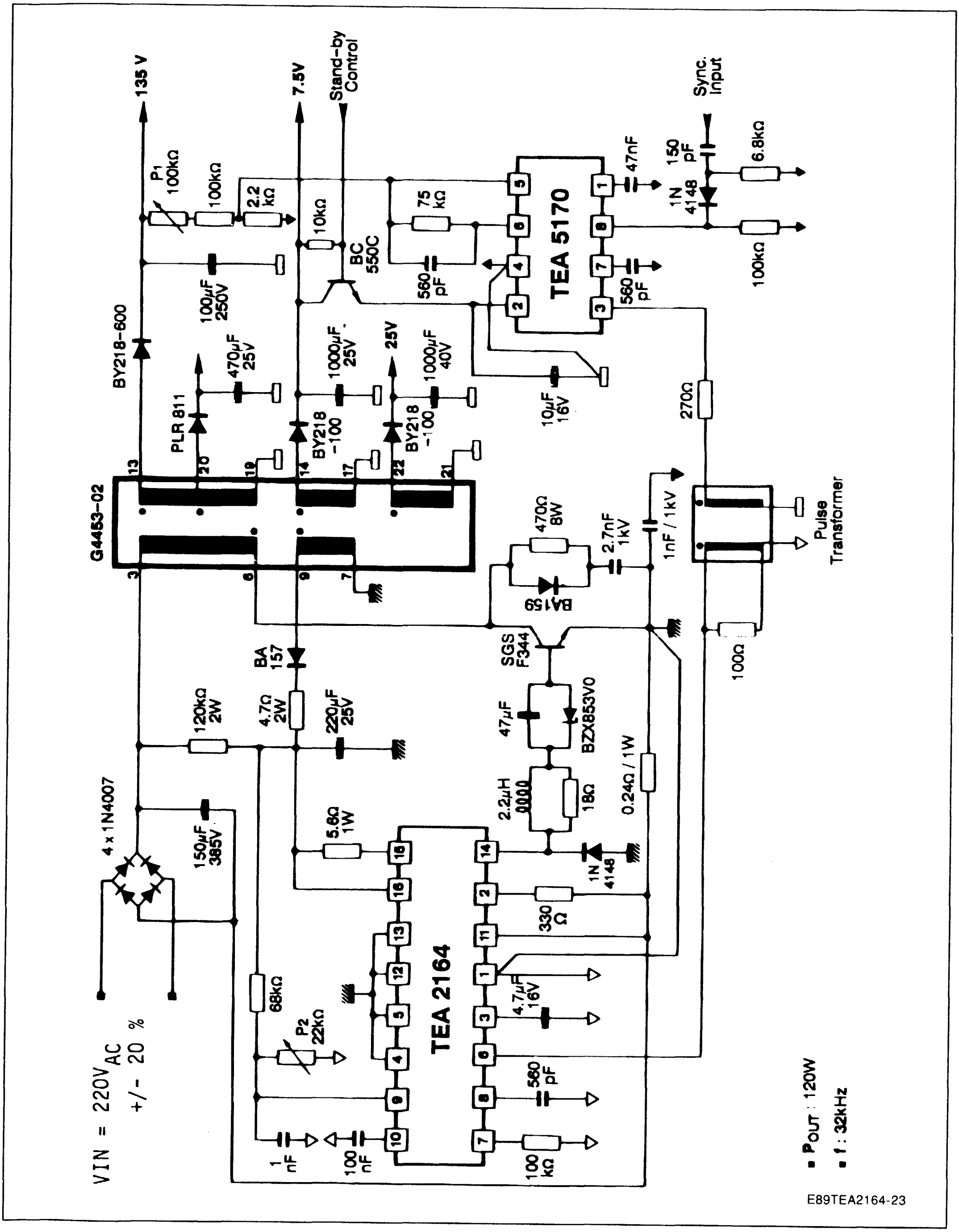


COMPLETE APPLICATION DIAGRAM

(SMPS + DEFLECTION) (with stand-by function)

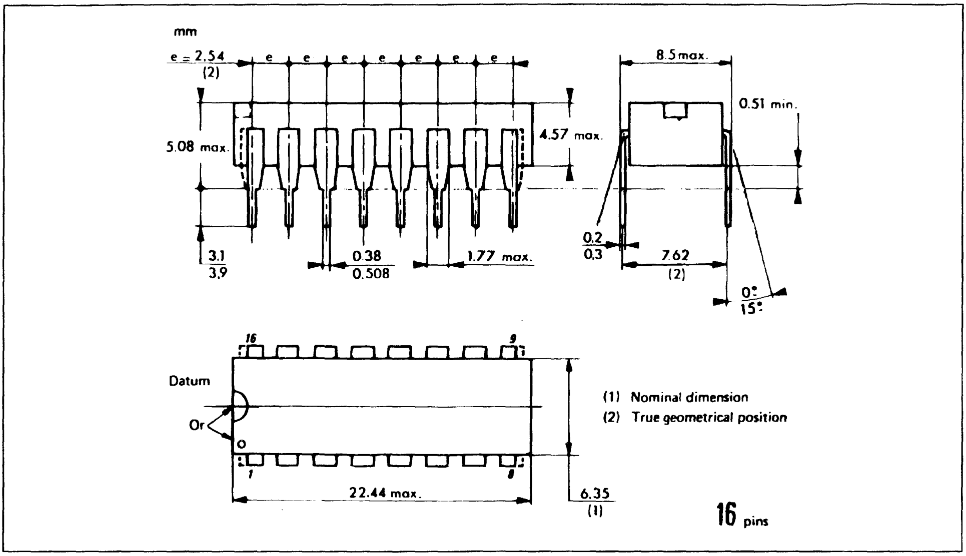


STANDALONE 32 KHz POWER SUPPLY ELECTRICAL DIAGRAM



PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP

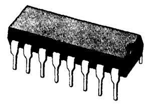


SGS-THOMSON
MICROELECTRONICS

TEA2260

SWITCH MODE POWER SUPPLY PRIMARY CIRCUIT

- POSITIVE AND NEGATIVE CURRENT UP TO 1.2A and – 2A
- LOW START-UP CURRENT
- DIRECT DRIVE OF THE POWER TRANSISTOR
- TWO LEVELS TRANSISTOR CURRENT LIMITATION
- DOUBLE PULSE SUPPRESSION
- SOFT-STARTING
- UNDER AND OVERVOLTAGE LOCK-OUT
- LARGE POWER RANGE CAPABILITY IN STAND-BY



TEA2260
BATWING
DIP16
(Plastic Package)

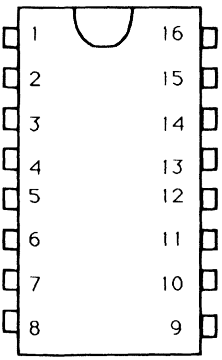
DESCRIPTION

The TEA2260 is a monolithic integrated circuit for the use in primary part of an off-line switching mode power supply.

All functions required for SMPS control under normal operating, transient or abnormal conditions are provided.

The capability of working according to the "master-slave" concept, or according to the "primary regulation" mode makes the TEA2260 very flexible and easy to use. This is particularly true for TV receivers where the IC provides an attractive and low cost solution.

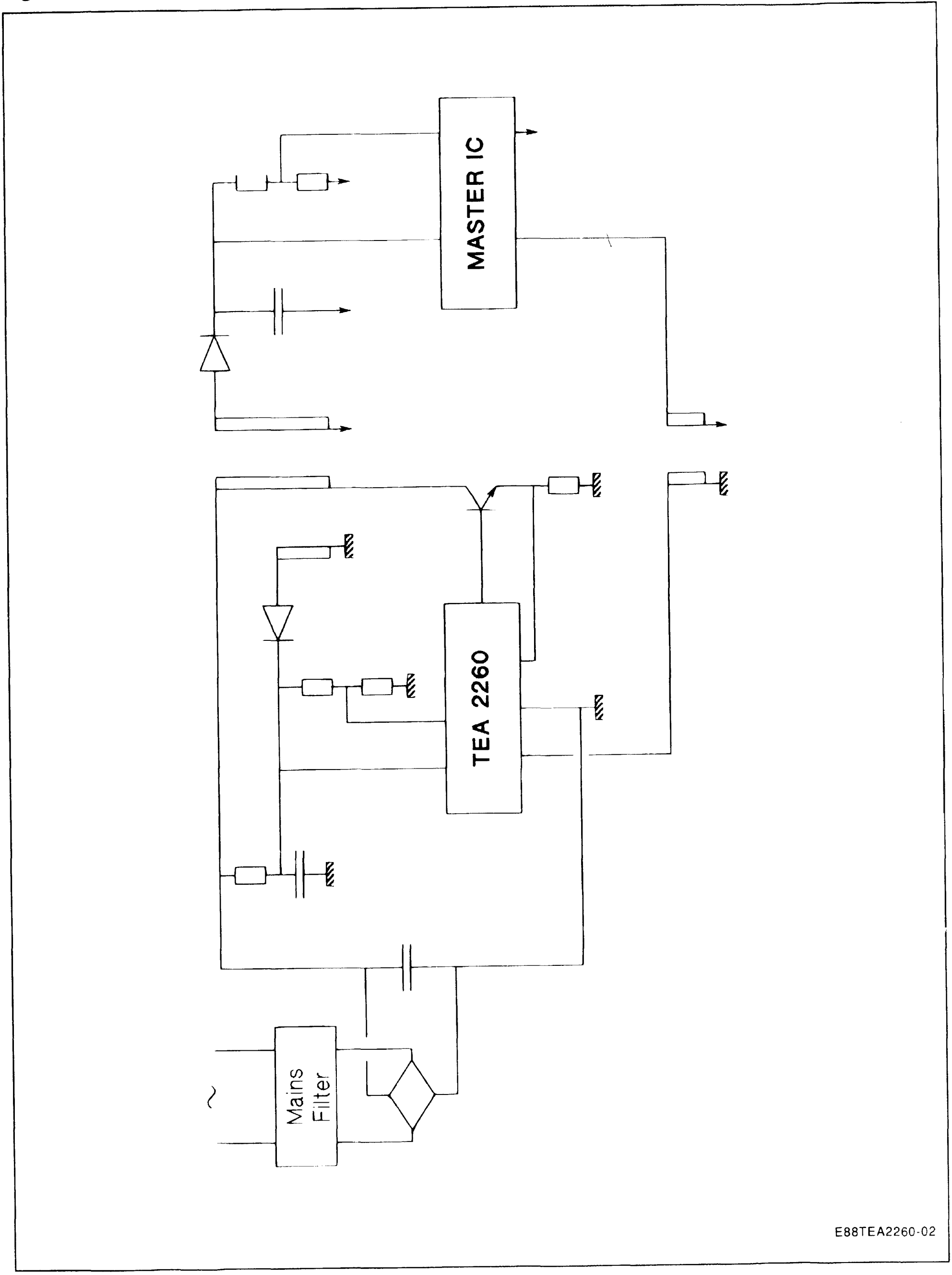
PIN CONNECTIONS



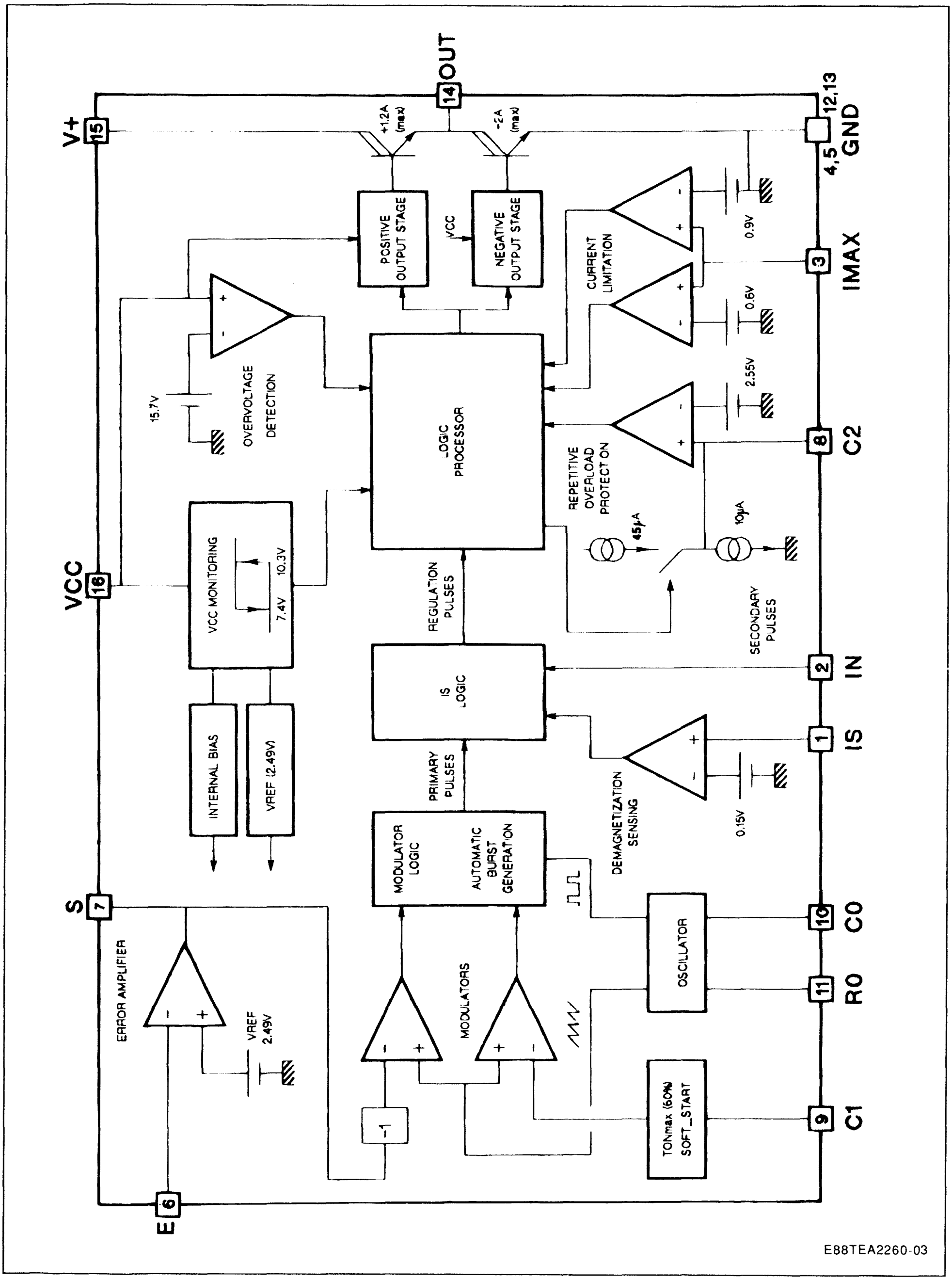
Pin	Name	Function
1	IS	Transformer demagnetization sensing input
2	IN	Secondary pulses input
3	IMAX	Power transistor current limitation input
4	GND	Ground
5	GND	Ground
6	E	Error amplifier input (invertin)
7	S	Error amplifier output
8	C2	Overload integration capacitor
9	C1	Soft-start capacitor
10	CO	Oscillator capacitor
11	RO	Oscillator resistor
12	GND	Ground
13	GND	Ground
14	OUT	Power output
15	V+	Positive output stage supply
16	VCC	Power supply

E88TEA2260-01

Figure 1 : Simplified Application Diagram.



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

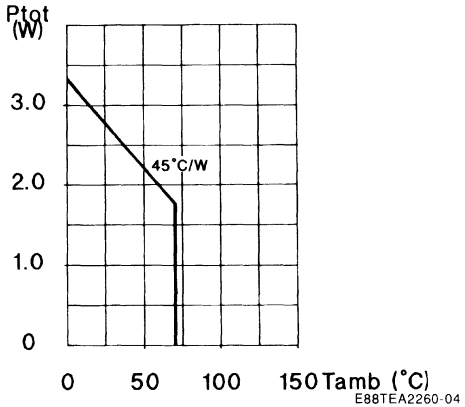
Symbol	Parameter	Value	Unit
VCC	Power Supply V16-V4, 5, 12, 13	20	V
V+	Output Stage Power Supply V15-V4, 5, 12, 13	20	V
IOUT+	Positive Output Current (source current)	1.5	A
IOUT–	Negative Output Current (sink current)	2.5	A
Tj	Operating Junction Temperature	150	°C
Tstg	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

Rth (j-c)	Junction-case Thermal Resistance	11	°C/W
Rth (j-a)*	Junction-ambient Thermal Resistance	45	°C/W

* Soldered on a 35μm, 40cm² board copper area.

MAXIMUM POWER DISSIPATION



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Power Supply	VCCstop	12	VCCmax	V
Iout+	Peak Positive Output Current			1.2	A
Iout–	Peak Negative Output Current			2.0	A
Iout+	Average Positive Output Current			0.6	A
Iout–	Average Negative Output Current			0.6	A
Fop	Operating Frequency	10		100	KHz
Vin	Input Pulses Amplitude (pin 2)	1.5	2.5	4.5	V
R0	Oscillator Resistor Range	20		150	KΩ
C0	Oscillator Capacitor Range	0.47		4.7	nF
C1	Soft-starting Capacitor Range	0.047	1		μF
C2	Overload Integration Capacitor	0.047	1		μF
C2/C1	Ratio C2/C1 (C2 must be ≥ C1)	1			
Tamb	Operating Ambient Temperature	– 2.0		70	°C

ELECTRICAL CHARACTERISTICS :
Tamb = 25°C, VCC = 12V (unless otherwise specified)

POWER SUPPLY

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCstart	Starting Voltage (VCC increasing)	9.3	10.3	11.3	V
VCCstop	Stopping Voltage (VCC decreasing)	6.4	7.4	8.4	V
HystVCC	Hysteresis (VCCstart-VCCstop)	2.4	2.9		V
ICCstart	Starting Current (VCC = 9V)		0.7	1.4	mA
ICC	Supply Current (VCC = 12V)		7.5	15	mA
VCCmax	Overvoltage Threshold on VCC	15	15.7		V
ICCover	Supply Current after Overvoltage Detection (VCC = 17V)		35		mA

OSCILLATOR / PWM SECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
$\frac{DeltaF}{F}$	Accuracy (R0 = 68Kohm, C0 = 1nF)		10		%
TONmax	Maximum Duty Cycle in Primary Regulation Mode	50	60	70	%

ERROR AMPLIFIER SECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Avo	Open Loop Gain		75		dB
Fug	Unity Gain Frequency		550		KHz
Isc	Short Circuit Output Current(pin 7 connected to ground)		2		mA
IBE	E Input Bias Current (pin 6)		0.08		µA
Vref	Internal Voltage Reference (connected to error amplifier input and not directly accessible)	2.34	2.49	2.64	V

INPUT SECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vin	IN Input Threshold (pin 2)	0.6	0.85	1.2	V
Vis	IS Input Threshold (pin 1)		0.15		V
IBin	IN Input Bias Current		0.3		µA
IBis	IS Input Bias Current		0.4		µA

CURRENT LIMITATION SECTION

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIM1	First Current Limitation Threshold	558	600	642	mV
VIM2	Second Current Limitation Threshold	837	900	963	mV
Δ VIM	Thresholds Difference VIM2 - VIM1		300		mV
VC2	Lock-out Threshold on Pin C2	2.25	2.55	2.85	V
IDC2	Capacitor C2 Discharge Current		10		µA
ICC2	Capacitor C2 Charge Current		45		µA
IBImax	IMAX Input Bias Current (pin 3)		0.2		µA

GENERAL DESCRIPTION

The new SMPS integrated circuit is suitable for the use in TV set working on the mains from 90 to 270Vac. The circuit can also be used in others consumer applications such as VCR, monitors...

The circuit ensures itself the starting of SMPS and the "stand-by" mode operating using the primary regulation principle.

The circuit ensures the "normal operating" mode in association with a secondary regulator, discrete or integrated device.

The power transmitted in standby can vary in a large range (e.g. 1 to 30W or more) with an acceptable voltage regulation.

The transition : normal mode - stand-by mode is made automatically by secondary regulation pulses occurence or disappearance.

The circuit can also be used alone, according to the primary regulation concept.

The circuit ensures the direct drive of a bipolar power transistor (without external boosters).

The circuit ensures security functions such as power transistor current limitation, power limitation in case of SMPS output overload or short circuit, overvoltage detection in case of primary or secondary regulator failure.

SMPS OPERATING DESCRIPTION

STARTING MODE - STAND BY MODE

Power for circuit supply is taken from the mains through a high value resistor before starting. As long as VCC of the TEA2260 is below VCCstart, the quiescent current is very low (typically 0.7mA) and the electrolytic capacitor across VCC is linearly charged. When VCC reaches VCCstart (typically 10.3V), the circuit starts, generating output pulses with a soft-starting. Then the SMPS goes into the stand-by mode and the output voltage is a percentage of the nominal output voltage (eg. 80%).

For this the TEA2260 contains all the functions required for primary mode regulation : a fixed frequency oscillator, a voltage reference, an error amplifier and a pulse width modulator (PWM).

For transmission of low power with a good efficiency in stand-by, an automatic burst generation system is used, in order to avoid audible noise.

NORMAL MODE (secondary regulation)

The normal operating of the TV set is obtained by sending to the TEA2260 regulation pulses generated by a regulator located in the secondary side of the power supply.

This architecture uses the "Master-slave Concept", advantages of which are now well-known especially the very high efficiency in stand-by mode, and the accurate regulation in normal mode.

Stand-by mode or normal mode are obtained by supplying or not the secondary regulator. This can be ordonnered for exemple by a microprocessor in relation with the remote control unit.

Regulation pulses are applied to the TEA2260 through a small pulse-transformer to the IN input (pin 2). This input is sensitive to positive square pulses. The typical threshold of this input is 0.85V.

The frequency of pulses coming from the secondary regulator can be lower or higher than the frequency of the starting oscillator.

The TEA2260 has no soft-starting system when it receives pulses from the secondary. The soft-starting has to be located in the secondary regulator.

Due to the principle of the primary regulation, pulses generated by the starting system automatically disappear when the voltage delivered by the SMPS increases.

STAND-BY MODE - NORMAL MODE TRANSITION

During the transition there are simultaneously pulses coming from the primary and secondary regulators.

These signals are not synchronized and some care has to be taken to ensure the safety of the switching power transistor.

A very sure and simple way consist in checking the transformer demagnetization state.

- A primary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the secondary regulator.
- A secondary pulse is taken in account only if the transformer is demagnetized after a conduction of the power transistor required by the primary regulator.

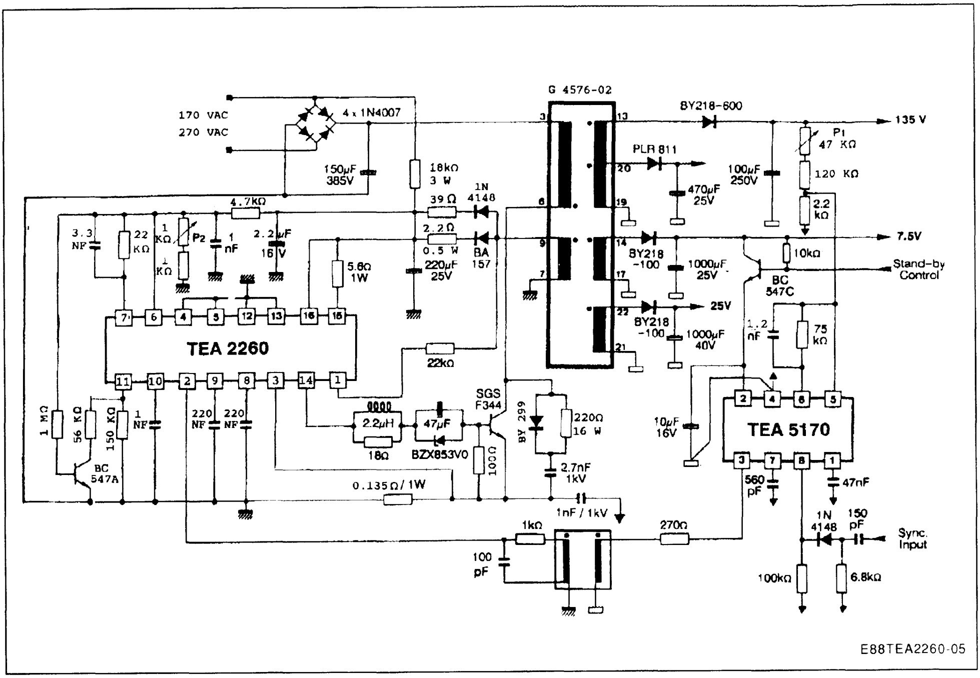
With this arrangement the switching safety area of the power transistor is respected and there is no risk of transformer magnetization.

The magnetization state of the transformer is checked by sensing the voltage across a winding of the transformer (generally the same which supplies the TEA2260). This is made by connecting a resistor between this winding and the demagnetization sensing input of the circuit (pin 1).

SECURITY FUNCTIONS OF THE TEA2260

- **Undervoltage detection.** This protection works in association with the starting device "V_{CC} switch" (see paragraph Starting-mode - standby mode). If V_{CC} is lower than V_{CC}stop (typically 7.4V) output pulses are inhibited, in order to avoid wrong operation of the power supply or bad power transistor drive.
- **Overvoltage detection.** If VCC exceeds VCCmax (typically 15.7V) output pulses are inhibited. Restarting of the power supply is obtained by reducing VCC below VCCstop.
- **Current limitation of the power transistor.** The current is measured by a shunt resistor. A double threshold system is used :
  - When the first threshold is reached, the conduction of the power transistor is stopped until the end of the period : a new conduction signal is needed to obtain conduction again.
  - Furthermore as long as the first threshold is reached (it means during several periods), an external capacitor C2 is charged. When the voltage across the capacitor reached VC2 (typically 2.55V) the output is inhibited. This is called the "repetitive overload protection". If the overload disappears before VC2 is reached, C2 is discharged, so transient overloads are tolerated.
  - second current limitation threshold (VIM2). When this threshold is reached the output of the circuit is immediatly inhibited. This protection is helpfull in case of hard overload for example to avoid the magnetization of the transformer.
- **Restart of the power supply**. After stopping due to VC2, VIM2, VCCMAX or VCCstop triggering, restart of the power supply can be obtained by the normal operating of the "VCC switch" but thanks to an integrated counter, if normal restart cannot be obtained after three trials, the circuit is definitively stopped. In this case it is necessary to reduce VCC below approximately 5V to reset the circuit. From a practical point of view, it means that the power supply has to be temporarily disconnected from any power source to get the restart.

TYPICAL APPLICATION



TV - SET SMPS (with TEA5170)

Input voltage range	170VAC – 270VAC
Input DC voltage range	210VDC – 370VDC
Output power in normal mode	25W < Po < 140W
Output power in stand by mode	2W < Po < 45W
Operating frequency	32 KHz
Efficiency at full load	> 80%
Efficiency in stand by mode (Po = 7W)	> 50%

Short circuit protected
Open load protected
Long duration overload protected
Complete shutdown after 3 restarts with default detection

load regulation (VDC = 310V)

Output 135V (± 0.18%) ——> (I_{135} : 0.01A to 0.8A ; I_{25} = 1A)
Output 25V (± 2%) ——> (I_{135} : 0.8A ; I_{25} : 0.5A —> 1A)

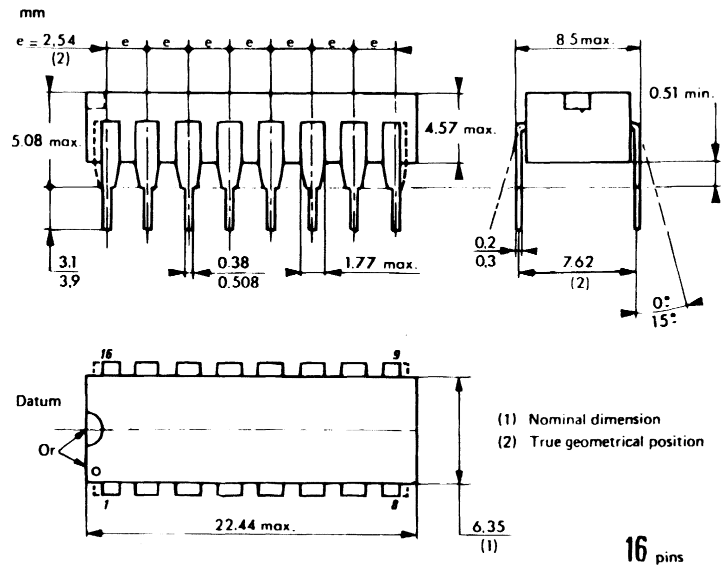
Line regulation

Output 135V (± 0.13%) ——> (210V < V_{DC} < 370V)
Output 25V (± 0.17%) ——> (I_{135} : 0.8A ; I_{25} : 1A)

PACKAGE MECHANICAL DATA

16 PINS - PLASTIC DIP

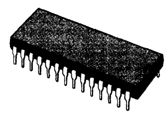
mm



TEA5031D

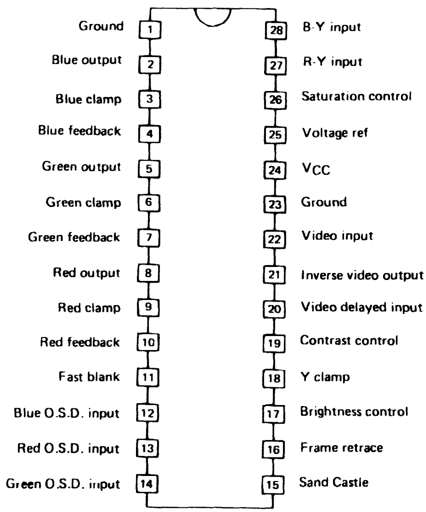
COLOR TV VIDEO PROCESSOR

- MATRIXING OF R, G, B SIGNAL FROM (R-Y) AND (B-Y)
- ELECTRONIC CONTROL OF CONTRAST, BRIGHTNESS AND SATURATION
- THREE CHANNELS VIDEO SWITCH, FOR SELECTION OF INTERNAL SIGNAL (broadcast) OR EXTERNAL R, G, B INFORMATION (teletext, TV games, home computer)
- AUTOMATIC COLOR PICTURE TUBES CUT-OFF ADJUSTMENT



TEA5031D
DIP 28
(Plastic Package)

PIN CONNECTIONS

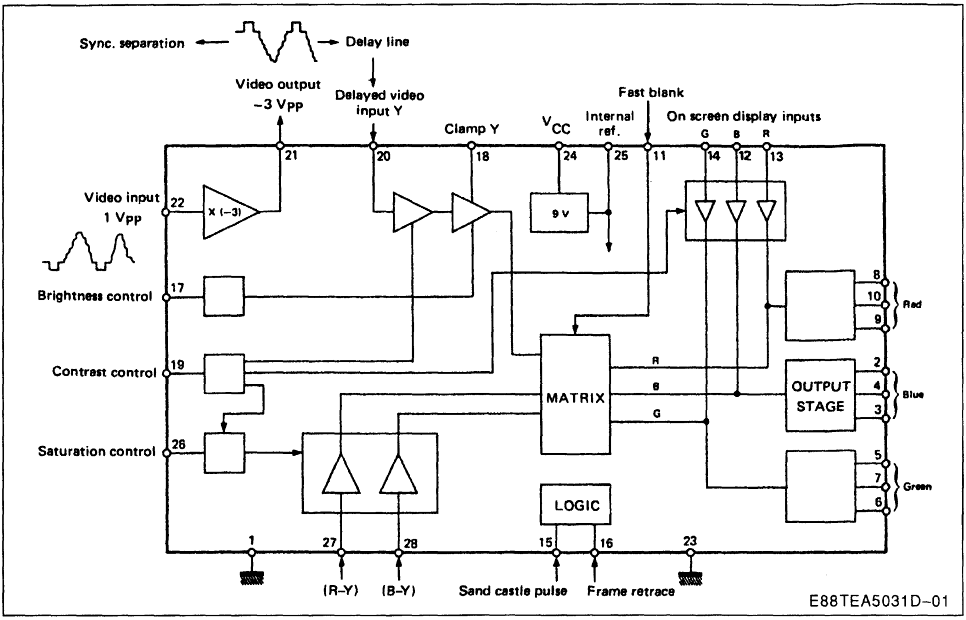


E88TEA5031D-02

DESCRIPTION

The TEA5031D is a color TV video processor compatible with all standards PAL/SECAM/NTSC and new needs such as teletext, Antiope, TV games, remote control etc...

BLOCK DIAGRAM



GENERAL DESCRIPTION

In order to ensure compatibility with standard video transmission systems the luma input is a high impedance, AC coupled, designed to accept a 1V video signal. After a X3 gain voltage amplifier the inverted luma signal is brought out to the luma delay line. This output is low impedance to match the delay accurately.

Following the luma delay line the video is controlled by an electronic gain control with a range of 40dB.

The DC luma level is locked on the black level (cutoff current) with a range of ± 1V depending of brightness. The DC voltage level is clamped during each line retrace and an external capacitor holds this voltage during the line trace.

After brightness and contrasts controls the luminance is fed to the matrix with R-Y and B-Y signals.

The R-Y and B-Y inputs are high impedance with AC coupling, compatible with decoder I'Cs such as the TEA5630 for SECAM and the TEA5620 for PAL.

The voltage gain of R-Y and B-Y is controlled by saturation. The saturation is in tracking with contrast and then the R-Y and B-Y signals are fed to the matrix and summed with on-screen display signals which are controlled in gain by the luma contrast control. Each input is AC coupled and black level clamped using the coupling capacitor as the storage element for the clamp voltage.

All the controls have an active range of 0.5 to 4.5 V making them compatible with D/A converter derived control signals, such as those from remote control systems. The three on-chip output stages are high gain class B amplifiers with the gain set by parallel feedback resistor.

This gives a well defined gain and stable output voltage level. The beam current in each cathode of the picture tube is monitored by a high-voltage PNP transistor or the TEA5101A video amplifier. A sample of this current is fed back to the IC.

In the luma signal a reference black level is inserted during the line and frame blanking periods. While this reference level is present, and after the frame flyback, the output stage feedback input goes high impedance and an internal comparator is actived.

This circuit compares an internal reference voltage (2V typ) to the voltage developed across an external resistor by the picture tube beam current, and the output voltage is trimmed to get the desired cathode current value.

An internal logic delivers blanking and clamping pulses from the normalized sandcastle and frame retrace signals.

A supersandcastle and a frame blanking signals can be used only if the frame blanking pulse is longer or equal than the frame level of SSC.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	16	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

THERMAL DATA

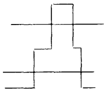
$R_{th(j-a)}$	Junction-ambient Thermal Resistance	55	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

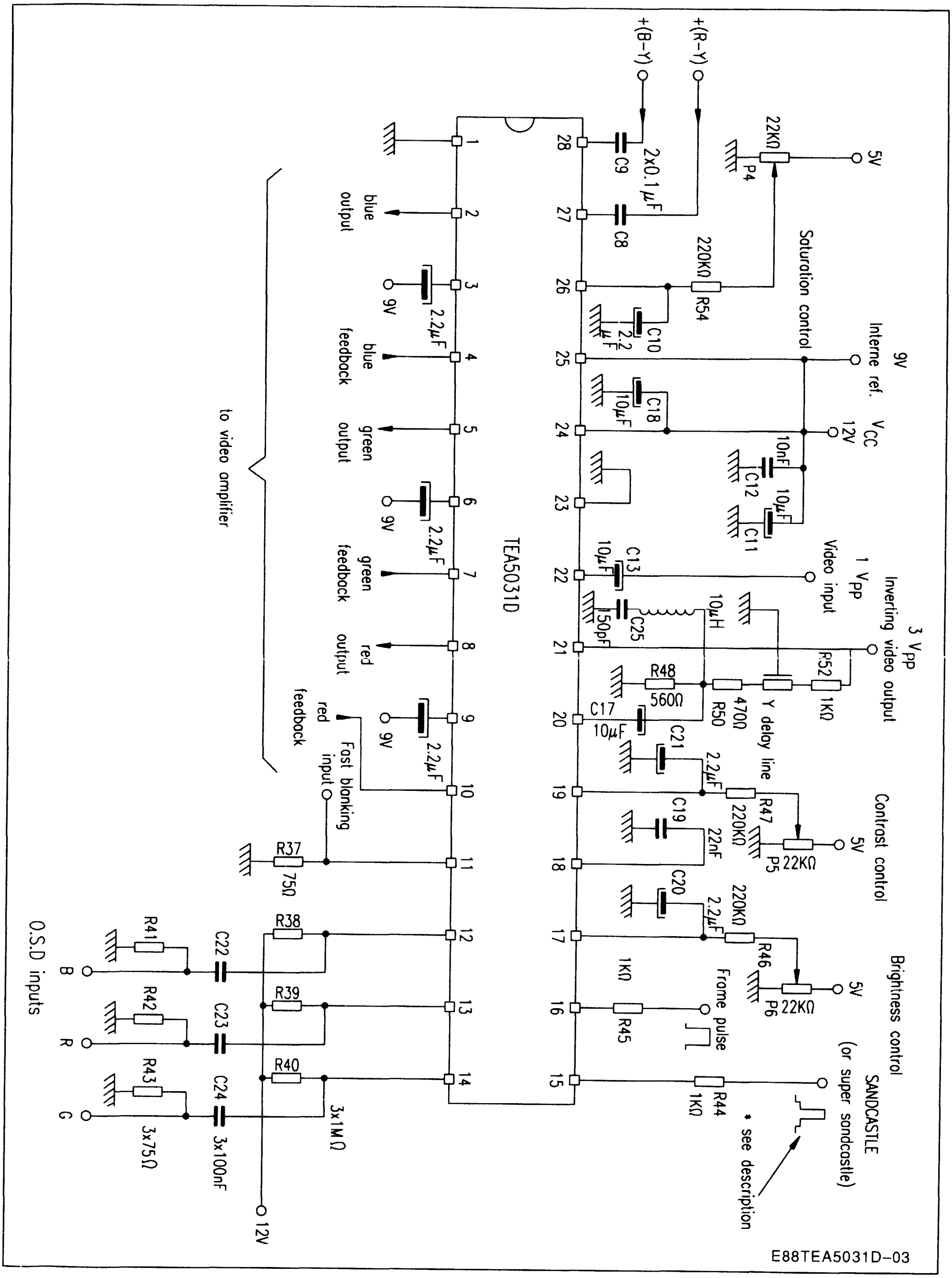
T_{amb} = + 25°C ; V_{CC} = 12V (unless otherwise noted)

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Pin 24	10.8	12	13.2	V
I_{CC}	Supply Current	Pin 24		55		mA
V_Z	Internal Voltage Ref.	Pin 25		9		V
	Input-output characteristics					
	Video Input	Pin 22		1		V_{PP}
	Output Voltage Inv. Video (V22 = 1 V_{PP})	Pin 21		3		V_{PP}
	Max Output Voltage Swing	Pin 21		7		V_{PP}
	– 3 dB Bandwidth	Pins 2-5-8	4.5	5		MHz
	(R-Y) Input Voltage (100% modulation)	Pin 27		1.4	2	V_{PP}
	(B-Y) Input Voltage (100% modulation)	Pin 28		1.0	2	V_{PP}
	– 3 dB Bandwidth		1.5			MHz
	Luma Gain					
	G21/22	Pin 21	8.5	10	11.5	dB
	G2/20, G5/20, G8/20 at Max Adjustement	Pins 2-5-8	13.5	15.5	19.1	dB
	Differential Gain Fault : Luma Channel				0.5	dB
	Chroma Gain					
	G8/27 at Max Adjustment		8.8	11.6	14.5	dB
	G2/28 at Max Adjustment		12	14.7	17.2	dB
	Chroma Gain Ratio at Max Adjustment		1.28	1.40	1.48	
	Voltage Control for Electronic Potentiometers					
	Contrast (pin 19) Saturation (pin 26)					
	Range of Adjustment					
	V19 = 5V ; V26 = 5V			G_{max}		dB
	V19 = 0V ; V26 = 0V Attenuation		40	46		dB
	Brightness (pin 17)					
	V_{out} Adjustment (V17 varying from 0 to 5V)			± 1		V
	On Screen Display Inputs	Pins 12-13-14				
	OSD Input Voltage (black to white level)			1	2	V
	OSD Gain (V2/12 ; V8/13 ; V5/14)		13.5	15	17	dB
	OSD Generator Max Impedance				75	Ω
	– 3 dB Bandwidth		5			MHz
	Fast Blanking Threshold			0.5		V
	Max Output Voltage Swing	Pins 2-5-8	7	8		V_{PP}
	Cut-off Control Feedback Threshold	Pins 4-7-10	1.7	2	2.4	V

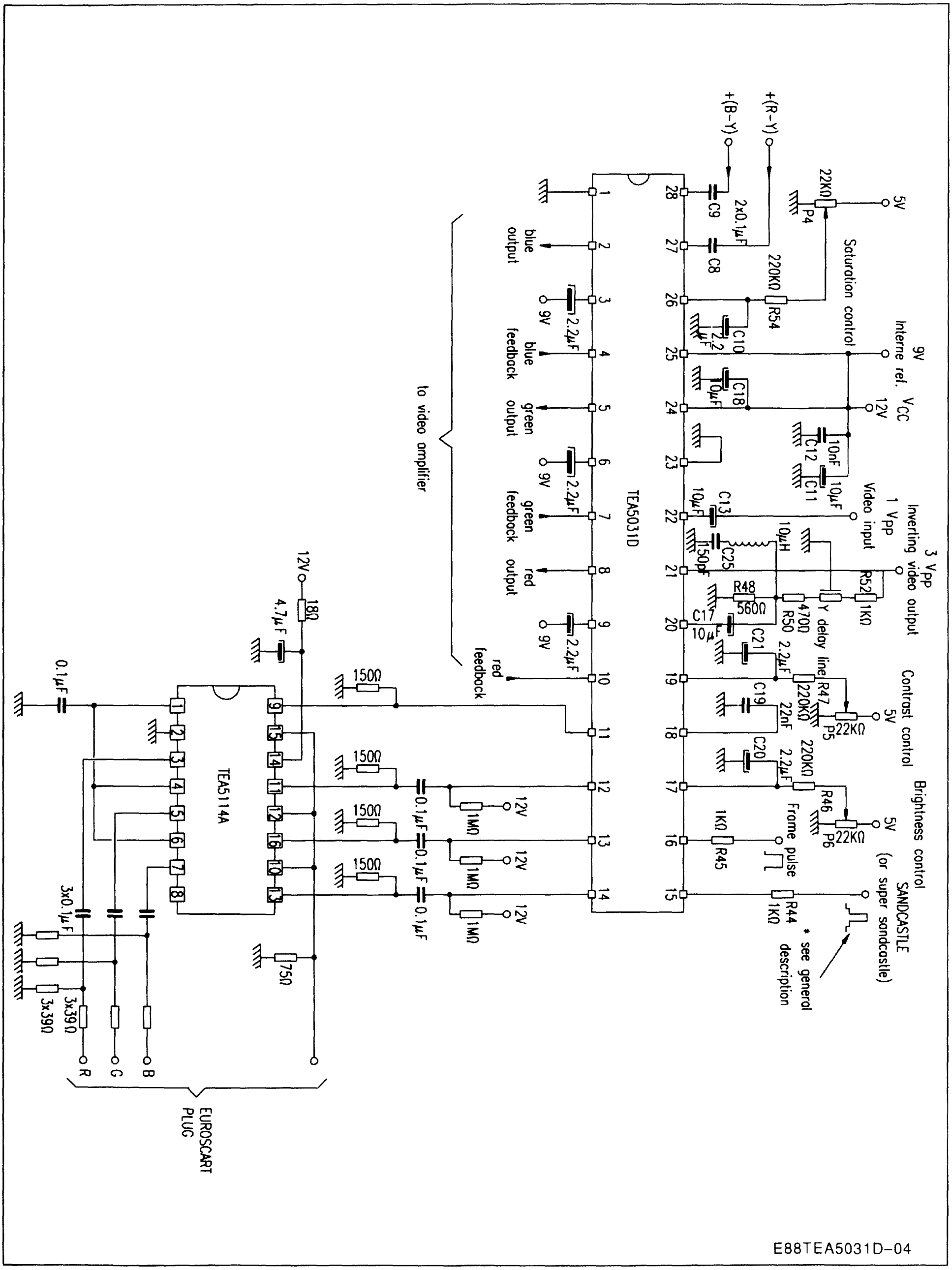
ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
	Sand-Castle Input Pin 15				
	Clamp Y 8V 		8		V
	Line Blanking 2.5V		2.5		V
	Frame Return Input Voltage Pin 16		2.5		V
	Control Current (V15 = V16 = 4V)		0.5		mA
	Matrix Coefficient				
	Red Output (V5/V8 with V27 = 1V ; V28 = 0 ; V20 = 0)		0.51		
	Blue Output (V5/V2 with V27 = 0 ; V28 = 1 ; V20 = 0)		0.19		

APPLICATION CIRCUIT



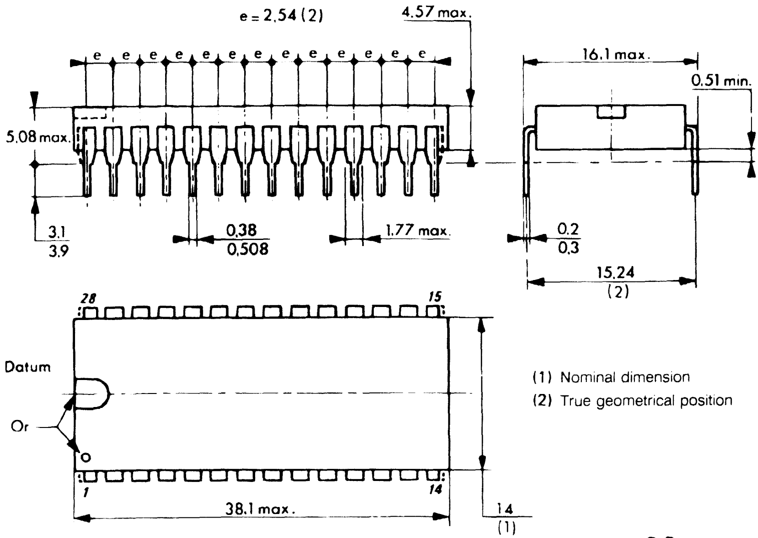
APPLICATION CIRCUIT
FULFILLING THE EURODCART SPECIFICATIONS



E88TEA5031D-04

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



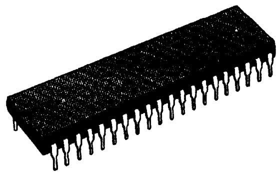
(1) Nominal dimension
(2) True geometrical position

28 Pins

WIDE BAND VIDEO PROCESSOR

PRODUCT PREVIEW

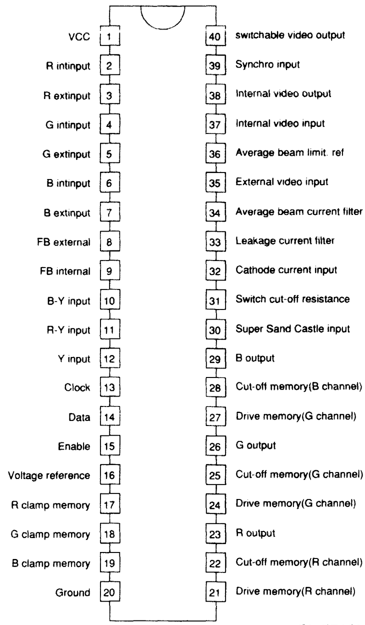
- DIGITAL CONTROL OF BRIGHTNESS, SATURATION AND CONTRAST ON TV SIGNALS AND R, G, B INTERNAL OR EXTERNAL SOURCES
- BUS DRIVE OF SWITCHING FUNCTIONS
- DEMATRIXING OF R, G, B SIGNALS FROM Y, R-Y, B-Y, TV MODE INPUTS
- MATRIXING OF R, G, B SOURCES INTO Y, R-Y, B-Y SIGNALS
- AUTOMATIC DRIVE AND CUT-OFF CONTROLS BY DIGITAL PROCESSING DURING THE FRAME RETRACE
- PEAK AND AVERAGE BEAM CURRENT LIMITATION
- ON-CHIP SWITCHING FOR R, G, B INPUT SELECTION
- ON-CHIP INSERTION OF INTERNAL OR EXTERNAL R, G, B SOURCES



DIP40
(Plastic Package)

ORDER CODE : TEA5040

PIN CONNECTIONS

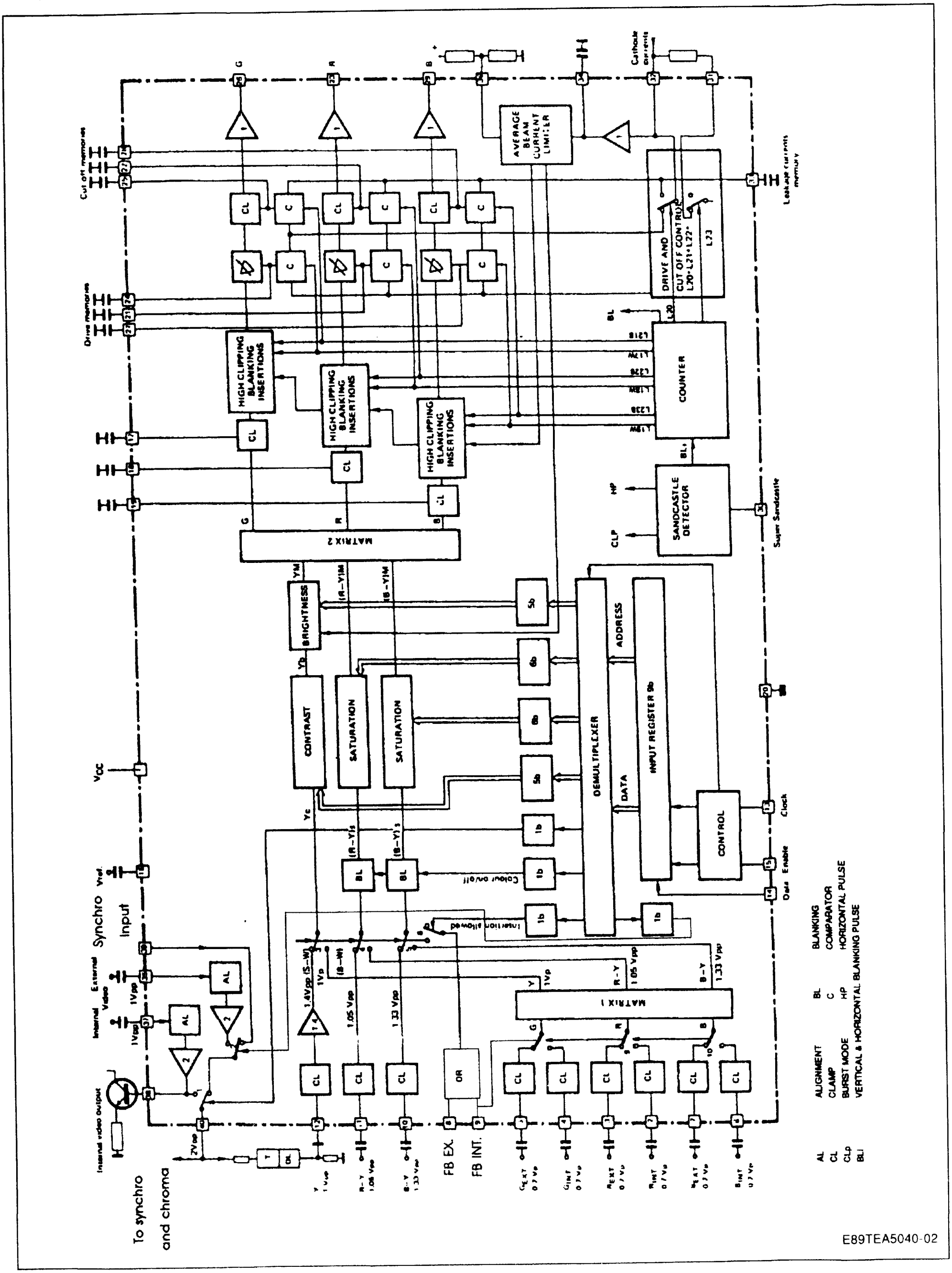


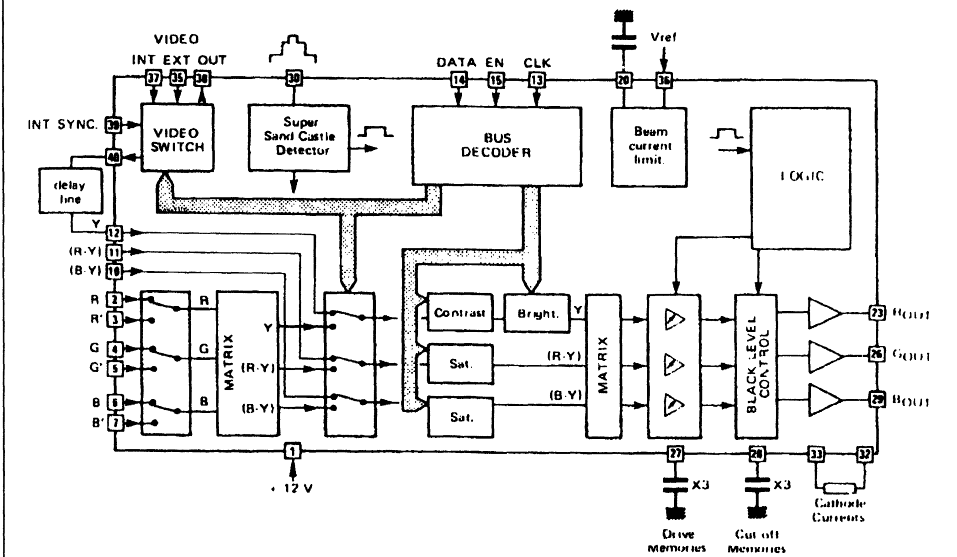
E89TEA5040-01

DESCRIPTION

The TEA5040 is a serial bus controlled videoprocessing device which integrates a complex architecture fulfilling multiple functions.

BLOCK DIAGRAM





E89TEA5040-03

GENERAL DESCRIPTION

BRIEF DESCRIPTION

This new integrated circuit incorporates the following features :

- a synchro and two video inputs
- a fixed video output
- a switchable video output
- normal Y, R-Y, B-Y TV mode inputs
- double set of R, G, B inputs
- brightness, contrast and saturation controls as well on a R, G, B picture as on a normal TV picture
- digital control inputs by means of serial bus
- peak beam current limitation
- average beam current limitation
- automatic drive and cut-off controls

BLOCK DIAGRAM DESCRIPTION

BUS DECODER.

A 3 lines bus (clock, data, enable) delivered by the microcomputer of the TV-set enters the videoprocessor integrated circuit (pins 13-14-15). A control system acts in such a way that only a 9 bit word is taken into account by the videoprocessor. Six of the bits carry the data, the remaining three carry the address of the subsystem.

Function	Address	Number of Bits
Brightness Control	0	5
Contrast Control	1	5
Colour on/off Selection	2	1
Insertion Allowed	3	1
Sync/Async Mode	4	1
Int/Ext Video Switching	5	1
B-Y Saturation Control	6	6
R-Y Saturation Control	7	6

Hereunder are mentioned the different 9 bit words it is necessary to send to each subsystem in order to make it fulfil all its functions.

Subsystem's Configuration		Data Bits LSB....MSB	Add. Bits LSB....MSB
BRIGHTNESS	Min. Max.	X00000 X11111	000
CONTRAST	Min. max.	X00000 X11111	100
COLOUR ON/OFF	Off On	XXXXX0 XXXXX1	010
INSERTION	Allowed Not Allowed	XXXXX0 XXXXX1	110
SYNC/ASYNC MODE	Sync. Async.	XXXX0X XXXX1X	001
VIDEO INT/EXT	Ext. Int.	XXXXX0 XXXXX1	101
SATURATION B-Y	Min. Max.	000000 111111	011
SATURATION R-Y	Min. Max.	000000 1111	111

A demultiplexer directs the data towards latches which drive the appropriate control. More detailed information about serial bus functioning is given in the following chapter.

VIDEO SWITCH

The video switch has three inputs :

- an internal video input (pin 37),
- an external video input (pin 35),
- a synchro input (pin 39),

and two outputs :

- an internal video output (pin 38),
- a switchable video output (pin 40)

The 1Vpp composite video signal applied on the internal video input is multiplied by two and then appears as a 2Vpp low impedance composite video output. This signal is used to deliver a 1Vpp/75Ω composite video signal to the peri-TV plug.

The switchable video output can be any of the three inputs. When the Int/Ext one bit word is high (address number 5), the internal video input is selected. If not, either a regenerated synchro pulse or the external video signal is directed towards this output depending on the level of the Sync/Async one bit word (address number 4). As this output is to be connected to the synchro integrated circuit, RGB information derived from an external source via the TV plug can be displayed on the screen, the synchronization of the TV-set being then made with an external video signal.

When RGB information is derived from a source integrated in the TV-set, a teletext decoder for example, the synchronization can be made either on the internal video input (in case of synchronous data) or on the synchro input (in case of asynchronous data).

R, G, B INPUTS

There are two sets of R, G, B inputs : one is to be connected to the peri-TV plug (Ext R, G, B), the second one receives the information derived from the TV-set itself (Int R, G, B).

In order to have a saturation control on a picture coming from the R, G, B inputs too, it is necessary to get R-Y, B-Y and Y signals from R, G, B information : this is performed on the first matrix that receives the three 0.9Vp (100% white) R, G, B signals and delivers the corresponding Y, R-Y, B-Y signals. These ones are multiplied by 1.4 in order to make the R-Y and B-Y signals compatible with the R-Y and B-Y TV mode inputs. The desired R, G, B inputs are selected by means of 3 switches controlled by the two fast blanking signal inputs. A high level on FB external pin selects the external RGB sources. The three selected inputs are clamped in order to give the required DC level at the output of this first matrix. The three not selected inputs are clamped on a fixed DC level.

Y, R-Y, B-Y INPUTS

The 2Vpp composite video signal appearing at the switchable output of the video switch (pin 40) is driven through the subcarrier trap and the luminance delay line with a 6 dB attenuation to the Y input

(1Vpp ; pin 12). In order to make this 1Vpp (synchro to white) Y signal compatible with the 1Vpp (black to white) Y signal delivered by the first matrix, it is necessary to multiply it by a 1.4 coefficient.

R, G, B INSERTION PULSE (fast blanking)

A R, G, B source has also to provide an insertion pulse. Since this integrated circuit is able to be directly connected to two different sources, it is necessary then to have two separated insertion pulse inputs (pin 8-9). Fast blanking information can be inhibited by the insertion allowed one bit word (address number 3). The two fast blanking inputs carry out an OR function to insert R, G, B sources into TV picture. The external fast blanking (FB ext.) selects the appropriate R, G, B source.

CONTROLS

The four brightness, contrast and saturation control functions are directly made in a digital way without using digital to analog converters.

The contrast control of the Y channel is obtained by means of a digital potentiometer which is an attenuator including several switchable cells directly controlled by a 5 bit word (address number 1). The brightness control is also made by a digital potentiometer (5 bit word, address number 0). Since a + 3dB contrast possibility is required, the Y signal output 0.7Vpp nominal. For both functions, the control characteristics are quasi-linear.

In each R-Y and B-Y channel, a six cell digital attenuator is directly controlled by a 6 bit word (address number 6 and 7). The tracking which is necessary to keep the saturation constant when changing the contrast has to be done externally by the microcomputer. Furthermore, the colour can be completely cancelled, blanking the R-Y and B-Y signals by means of a switch controlled by the colour ON/OFF one bit word (address number 2).

SECOND MATRIX, CLAMP, PEAK CLIPPING, BLANKING

The second matrix receives the Y, R-Y and B-Y signals and delivers the corresponding R, G, B signals. As it is required to have the possibility of + 6dB saturation, an internal gain of 2 is applied on both R-Y and B-Y signals.

A low clipping level is included in order to ensure a correct blanking during the line and frame retraces. A high clipping level ensures the peak beam current limitation. These limitations are correct only if the DC bias of the three R, G, B signals are precise enough. Therefore, a clamp is necessary in each channel because this bias is not kept with enough accuracy in the matrix.

SANDCASTLE DETECTOR AND COUNTER

The three level supersandcastle is used in the integrated circuit to deliver the burst pulse (CLP), the horizontal pulse (HP), and the composite verticaland horizontal blanking pulse (BLI). This last one is regenerated in the conter which delivers a new composite pulse (BL) in which the vertical part lasts 23 lines since the vertical part of the supersandcastle lasts more than 11 lines.

The TEA5040 cannot work properly if this minimum duration of 11 lines is not ensured.

The counter delivers different pulses needed in the integrated circuit and especially the line pulses 17 to 23 used in the automatic drive and cut-off control system.

AUTOMATIC DRIVE AND CUT-OFF CONTROL SYSTEM

Cut-off and drive adjustments are no longer necessary with this integrated circuit as it has a sample and hold feedback loop incorporating the final stages of the TV-set. This system works in a sequential mode. For this purpose, special pulses are inserted in G, R and B channels. During the lines 17, 18 and 19, a "drive pulse" is inserted respectively in the green, red and blue channels. The line 20 is blanked on the three channels. During the lines 21, 22 and 23, a "quasi cut-off pulse" is inserted respectively in the green, red and blue guns.

The resulting signal is then applied to the input of a voltage controlled amplifier. In the final stages of the TV-set, the current flowing in each green, red and blue cathode is measured and sent to the videoprocessor with a current source.

The three currents are added together in a matrix comprised of resistors. By means of this matrix, it is possible to program the ratio between the three currents in order to get the appropriate colour temperature. The output of the matrix forms a high impedance voltage source which is connected to the integrated circuit (pin 32), a lower impedance is grounded by the IC on this pin during the drive pulses (line 17, 18, 19) to keep the measured voltages in the same range.

This is due to the fact that the drive currents are about one hundred times as high as the cut-off and leakage ones.

Each voltage appearing sequentially on the wire pin 32 is then a function of specific cathode current :

- When a current due to a drive pulse occurs, the voltage appearing on the pin 32 is compared within the IC with an internal reference, and the result of the comparison charges or discharges an external appropriate drive capacitor which memorizes the value during the frame. This voltage is applied to a voltage controlled amplifier and the system works in such a way that the pulse current drive derived from the cathode is kept constant.
- During the line 20, the three guns of the picture tube are blanked. The leakage current flowing out of the final stages is transformed into a voltage which is stored by an external leakage capacitor to be used later as a reference for the cut-off current measurement.
- When a current due to a cut-off pulse occurs, the voltage appearing on the pin 32 is compared within the IC to the voltage present on the leakage memory. An appropriate external capacitor is then charged or discharged in such a way that the difference between each measured current and the leakage current is kept constant, that means the quasi cut-off current is kept constant.

AVERAGE BEAM CURRENT LIMITATION

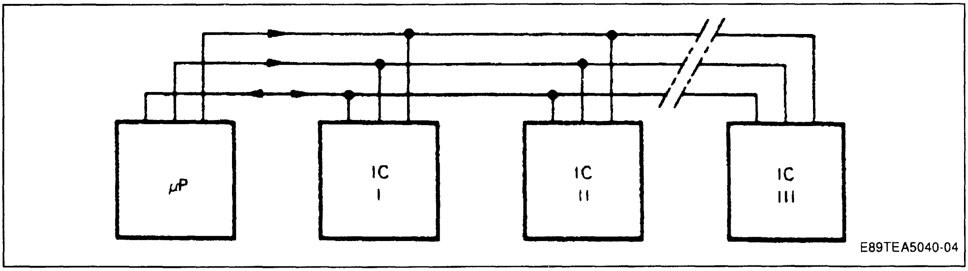
The total current of the three guns is integrated by means of an internal resistor and an external capacitor (pin 34) and then compared with a programmable voltage reference (pin 36). When 70% of the maximum permitted beam current is reached, the drive gain begins to be reduced ; for that purpose, the amplitude of the inserted pulse is increased.

In order to keep enough contrast, the maximum drive reduction is 6dB limited. If it is not sufficient, the brightness is suppressed.

SPECIFICATION FOR THE THOMSON BI-DIRECTIONAL DATA BUS

The bi-directional data bus has three lines (ENABLE, CLOCK, DATA) and is working in series. Transmission on the DATA line is effected bi-directionally. The ENABLE and CLOCK lines are only driven by the microcomputer.

Figure 1 : Peripheral Connections on Bus.



It is possible to select several IC's from the microprocessor via the bus. The identification of each particular IC is achieved by the length of the word (number of data bits/clock impulses), meaning that each IC is responding with its own particular word length.

The number is determined while ENABLE is low and by counting the negative clock edges. As soon as the high edge of the ENABLE signal is applied, the number is fixed (see figure 2).

The reply word lenght from any of the IC's on the bi-directional line is four bits. If it is found insufficient then the reply word can be expanded to include two repetitive reply sequences one after the other.

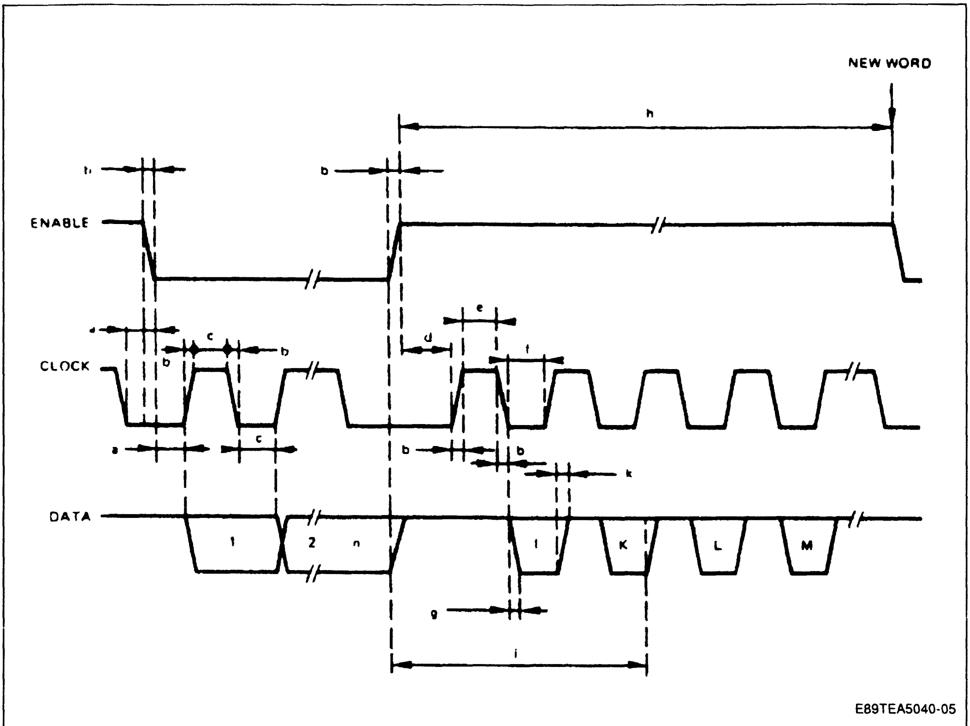
The bi-directional transmission is present :

- If the IC has been previously addressed than at the positive going edge of the enable pulse, the bi-directional function is enabled.
- If ENABLE remains high.
- And DATA is available only during the period when the clock remains low.

- number of identification bits : n
- number of bi-directional clocks : 4

1...n : data from the microcomputer
1...M : data to the microcomputer

Figure 2.



The four bit reply word (synchronized with the clock coming from the microcomputer) from the addressed IC to the microcomputer is sent only once. Subsequent clock pulses present on the clock line will be ignored by the IC in question. The data sent to the microcomputer can generally be suppressed completely or partially, but in the case of the videoprocessor it is necessary to maintain a minimum reply word lenght of 1 (see figure 3).

This implies that a bi-directional bus that incorporates other IC's together with a videoprocessor IC is then also limited by the minimum reply word restriction of 1.

The data word from the microcompter is divided into :

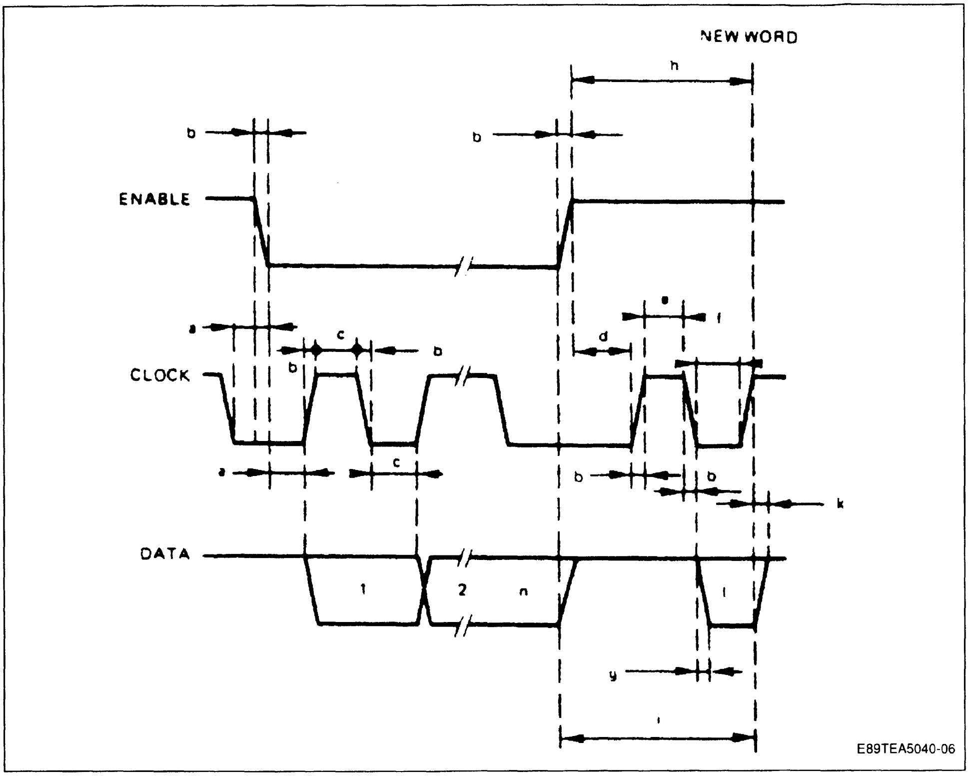
- addresses within the IC
- data

The data word to the microcomputer is divided into

- two data bits,
- two address bits

After the operating voltage is applied, the first transmission will be used as a reset command, that means that the data word will not be detected.

Figure 3.



- number of identification bits : n 1...n : data from the microcomputer
- number of bi-directional clocks : 1 1 : data the microcomputer (which is the minimum number for the videoprocessor)

BI-DIRECTIONAL DATA BUS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	TIMING Identification nr-9 (9 video processor address) (see figures 2-3)				
a		5			µs
b		0			µs
c		5			µs
d		70			µs
e					
f					
g					
h	(new word to same IC)	24			ms
h	(new word to other IC)	70			µs

ABSOLUTE MAXIMUM RATINGS

T_{AMB} = 25°C (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	14		V
T_{OPER}	Operating Temperature Range	0	+ 60	°C
T_{STG}	Storage Temperature Range	– 25	+ 125	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambiant Thermal Resistance	Max	55	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{AMB} = 25°C, V_{CC} = 12V (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	10.8	12	12.5	V
I_{CC}	Supply Current Pin 1		80	104	mA
	Video Switch				
	External Video Input (75Ω source impedance)				
V_{35}	Signal Amplitude Pin 35		1	1.4	
I_{35}	Input Current Pin 35		10	30	Vpp
					µA
	Internal Video Input (300Ω source impedance)				
V_{37}	Signal Amplitude Pin 37		1	14	Vpp
I_{37}	Input Current Pin 37		10	30	µA
	Synchro Input				
	Output Signal Amplitude Pin 39 (for a 0.5V to 2.5V input signal on pin 39)	0.5	0.6		V
	Internal Video Output Pin 38				
	Dynamic	2.7			Vpp
	DC Level (bottom of synchro pulse)	1		2	V
	Gain between Pin 38 and Pin 37 (for 1Vpp on pin 37)	5	6	7	dB
	Crosstalk between Pin 35 and Pin 38			50	dB
	Bandwidth (– 1dB)	6			MHz
	Switchable Video Output Pin 40				
	Dynamic (pin 35 or pin 37 selected)	2.7			Vpp
	Gain between Pins 35-40 (for 1VPP on pin 35)	5		7	dB
	Gain between Pins 37-40 (for 1VPP on pin 37)	5		7	dB
	Crosstalk between Pins 35-40			– 50	dB
	Crosstalk between Pins 37-40			– 50	dB
	Bandwidth (– 1dB)	6			MHz
	TV Mode Inputs				
	Luminance Input Pin 12				
Y	Signal Amplitude (100% white)		1	1.5	V_{pp}
V_{12}	DC Level (on black level)		4		V
I_{12}	Input Current			10	µA
	R-Y Input Pin 11				
R-Y	Signal Amplitude (75% saturation)		1.05	1.47	V_{pp}
V_{11}	DC Level (on black level)		4.7		V
I_{11}	Input Current			2	µA
	B-Y Input Pin 10				
B-Y	Signal Amplitude (75% saturation)		1.33	1.86	V_{pp}
V_{10}	DC Level (on black level)		4.7		V
I_{10}	Input Current			2	µA
	RGB Inputs Pins 2-3-4-5-6-7				
	Signal Amplitude (100% saturation without synchro pulse)		0.7	1	V_{pp}
	DC Level (on black level)		3.2		V
	Input Current			3	µA

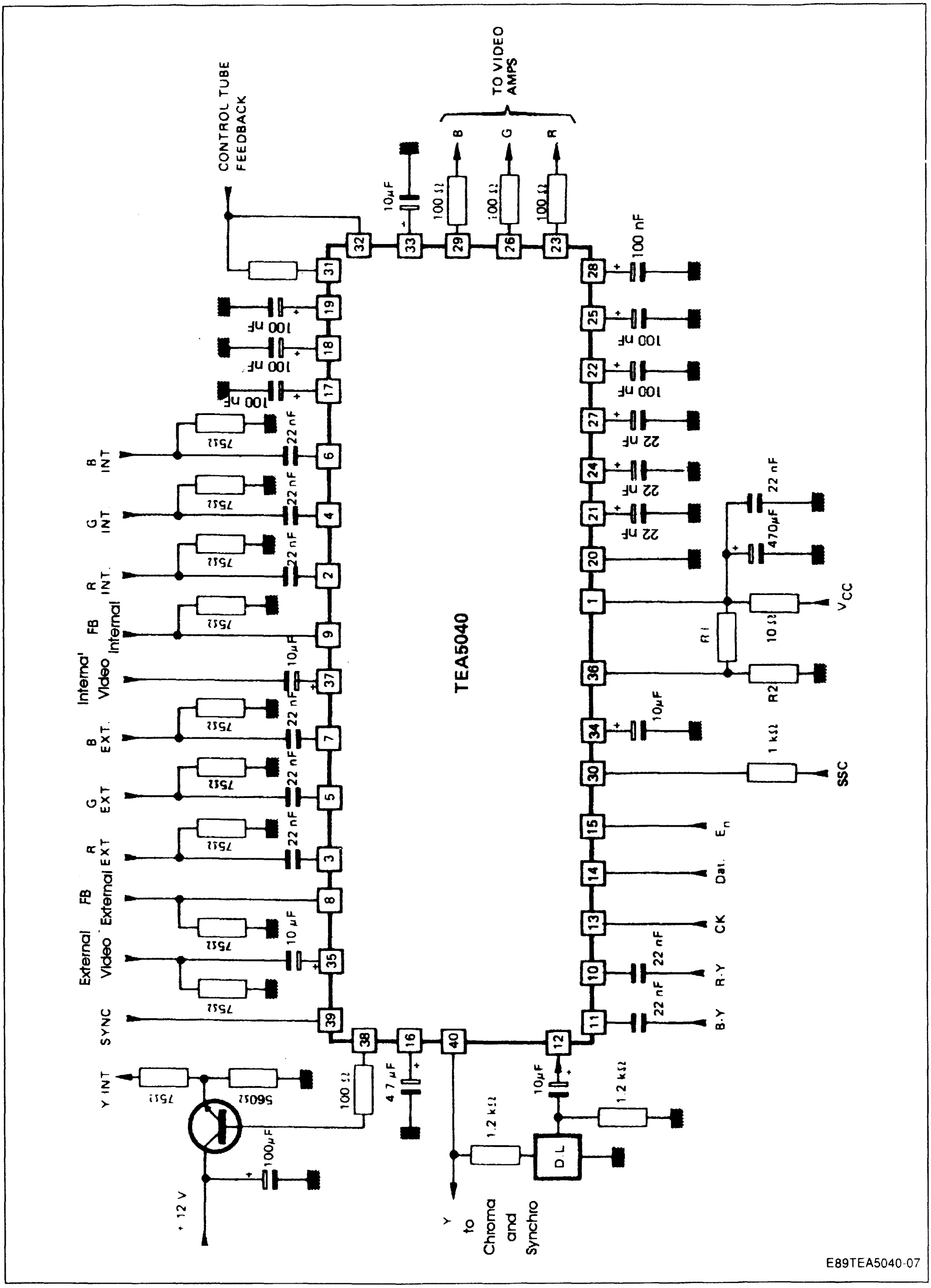
ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Fast Blanking Inputs Pins 8-9				
	TV/RGB Mode Threshold	0.5		0.9	V
	Switching Time		70		ns
	Switching Time Delay		70		ns
	Clamp Memory Output Pins 17-18-19				
	Voltage Range	8	10	11	V
	Input Current			2	µA
V_{REF}	**Reference Voltage Pin 16**		4		V
	Sandcastle Input Pin 30				
	Blanking Threshold	1	1.4	1.8	V
	Burst Gate Threshold	6.4	6.9	7.6	V
	Line Retrace Threshold	3.1	3.4	3.8	V
	Input Current Pin 30 Grounded			100	µA
	Drive and Cut-off Memory Output Pins 21-22-24-25-27-28				
	Drive Leakage Current Pins 21-24-27			1	µA
	Cut-off Leakage Current Pins 22-25-28			1	µA
	Minimum Active Level Pins 22-25-28		4		V
	Leakage Current Memory Output Pin 33				
	Voltage Range	3			V
	Input Current (during picture pin 33 = 5V)			0.5	µA
	Charging Output Impedance			500	Ω
	Minimum Voltage (pin 32 grounded)		3		V
	Cathode Currents Input Pin 32				
	Output Current during the Line Trace (pin 32 grounded)			10	µA
	Voltage during Lines 17, 18, 19		0.4		V
	Voltage Difference during Lines 21, 22, 23 and during Line 20		0.4		V
	Voltage Amplitude on Cathode Currents Input for Drive Decrease Threshold 10% on Drive/cut-off				
V32	1V on Pin 36		0.7		V
V32	2V on Pin 36		1.4		V
	Voltage Amplitude on Cathode Currents Input for Brightness Decrease Threshold				
V32	1V on Pin 36		1		V
V32	2V on Pin 36		2		V
	Impedance SWITCH Pin 31				
	Saturation Impedance [for 5mA] (open during lines 20, 21, 22, 23)		250		Ω
	Reference Voltage Input for the Average Beam Current Limiter Pin 36				
V36	Reference Voltage	0		5	V
I36	Input Current (V36 = 1V)			– 20	µA
	Average Beam Current FILTER Pin 34 Voltage Range 0 < V32 < 7V	6			V

ELECTRICAL OPERATING CHARACTERISTICS (cont'd)

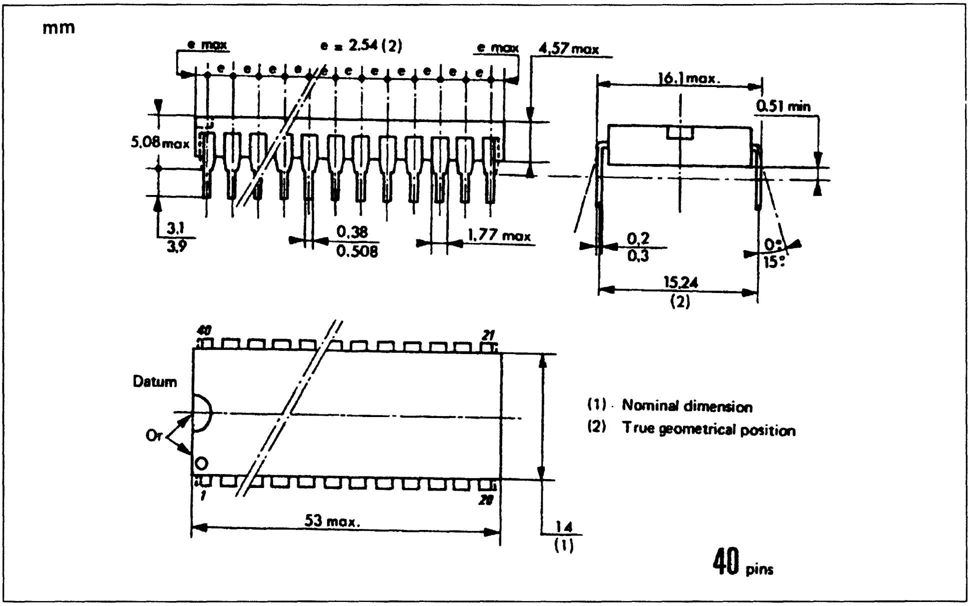
Symbol	Parameter	Min.	Typ.	Max.	Unit
	RGB Outputs R (pin 23), G (pin 26), B (pin 29) Inserted Levels Low Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)		45		%
	High Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)		115		%
	Drive Inserted Level Referred to quasi Cut-off Inserted Level (without beam limitation, V36 = 6V, V32 grounded)		35		%
	Bandwidth (– 3dB) (TV mode and R, G, B mode)		10		MHz
	Crosstalk for any of the 11 Inputs Pins 2-3-4-5-6-7-10-11-12-35-37 on any of the 5 Outputs Pins 23-26-29-38-40 (range : DC to 1MHz)			– 50	dB
	Brightness Nominal Brightness Referred to quasi Cut-off Inserted Level (bit word "10000" address = 0)		– 25		%
	Total Brightness Range (100 % = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		78		%
	Maximum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		38		%
	Minimum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)		– 40		%
	Differential Brightness between any two Channels (TV mode, colour off, pins 10-11-12 AC grounded, 0.5 (W/B) signal on pin 12, maximum contrast = 100% on RGB outputs)			2*	%
	Variation of the Differential Brightness (in the whole saturation control range (including colour off))			0.5*	%
	Contrast : Max. Contrast Attenuation	11			dB
	Saturation Max. Saturation Max. Saturation Attenuation Colour off Attenuation	 20 40	 6		 dB dB dB
	Output Signal Amplitude Pins 23-26-29 (blanking to high clipping) • Y Input : 0.7V B/W • 0dB Contrast, Bit Word = 010110, Address = 1 • Maximum Brightness • Maximum Drive Efficiency (pins 21-24-26-27 grounded) • No Average Beam Current Limitation (pin 36 to 6V)		6.2		V
	Black to White Output Voltage Y Input : 0.5V (B/W) Maximum Contrast (pin 36 to 6V, pins 21-24-27 grounded)		3.6		V
	Drive Efficiency Ratio : $\frac{\text{VOUT (pins 21-24-27 grounded)}}{\text{VOUT (pins 21-24-27 to VCC)}}$ (no average beam current limitation pin 36 to 6V)		3.4		
	Black Level Control (variable DC voltage from 4V to VCC on pins 22-25-28)	4.3			V
 VHL VLL	**Bus Inputs Pins 13-14-15** High Level Low Level	 3.5		 1	 V V

* To be confirmed.


TEA5040
CONTROL TUBE FEEDBACK
TO VIDEO AMPS
B
G
R
100 Ω
10μF
100 nF
22 nF
470μF
10 Ω
R1
R2
1 kΩ
V_{CC}
SSC
E_n
Dat.
CK
R-Y
B-Y
B INT
G INT
R INT.
FB Internal
Internal Video
B EXT.
G EXT
R EXT
FB External
External Video
SYNC
Y INT
75Ω
560Ω
4.7 μF
100μF
+ 12 V
1.2 kΩ
D.L
Y to Chroma and Synchro
E89TEA5040-07

PACKAGE MECHANICAL DATA

40 PINS – PLASTIC DIP



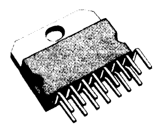
SGS-THOMSON
MICROELECTRONICS

TEA5101A

RGB HIGH VOLTAGE VIDEO AMPLIFIER

ADVANCE DATA

- BANDWIDTH : 10 MHz TYPICAL
- RISE AND FALL TIME : 50 ns TYPICAL
- CRT CATHODES CURRENT OUTPUTS FOR PARALLEL OR SEQUENTIAL CUT-OFF OR DRIVE ADJUSTMENT
- FLASHOVER PROTECTION
- POWER DISSIPATION : 3.5 W
- ESD PROTECTED



SIL15
(Plastic Package)

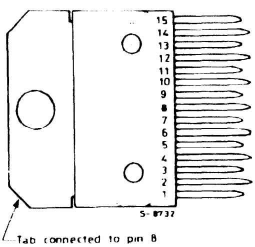
ORDER CODE : TEA5101A

DESCRIPTION

The TEA5101A includes three video amplifiers designed with a high voltage DMOS/bipolar technology. It drives directly the three CRT cathodes. The device is protected against flashovers. Due to its three cathode current outputs, the TEA5101A can be used with both parallel and sequential sampling applications.

PIN CONNECTION

1 Blue input
2 V_{CC} low voltage
3 Green input
4 Red input
5 V_{DD} high voltage
6 Red cathode current
7 Red output
8 Ground

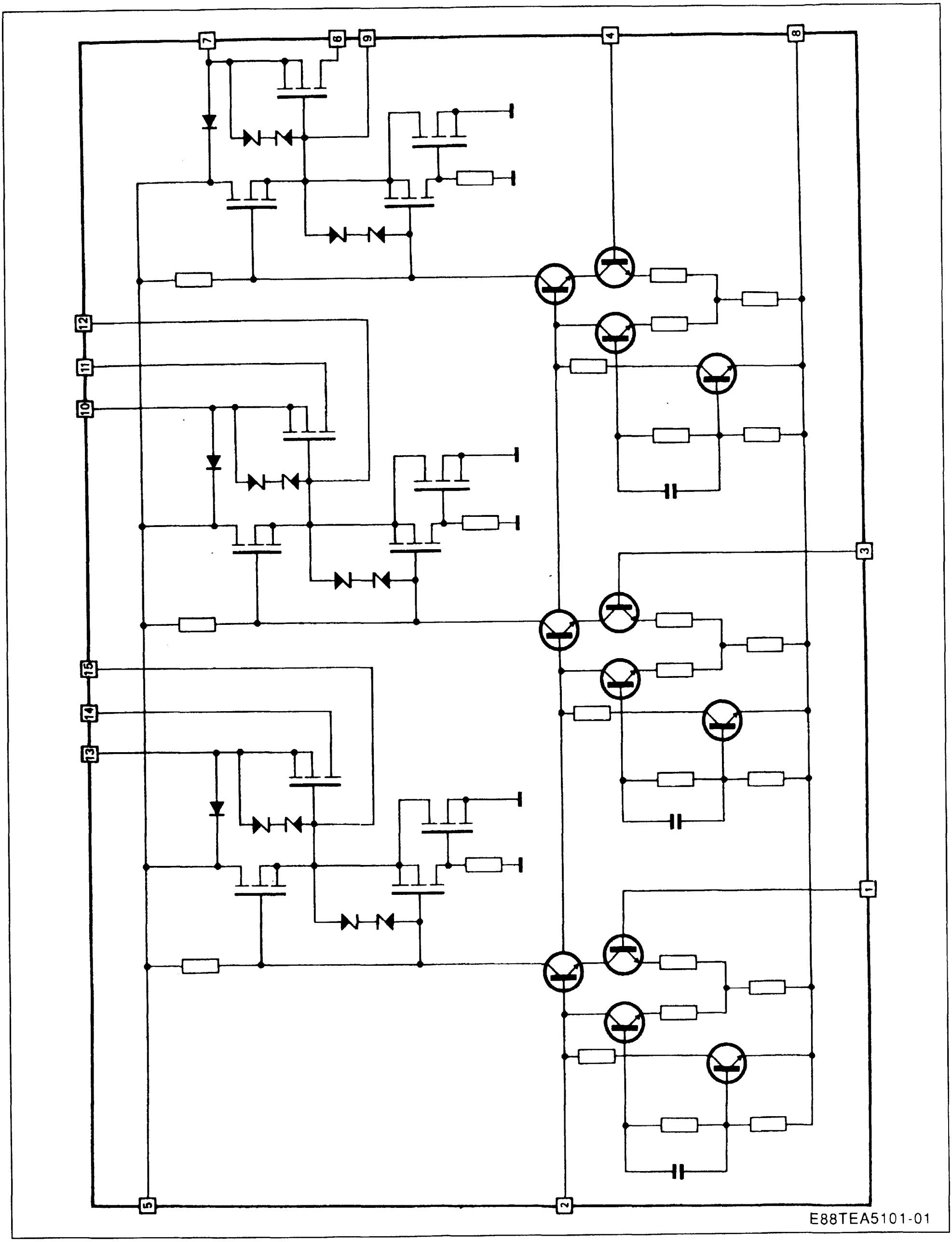


9 Red feedback
10 Green output
11 Green cathode current
12 Green feedback
13 Blue output
14 Blue cathode current
15 Blue feedback

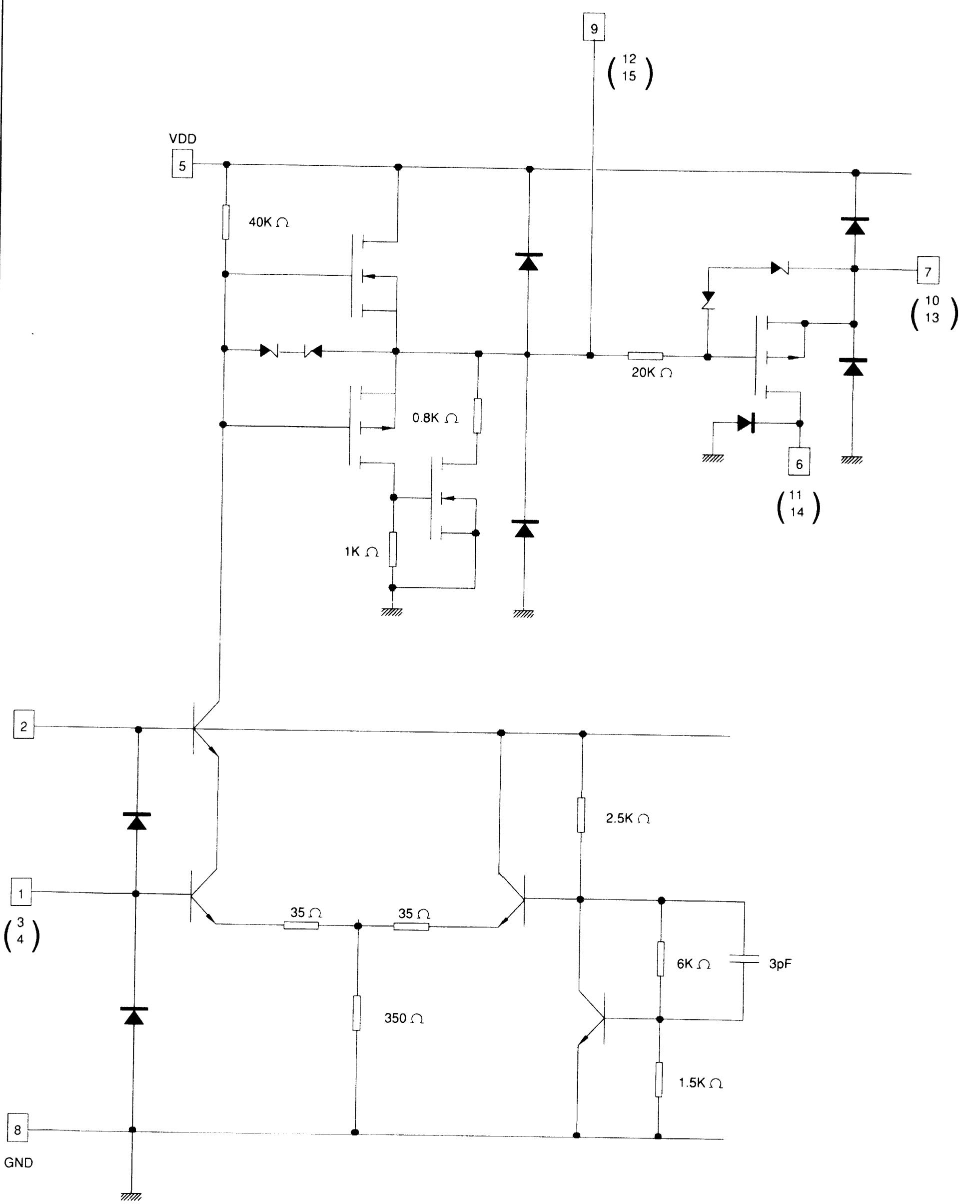
This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

CIRCUIT DESCRIPTION

BLOCK DIAGRAM



BLOCK DIAGRAM OF EACH CHANNEL

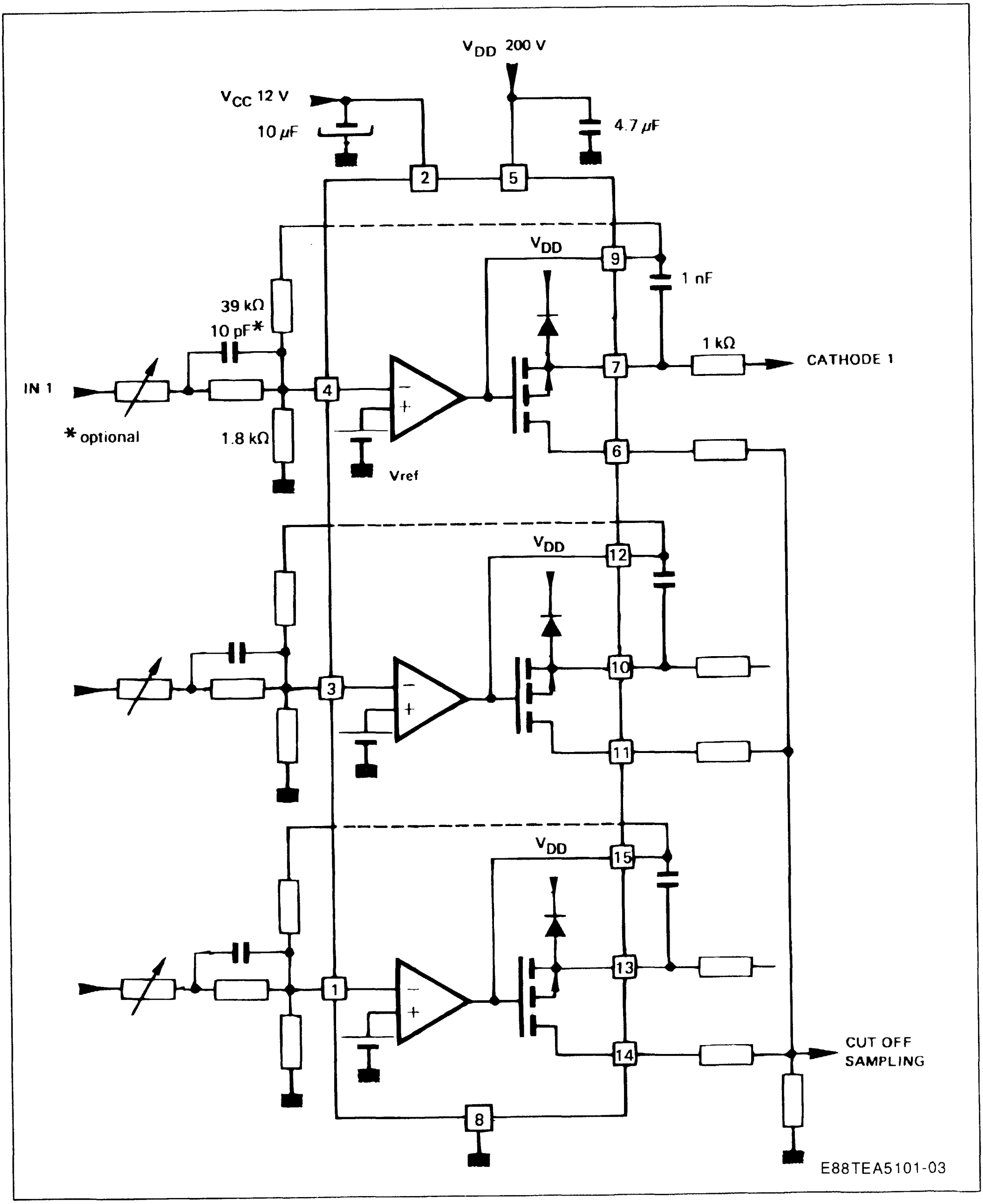


E88TEA5101-02

TYPICAL APPLICATION

The TEA5101A consists of three independent amplifiers. Each of them includes :

- A differential amplifier, the gain of which is fixed by external feedback resistors,
- A voltage reference,
- A PMOS transistor providing a copy of the cathode current,
- A protection diode against CRT arc discharges.



PIN FUNCTION

N°	Function	Description
1	Blue Input	Input of the "blue" amplifier. It is a virtual ground with 3.8 V bias voltage, 15 microamperes input bias current with 14 kΩ input resistance.
2	V_{CC}	Low voltage power supply, typically 12 V.
3	Green Input	See pin 1.
4	Red Input	See pin 1.
5	V_{DD}	High voltage power supply, typically 200 V.
6	Red Cathode Current	Provides the video processor with a copy of the DC current flowing into the red cathode, for automatic cut-off or gain adjustment. If this control is not used, pin 6 must be grounded.
7	Red Output	Output driving the red cathode. Pin 7 is internally protected against CRT arc discharges by a diode limiting the output voltage to V_{DD}.
8	Ground	Also connected to the heat sink.
9	Red Feedback	Output driving the feedback resistor network for the red amplifier.
10	Green Output	See pin 7.
11	Green Cathode Current	See pin 6.
12	Green Feedback	See pin 9.
13	Blue Output	See pin 7.
14	Blue Cathode Current	See pin 6.
15	Blue Feedback	See pin 9.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{DD}	Supply High Voltage	Pin 5	250	V
V_{CC}	Supply Low Voltage	Pin 2	35	V
	Output Current	Pins 7 - 10 - 13		
I_O	to V_{DD}		Protected	
I_O	to Ground		8	mA
	Output Current	Pins 9 - 12 - 15		
I_F	to V_{DD}		45	mA
I_F	to Ground		45	mA
I_i	Input Current	Pins 1 - 3 - 4	60	mA
T_j	Junction Temperature		150	°C
T_{oper}	Operating Ambient Temperature		0 to 70	°C
T_{stg}	Storage Temperature		– 55 to + 150	°C

THERMAL DATA

$R_{th}(j\text{-}c)$	Maximum Junction Case Thermal Resistance	Max 3	°C/W
$R_{th}(j\text{-}a)$	Typical Junction Ambient Thermal Resistance	Typ 35	°C/W

ELECTRICAL CHARACTERISTICS T_{amb} = 25 °C ; V_{CC} = 12 V ; V_{DD} = 200 V ; AV = 50
(unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	High Supply Voltage	Pin 5		200	220	V
V_{CC}	Low Supply Voltage	Pin 2	10	12	15	V
I_{DD}	High Voltage Supply Internal DC Current (V_{out} 100 V) (without the current due to the feedback network)	Pin 5		8	12	mA
V_{sath}	Output Saturation Voltage (High level) I_O = – 10 µA	Pins 7 - 10 - 13		3	10	V
R_{ON}	Output Mos Transistor (Low level) R_{ON} @ I_O = 3 mA	Pins 7 - 10 - 13		1.7		kΩ
BW	Bandwidth (– 3 db) (measured on CRT cathodes) (C_{LOAD} : 10 pF – R Protect = 1 kΩ – V_{out} = 100 V) Δ V_{out} : 50 V_{PP} Δ V_{out} : 100 V_{PP}			 10 8		 MHz MHz
T_R - T_F	Rise Time and Fall Time : measured between 10 % and 90 % of output pulse (C_{LOAD} : 10 pF – R Protect = 1 kΩ – V_{out} = 100 V) Δ V_{out} : 100 V_{PP}			50		ns
G_O	Open Loop Gain		47	50		dB
P	Internal Power Dissipation (see calculation below)			3.5		W
V_{REF}	Internal Voltage Reference	Pins 1 - 3 - 4	3.55	3.8	4.05	V
	Internal Reference Voltage Difference Between 2 Channels				3	%
	Voltage Reference Temperature Coefficient			– 5		mV/°C
I_{IB}	Input Bias Current (V_{out} : 100 V)	Pins 1 - 3 - 4		15		µA
R_I	Input Resistance			14		kΩ

APPLICATION INFORMATIONS

PC BOARD LAYOUT

The best performances of the high voltage video amplifier will be obtained only with a carefully designed PC board. Output to input capacitances are of particular importance.
For a single amplifier, the input-output capacitance, in parallel with the relatively high feedback resistance, creates a pole in the closed-loop transfer function. A low parasitic capacitance (0.3 pF) feedback resistor and HF isolated printed wires are necessary. Further more, capacitive coupling from the output of an amplifier toward the input of another one may induce excessive crosstalk.

POWER DISSIPATION

The power dissipation consists of a static part and a dynamic part. The static dissipation varies with the output voltage. With VDD = 200 V, P_{stat} = 2.6 W typ(3.5 W max) at V_{out} = 100 V, 1.5 W typ at 150 V and 3 W typ at 50 V (with R feedback = 39 k ohms).
Vout first value (100 V) will be the reference.
The dynamic dissipation depends on the signal spectrum and the load capacitance.

- Dynamic power with a typical picture with 150 V_{pp} modulation is typically 1 W.
- For a sine wave, dynamic dissipation per amplifier is $P_d = F \times C_l \times V_{opp} \times V_{dd} \times 0.8$.

The load capacitance CL includes CRT and board capacitance (10 pF), and amplifier output capacitance (8 pF) : total CL value is about 20 pF. For a 5 MHZ, 50 V_{pp} sine wave and a 20 pF load capacitance, the maximum dynamic power is 2.5 W.

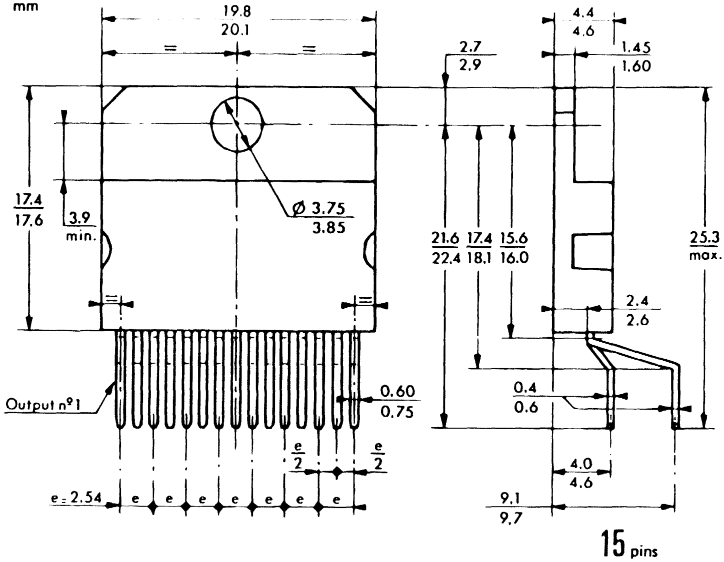
- Generally, the maximum dynamic power is reached with a white noise (tuner noise).
- Typical value is about 2 W.

Total dissipation is typically 3.6 W (2.6 W + 1 W). With a maximum static dissipation of 3.5 W, total dissipation is :

- 4.5 W with a typical picture (UER pattern)
- 5.5 W with white noise

PACKAGE MECHANICAL DATA

15 PINS – PLASTIC SIP



SGS-THOMSON MICROELECTRONICS

TEA5110

LOW DROP-OUT 5V DUAL VOLTAGE REGULATOR

- OUTPUT CURRENT OF BOTH REGULATORS : 100 mA GUARANTEED
- INTERNAL SHORT-CIRCUIT AND THERMAL PROTECTION
- FIRST REGULATOR OUTPUT : LOW DISCHARGE CURRENT
- SECOND REGULATOR OUTPUT : SWITCHED-OFF WITH ACTIVE DISCHARGE
- RESET OUTPUT WITH ADJUSTABLE PULSE WIDTH

DESCRIPTION

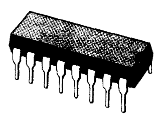
The TEA5110 is a dual positive 5V voltage regulator specially designed to supply a microprocessor and associated circuits.

The first regulator supplies the microprocessor in normal operating conditions. In standby mode, the regulator has a very high output impedance (current drain less than 1 µA) and the microprocessor may be powered by a battery.

The second regulator supplies the peripherals and provides a halt signal to the microprocessor to turn it in standby mode.

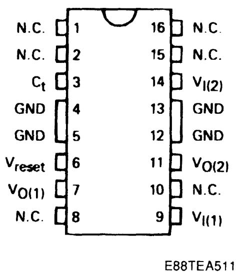
The circuit generates a reset pulse when :

- the supply voltage is applied to the circuit and the output of the second regulator is at its nominal value, and
- when the output of the second regulator is at its nominal value again after a shut-down on the output of the first regulator (see figure 2 page 4).



TEA5110
BATWING DIP16
(Plastic Package)

PIN CONNECTIONS



E88TEA5110-01

1 -	N.C.	
2 -	N.C.	
3 -	C_t	: Time constant capacitor
4 -	GND	: Ground
5 -	GND	: Ground
6 -	V_{reset}	: Reset output
7 -	$V_{O(1)}$	: Output voltage 1
8 -	N.C.	
9 -	$V_{I(1)}$	: Input voltage
10 -	N.C.	
11 -	$V_{O(2)}$	: Output voltage 2
12 -	GND	: Ground
13 -	GND	: Ground
14 -	$V_{I(2)}$	: Input voltage 2
15 -	N.C.	
16 -	N.C.	

ABSOLUTE MAXIMUM RATINGS

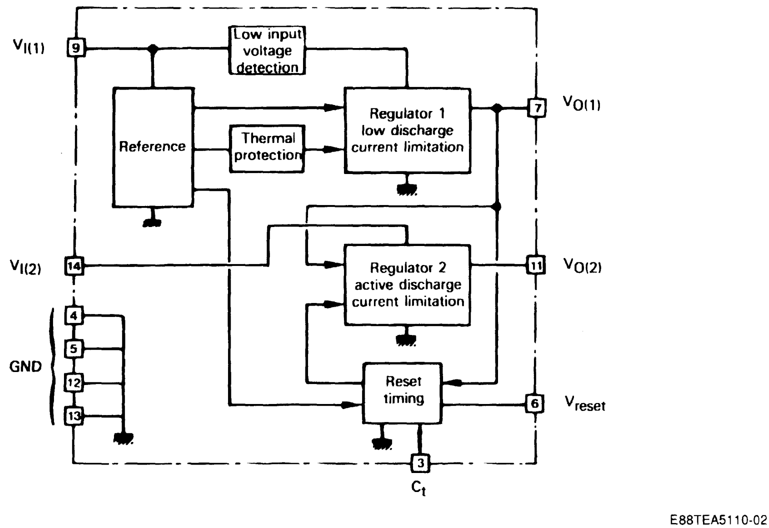
Symbol	Parameter	Value	Unit
V_I	Input Voltage	20	V
I_O	Output Current	Internally Limited	A
P_{tot}	Power Dissipation	Internally LImited	W
T_{oper}	Operating Ambient Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C

THERMAL DATA

$R_{th\,(j\text{-}a)}$*	Junction–ambient Thermal Resistance	45	°C/W
$R_{th\,(j\text{-}c)}$	Junction–case Thermal Resistance	11	°C/W

* The $R_{th(j\text{-}a)}$ is measured on devices soldered on 35 µm thick copper surface of 40 cm2.

BLOCK DIAGRAM



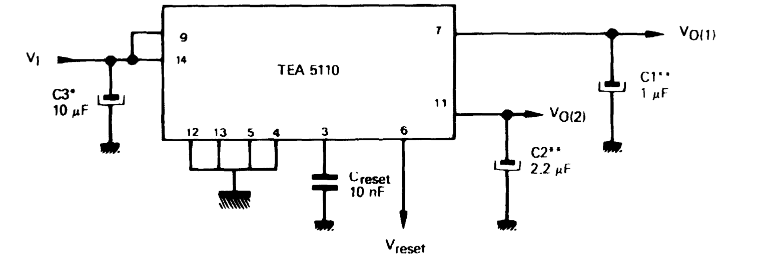
ELECTRICAL CHARACTERISTICS

T_j = + 25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{O(1)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA)	4.9	5.05	5.2	V
$V_{O(2)}$	Output Voltage (+ 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(2)}$ ≤ 100 mA)	4.8	5	5.2	V
$V_{O(1)}$–$V_{O(2)}$	Output Voltage Difference + 7 V ≤ V_I ≤ + 18 V, 0 ≤ $I_{O(1)}$ ≤ 100 mA, 0 ≤ $I_{O(2)}$ ≤ 100 mA	0	50	100	mV
 $K_{VI(1)}$ $K_{VI(2)}$	Line Regulation + 6.8 V ≤ V_I ≤ + 18 V, $I_{O(1)}$ = 50 mA + 6.8 V ≤ V_I ≤ + 18 V, $I_{O(2)}$ = 50 mA		 10 20	 50 50	 mV mV
 $K_{VO(1)}$ $K_{VO(2)}$	Load Regulation 5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V 5 mA ≤ $I_{O(2)}$ ≤ 100 mA, V_I = + 10 V		 10 20	 50 50	 mV mV
I_Q	Quiescent Current (+ 6.8 V ≤ V_I ≤ + 18 V, $I_{Q(1)}$ = $I_{Q(2)}$ = 0)		6	8	mA
 $I_{SC(1)}$ $I_{SC(2)}$	Short–circuit Current V_I = + 10 V, 0 ≤ $V_{O(1)}$ ≤ + 5 V V_I = + 10 V, 0 ≤ $V_{O(2)}$ ≤ + 5 V		 200 200		 mA mA
 V_I–$V_{O(1)}$ V_I–$V_{O(2)}$	Minimum Dropout Voltage - (note 1) Output 1 $I_{O(1)}$ = 0 $I_{O(1)}$ = 0.1 A Output 2 $I_{O(2)}$ = 0 $I_{O(2)}$ = 0.1 A		 1.4 1.6 1.5 1.7		 V V V V
$I_{dis(1)}$	$V_{O(1)}$ Discharge Current (V_I = 0. $V_{O(1)}$ = + 5 V)			1	µA
	Minimum Input Voltage to Switch on $V_{O(2)}$ Output (fig. 1, note 2)	(V_{O1}+1.4)	(V_{O1}+1.6)	(V_{O1}+1.8)	V
ΔV_{IL}	Input Hysteresis to Switch off $V_{O(2)}$ Output (fig. 1)	200	300	400	mV
	Minimum $V_{O(1)}$ Output Voltage to Switch on $V_{O(2)}$	4.5	4.6	4.7	V
$\Delta V_{C(1)}$	$V_{O(1)}$ Hysteresis Voltage to switch off $V_{O(2)}$ (fig. 2)	30	50	70	mV
$V_{L(02)}$	$V_{O(2)}$ Low Output Voltage (active discharge) V_I = + 10 V, $I_{O(2)}$ = – 90 mA V_I = + 10 V, $I_{O(2)}$ = – 10 mA		 1.3 120	 1.6 180	 V mV
$V_{L(reset)}$	Reset Low Output Voltage (V_I = + 10 V, I_{reset} = – 16 mA)		120	400	mV
$V_{H(reset)}$	Reset High Output Voltage (V_I = + 10 V, I_{reset} = 1 mA)	$V_{O(2)}$–1V		$V_{O(2)}$	V
t_{reset}	Reset Pulse Duration (V_I = + 10 V, C_{reset} = 10 nF) – Note 3	4	8	16	ms
KVT	Average Temperature Coefficient of Output Voltage (T_j = 0 °C to – 70 °C)		0.5		mV/°C
θ	Thermal Shut Down Temperature	110			°C
SVR	Supply Voltage Rejection Ratio V_I = + 12 V, ΔV_I = 4 Vpp, I_O = 10 mA, f = 100 Hz		50		dB

Notes : 1. The dropout voltage (input-output voltage difference) is measured when the output voltage has dropped 100 mV from the nominal value obtained at 10 V input voltage.
Dropout voltage is dependent upon load current and junction temperature.
2. $V_{O(1)}$ voltage is measured at 10 V input voltage.
3. t_{reset} (ms) = 0.8 C_{reset} (nF).

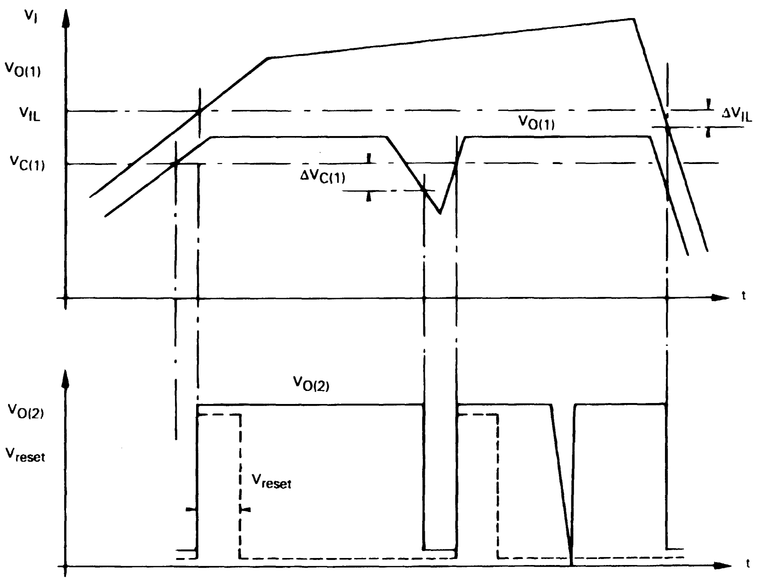
Figure 1 : Typical Application and Test Circuit.



C1, C2, C3 solid tantalum capacitors.
* Required when the circuit is far from power supply capacitors.
** Required for current limitation stability.

E88TEA5110-03

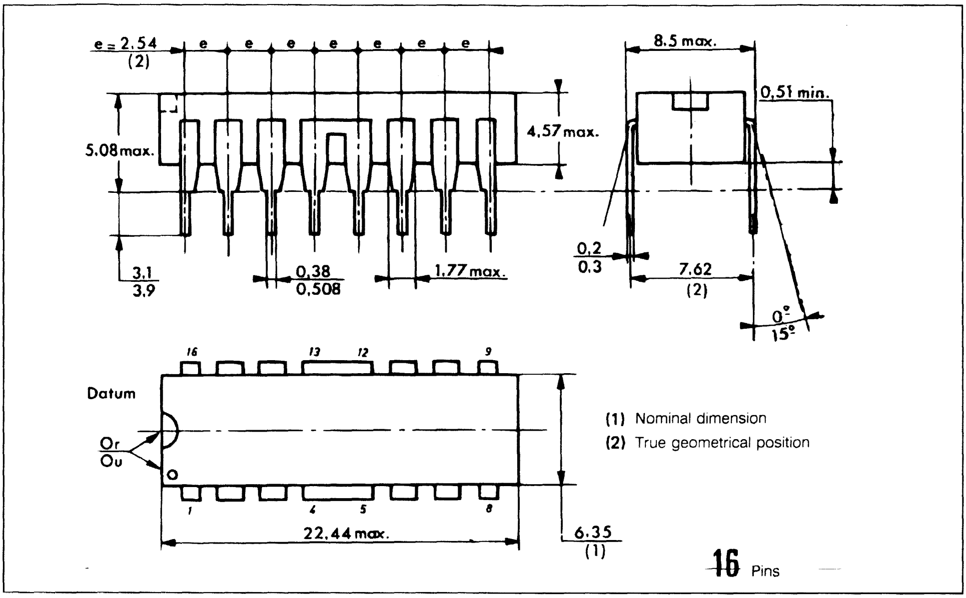
Figure 2 : Dynamic Characteristics of $V_{O(1)}$, $V_{O(2)}$, V_{reset} Outputs.



E88TEA5110-03

PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP

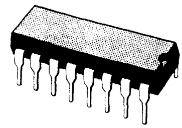


SGS-THOMSON MICROELECTRONICS

TEA5114A

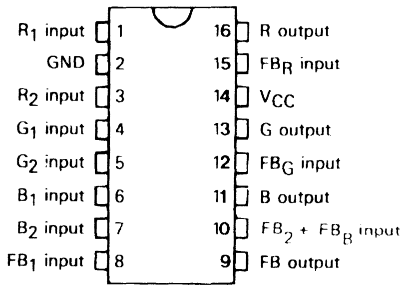
RGB SWITCHING CIRCUIT

- 25 MHz BANDWIDTH
- CROSSTALK : 55 dB
- SHORT CIRCUIT TO GROUND OR V_{CC} PROTECTED
- ANTI SATURATION GAIN CHANGING
- VIDEO SWITCHING



TEA5114A
DIP 16
(Plastic package)

PIN CONNECTIONS



E88TEA5114A-02

DESCRIPTION

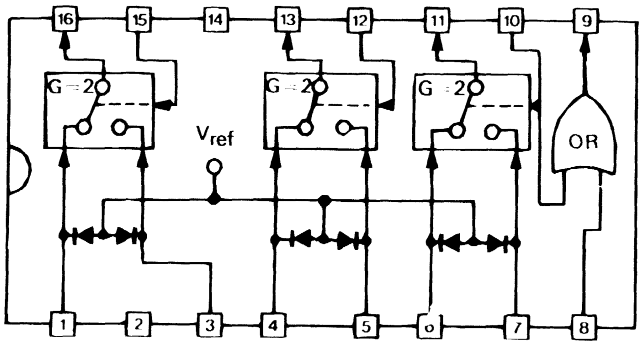
This integrated circuit provides RGB switching allowing connections between peri TV plug, internal RGB generator and video processor in a TV set.

The input signal black level is tied to the same reference voltage on each input in order to have no differential voltage when switching two RGB generators.

An AC output signal higher than 2 Vpp makes gain going slowly down to 0 dB to protect the TV set video amplifier from saturation.

Fast blanking output is a logicial OR between FB1 (Pin 8) and FB2 (Pin 10).

BLOCK DIAGRAM



E88TEA5114A-01

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	18	V
T_j	Junction Temperature	– 40 to 150	°C
T_{stg}	Storage Temperature	– 40 to 150	°C
Z_L	Minimum Load Resistor on Each Output V_{CC} = 12 V $V_{CC} \doteq 10$ V	300 150	Ω Ω
T_{amb}	Operating Ambient Temperature	0 to 70	°C

THERMAL DATA

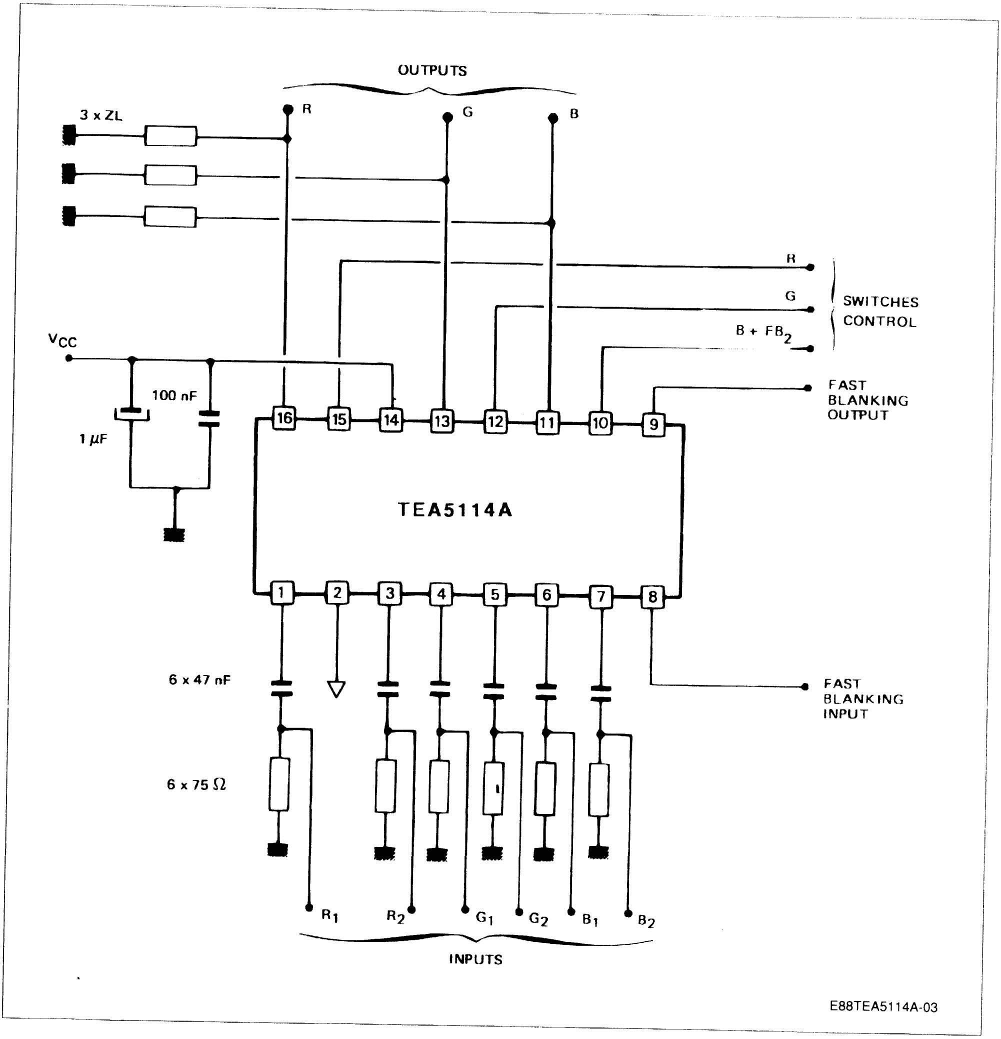
$R_{th\,(j\text{-}a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 12 V, Z_L (RGB) = 300 Ω
V_{CC} = 10 V, Z_L (RGB) = 150 Ω (unless otherwise specified)

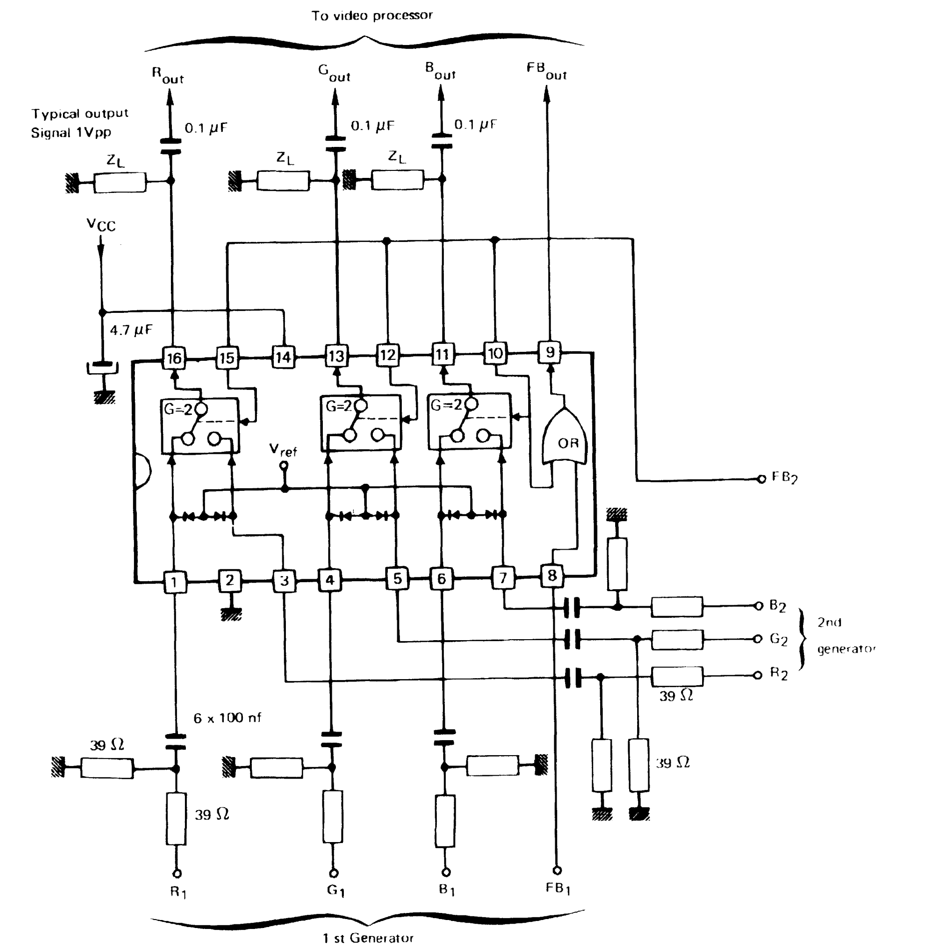
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	9	12	13.2	V
I_{CC}	Supply Current without Load V_{CC} = 12 V	20	30	40	mA
V_{ON}	Black Level Output Voltage (on pins 11, 13, 16 square wave output signal 1 kHz - 1 Vpp) T_j = 25 °C (5mV/°C typical variation)	1.8	2.5	2.9	V
G_{RGB}	Gain of Each Channel Pins 11, 13, 16 F = 1 MHz , V_{in} = 0.5 V_{pp}	5	5.5	6	dB
B_{RGB}	Bandwidth (– 3 dB) V_O = 1 V_{pp}	20	25		MHz
V_{GC}	Threshold Output Voltage for Gain Changing (– 0.5 dB)	2			V_{pp}
V_R	Video Rejection between Two Inputs R, G or B F = 1 MHz Sinus V_O = 1 V_{pp}	50	55		dB
Z_{IRGB}	Input Impedance on Pins 1, 3, 4, 5, 6, 7 V_O = 1 V_{pp}	10			kΩ
Z_{ORGB}	R, G, B Output Impedance on Pins 11, 13, 16			15	Ω
T_{FB}	FB rising and falling time on pin 9. 1 Vpp Input Voltage Pins 8, 10		20		ns
V_{IHFB}	FB High Level Input Voltage on Pins 8, 10, 12, 15	1		4	V
V_{ILFB}	FB Low Level Input Voltage on Pins 8, 10, 12, 15	0		0.4	V
Z_{IFB}	Input Impedance on Pins 8, 10, 12, 15	0.7	1	1.3	kΩ
V_{OHFB}	High Level FB Output Voltage (pin 9) Input 1 V on Pins 8, 10	0.8	1	1.2	V
V_{OLFB}	Low Level FB Output (pin 9) Input 0 V on Pins 8, 10			0.3	V
Z_{OFB}	FB Output Impedance Pin 9 High Level			30	Ω
T_{dFBRGB}	Delay Time between FB Inputs and R, G, B Switching		20		ns

TEST DIAGRAM



TYPICAL R, G, B SWITCHING APPLICATION

V_{CC} = 12 V $Z_L \geq 300\ \Omega$.
V_{CC} = 10 V $Z_L \geq 150\ \Omega$.

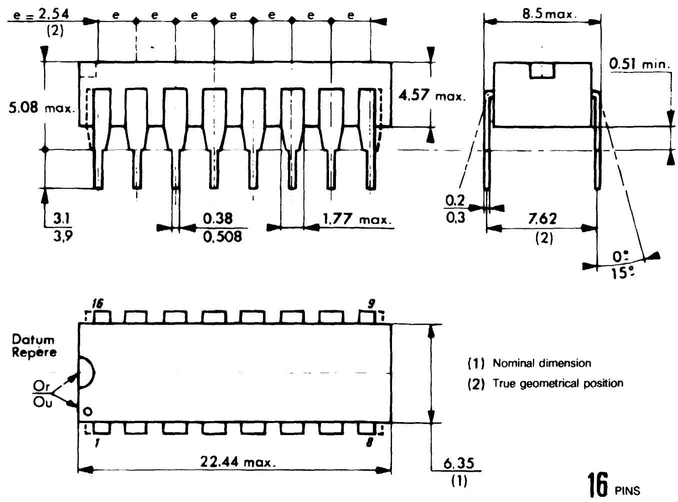


Peritelevision plug standard input value 1 Vpp.

E88TEA5114A-04

PACKAGE MECHANICAL DATA

16 Pins – Plastic DIP

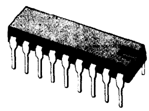


SGS-THOMSON
MICROELECTRONICS

TEA5115

5 CHANNELS VIDEO SWITCH

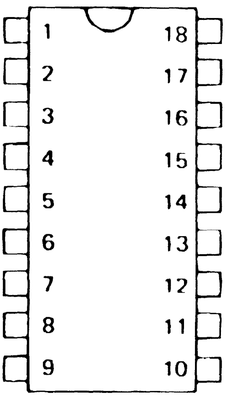
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6dB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30MHz BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7V SHUNT REGULATOR FOR :
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- INDEPENDANT VIDEO OR SYNCHRONIZING SIGNAL SELECTION
- SIMULTANEOUS SWITCHING OF R, G, B AND FB SIGNALS BY FB1 INPUT (internal)



DIL18
(Plastic Package)

ORDER CODE : TEA5115

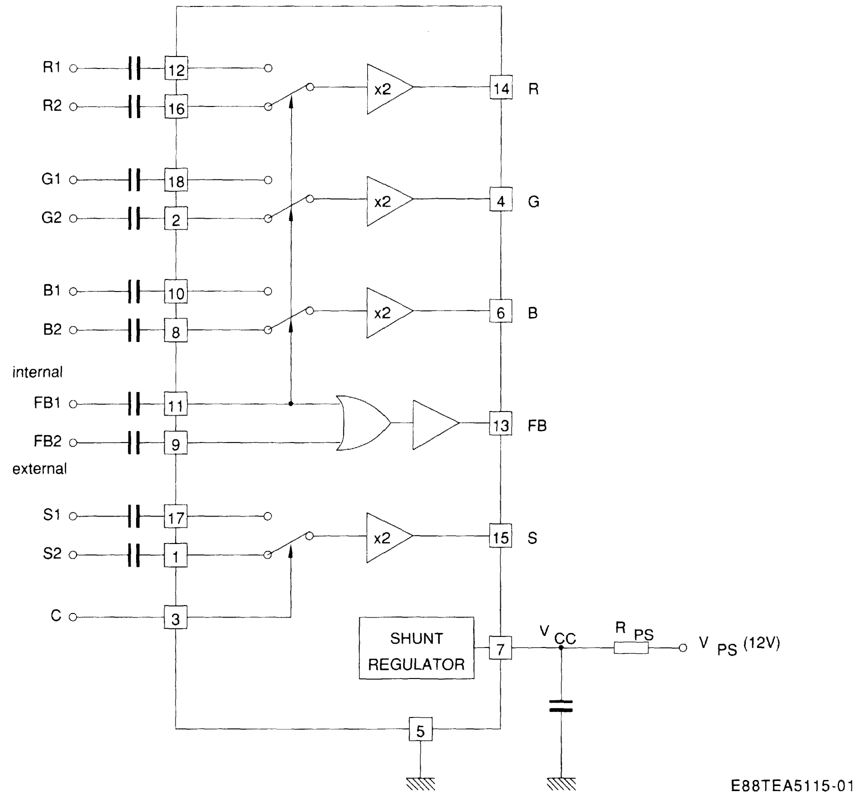
PIN CONNECTION



E88TEA5115-02

1 - Synchro signal input 2
2 - Green signal input 2
3 - "C" select input
4 - Green signal output
5 - Ground
6 - Blue signal output
7 - Shunt regulator supply input
8 - Blue signal input 2
9 - Fast blanking input 2 (external)
10 - Blue signal input 1
11 - Fast blanking input 1 (internal)
12 - Red signal input 1
13 - Fast blanking output
14 - Red signal output
15 - Synchro signal output
16 - Red signal input 2
17 - Synchro signal input 1
18 - Green signal input 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	– 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	– 40 to + 150	°C
T_{stg}	Storage Temperature	– 40 to + 150	°C

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

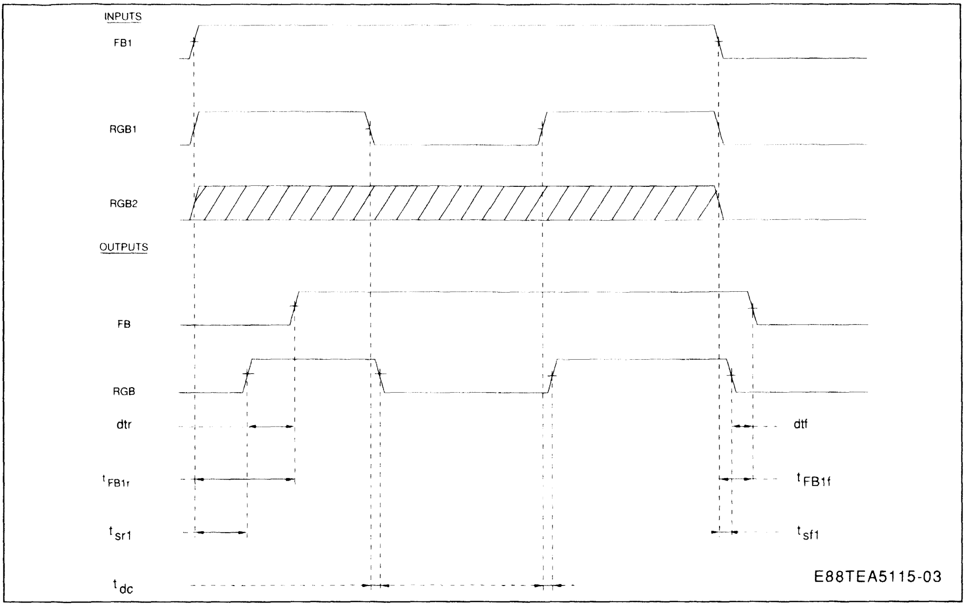
ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω (sequentially switched) (unless otherwise specified, refer to test circuit page 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator I_{CC} = 120 mA I_{CC} = 90 mA I_{CC} = 150 mA	6.3 6.2 6.2	6.7	7.2 7.3 7.3	V V V
R, G, B Switches (pins 4, 6, 14) (Time Measurement Conditions : Δ inputs RGB = 0.7 V_{pp} ; FB input pulse amplitude = 2 V)					
V_C	DC Output Voltage $T_{junction}$ = 25 °C (no input voltage) $T_{junction}$ stabilized		0.9 1.2	1.25	V
V_{AC}	Max Output Swing Voltage	2	4.0		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})	20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; F = 1MHz)	5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; F = 1 MHz)		0.1	0.5	dB
	Input Swing		0.7 V ± 3dB		
z_{ic}	DC Input Impedance		10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; F = 1MHz) with R_{load} = 300 Ω		10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; F = 1 MHz).	45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; F = 1 MHz).	40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.		10		ns
t_{sr1}	Switching rise time between FB1 input signal and R, G, B output signal.		60	110	ns
t_{sf1}	Switching fall time between FB1 input signal and R, G, B output signal.		10	40	ns
t_{sr2}	Switching rise time between FB2 input signal and R, G, B output signal.		10		ns
t_{sf2}	Switching fall time between FB2 input signal and R, G, B output signal.		10		ns
t_{d11} t_{d12}	R1, G1, B1 Decay Time		30 60		ns ns
t_{d21} t_{d22}	R2, G2, B2 Decay Time		45 40		ns ns
Fast Blanking Switch (pin 13) (time measurement conditions : FB input pulse amplitude = 2 V)					
V_{IL} V_{IH} V_{IH} V_{OL} V_{OH}	Low Level Input Voltage FB1 and FB2 High Level Input Voltage FB2 External High Level Input Voltage FB1 Internal Low Level Output Voltage High Level Output Voltage $T_{junction}$ = 25 °C $T_{junction}$ stabilized	– 0.5 1 1.2 1.4 1.5	 1.7 1.9	0.45 V_{CC}+0.5 V_{CC}+0.5 0.6 3.5	V V V V V V
	Input Current (without load)		1.5		µA
	Dynamic Output Impedance : with R_{load} = 300 Ω		10		Ω
t_{FB1r}	Switching rise time between FB1 input and FB output.		120	160	ns
t_{FB1f}	Switching fall time between FB1 input and FB output.		25	60	ns

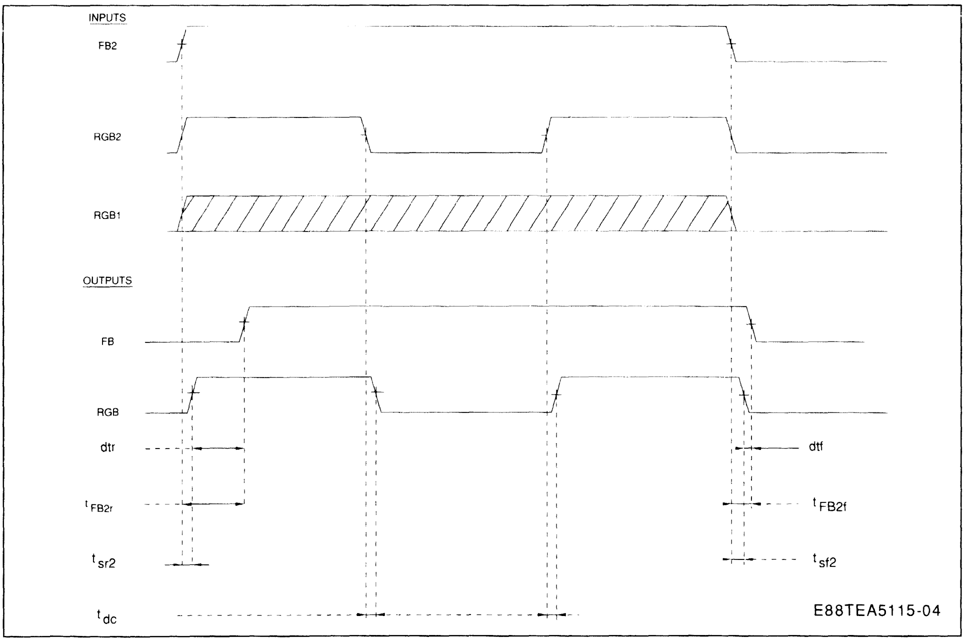
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{FB2r}	Switching rise time between FB2 input and FB output.		70		nsec
t_{FB2f}	Switching fall time between FB2 input and FB output.		35		nsec
d_{tr}	Delay Between RGB Output Signal and FB Output Signal (rise time)		50	100	
d_{tf}	Delay Between RGB Output Signal and FB Output Signal (fall time)		20	40	
Video (or synchro) **Signal Switch** (pin 15)					
V_S	DC Output Voltage (no input voltage) $T_{junction}$ = 25 °C $T_{junction}$ stabilized Max Output Swing Voltage DC Input Impedance Dynamic Output Impedance (input voltage 1V_{pp} ; F = 1 MHz) with R_{load} = 300 Ω Gain (input voltage 1 V_{pp} ; F = 1 MHz) Bandwidth (– 3 dB) (input voltage 1 V_{pp})	 2.6 5.5 15	 0.9 1.2 10 10 6 20	 1.25 6.5	 V V V_{pp} kΩ Ω dB MHz
	Input Swing		1V ± 3 dB		
t_{cr}	Switching rise time between C input signal and S output signal (C pulse amplitude 3 V).		30		ns
t_{cf}	Switching fall time between C input signal and S output signal (C pulse amplitude 3 V).		10		ns
t_{dc}	Delay Time Between S Input and S Output (Δ input 0.7 V_{pp})		10		ns
Select Input "C" (pin 3)					
V_{IL} V_{IH} I_{IL} I_{IH}	Low Level Input Voltage High Level Input Voltage Low Level Input Current (V_{IL} = 1 V) High Level Input Current (V_{IH} = 3 V)	– 0.5 2 – 0.6		1 V_{CC}+0.5 – 0.1 0.5	V V mA mA

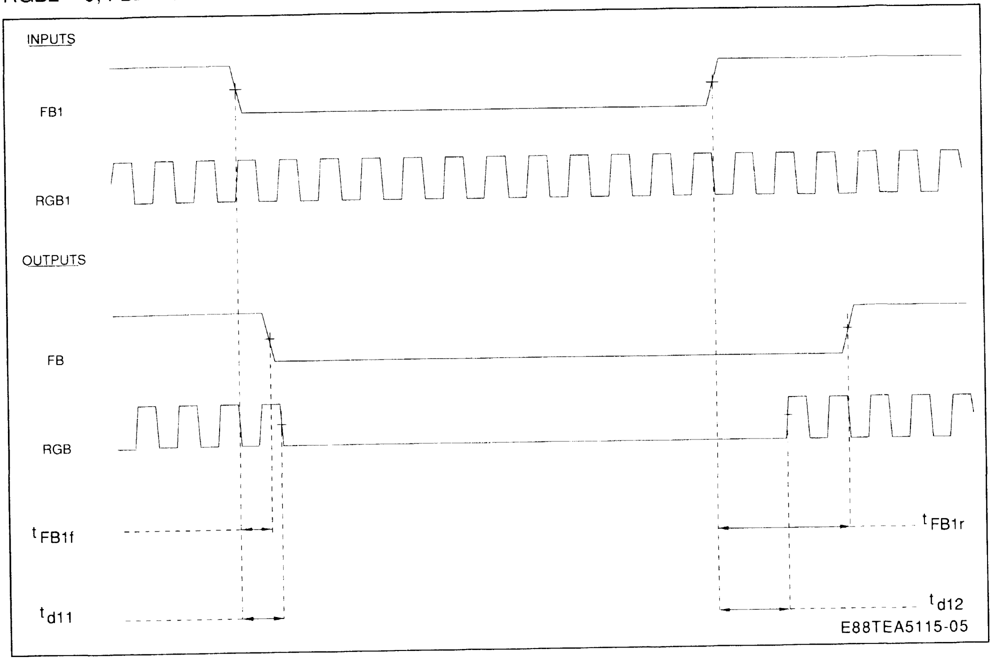
FB2 = 0


INPUTS
FB1
RGB1
RGB2
OUTPUTS
FB
RGB
dtr
dtf
t_{FB1r}
t_{FB1f}
t_{sr1}
t_{sf1}
t_{dc}
E88TEA5115-03

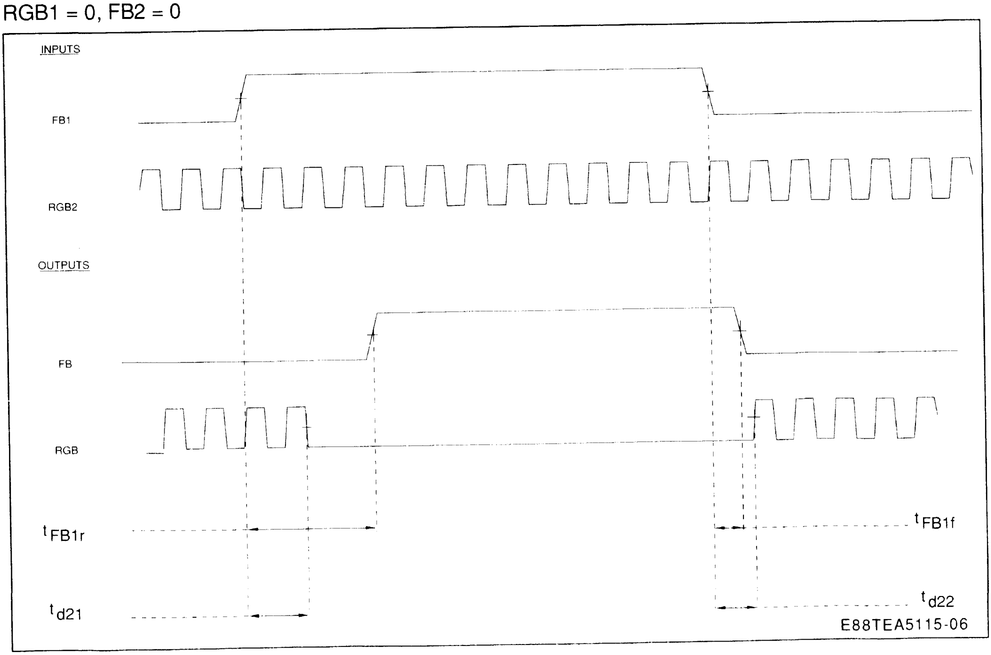
FB1 = 0

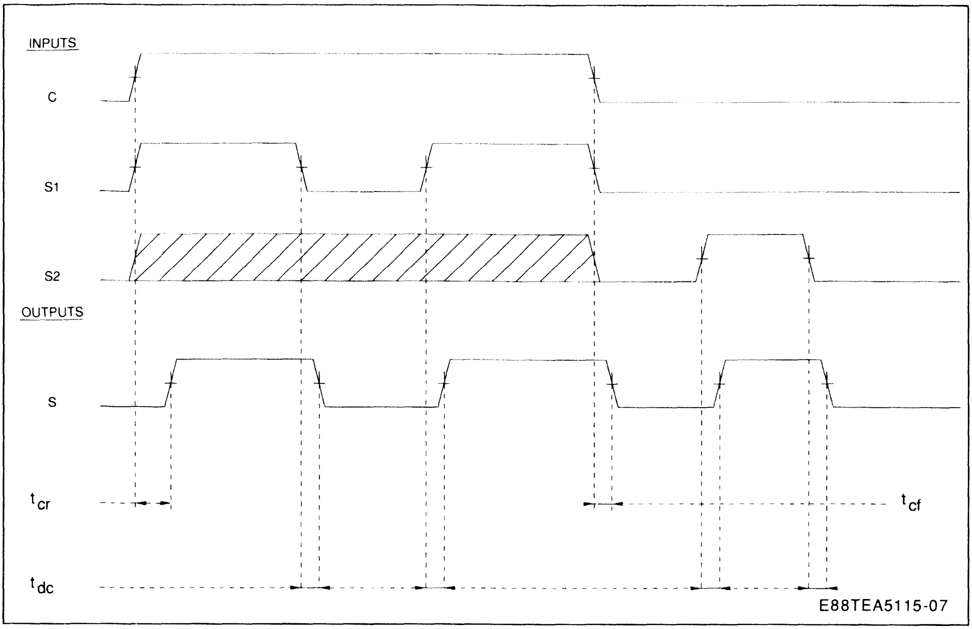

INPUTS
FB2
RGB2
RGB1
OUTPUTS
FB
RGB
dtr
dtf
t_{FB2r}
t_{FB2f}
t_{sr2}
t_{sf2}
t_{dc}
E88TEA5115-04

RGB2 = 0, FB2 = 0

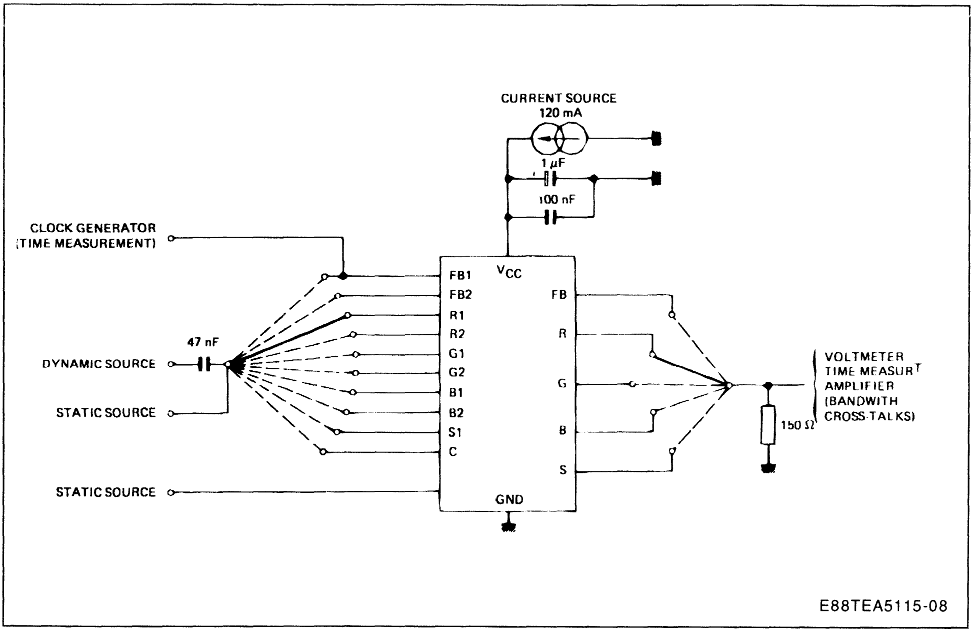


RGB1 = 0, FB2 = 0



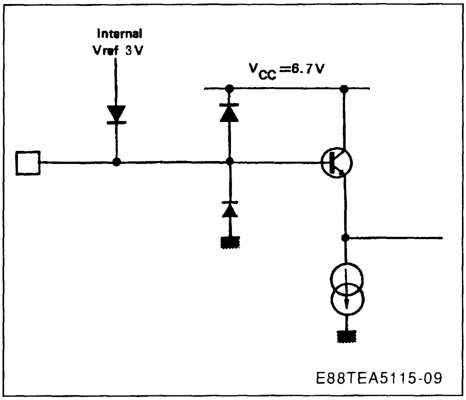


TEST CIRCUIT

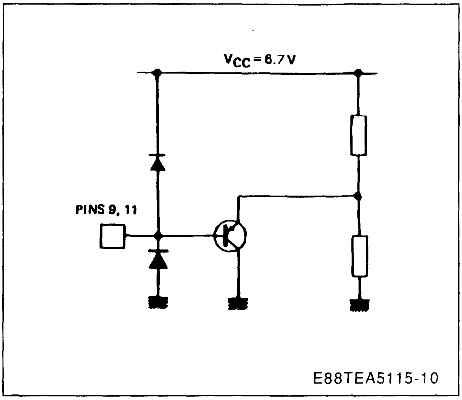


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

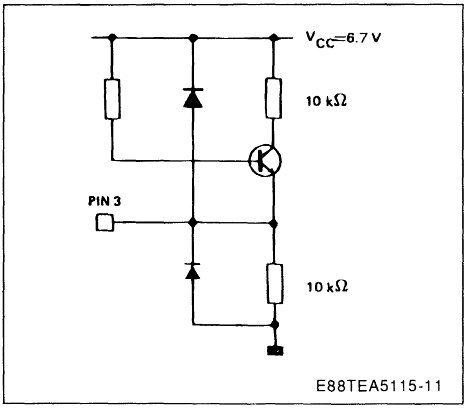
R, G, B, S inputs (pins 1, 2, 8, 10, 12, 16, 17, 18)



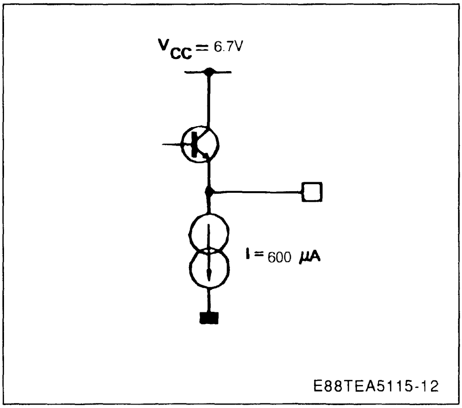
FB inputs (pins 9, 11)



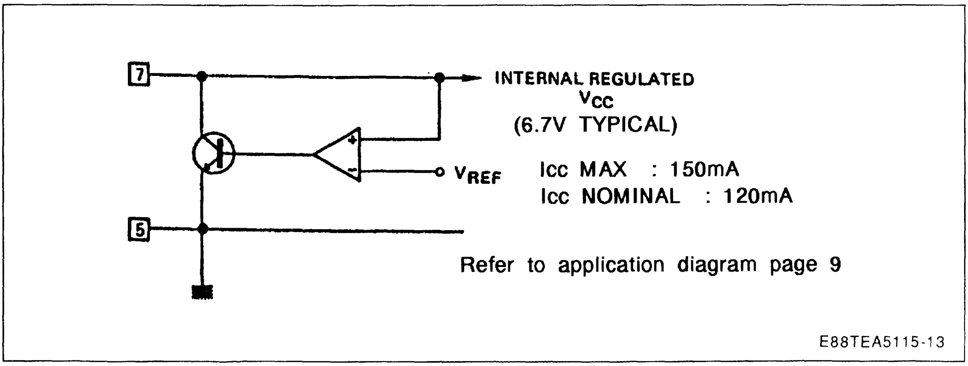
C input (pin 3)



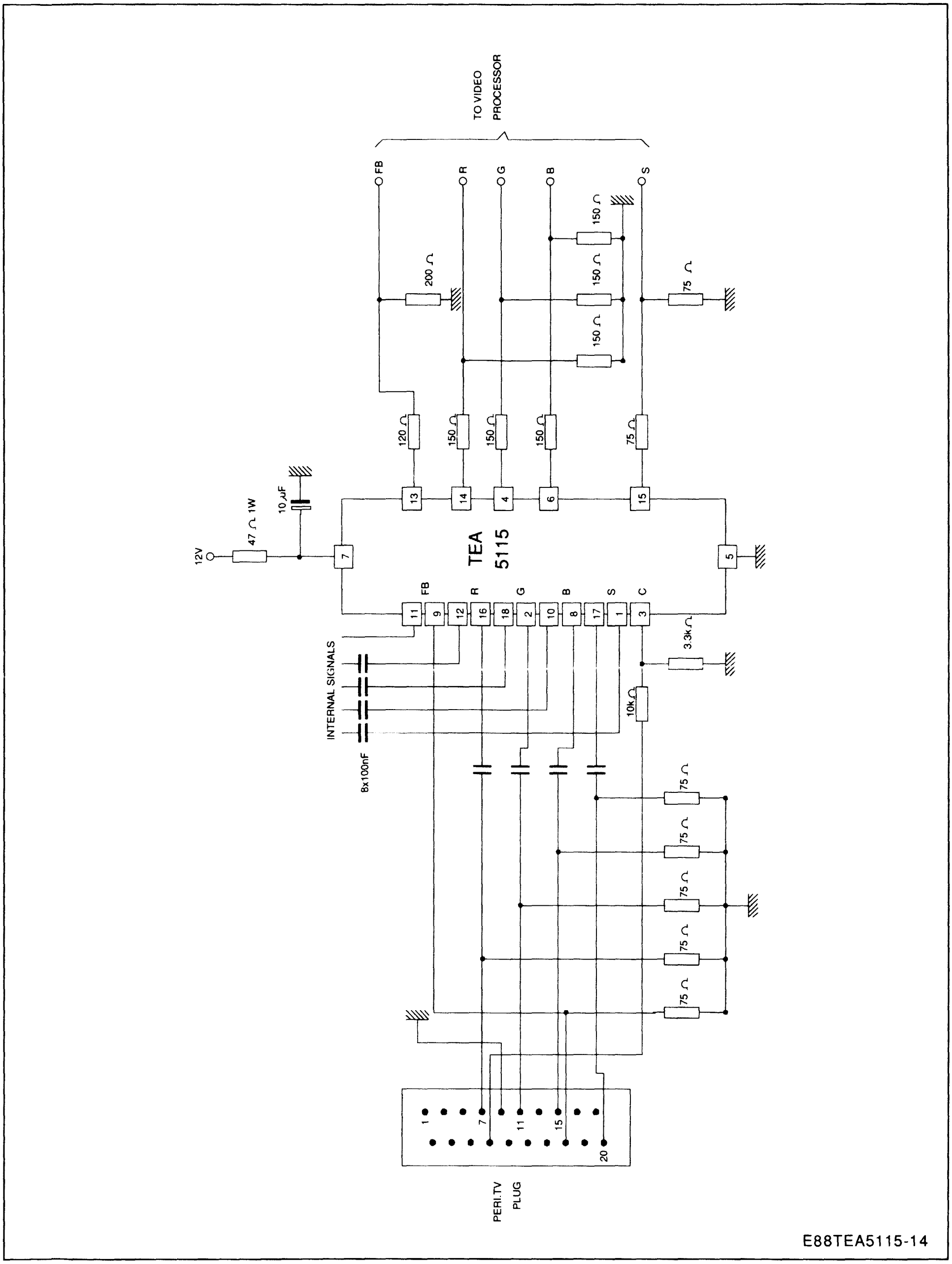
All Outputs (pins 4, 6, 13, 14, 15)



I_{CC} Supply (shunt transistor regulation system) (pin 7)

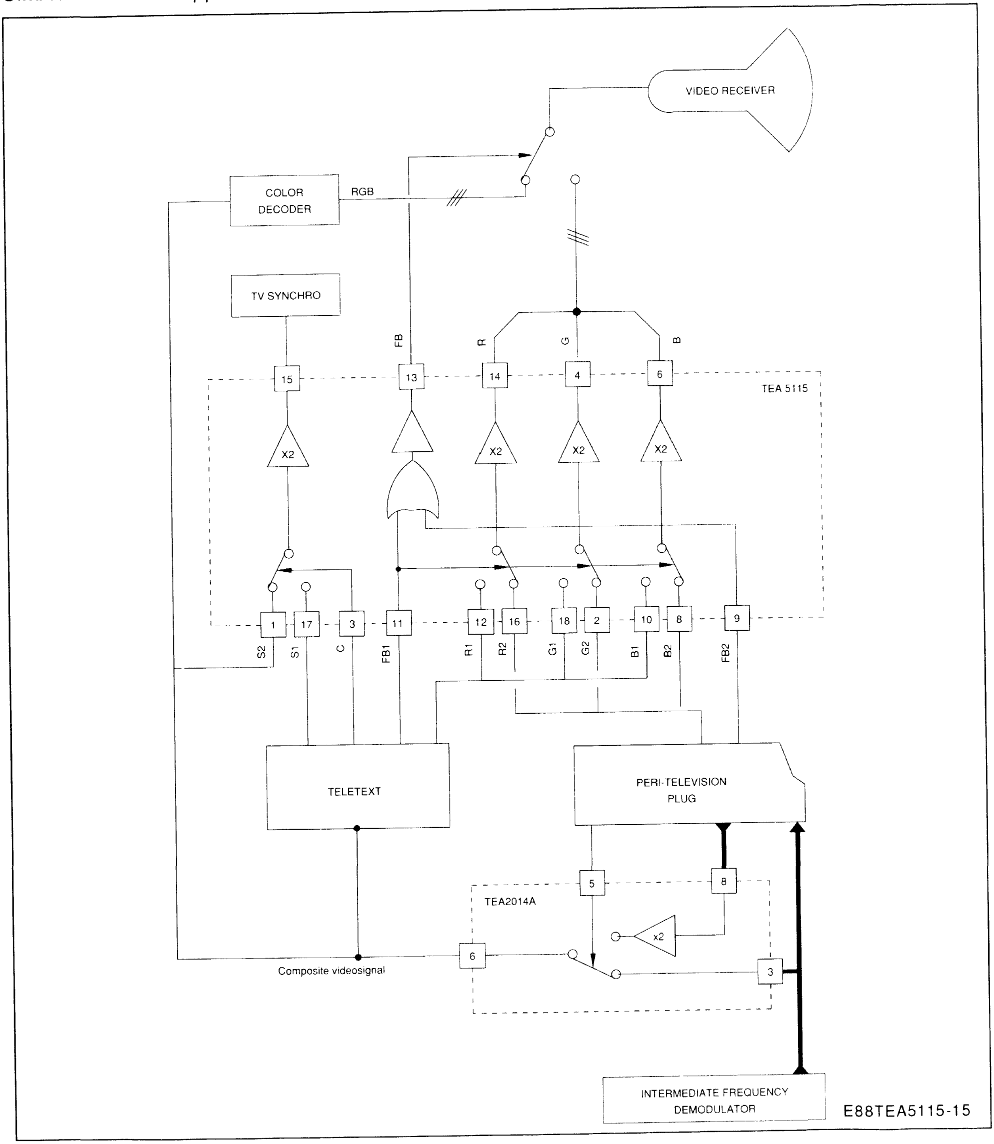


TYPICAL APPLICATION DIAGRAM



- Above given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

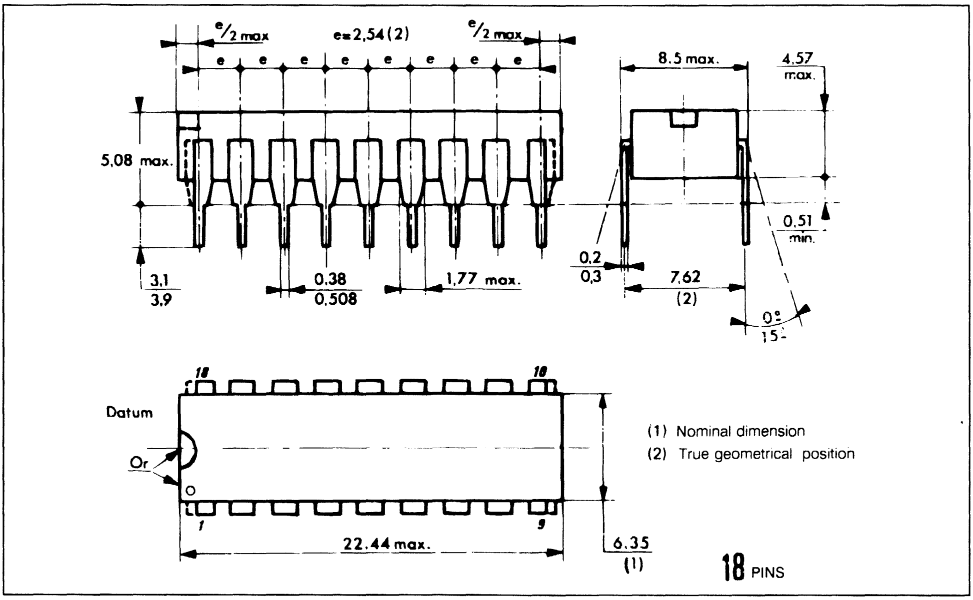
SIMAVELEC norm application with TEA5115 and TEA2014A.



E88TEA5115-15

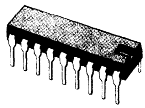
PACKAGE MECHANICAL DATA

18 PINS – PLASTIC PACKAGE



5 CHANNELS VIDEO SWITCH

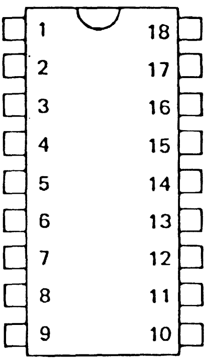
- EACH CHANNEL EXCEPT FAST BLANKING HAS 6 DB GAIN
- R, G, B AND VIDEO SIGNALS ARE CLAMPED TO THE SAME REFERENCE VOLTAGE IN ORDER TO HAVE NO OUTPUT DIFFERENTIAL VOLTAGE WHEN SWITCHING
- ALL INPUT LEVELS COMPATIBLE WITH NFC 92250 AND EN 50049 NORMS
- 30 MHZ BAND WIDTH FOR R, G, B SIGNALS
- INTERNAL 6.7 V SHUNT REGULATOR FOR
  - LOW IMPEDANCE LOADS,
  - POWER DISSIPATION LIMITATION
- THE FIVE CHANNELS ARE SIMULTANEOUSLY SWITCHED BY ONLY ONE SELECT INPUT



DIP18
(Plastic Package)

ORDER CODE : TEA5116

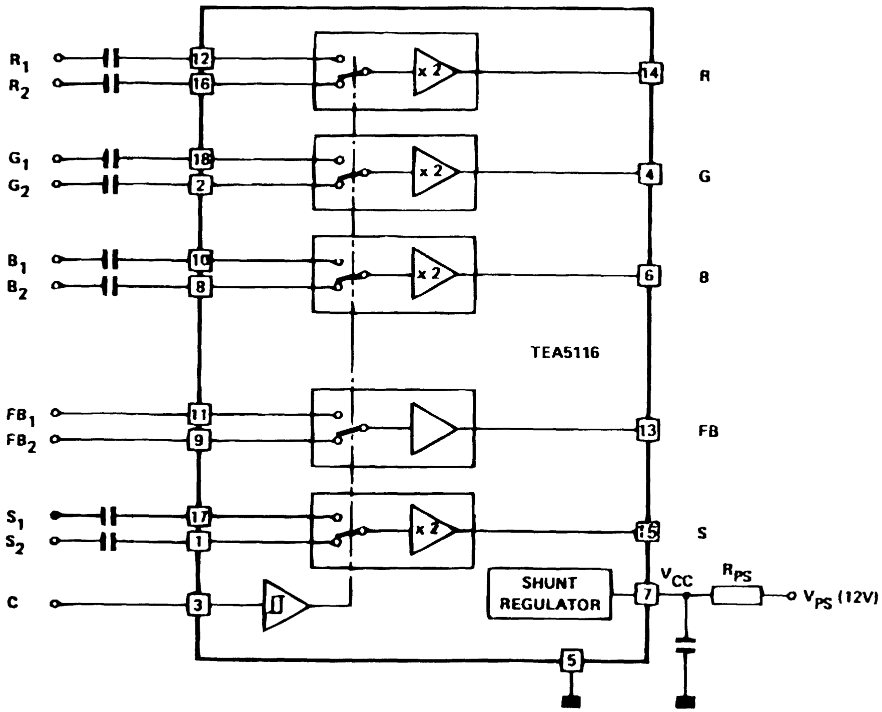
PIN CONNECTIONS



E88TEA5116-02

1 – Synchro signal input 2
2 – Green signal input 2
3 – "C" select input
4 – Green signal output
5 – Ground
6 – Blue signal output
7 – Shunt regulator supply input
8 – Blue signal input 2
9 – Fast blanking input 2
10 – Blue signal input 1
11 – Fast blanking input 1
12 – Red signal input 1
13 – Fast blanking output
14 – Red signal output
15 – Synchro signal output
16 – Red signal input 2
17 – Synchro signal input 1
18 – Green signal input 1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_{CC}	Supply Current (see note)	150	mA
V_{in}	Input Voltage (all inputs)	– 0.5 to V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0 to 70	°C
T_j	Junction Temperature	– 40 to + 150	°C
T_{stg}	Storage Temperature	– 40 to + 150	°C

Note : Minimum output load is 300 Ω in case of all outputs loaded.

THERMAL DATA

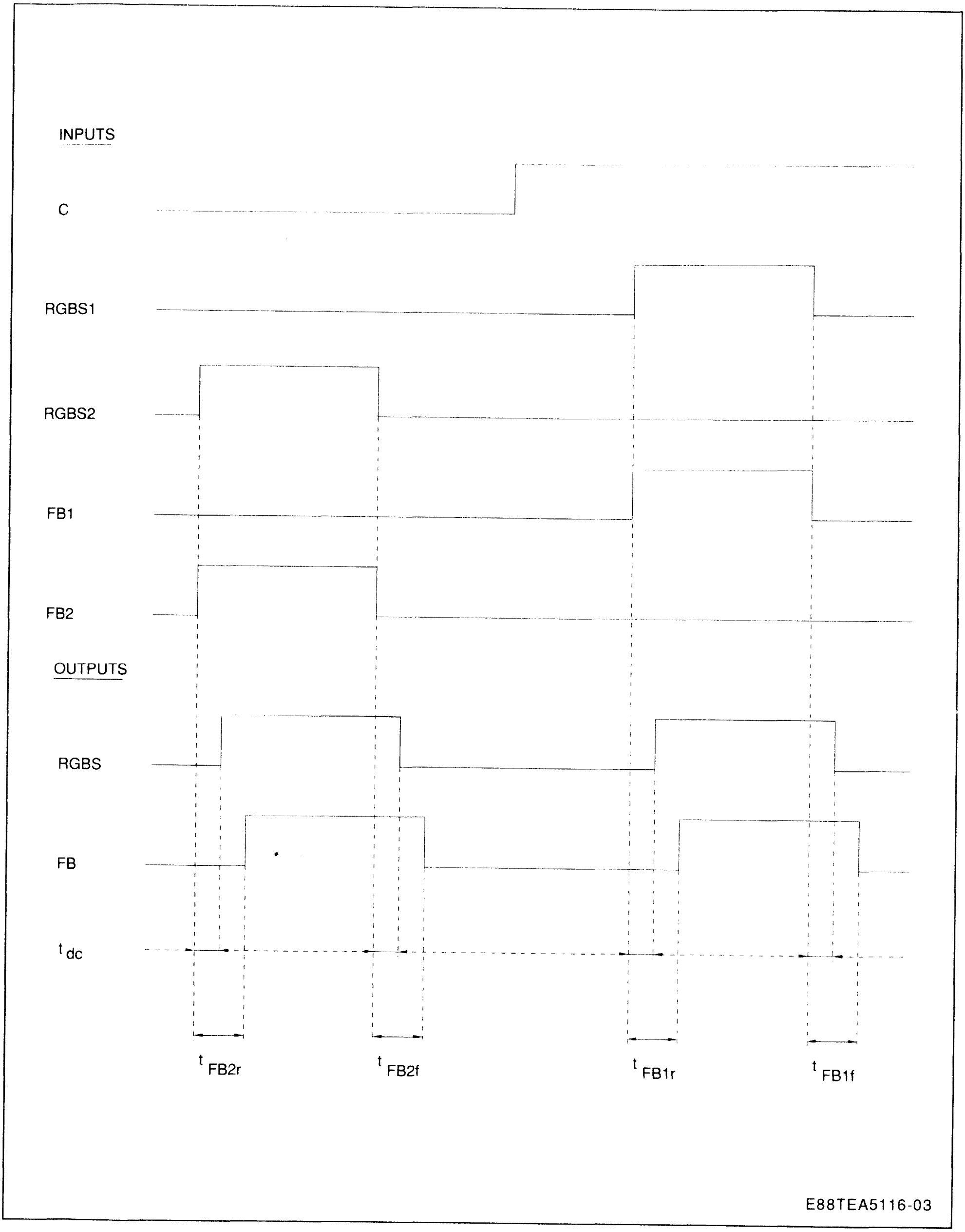
$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, I_{CC} = 120 mA ; Load value = 150 Ω (sequentially switched) (unless otherwise specified, refer to test circuit page 7)

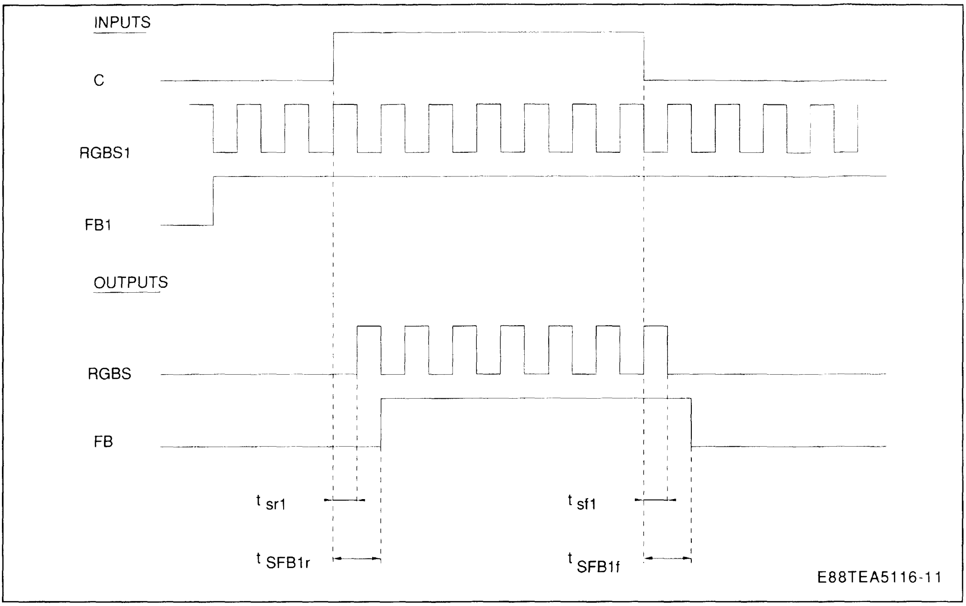
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Internal Shunt Regulator I_{CC} = 120 mA I_{CC} = 90 mA I_{CC} = 150 mA	6.3 6.2 6.2	6.7	7.2 7.3 7.3	V V V
R, G, B Switches (pins 4, 6, 14) - time measurement conditions : (Δ inputs RGB = 0.7 V_{pp} ; C pulse amplitude = 3 V)					
V_C	DC Output Voltage $T_{junction}$ = 25 °C (no input voltage) $T_{junction}$ stabilized		0.9 1.2	1.25	V
V_{AC}	Max Output Swing Voltage	2	4		V_{pp}
B	Bandwidth (– 3 dB) (input voltage 0.7 V_{pp})	20	30		MHz
A_v	Gain of Each Channel (input voltage 0.7 V_{pp} ; F = 1MHz)	5.5	6	6.5	dB
A_{dc}	Gain Difference Between any two R, G, B Channels (input voltage 0.7 V_{pp} ; F = 1 MHz)		0.1	0.5	dB
	Input Swing		0.7 ± 3 dB		
z_{ic}	DC Input Impedance		10		kΩ
z_{oc}	Dynamic Output Impedance (input voltage 0.7 V_{pp} ; F = 1MHz) with R_{load} = 300 Ω		10		Ω
	Crosstalk between any inputs (R1 and R2 or B1 and B2 or G1 and G2) (input voltage 0.7 V_{pp} ; F = 1 MHz).	45	55		dB
	Crosstalk between any outputs (input voltage 0.7 V_{pp} ; F = 1 MHz).	40	55		dB
t_{dc}	Delay time between R, G, B inputs and RGB outputs.		10		nsec
t_{sr1}	Switching rise time between C input signal and R, G, B output signal (input signal on RGB1).		45		nsec
t_{sf1}	Switching fall time between C input signal and R, G, B output signal (input signal on RGB1).		25		nsec
t_{sr2}	Switching rise time between C input signal and R, G, B output signal (input signal on RGB2).		55		nsec
t_{sf2}	Switching fall time between C input signal and R, G, B output signal (input signal on RGB2).		25		nsec
Fast Blanking Switch (pin 13) (time measurement conditions : FB input pulse amplitude = 2 V ; C pulse amplitude = 3 V)					
V_{IL} V_{IH} V_{OL} V_{OH}	Low Level Input Voltage High Level Input Voltage Low Level Output Voltage High Level Output Voltage $T_{junction}$ = 25 °C $T_{junction}$ stabilized	– 0.5 1 1.4 1.5	 1.7 1.9	0.4 V_{CC} + 0.5 0.6 3.5	V V V V
	Dynamic Output Impedance : with R_{load} = 300 Ω		10		Ω
t_{FB1r}	Delay rise time between FB1 input and FB output.		60	110	nsec
t_{FB1f}	Delay fall time between FB1 input and FB output.		40	60	nsec

ELECTRICAL CHARACTERISTICS (continued)

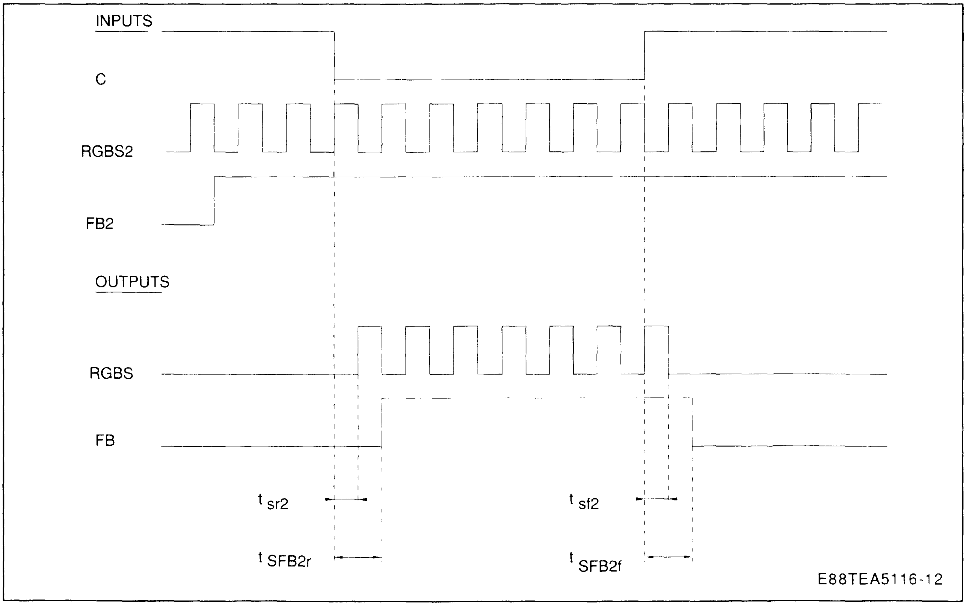
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{FB2r}	Delay rise time between FB2 input and FB output.		60		nsec
t_{FB2f}	Delay fall time between FB2 input and FB output.		40		nsec
t_{SFB1r}	Switching rise time between C input and FB output (input signal on FB1 input).		75		nsec
t_{SFB1f}	Switching fall time between C input and FB output (input signal on FB1 input).		50		nsec
t_{SFB2r}	Switching rise time between C input and FB output (input signal on FB2 input).		85		nsec
t_{SFB2f}	Switching fall time between C input and FB output (input signal on FB2 input).		50		nsec
Video (or synchro) **Signal Switch** (pin 15) - time measurement conditions : (C pulse amplitude = 3 V)					
V_S	DC Output Voltage (no input voltage)				
	$T_{junction}$ = 25 °C		0.9	1.25	V
	$T_{junction}$ stabilized		1.2		V
V_{as}	Max Output Swing Voltage	2.6			V_{pp}
Z_{ic}	DC Input Impedance		10		kΩ
Z_{oc}	Dynamic Output Impedance (input voltage 1 V_{pp} ; F = 1 MHz) with R_{load} = 300 Ω		10		Ω
A_v	Gain (input voltage 1 V_{pp} ; F = 1 MHz)	5.5	6	6.5	dB
B	Bandwidth (– 3 dB) (input voltage 1 V_{pp})	15	20		MHz
	Input Swing		1 V ± 3 dB		
t_{dc}	Delay Time Between S Input and S Output (Δ input : 0.7 V_{pp})		10		nsec
t_{sr1}	Switching rise time between C input signal and S output signal (input signal on S1)		45		nsec
t_{sf1}	Switching fall time between C input signal and S output signal (input signal on S1)		25		nsec
t_{sr2}	Switching rise time between C input signal and S output signal (input signal on S2)		55		nsec
t_{sf2}	Switching fall time between C input signal and S output signal (input signal on S2)		25		nsec
Select Input "C" (pin 3)					
V_{IL}	Low Level Input Voltage	– 0.5		1	V
V_{IH}	High Level Input Voltage	2		V_{CC} + 0.5	V
I_{IL}	Low Level Input Current (V_{IL} = 1 V)	– 0.6		– 0.1	mA
I_{IH}	High Level Input Current (V_{IH} = 3 V)			0.5	mA


INPUTS
C
RGBS1
RGBS2
FB1
FB2
OUTPUTS
RGBS
FB
t_{dc}
t_{FB2r}
t_{FB2f}
t_{FB1r}
t_{FB1f}
E88TEA5116-03

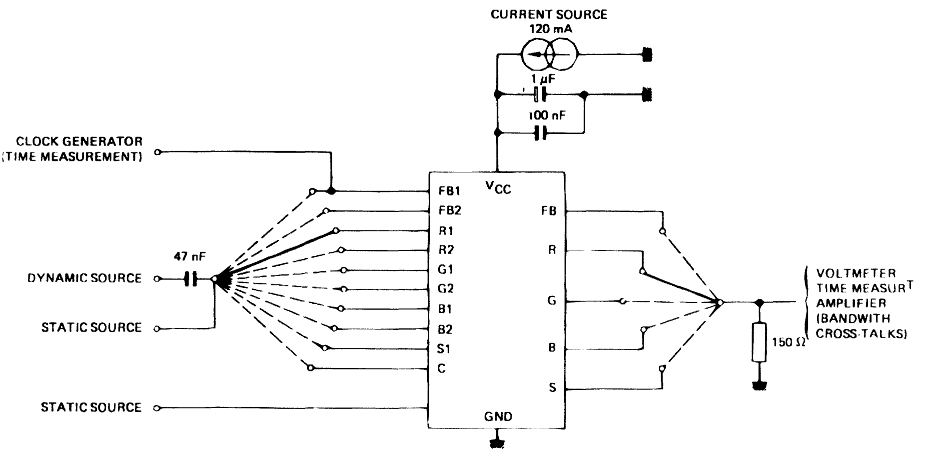
RGBS2 = 0, FB2 = 0



RGBS1 = 0, FB1 = 0



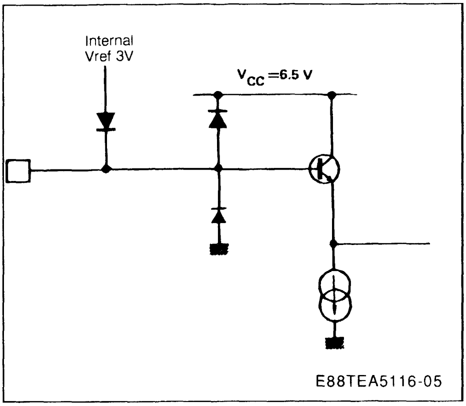
TEST CIRCUIT



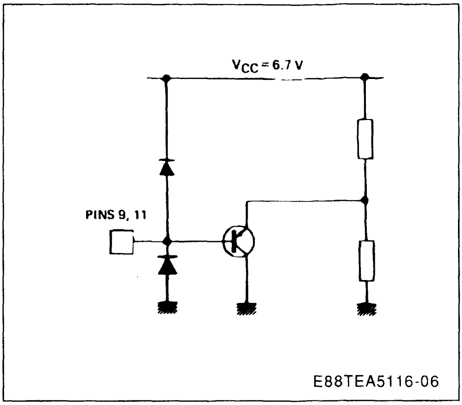
E88TEA5116-04

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

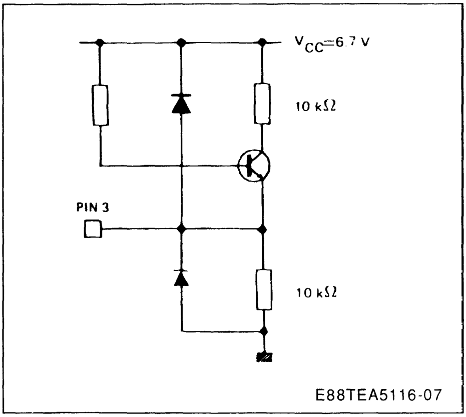
R, G, B, S INPUTS (pins 1, 2, 8, 10, 12, 16, 17, 18)



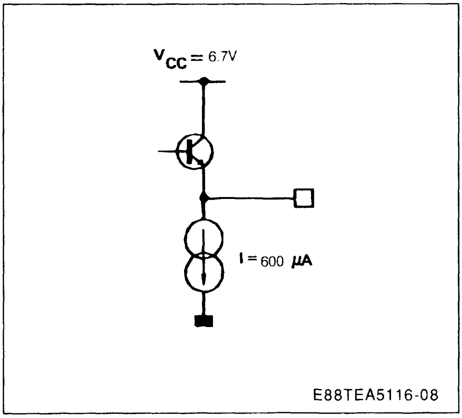
FB INPUTS (pins 9, 11)



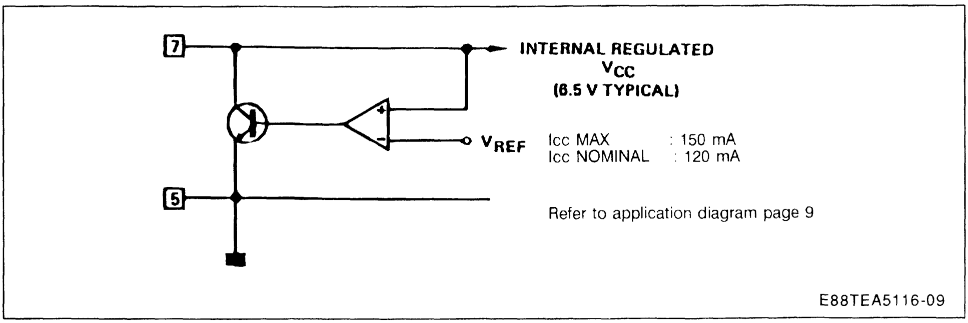
C INPUT (pin 3)



ALL OUTPUTS (pins 4, 6, 13, 14, 15)

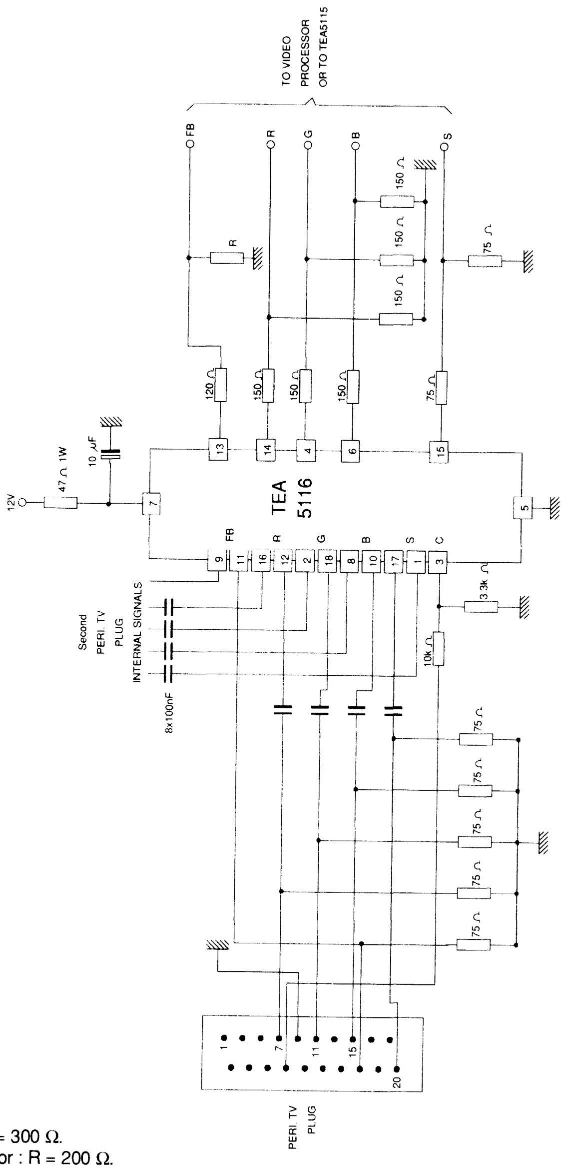


Icc SUPPLY (shunt transistor regulation system) (pin 7)



TYPICAL APPLICATION DIAGRAM

- Under given output load values are minimum values, in case of all output loading.
- Minimum output load is 150 Ω individually, provided that total supply current is less than 150 mA.

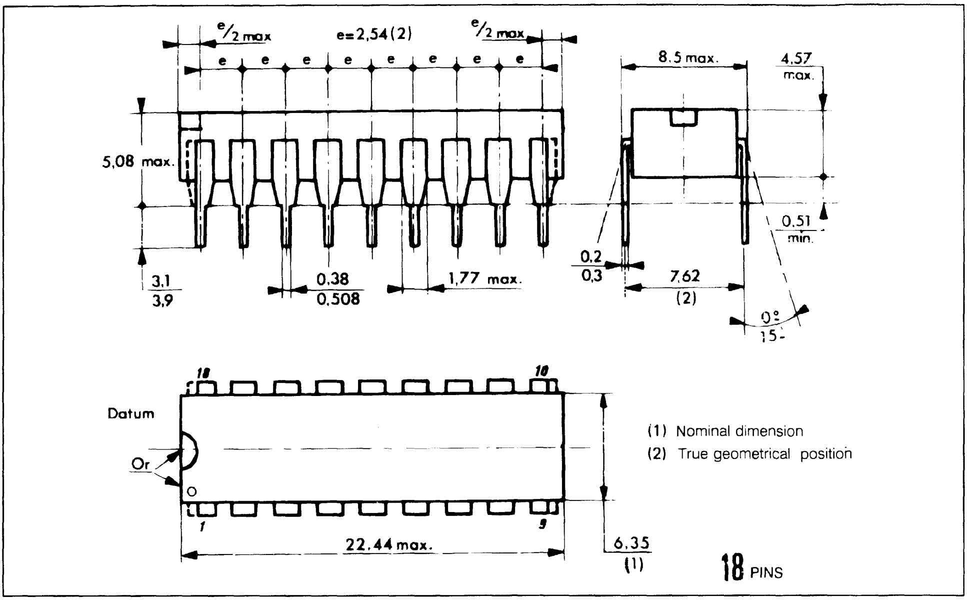


R values
1) towards TEA5115 : R = 300 Ω.
2) towards video processor : R = 200 Ω.

E88TEA5116-10

PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP

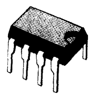


SGS-THOMSON
MICROELECTRONICS

TEA5170

SWITCH MODE POWER SUPPLY SECONDARY CIRCUIT

- POWER SUPPLY WIDE RANGE 4.5V – 14.5V
- SOFT START
- REFERENCE VOLTAGE 2V ± 5%
- WIDE FREQUENCY RANGE 250KHz
- MINIMUM OUTPUT PULSE WIDTH 500nS
- MAXIMUM PRESET DUTY CYCLE
- SYNCHRONIZATION WINDOW
- OUTPUT SWITCH
- UNDERVOLTAGE LOCKOUT
- FREQUENCY RANGE WITH SYNCHRONIZATION 64KHz



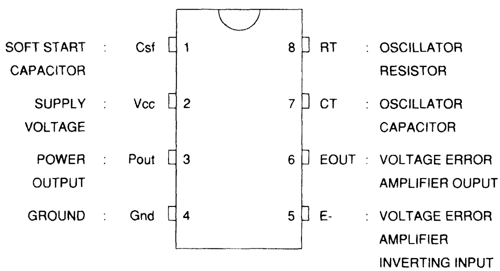
DIP8
(Plastic Package)

ORDER CODE : TEA5170

DESCRIPTION

The TEA5170 is designed to work in the secondary part of an off-line SMPS, sending pulses to the slaved TEA2164 or TEA2260 which are located on the primary side of the main transformer. An accurate regulated vol-tage is obtained by duty cycle control. The TEA5170 can be externally synchronized by higher or lower frequency signal, then it could be used in applications like TV set ones.

PIN CONNECTIONS



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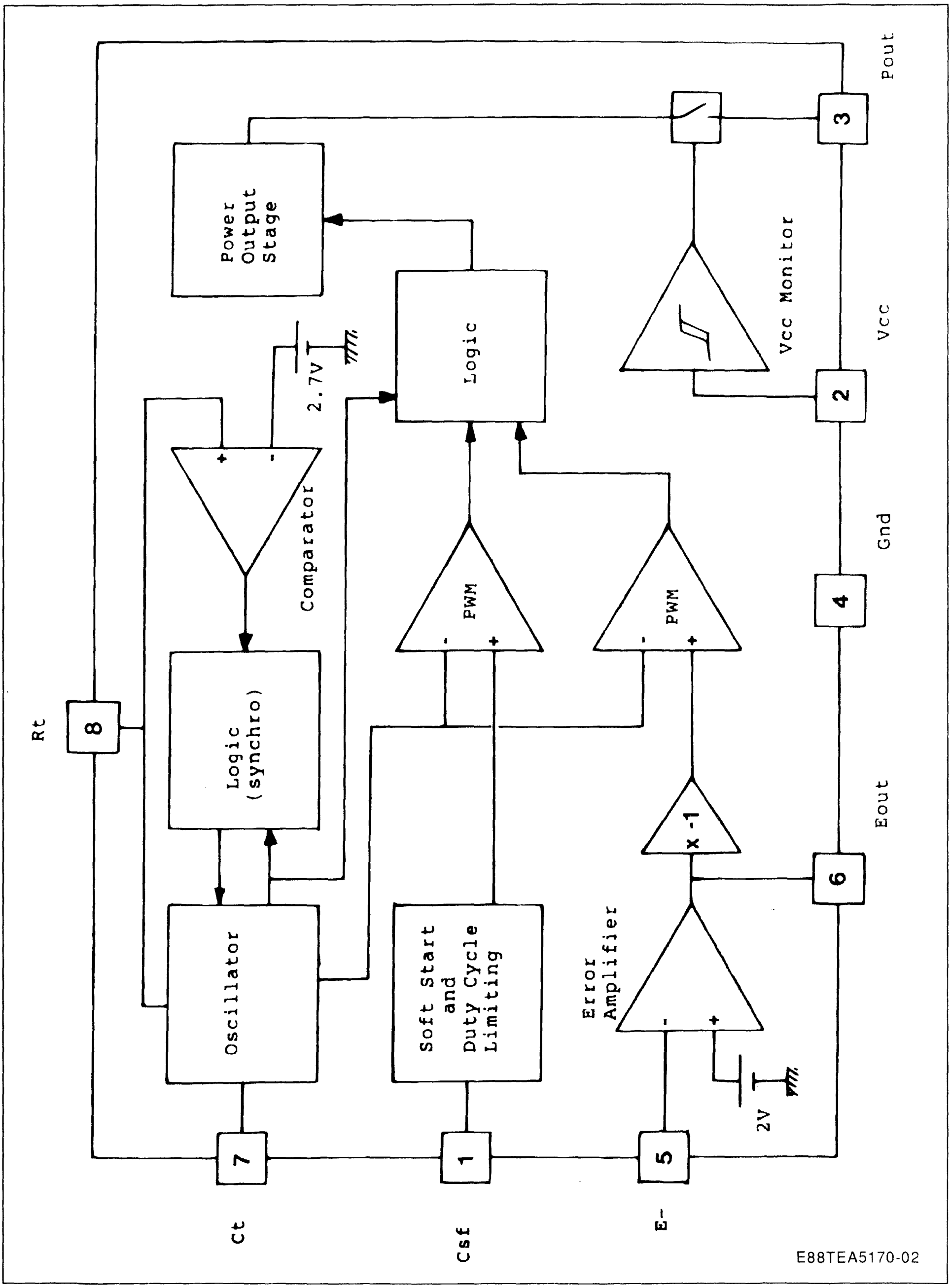
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	15	V
T_j	Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature Range	– 40 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction-ambient Thermal Resistance	90	°C/W

RECOMMANDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	5		14	V
RT	Timing Resistor	47		180	KΩ
CT	Timing Capacitor	0.12		1.8	nF
Fosc	Oscillator Frequency	12		250	KHz
Fsy	Synchro Frequency	12		64	KHz
T_{amb}	Operating Ambient Temperature	– 20		70	°C
VRT	Voltage on Pin RT (8)			7	Volt
VCT	Current on Pin CT (1)			100	µA
ISOURCE	Output Current		30	60	mA

ELECTRICAL CHARACTERISTICS (TA = 25°C)

T_A = 25°C ; V_{CC} = 12V (unless otherwise specified)

OSCILLATOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TA	Free Period	RT = 100KΩ ± 0% CT = 1.2nF ± 0% Vcc = 12V	60.40	65.60	70.80	µS
TB		RT = 100KΩ ± 0% CT = 560pF ± 0% Vcc = 12V	29.18	31.70	34.22	µS
ΔFosc (T)	Frequency drift due to ambient temperature variation from 0C to 70C $\frac{\text{Fosc (70°C) – Fosc (0°C)}}{\text{70°C x Fosc (25°C)}}$	RT = 100KΩ ± 0% CT = 1.2nF ± 0% Vcc = 12V		0.01		%/°C
ΔFosc (Vcc)	Frequency drift due to Vcc variation from 5V to 12V $\frac{\text{Fosc (12V) – Fosc (5V)}}{\text{7V x Fosc (12V)}}$	RT = 100KΩ ± 0% CT = 1.2nF ± 0%		0.07		%/V

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^{\circ}C$; $V_{CC} = 12V$ (unless otherwise specified)

ERROR VOLTAGE AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ibias	Input Bias Current	Ein = 2V	0	0.2	1	μA
Gvol	Voltage Gain			80		dB
GB	Gain Bandwidth			2		MHz
	Slew Rate			2		V/μs

INTERNAL VOLTAGE REFERENCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VREF	Voltage Reference	Using the voltage error amp. as a follower	1.9	2	2.1	V
ΔVREF (Vcc)	Line Regulation $\frac{VREF(12V) - VREF(5V)}{7V}$	Vcc = 5V to 12V	– 3	0.4	3	mV/V
ΔVREF (T)	VREF drift with temperature $\frac{VREF(70^{\circ}C) - VREF(0^{\circ}C)}{70}$	TA = 0°C to 70°C		0.2		mV/°

TON MIN

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TONMIN A	Minimum Duty Cycle	Ct = 1.2nF ± 0% Rt = 100KΩ ± 0%	1.77	2.53	3.29	μs
TONMIN B	Minimum Duty Cycle	Ct = 560pf ± 0% Rt = 100KΩ ± 0%	1.04	1.49	1.94	μs

POWER OUTPUT STAGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VPOUTH	Output High Level	Iload = 1mA	6.3	6.9	7.5	V
VPOUTL	Output Low Level	Iload = – 1mA	0.5	0.8	1.1	V
ISINK	Sink Current	VPOUT = 3V	30	60	190	mA
ISOURCE	Source Current	VPOUT = 3V	30	110	190	mA

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^\circ C$; $V_{CC} = 12V$ (unless otherwise specified)

SYNCHRONISATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Ftrig Max	Maximum Synchro Frequency		64			KHz
Vtrig	Synchro Triggering Threshold			2.7	3	V
Ttrigp	Synchro Triggering Pulse Width	at VRT = 2.7Volt (fig 5)	800			nS
Wtrig +	Positive Triggering Window $\frac{\text{Ttrig + − To}}{\text{To}}$	CT = 1.2nF ± 0% RT = 100KΩ ± 0%	25	35	40	%
Wtrig −	Negative Triggering Window $\frac{\text{To − Ttrig −}}{\text{To}}$	CT = 1.2nF ± 0% RT = 100kΩ ± 0%	9	29	42	%

SOFT START

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icsf	*Csf Load Current	Vcsf = 1V	2.5	3.7	6	µA
Donmax	Maximum Duty Cycle *Csf is a high impedance capacitor	Vcs > 2.5V Vcc = 12V CT = 1.2nf ± 0% RT = 100KΩ ± 0%	60	78	95	%

VCC MONITOR

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VSTART	Turn-on Threshold		3.60	4	4.40	V
VHYST	Hysteresis Voltage		100			mV
VSTOP	Turn-off Threshold		3.50			V

TOTAL DEVICE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Icc	Supply Current	RT = 100KΩ ± 0% CT = 1.2nf ± 0% No Load on Pin 3 Vcc = 12V	7	12	25	mA

GENERAL DESCRIPTION

The TEA5170 takes place in the secondary part of an isolated off-line SMPS. During normal mode operation, it sends pulses to the slave circuit (TEA2164 or TEA2260) through a pulse transformer to achieve a very precisely regulated voltage by duty cycle control.

The main blocs of the circuit are :

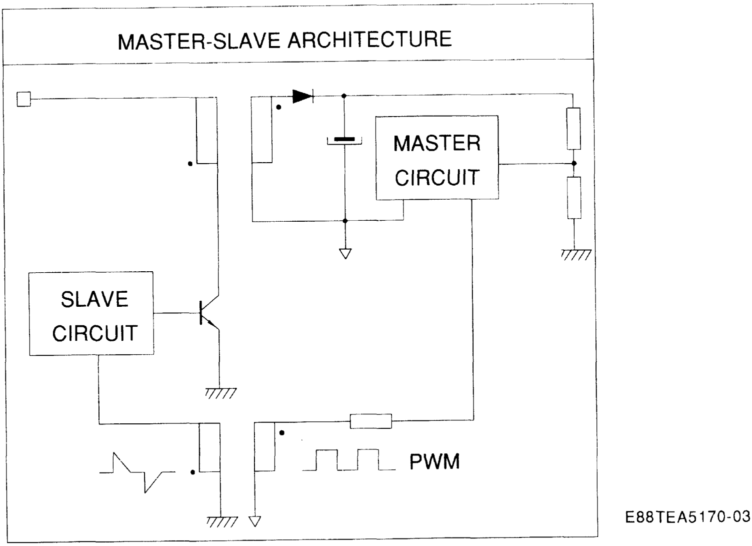
- an error voltage amplifier
- an RC oscillator
- an output stage
- a V_{CC} monitor
- a voltage reference bloc
- a pulse width modulator
- two logic blocs
- a soft start and Duty cycle limiting bloc

PRINCIPLE OF OPERATION

The TEA5170 sends pulses continuously to the slave circuit in order to insure a proper behaviour of the primary side.

- According to this, the output duty cycle is varying between Donmin (0.05) and Donmax. (0.75) : then even in case of open load, pulses are still sent to the slave circuit.

Figure 1 : Basic Concept.

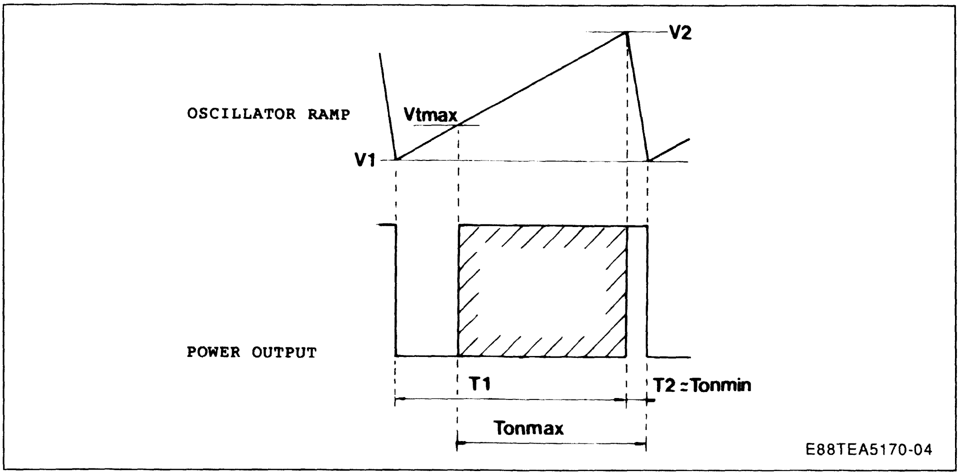


ASYNCHRONIZED MODE

The regulated voltage image is compared to 2V voltage reference. The error voltage amplifier output and the RC oscillator voltage ramp are applied to the internal Pulse Width Modulator Inputs.

The PWM logic Output is connected to a logic bloc which behaves like a RS latch, sets by the PWM output and resets when Ct downloading occurs. Finally, the push-pull output bloc delivers square wave signal whom output leading edge occurs during Ct uploading time, and output trailing edge at Ct downloading time end. The duty cycle is limited to 75% of oscillator period as maximum value and to Ct downloading time/oscillator period as minimum value (Figure 2).

Figure 2 : Asynchronized Mode.



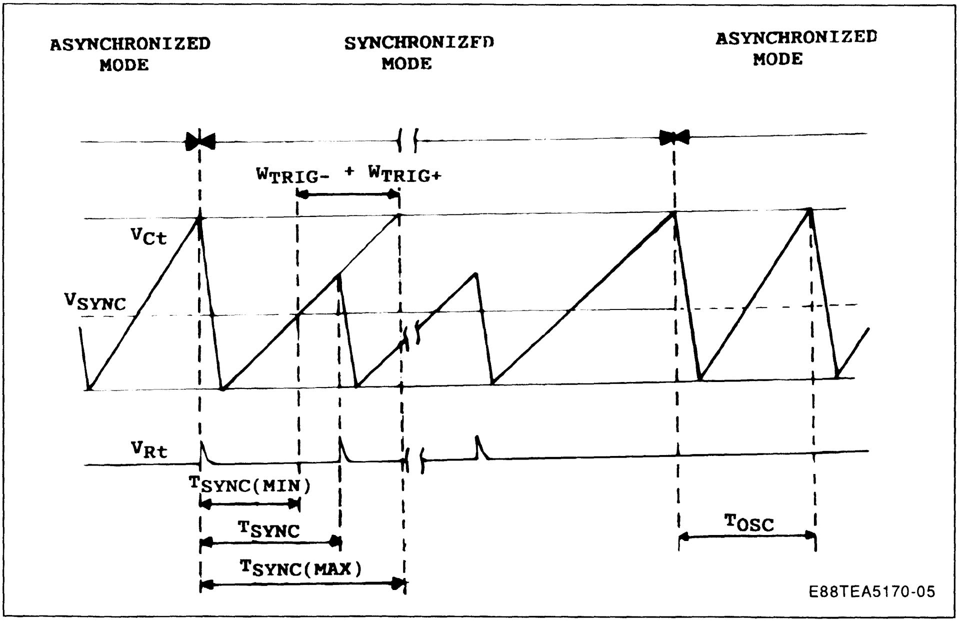
SYNCHRONIZED MODE (figures 3, 4, 5)

The TEA5170 will enter the Synchronized Mode when it receives one pulse through Rt during Ct discharge.

At that time Ct charging current will be multiplied by 0.75 and period will increase up to To x 1.33.

A pulse occuring during the synchro window, commands the Ct downloading. If none, the TEA5170 will return to normal mode at the end of the period.

Figure 3 : Synchronized Mode.



Remark : In case of an application between TEA5170 and TEA2164, to optimize the synchronization windows of these circuits, the following relations have to be used :

$$T_m = \frac{T_{SYNC}}{1.06} \qquad T_e = \frac{T_m}{1.223}$$

with - T_e : Free period of the TEA2164 oscillator.
- T_m : Free period of the TEA5170 oscillator.

BLOCK DESCRIPTION

The error voltage amplifier inverting-input and output are accessible to use different feed-back network and allowing parasitic filtering network. The non-inverting input is internaly connected to 2V reference voltage.

The RC oscillator is designed to work at high frequency (up to 250KHz). R_T sets the capacitor charging current $I_o = 2/R_T$.

The capacitor C_T is loaded from $V1 \approx 1V$ to $V2 \approx 2V$ during

$T1 = \frac{C_T R_T}{1.985}$ and then down loaded through an integrated resistor

$R_2 \approx 1K\Omega$ during $T_2 = 1300\ C_T$

The ramp is used to limit the duty cycle. Then the maximum duty cycle is

$$DONMAX = \frac{1}{T1 + T2}\ (0.73\ T1 + T2)$$

The output level is V_{CC} independant when V_{CC} is over 8V.

The V_{CC} monitoring switches the circuit on when V_{CC} is over 4V and switches it off when under 3.8V. This function insures a proper starting procedure (made by the primary side circuit).

SYNCHRONIZATION

Figure 4 : Triggering Schematic.

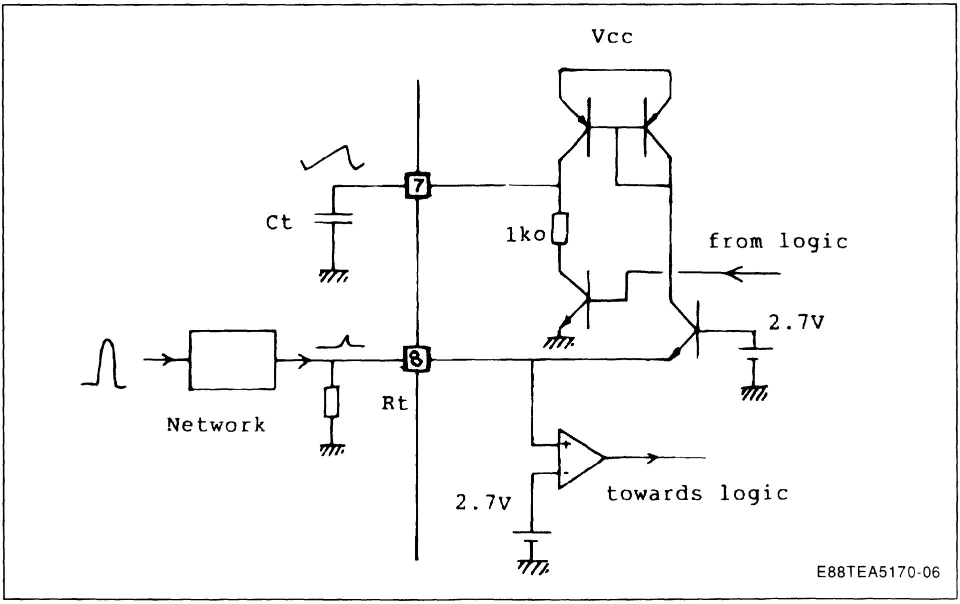
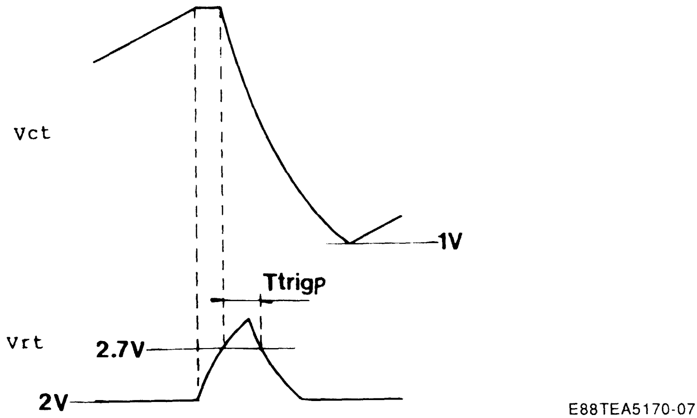


Figure 5 : Typical Wave Forms.



STARTING

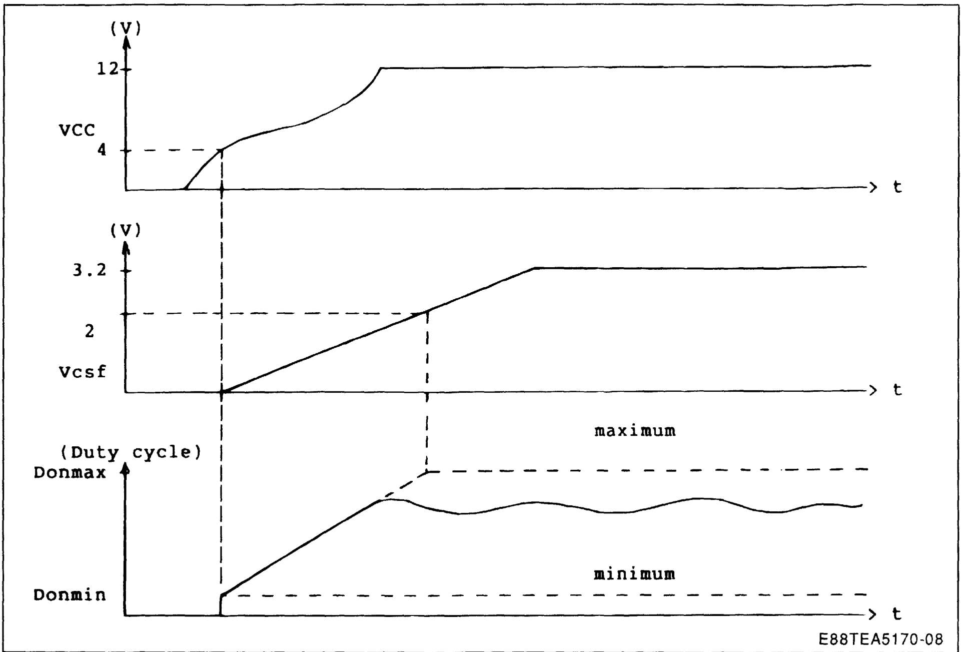
When V_{CC} is under 4V, output pulses are not allowed and the slave circuit keeps its own mode. When V_{CC} is going over 4V, output pulses are sent via the pulse transformer (or an optical device) to the slave circuit which is synchronizing and entering the slaved mode. Output pulses can be shut down only if V_{CC} goes below 3.8 Volt.

SOFT START

Using Csf, it is possible to make a soft start sequence. When V_{CC} grows from 0V to 4V, voltage on Csf equals 0V. When V_{CC} is higher than 4V, Csf is loaded by a 3.7μA current, then TonMAX (Vcsf) will vary linearly from Tonmin to Tonmax according to Csfst bias.

When V_{CC} will go low (3.8 Volt threshold), Csf will be downloaded by an internal transistor.

Figure 6 : Soft Start Sequence.



POWER OUTPUT STAGE

Figure 7 : Electrical Schematic.

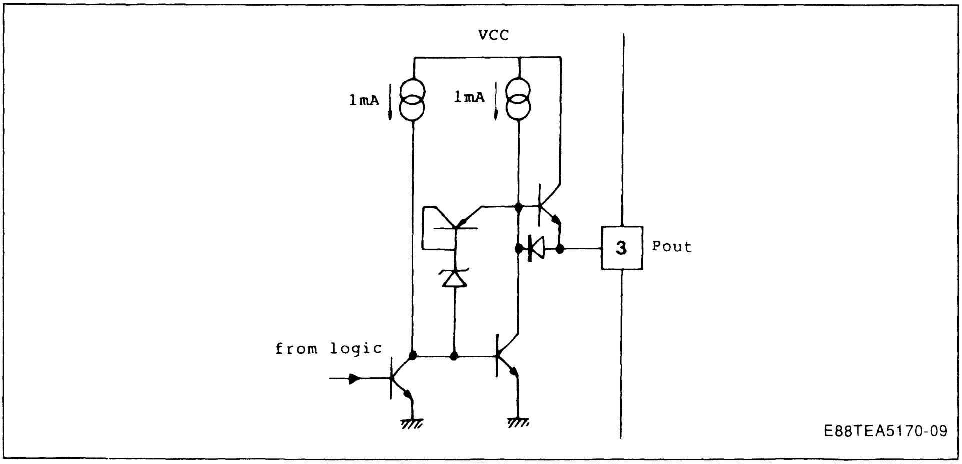


Figure 8.

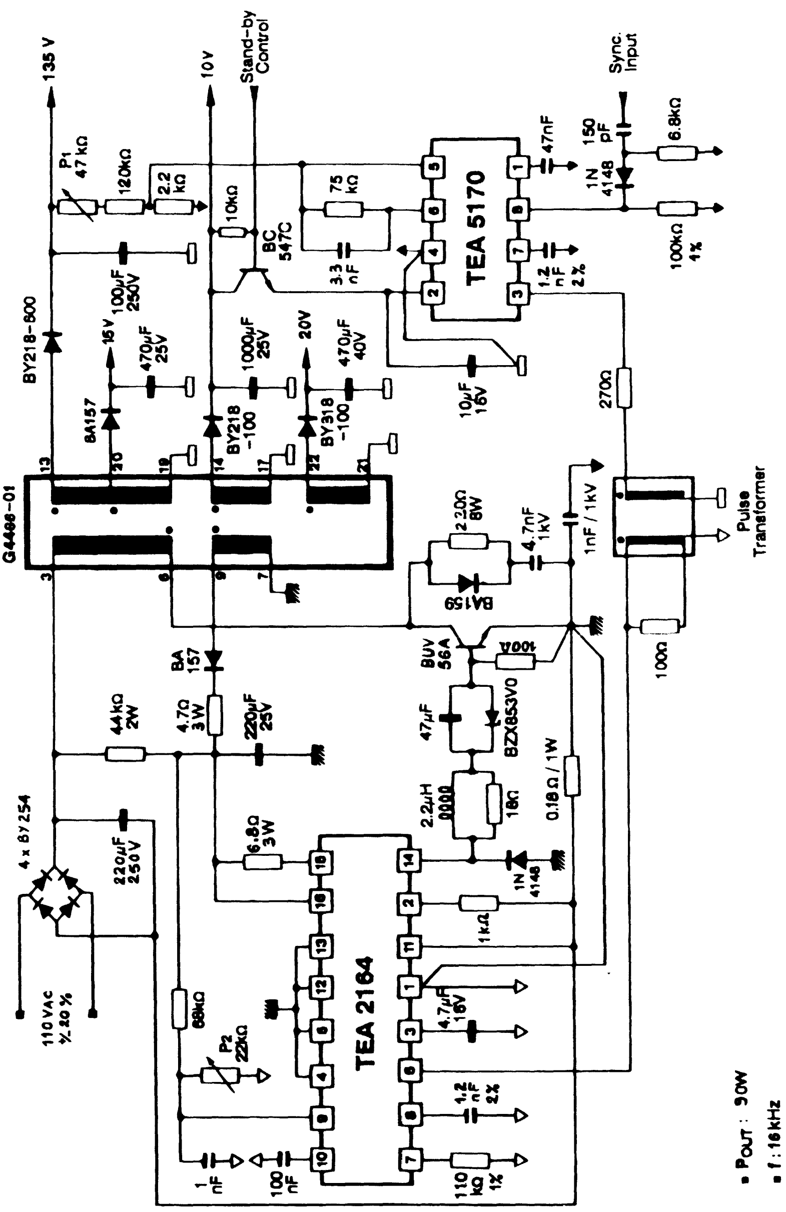


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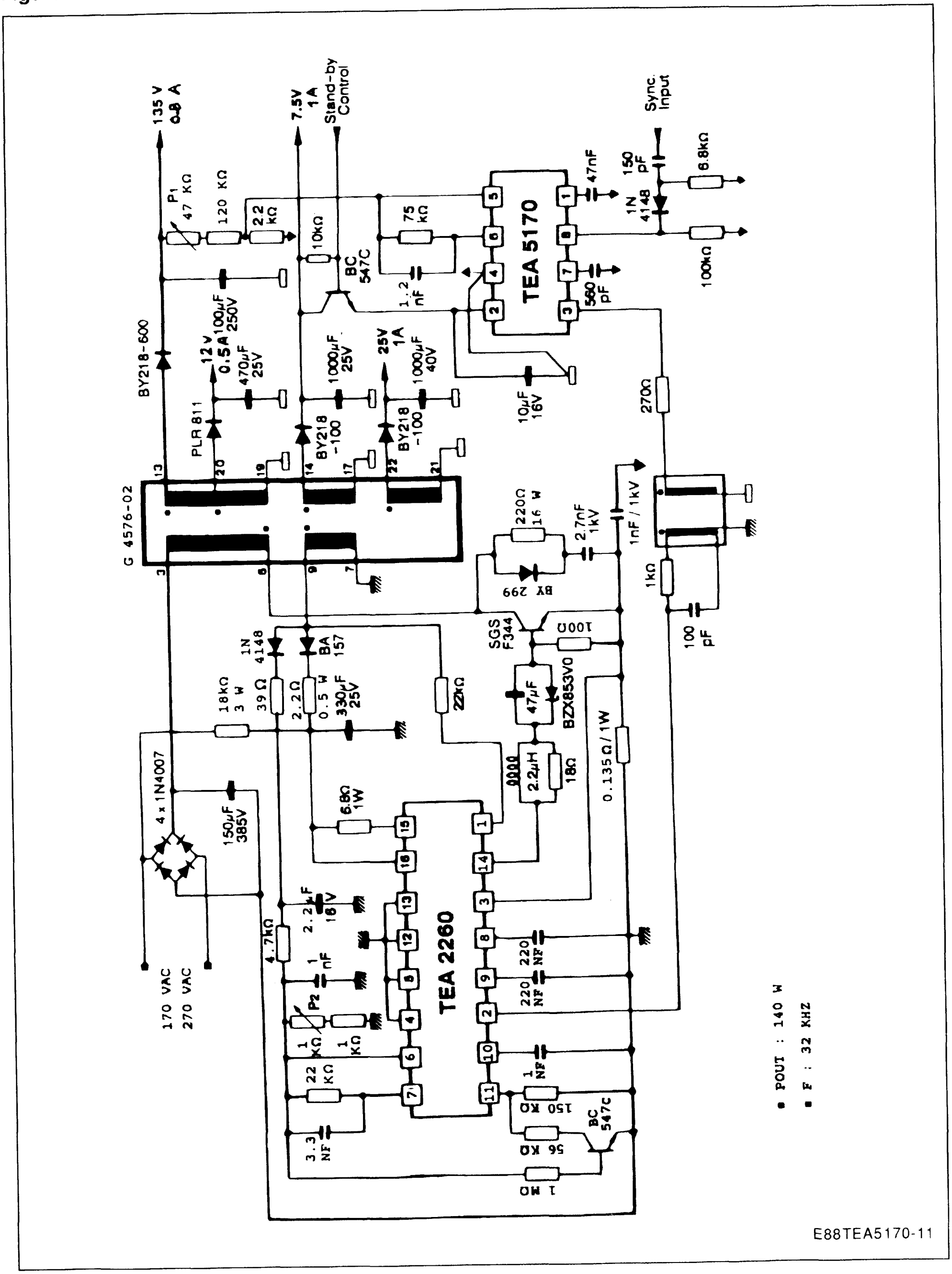
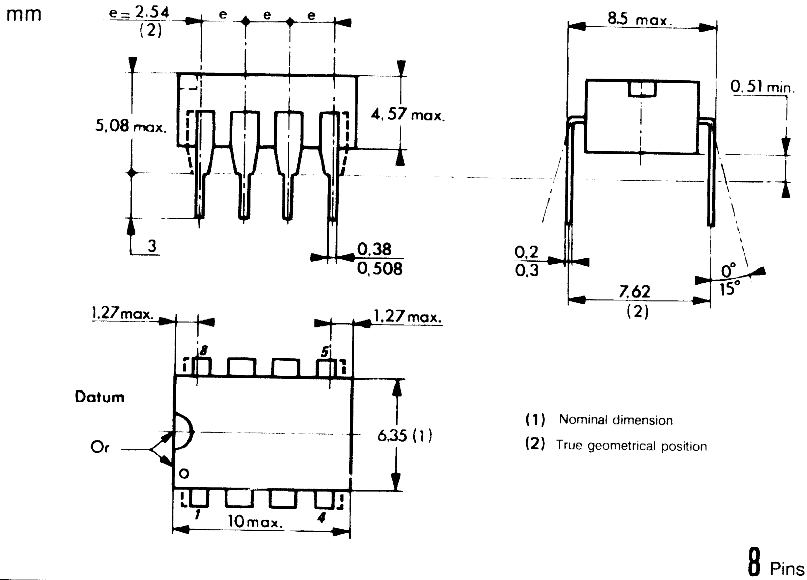
Figure 9.


135 V
0.8 A
7.5V
1A
Stand-by
Control
Sync.
Input
P1
47 KΩ
120 KΩ
2.2 KΩ
10kΩ
75 KΩ
47nF
150 pF
6.8kΩ
1N 4148
100kΩ
BC 547C
1.2 nF
TEA 5170
560 pF
100µF 250V
BY218-600
12 V
0.5A
470µF 25V
1000µF 25V
25V
1A
1000µF 40V
10µF 16V
270Ω
PLR 811
BY218 -100
G 4576-02
220Ω 16 W
2.7nF 1kV
1nF / 1kV
BY 299
1kΩ
100 pF
SGS F344
100Ω
1N 4148
BA 157
18kΩ 3 W
39 Ω
2.2Ω 0.5 W
330µF 25V
22kΩ
47µF
BZX853V0
2.2µH
18Ω
0.135Ω/1W
4 x 1N4007
150µF 385V
6.8Ω 1W
TEA 2260
4.7kΩ
2.2µF 16V
1 nF
220 NF
P2
1 KΩ
22 KΩ
3.3 NF
150 KΩ
56 KΩ
1 MΩ
BC 547C
170 VAC
270 VAC
POUT : 140 W
F : 32 KHZ
E88TEA5170-11

PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP



(1) Nominal dimension

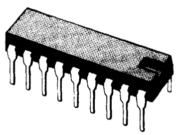
(2) True geometrical position

SGS-THOMSON MICROELECTRONICS

TEA5620

COLOR TV PAL DECODER

- PHASE LOCKED REFERENCE OSCILLATOR
- U AND V AXIS DECODERS
- ACC AND IDENTIFICATION DETECTORS
- KILLER
- USE OF A STANDARD 4.43 MHz Xtal
- COMPATIBILITY WITH THE SECAM DECODER TEA5630 FOR PAL-SECAM APPLICATION

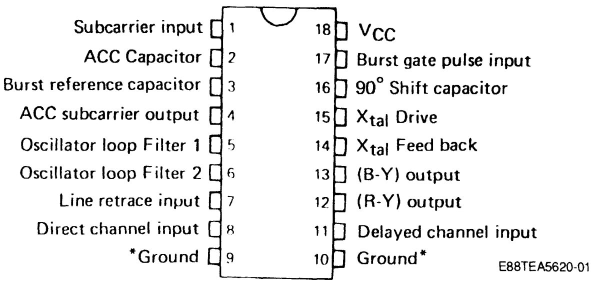


TEA5620
DIP18
(Plastic Package)

DESCRIPTION

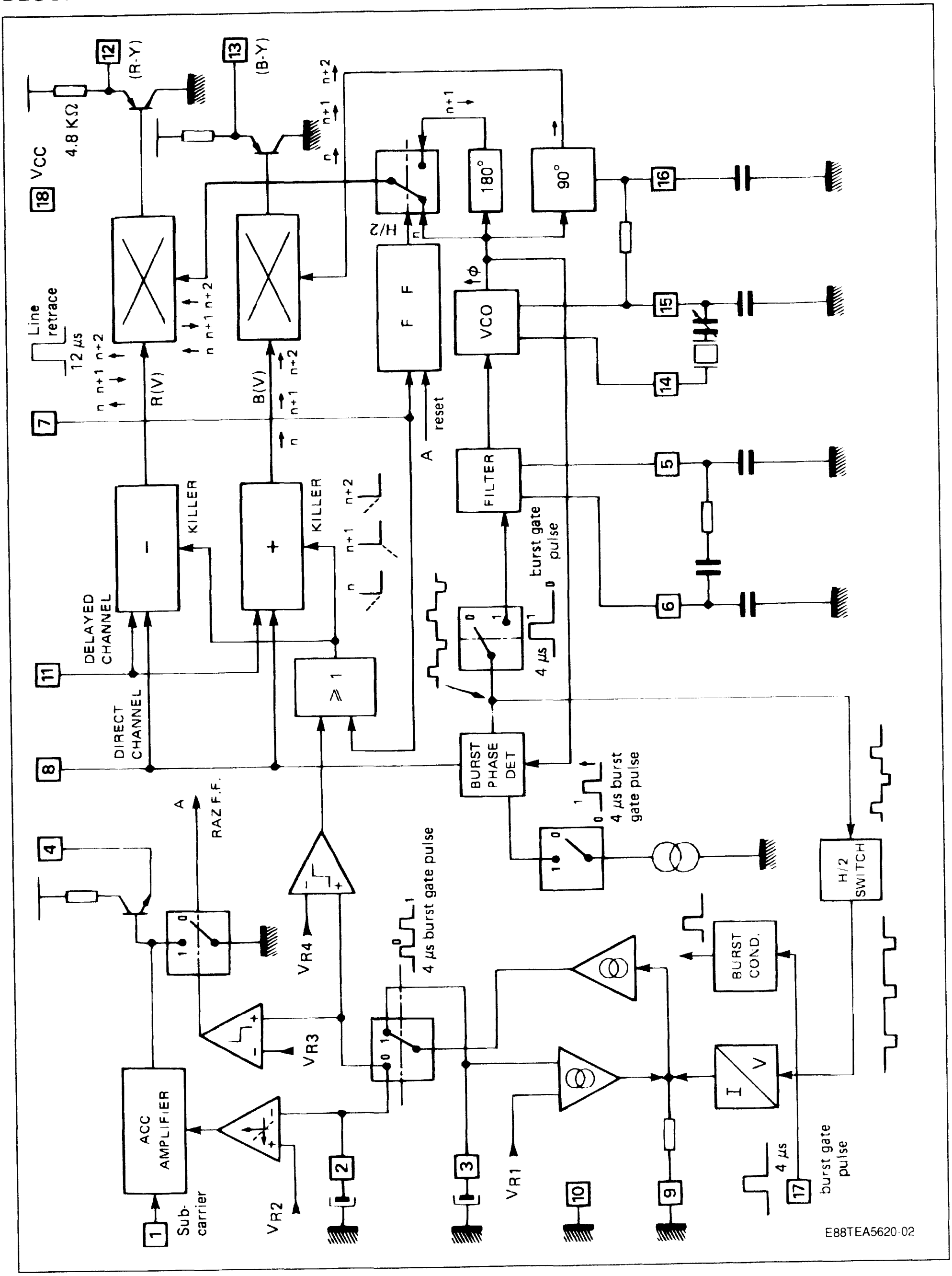
The TEA5620 is a color TV PAL decoder. It combines all functions required for the identification and demodulation of PAL signal.

PIN CONNECTIONS



* Pins 9 and 10 have to be both grounded.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14.4	V
P_D	Power Dissipation	800	mW
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j\text{-}a)}$	Junction–ambient Thermal Resistance	70	°C/W

DC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C V_{CC} = 12 V (unless otherwise specified)

(see test circuit 1)

Parameter		Switch State		Min.	Typ.	Max.	Unit
		S1	S2				
Operating Supply VOltage	Pin 18	1	1	10	12	14.4	V
Supply Current	Pin 18	1	1		40	52	mA
DC Voltage at :							
	Pin 1	1	1	5.1	5.7	6.3	V
	Pin 4	0	1	7.6	8.5	9.4	V
	Pin 5	1	2	6.2	7.7	9.2	V
	Pin 6	1	2	6.2	7.7	9.2	V
	Pin 8 - Pin 11	1	1	2.2	2.5	2.8	V
	Pin 12 - Pin 13	1	1	9.5	10.3	11.1	V
	Pin 14	1	2	8.7	9.5	10.7	V
	Pin 15 - Pin 16	1	1	2.7	3.3	3.9	V
DC Voltage, with Sample Pulse to Pin 17, at :	Pin 2 – Pin 3	0	3	4.3	4.7	5.3	V

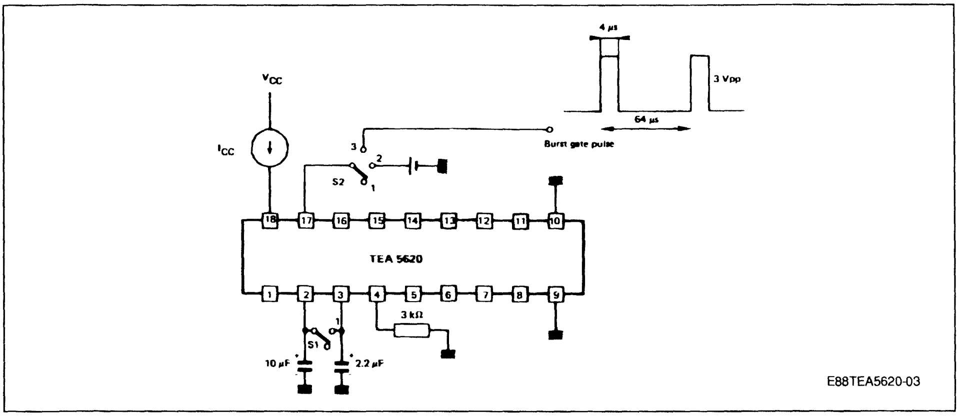
AC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C V_{CC} = 12 V (unless otherwise specified)

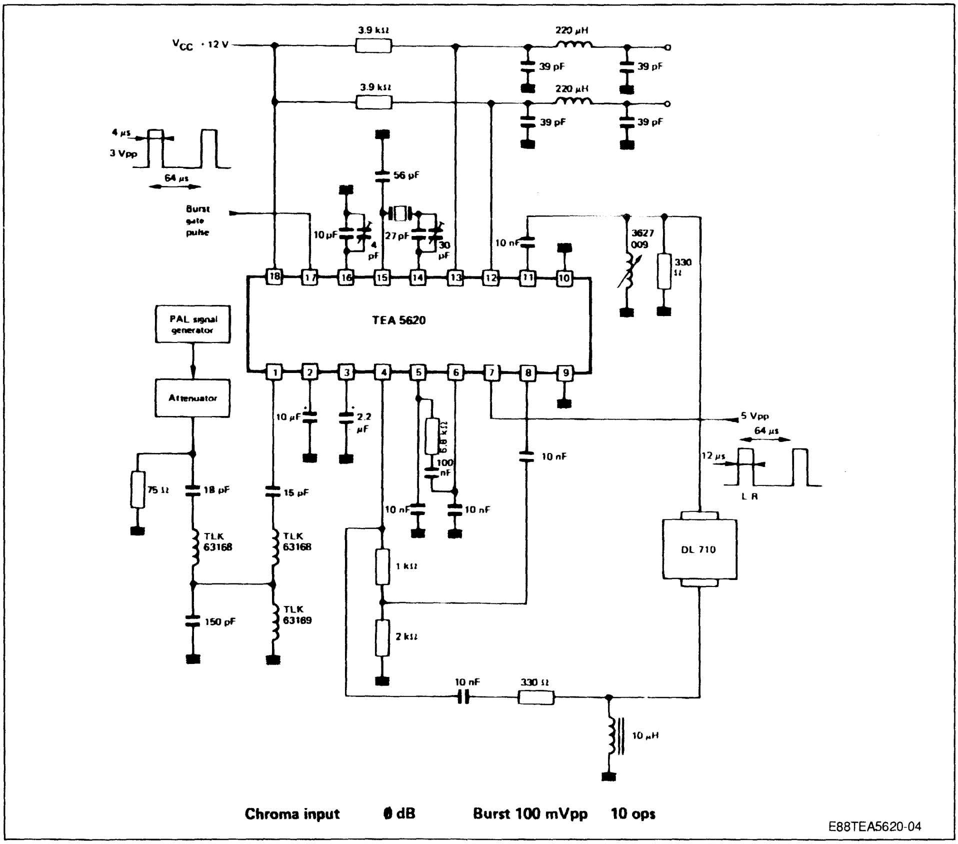
(see test circuit 2)

Symbol	Parameter		Min.	Typ.	Max.	Unit
BoV	ACC Amplifier Output Voltage (burst input : 0.1 Vpp)	Pin 4	0.45	0.6	0.76	Vpp
ΔBoV_1	ACC Amplifier Output Voltage Variation (burst input : + 6 dB = 0.2 Vpp)	Pin 4	– 1	0	+ 1	dB
ΔBoV_2	ACC Amplifier Output Voltage Variation (burst input : – 20 dB = 10 mVpp)	Pin 4	– 5	– 2	+ 1	dB
$ED1_{RY}$	R–Y Output Voltage (colour bar input signal : 0.1 Vpp)	Pin 12	0.7	1.4	1.95	Vpp
$ED1_{BY}$	B–Y Output Volage (colour bar input signal : 0.1 Vpp)	Pin 13	0.9	1.5	1.95	Vpp
$\frac{ED1_{BY}}{ED1_{RY}}$	Output Voltage Ratio : B–Y/R–Y		0.9	1.05	1.15	
$\Delta ED1_{RY}$	R–Y Output Voltage Variation (V_{CC} : 12 V to 14.4 V or V_{CC} : 12 V to 9.6 V)	Pin 12	0.15		0.55	Vpp
$\Delta ED1_{BY}$	B–Y Output Voltage Variation (V_{CC} : 12 V to 14.4 V or V_{CC} : 12 V to 9.6 V)	Pin 13	0.15		0.55	Vpp
EL	HF Residual Voltage (colour bar input signal : 0.1 Vpp)	Pins 12 – 13		100	120	mVpp
EK	Colour Killer Level (reference input signal : 0.1 Vpp)		– 40	– 35	– 30	dB
ELK	Colour Killer Leakage (colour killer on)	Pins 12 – 13			20	mVpp
V_{CC}	Minimum Supply Voltage for Internal Oscillator Operation			6	8	V
Ri_1 Cl_1	Input Impedance (input signal : F = 4.43 MHz V_i = 100 mVpp)	Pin 1		2.8 10		kΩ pF
To	Delay time between line retrace pulse and first colour response	Pin 12	0.4	1.3	2	µs
	VCO Control Sensitivity : Variation of Frequency Oscillator Versus Pin 5 to Pin 6 Difference Voltage (burst input 0.7 Vpp on pin 8)			1.8		Hz/mV
Fp	Pull–in Frequency Range (variation of burst frequency)	Pin 15		± 800		Hz
∅	Phase Hold Characteristics (phase deviation for ΔF burst = 100 Hz)			0.03		°/Hz
V_{dir}	Line retrace threshold	Pin 7		2.5		V
V_{dl}	Sampling Pulse Threshold	Pin 17	0	.6	0.8	1

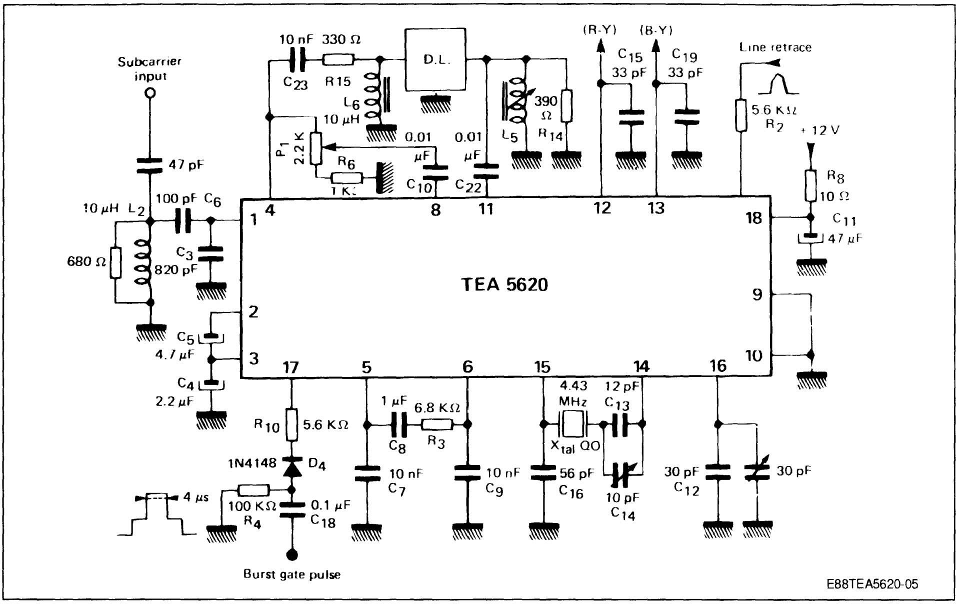
Test Circuit 1.



Test Circuit 2.



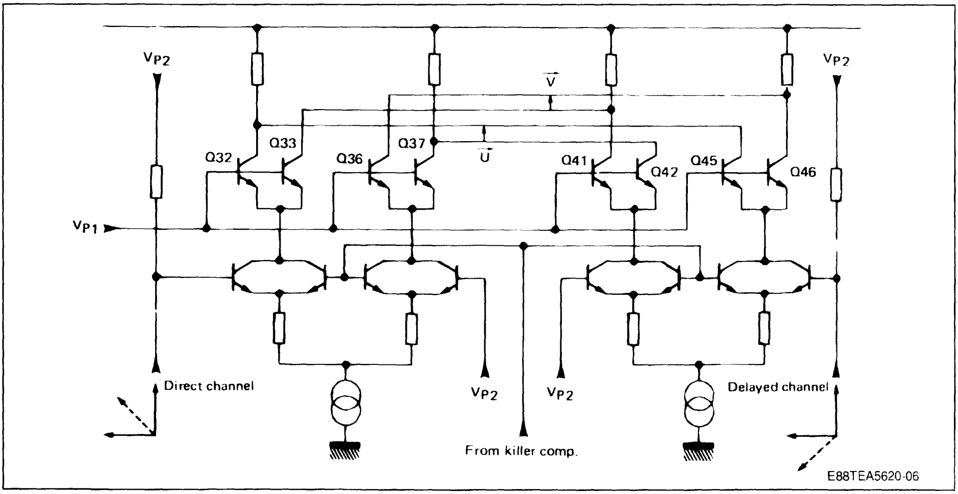
TYPICAL PAL APPLICATION



GENERAL DESCRIPTION

DL MATRIX

The adding and substraction function for the direct signal and the delayed signal are also performed by the IC with the under circuit. The U matrix is made with Q32 - Q45 - Q37 - Q42 ; the V matrix is made with Q33 - Q41 - Q46 - Q36. The integration of the DL matrix only requires one delay line for the PAL/SECAM application with the TEA5630. It also allows lower cost for external components.



ACC AMPLIFIER

This ACC amplifier is performed with a double differential stage. The subcarrier is sent to the input of the first pair, while the second is connected to a reference voltage. The gain of the amplifier is controlled by the ACC voltage, by switching the bias current through a third differential pair.

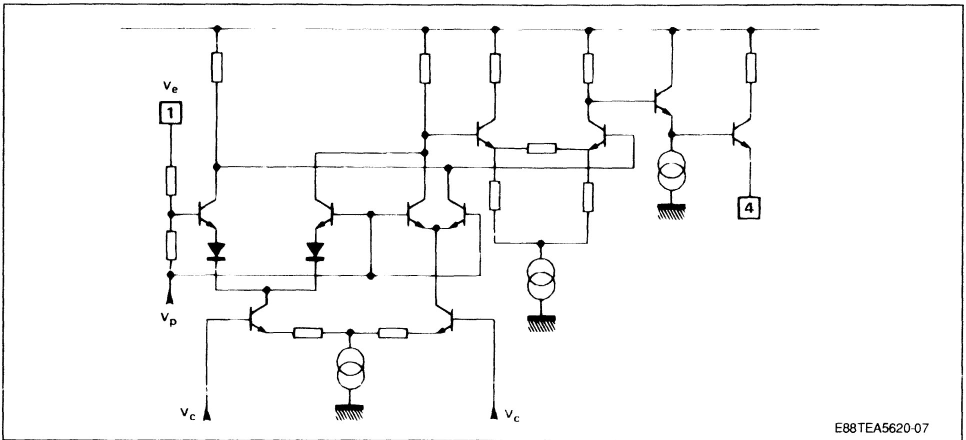
The dynamic range obtained by this device is 32 dB. The bias voltage on the pin 1 is 5.6 V. The burst signal delivered by the pin 4 is about 0.6 Vpp for an input signal on pin 1 variable from 5 to 200 mV.

U AND V AXIS DECODERS

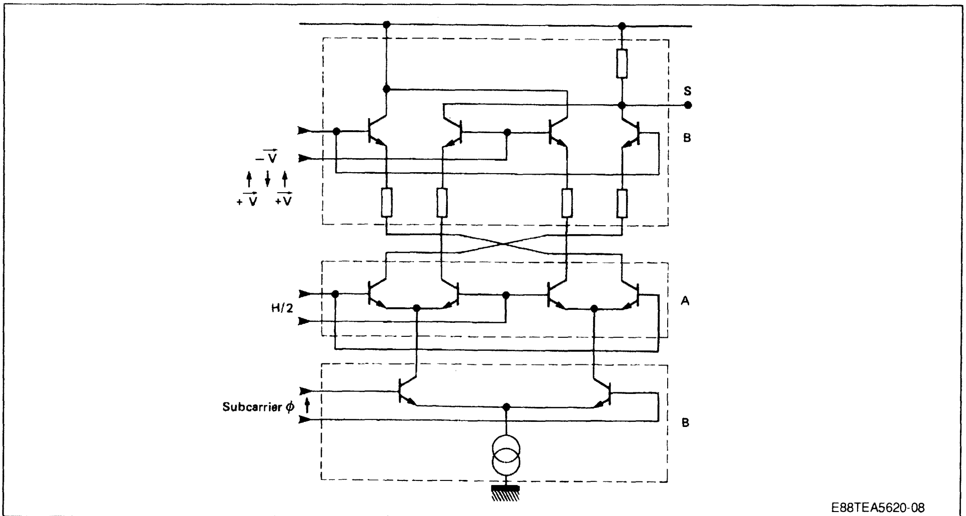
They consist on two phase detector stages (B). They provide output signals proportionnal to the magnitude of the chroma signal phased with the regenerated subcarrier feeding the stage.

The subcarrier is fed to the Vaxis decoder through an H/2 switch (A). This switch is required to make the phase of this signal the same than the burst.

ACC amplifier.



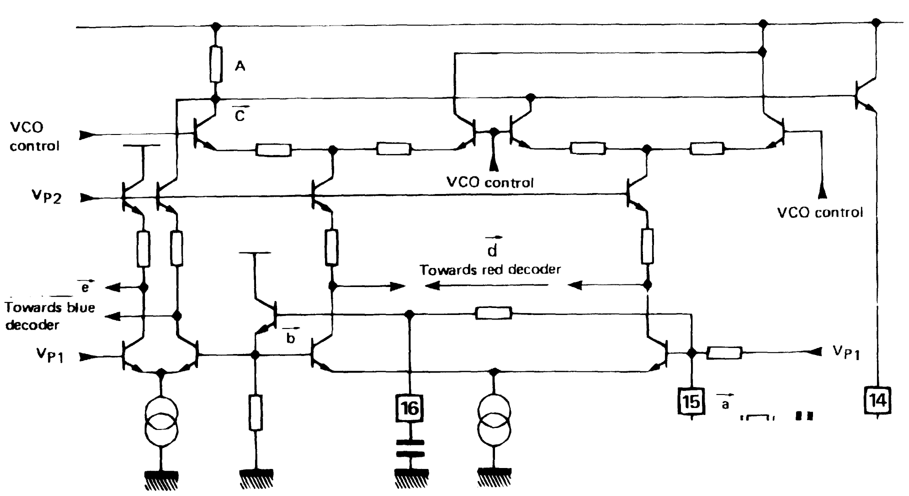
U and V Axis Decoders.



VOLTAGE CONTROL OSCILLATOR

The frequency of the VCO is depending on the vector adding performed at point A between $\vec{b}$ and $\vec{d}$ (see graphe). This adding is controlled by the voltage coming from the burst phase detector. This VCO is attractive because it uses a standard low cost Xtal. The 90 ° phase shift is made by vector addition and by a 45 ° phase shifter connected to the pin 16.

Voltage Control Oscillator.



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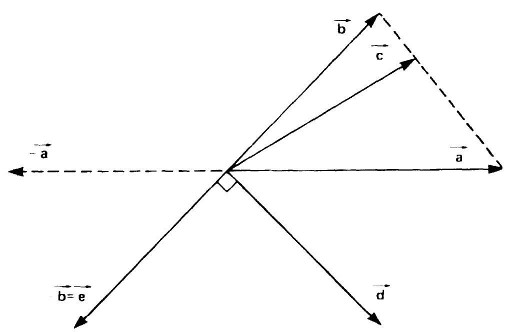
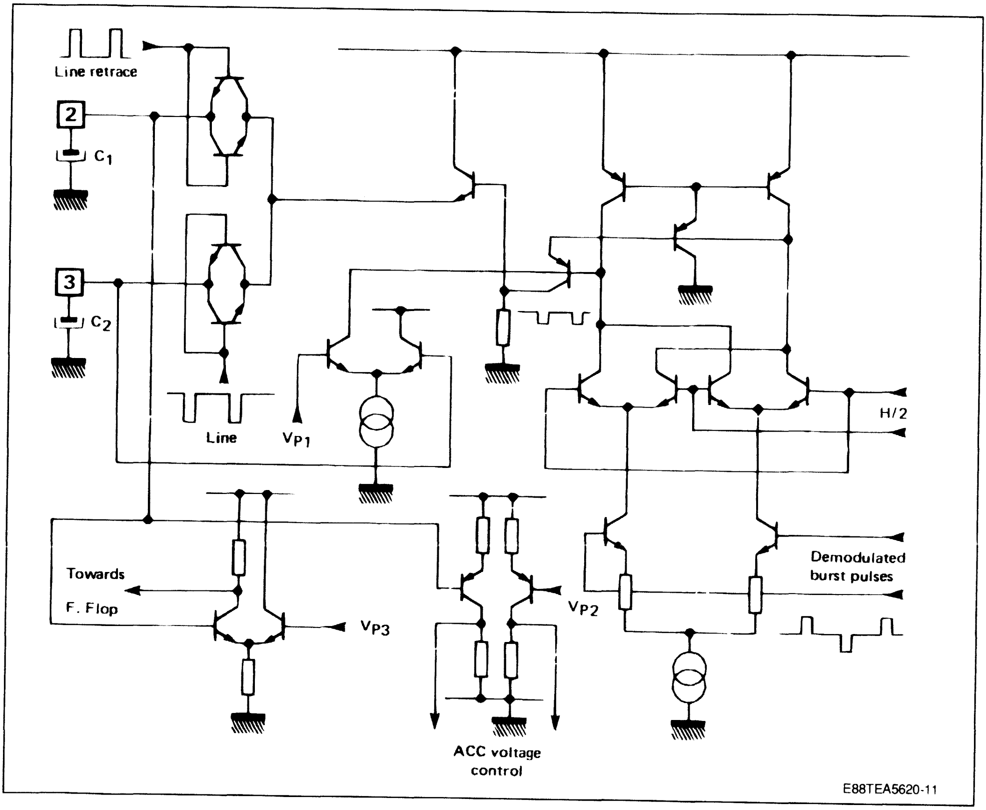


E88TEA5620-10

SAMPLING AND HOLD STAGE

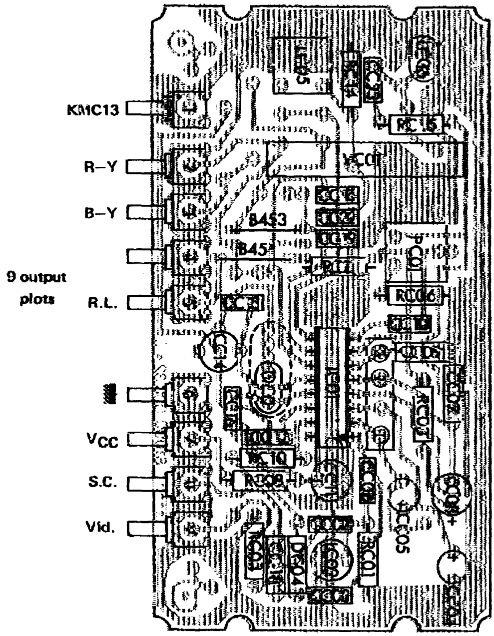
This stage performs the identification and provides the ACC control voltage. A bias voltage is stored in C_2 capacitor during the line trace. The C_1 capacitor stores this bias voltage decreased by the demodulated burst peak value. So the differential voltage between C_1 and C_2 is not depending of a bias voltage, out of any drift, and therefore suitable to control the ACC amplifier.

Sampling and Hold Stage.



TYPICAL APPLICATION (see electric diagram page 6)

Component Side.



E88TEA5620-12

N°	Capa.	U	%
CC02	47 pF		
CC03	820 pF		
CC04	2.2 µF	63	
CC05	4.7 µF	35	
CC06	100 µF		
CC07	0. 01 µF	250	
CC08	1 µF	63	
CC09	0.01 µF	250	
CC10	10 nF		
CC11	47 µF	16	
CC12	56 pF		
CC13	12 pF		
CC14	10-30 pF		
CC15	33 pF		
CC16	56 pF		
CC18	0.1 µF	100	
CC19	33 pF		
CC22	10 nF		
CC23	10 nF		

N°	Value	P	%
RC01	820 Ω		5
RC02	5.6 k		5
RC03	6.8 kΩ		5
RC04	100 kΩ		5
RC06	1 kΩ		5
RC08	27 Ω		
RC10	5.6 kΩ		5
			5
			5
RC14	390 Ω		5
RC15	330 Ω		5

N°	Value
LC02	10 µH
LC05	7 - 13 µH
LC06	10 µH

N°	Value
VC01	DL710

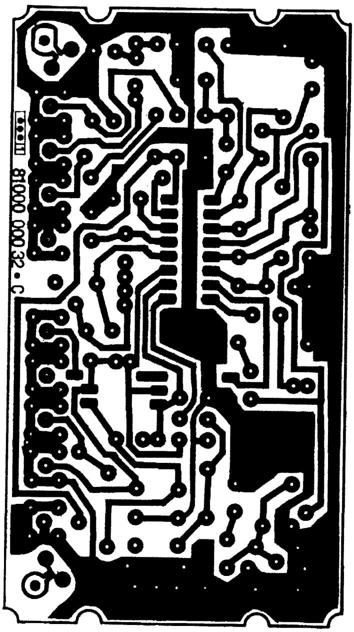
N°	Value
PC01	2.2 kΩ

N°	Value
QC0	4433.619 kHz

N°	Type
DC04	1N4148

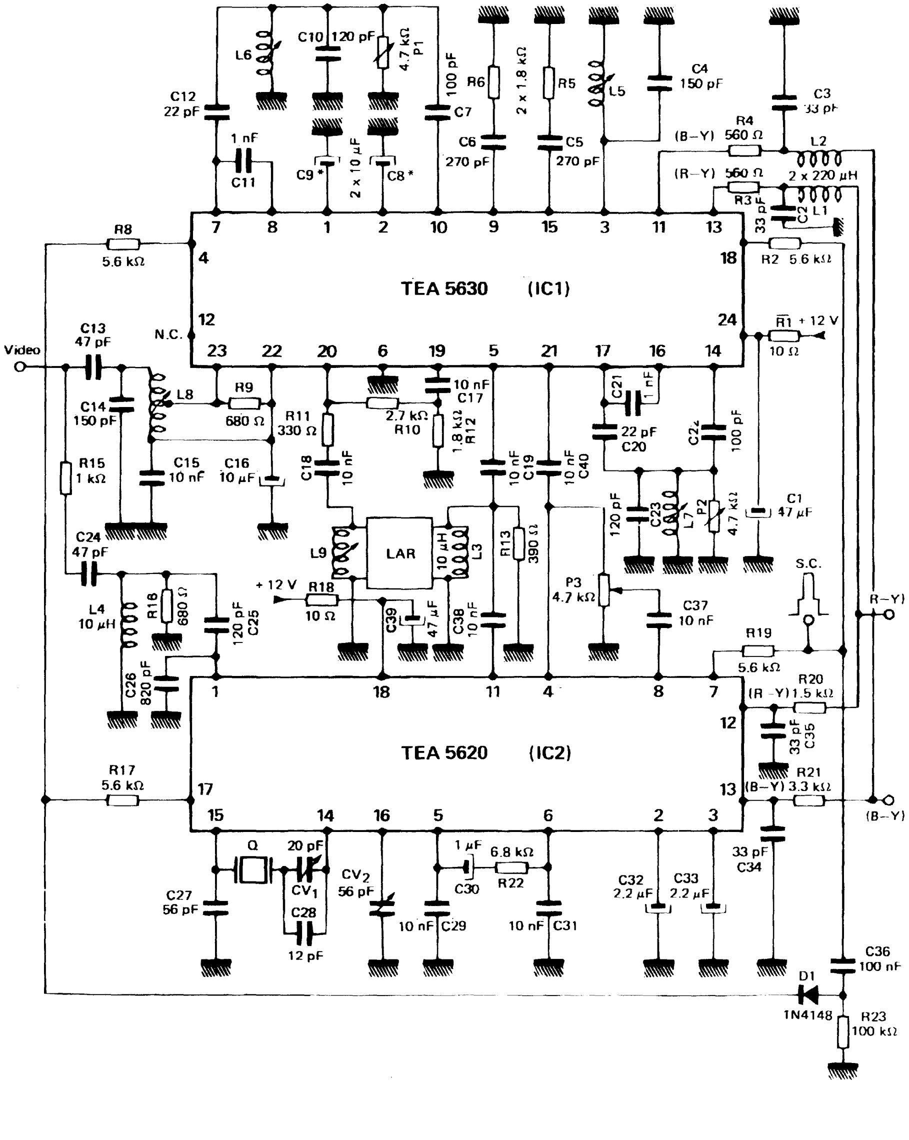
N°	Type
IC01	TEA5620

Copper Side.



E88TEA5620-13

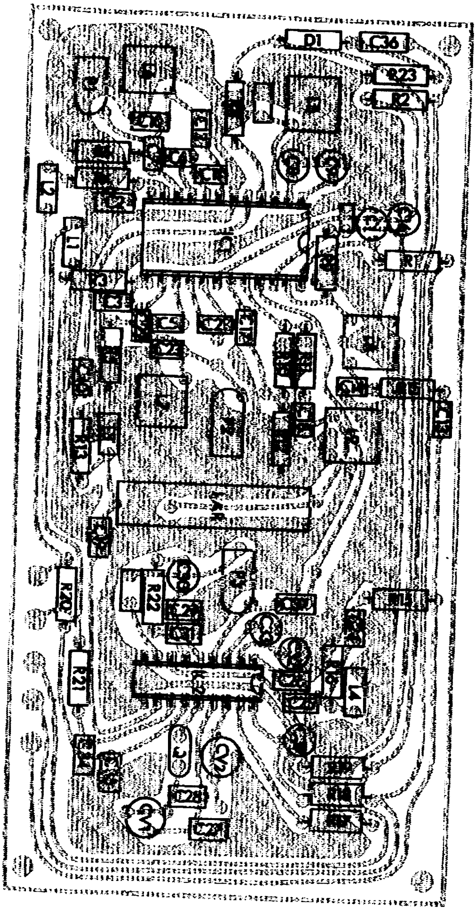
PAL SECAM APPLICATION TEA5620-TEA5630



E88TEA5620-14

* C8, C9 values can be reduced to 1 μF (polypropylène capacitors) if line identification only.

Component Side.



E88TEA5620-15

N°	Value
C1	47 µF
C2	33 pF
C3	33 pF
C4	150 pF
C5	270 pF
C6	270 pF
C7	100 pF
C8-C9	10 µF/16 V
C10	120 pF
C11	1 nF
C12	22 pF
C13	47 pF
C14	150 pF
C15	10 nF
C16	10 µF/16 V
C17	10 nF
C18	10 nF
C19	10 nF
C20	22 pF
C21	1 nF
C22	100 pF
C23	120 pF
C24	47 pF
C25	120 pF
C26	820 pF
C27	56 pF
C28	12 pF
C29	10 nF
C30	1 µF/16 V
C31	10 nF
C32	2.2 µF/16 V
C33	2.2 µF/16 V
C34	33 pF
C35	33 pF
C36	100 nF
C37	10 nF
C38	10 nF
C39	47 µF/25 V
C40	10 nF

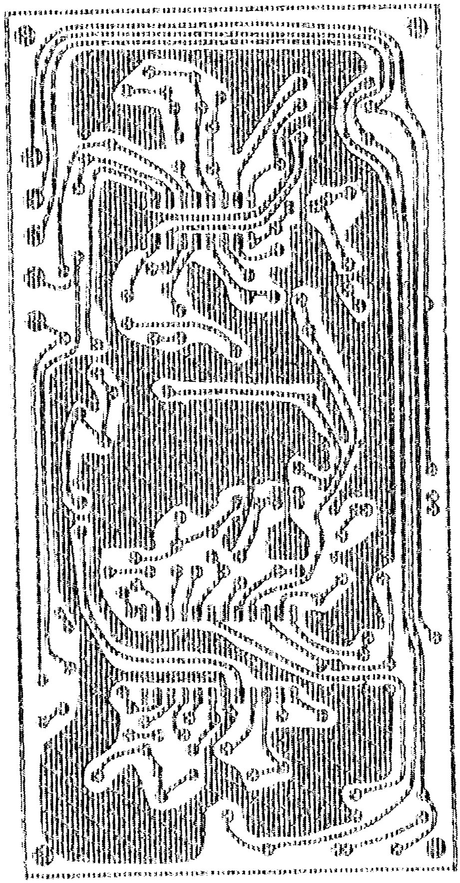
N°	Value
R1	10 Ω
R2	5.6 kΩ
R3	560 Ω
R4	560 Ω
R5	1.8 kΩ
R6	1.8 kΩ
R8	5.6 kΩ
R9	680 Ω
R10	2.7 kΩ
R11	330 Ω
R12	1.8 kΩ
R13	390 Ω
R15	1 kΩ
R16	680 Ω
R17	5.6
R18	kΩ
R19	10 Ω
R20	5.6 kΩ
R21	1.5 kΩ
R22	3.3 kΩ
R23	6.8 kΩ

N°	Value
P1	4.7 kΩ
P2	4.7 kΩ
P3	4.7 kΩ
Q Quartz	4.433 MHz
CV_1	3-30 pF
CV_2	6-60 pF

N°	Type or Value
D1	1N4148
LAR :	LAA64 µs
IC_1	TEA5630
IC_2	TEA5620
L1	220 µH
L2	220 µH
L3	10 µH
L4	10 µH
L8	0.7-1.3 µH

N°	Type	Value
L5	TOKO RCL 36270-14	10-15 µH
L6	TOKO RCL 36270-13	7 µH
L7	TOKO RCL 36270-13	7 µH
L8	TOKO RCL 36270-09	10 µH

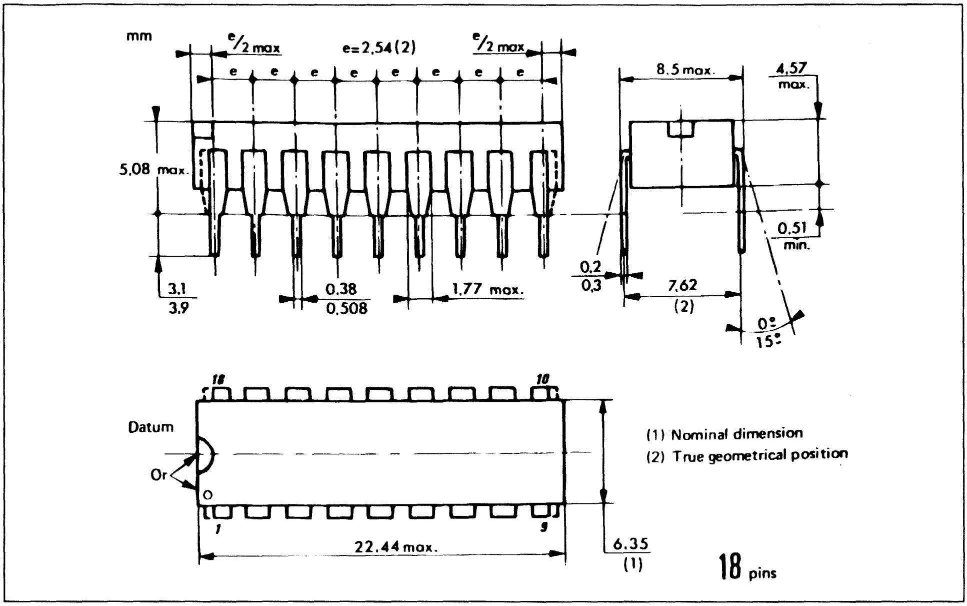
Copper Side.



E88TEA5620-16

PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP

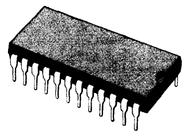


SGS-THOMSON
MICROELECTRONICS

TEA5630

COLOR TV SECAM DECODER FOR LOW-COST TV SETS

- SUBCARRIER LIMITER
- R - Y, B - Y } DEMODULATORS
- IDENTIFICATION AND KILLER
- PAL-SECAM SWITCHES FOR MULTISTANDARD APPLICATION.

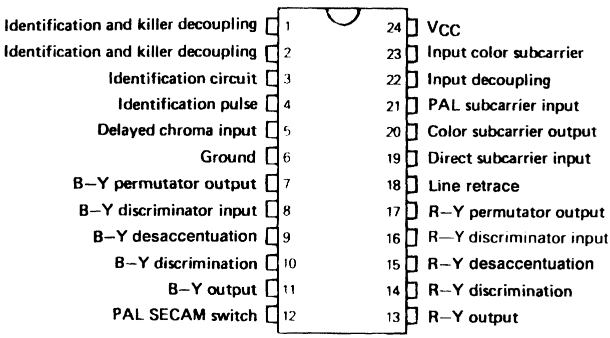


TEA5630
DIP24
(Plastic Package)

DESCRIPTION

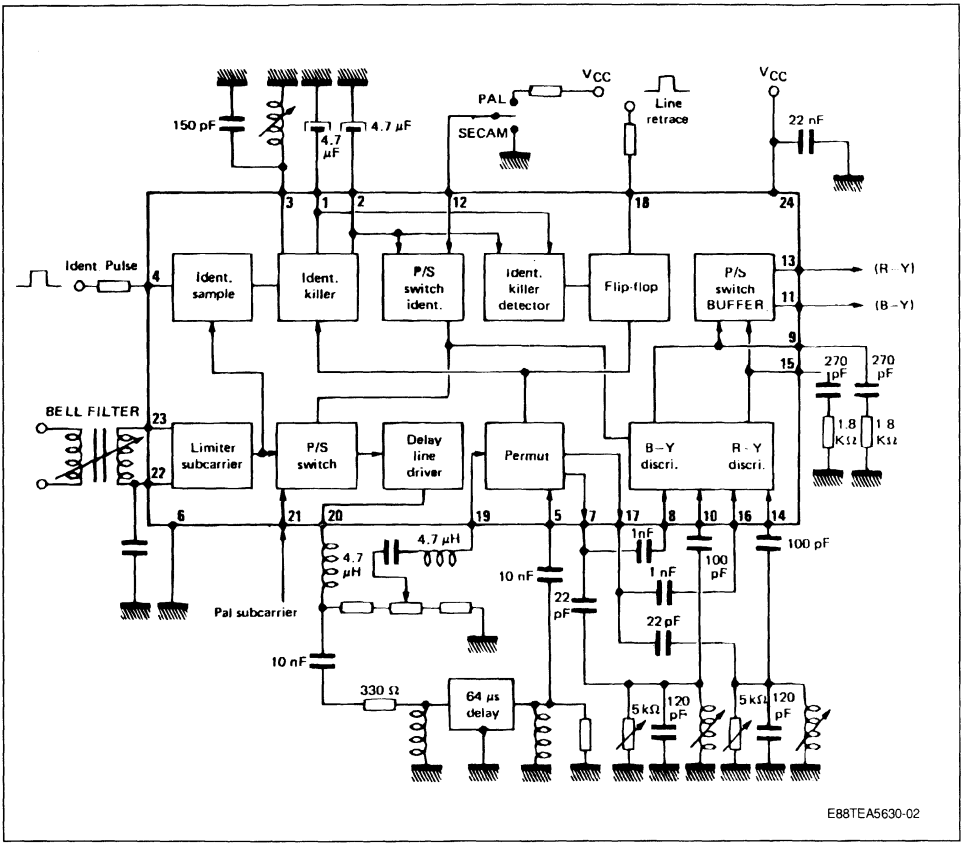
The TEA5630 is a complete color TV secam decoder which has PAL-SECAM switches for Multistandard application (in association with the TEA5620).

PIN CONNECTIONS



E88TEA5630-01

BLOCK DIAGRAM



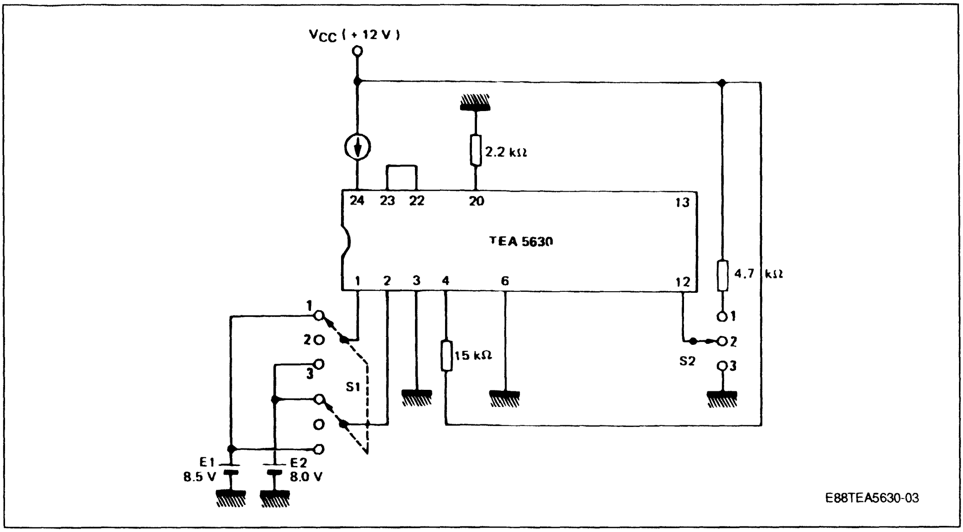
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	14.4	V
P_{tot}	Power Dissipation	760	mW
T_{oper}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th(j-a)}$	Junction-ambient Thermal Resistance	60	°C/W

TEST CIRCUIT 1



DC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25 °C V_{CC} = 12 V (unless otherwise specified)

TEST CIRCUIT 1

Parameter		Switch State		Min.	Typ.	Max.	Unit
		S1	S2				
Operating Supply Voltage	Pin 24	2	2	9.6	12	13	V
Supply Current	Pin 24	2	2	20	30	40	mA
DC Voltage at :							
	Pin 1, Pin 2	2	3	4.8	5.7	6.4	V
	Pin 5, pIn 19	2	3	1.8	2.4	3	V
	Pin 7, Pin 17	2	3	10.6	11.2	11.8	V
	Pin 8, Pin 16	2	3	4.7	5.4	6.1	V
	Pin 9, Pin 15	2	3	6.3	7.2	8	V
	Pin 10, Pin 14	2	3	2.5	3.3	4	V
	Pin 11, Pin 13	2	3	6.8	8	9	V
	Pin 20	2	3	6.8	7.9	9	V
	Pin 21	2	3	2.6	3.3	4	V
	Pin 22	2	3	2.3	3	3.7	V
	Pin 9, Pin 15	2	1	11.7	11.9		V
	Pin 11, Pin 13	2	1	11.7	11.9		V
	Pin 12	2	2	0.85	1.1	1.3	V
	Pin 12	1	2	0	0.1	0.2	V
	Pin 12	3	2	0	0.1	0.2	V

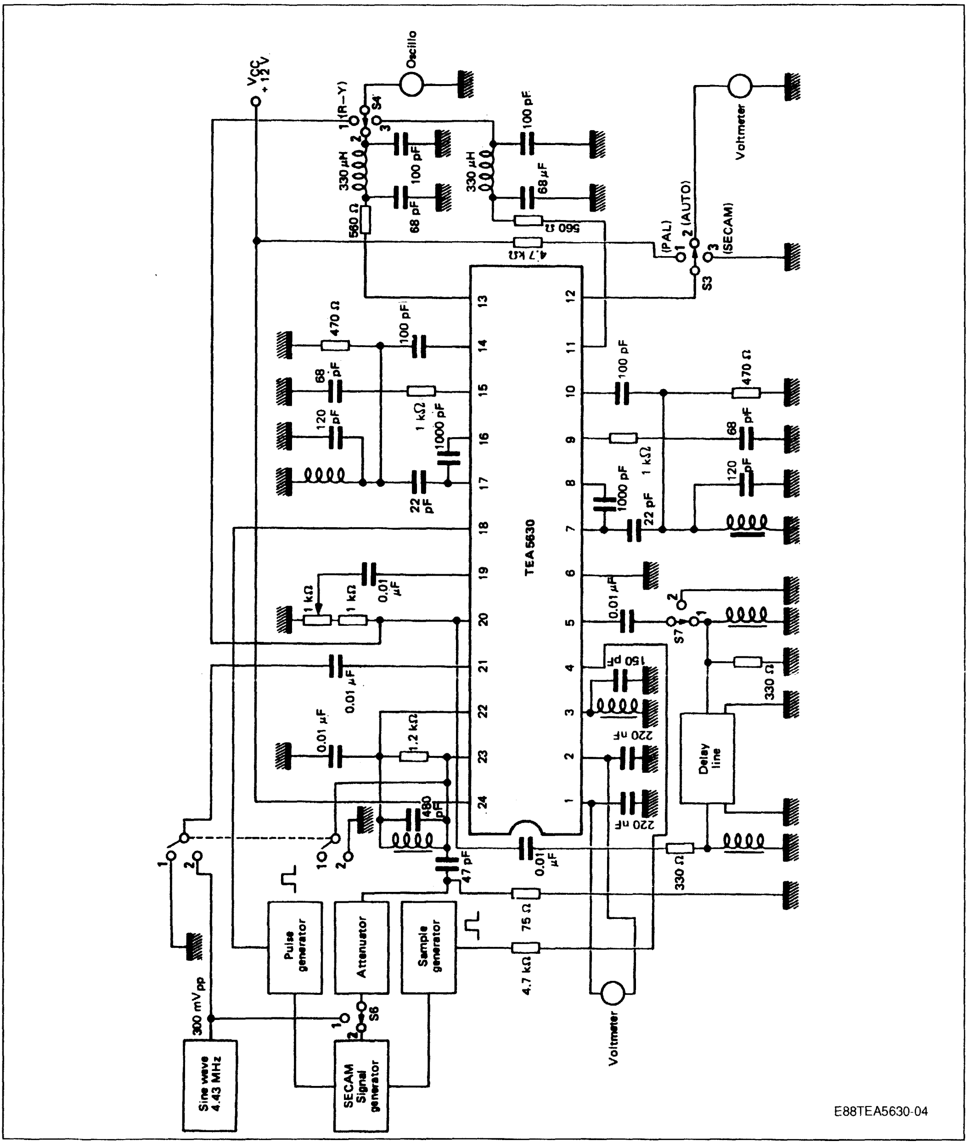
AC ELECTRICAL CHARACTERISTICS

T_{amb} = + 25°C, V_{CC} = 12V (unless otherwise specified)

TEST CIRCUIT 2

Symbol	Parameter		Min.	Typ.	Max.	Unit
Elim-1	Limiter Amplifier Output Voltage (V_I = 100 mVpp)	Pin 20	1.7	2.2	2.7	Vpp
Elim-2	Limiter Amplifier Output Voltage (V_I = – 30 dB = 3.2 mVpp)	Pin 20	0.6	1.4	2.4	Vpp
AvPAL	PAL Amplifier Gain : VO (pin 20)/V_I(pin 21) (V_I = 300 mVpp)		0.95	1.1	1.3	
	Permutator Output (V_{19} = V_5 = 400 mVpp)	Pin 7-Pin 17		1.4		Vpp
	Permutator Input Impedance	Pin 19-Pin 5		2.5		kΩ
CT1	Permutator Crosstalk (S7 = position 2)			– 60		dB
$ED1_{BY}$	B-Y Output Voltage (colour bar signal generator 75 %)	Pin 11	0.6	1	1.3	Vpp
$ED1_{RY}$	R-Y Output Voltage (colour bar signal generator 75 %)	Pin 13	0.7	1.2	1.6	Vpp
R_o	output Voltage Ratio R-Y/B-Y (colour bar signal generator 75 %)		0.95	1.2	1.5	
$ED2_{BY}$	B-Y Output Voltage (colour bar signal generator 75 %, – 16 dB)	Pin 11	0.6	1	1.3	Vpp
$ED2_{RY}$	R-Y Output Voltage (colour bar signal generator 75 %, – 16 dB)	Pin 13	0.7	1.2	1.6	Vpp
	PAL/SECAM Switch Threshold	Pin 12		1.1		V
V12R1	Input Level Attenuation for PAL/SECAM switching - Measure on Pin 12 (colour bar generator 75 %, – 40 dB)		0.9	1.05	1.2	V
V12R2	Input Level Attenuation for NO PAL/SECAM Switching - Measure on Pin 12 (colour bar generator 75 %, – 18 dB)				0.2	V
PRS1	PAL/SECAM Switching Crosstalk (SECAM mode - PAL input signal pin 21 : 300 mVpp)			– 33		dB
PRS2	PAL/SECAM Switching Crosstalk (PAL mode - SECAM input signal pins 23-22 : 5 mVpp)			– 50		dB
FF	Line retrace Threshold	Pin 18	0.85	1	1.07	V
	Identification Sampling Pulse Threshold	Pin 4		0.8		V

TEST CIRCUIT 2



	$V_O(1)$	$V_O(2)$	A_V	$e_o(1)$ B–Y	$e_o(1)$ R–Y	e_k	C_{T1}	C_{T2}
S_3	2	3	1	2	2	3	2	3
S_4	1	1	1	3	3	3	3	1
S_5	1	1	2	1	1	1	1	2
S_6	2	2	2	2	2	2	2	2

GENERAL DESCRIPTION

LIMITER AND CHROMA PAL/SECAM SWITCHING

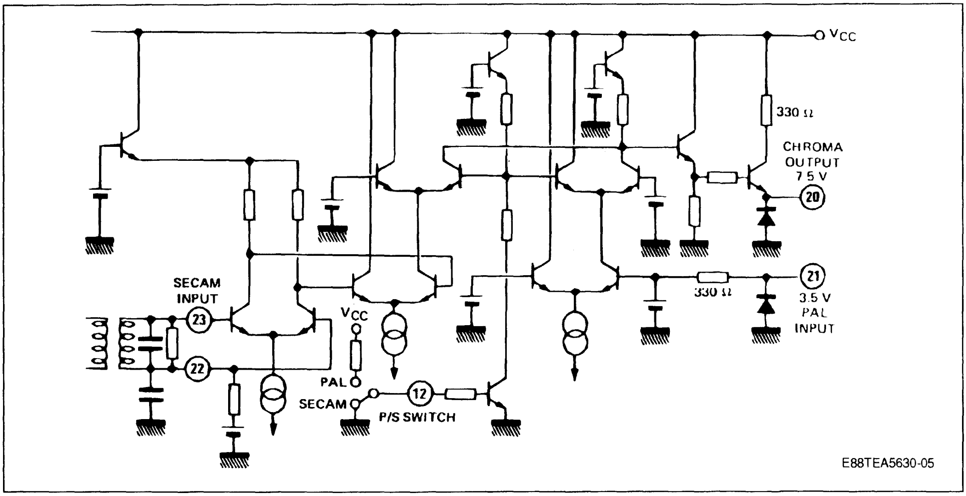
The chroma signal is applied to the input of a limiter stage. After limitation the output signal is sent to an electronical switch which selects the signal coming from the limiter (for SECAM) or from the PAL input (Pin 21). The high output voltage of chrominance signal, 2.2 V_{pp} in SECAM operation, permits to obtain a minimum of crosstalk in the permutation and discrimination. The DC output voltage of the PAL IC connected in parallel for PAL/SECAM must be higher than $V_{CC} - 5$ V.

IDENTIFICATION AND KILLER

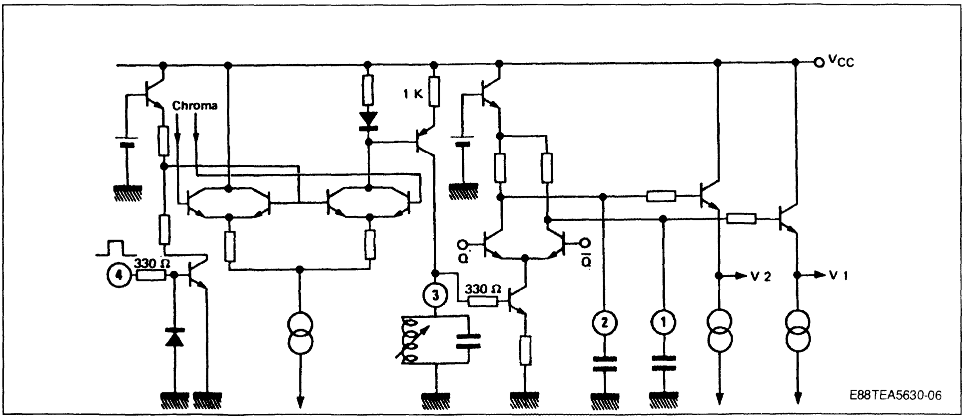
The identification information is sampled during the identification pulse (pin 4). The burst differential amplitude voltage on the according circuit pin 3 is amplified and held by capacitors pin 2 and pin 1 to give the right flip-flop phase and killer information.

The circuit is able to identify line by line or line and frame. The choice of identification mode is programmable by the user depending on the identification pulse pin 4.

LIMITER AND CHROMA PAL/SECAM SWITCH.



IDENTIFICATION AND KILLER.



PERMUTATOR

Two inputs on the permutator :
- the direct signal is sent on pin 19,
- the delayed signal is sent on pin 5.

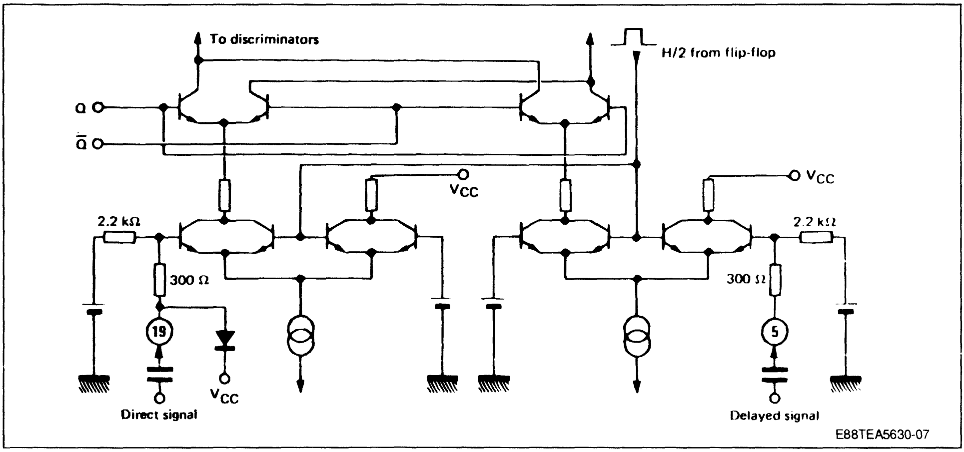
The permutator is controled by a flip-flop at H/2 frequency in order to have (R – Y) signal on pin 17 and (B – Y) signal on pin 7. The output chroma signal typical value is 1.4 V.

DISCRIMINATORS

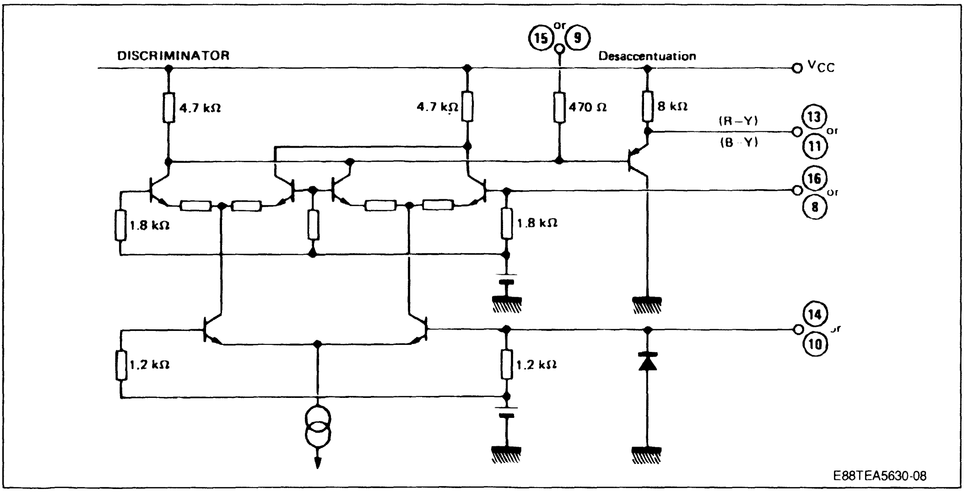
They use coincidence detectors with external according circuit L-C. The (R – Y) and (B – Y) demodulated signal amplitude and linearity can be adjusted by the choice of the damping resistor value in parallel with the L-C circuit. The desaccentuation circuit is connected on the load of the coincidence detection.
Two PNP emitter followers provide the (R – Y) and (B – Y) signals at low impedance output.

In PAL operating the output impedance is equivalent to a 8 KΩ resistance between output and V_{CC}.

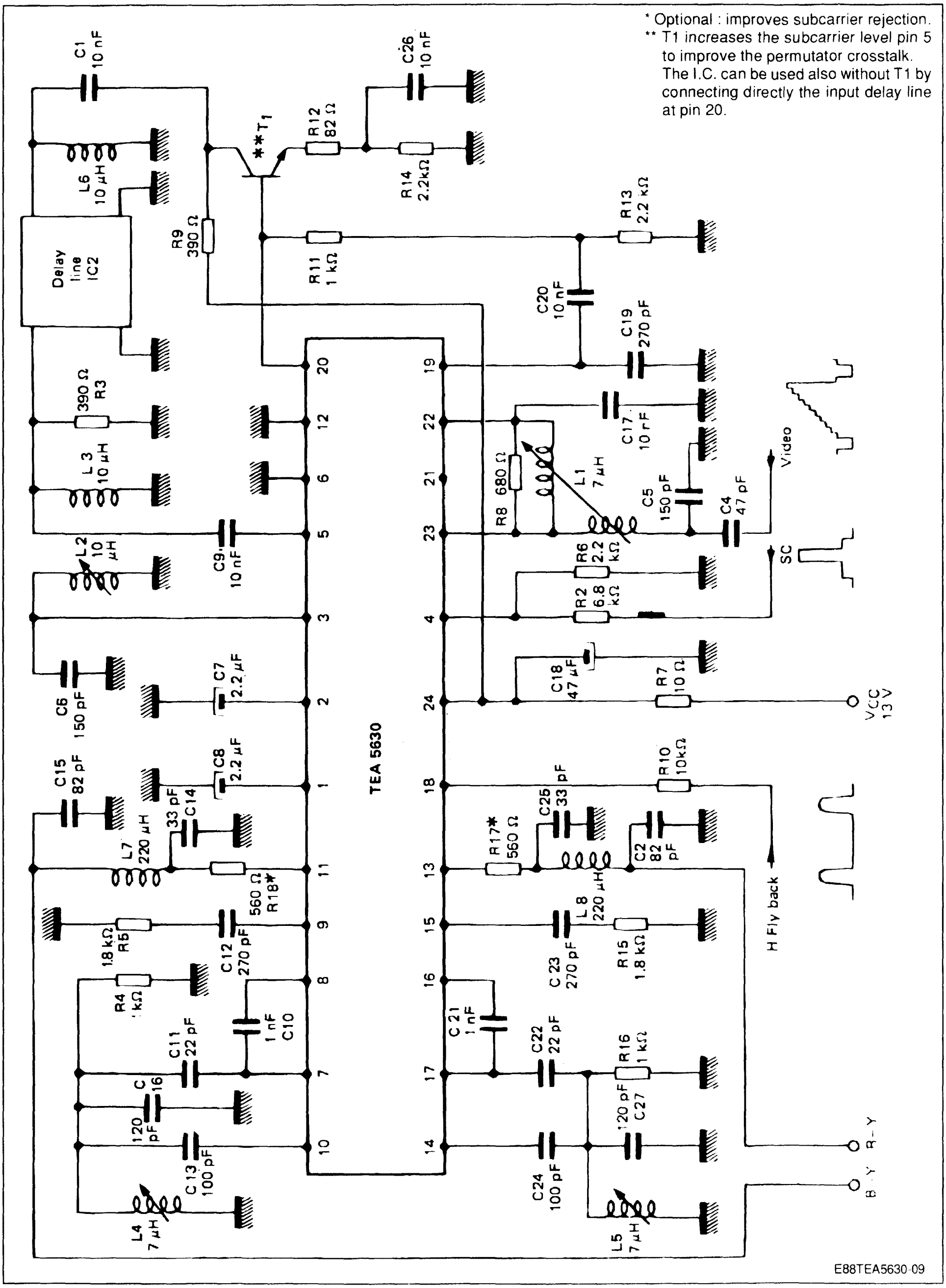
PERMUTATOR.



DISCRIMINATORS.



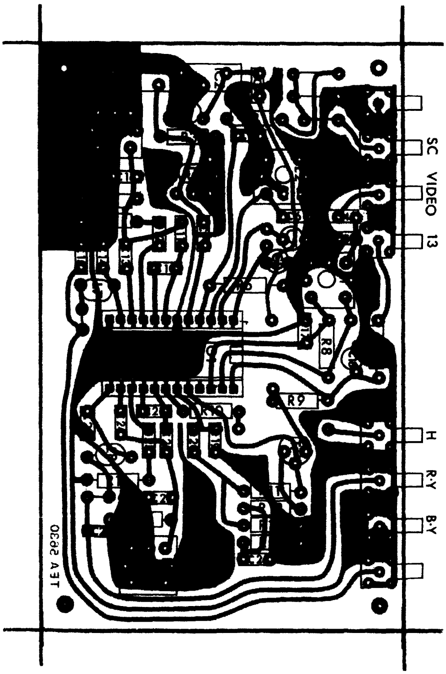
TYPICAL APPLICATION



E88TEA5630-09

P.C. BOARD AND COMPONENT LAYOUT (for secam decoder)

COMPONENT SIDE



E88TEA5630-10

N°	Type
Tr1	BC548 B

N°	Value
R2	6.8 kΩ
R3	390 Ω
R4	1 kΩ
R5	1.8 kΩ
R6	2.2 kΩ
R7	10 Ω
R8	680 Ω
R9	390 Ω
R10	10 kΩ
R11	1 kΩ
R12	82 Ω
R13	2.2 kΩ
R14	2.2 kΩ
R15	1.8 kΩ
R16	1 kΩ
R17*	560 Ω
R18*	560 Ω

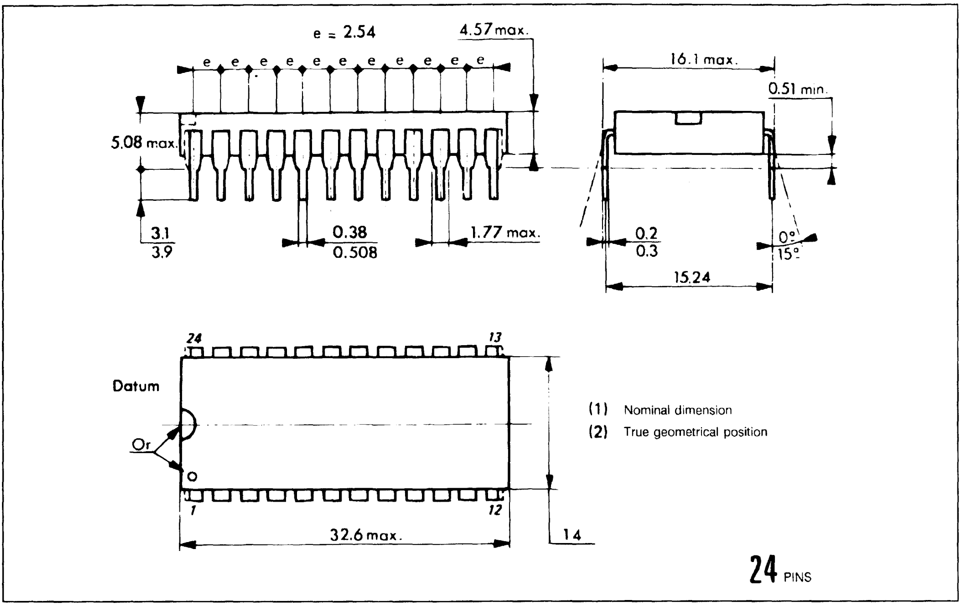
N°	Capa.
C1	10 nF
C2	82 pF
C3	100 pF
C4	47 pF
C5	150 pF
C6	150 pF
C7	2.2 µF
C8	2.2 µF
C9	10 nF
C10	1 nF
C11	22 pF
C12	270 pF
C13	100 pF
C14	33 pF
C15	82 pF
C16	120 pF
C17	10 nF
C18	47 µF
C19	270 pF
C20	10 nF
C21	1 nF
C22	22 pF
C23	270 pF
C24	100 pF
C25	33 pF
C26	10 nF
C27	120 pF

N°	Type	Val.
L1	Toko RCL 3627010	≈ 7 µH
L2	" " 3627014	10-15 µH
L3		10 µH
L4	" " 3627013	≈ 7 µH
L5	" " 3627013	≈ 7 µH
L6		10 µH
L7		220 µH
L8		220 µH

* Optional improves subcarrier rejection.

PACKAGE MECHANICAL DATA

24 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

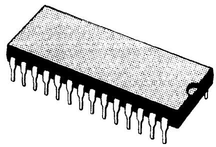
TEA5640B

PAL/SECAM COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

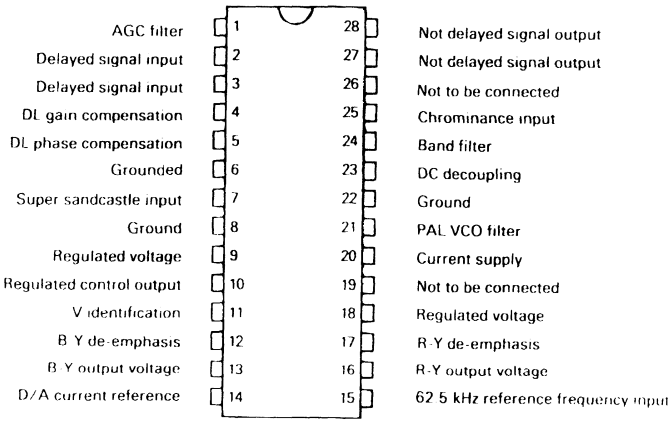
DESCRIPTION

The TEA5640B is a multistandard TV decoder for PAL-SECAM. The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are, four numerical frequency locked loops that allow the elimination of PAL crystal. The circuit uses an external reference frequency of 62.5 kHz generally provided by the frequency synthesis tuner of the TV set.



TEA5640B
DIP28
(Plastic Package)

PIN CONNECTIONS

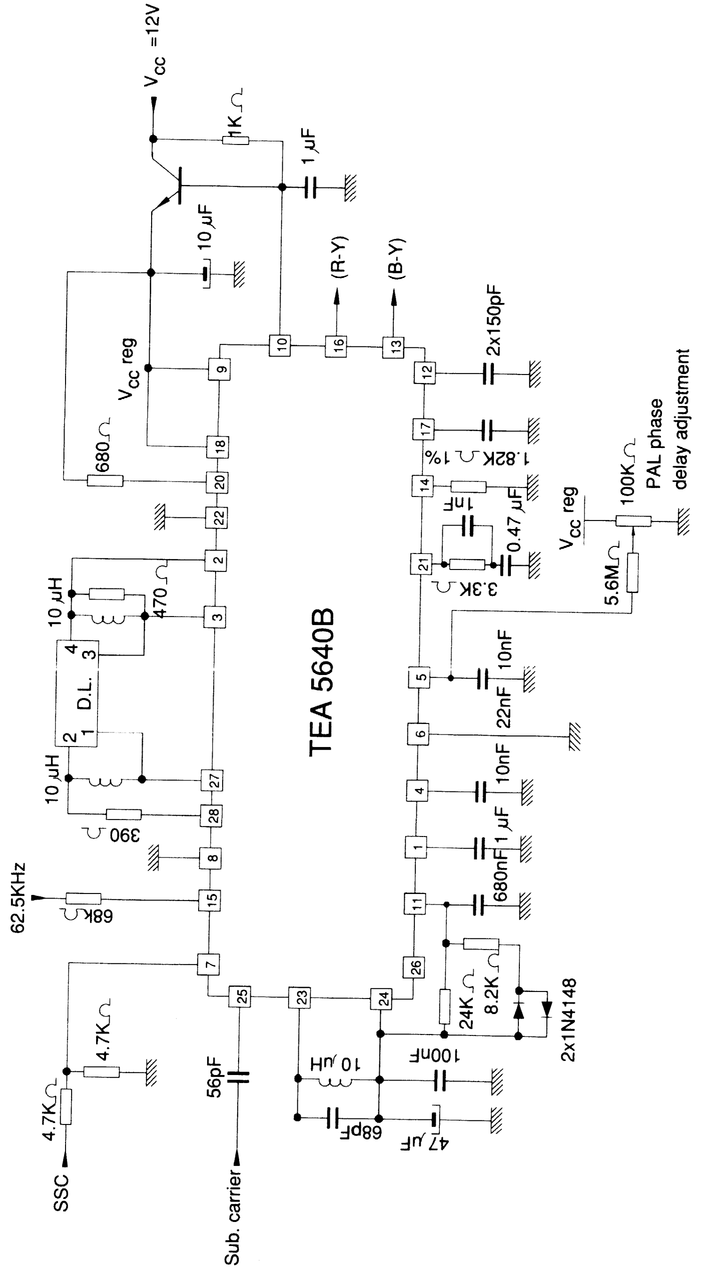


E88TEA5640B-01

FEATURES

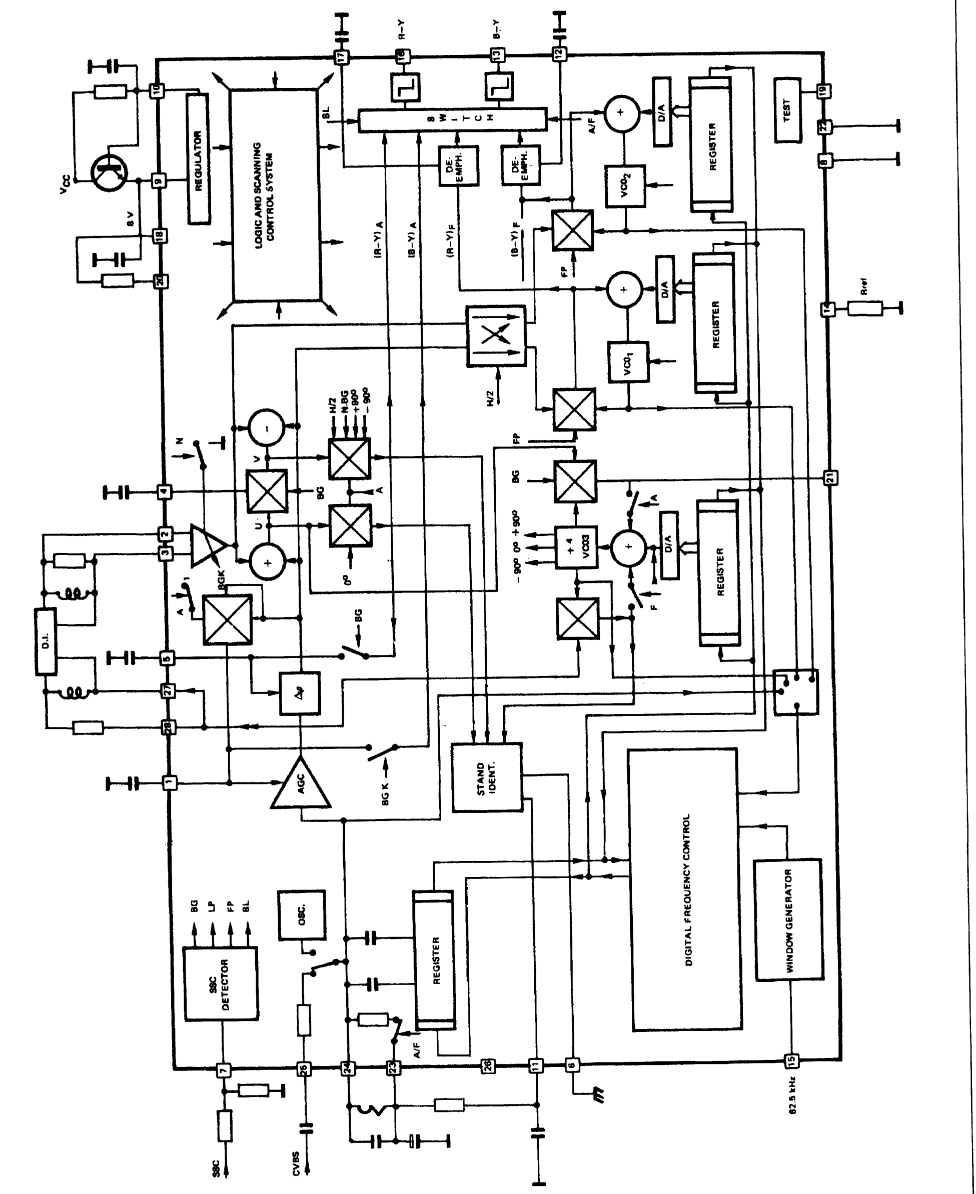
- FULL AUTOMATIC MULTISTANDARD SWITCHING :
- THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM THAT PROVIDES ALL THE SWITCHINGS REQUIRED FOR THE AUTOMATIC STANDARD RECOGNITION. THIS SYSTEM IS SYNCHRONIZED BY THE FRAME PULSE.
- NO CRYSTAL REQUIREMENT :
  THE PAL FREQUENCIES ARE SYNTHESIZED ORIGINALLY BY THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz AND DATA STORED IN THE ROM.
- AUTOMATIC GAIN ADJUSTMENT OF THE BELL
  FILTER : BY SWITCHING AN INTERNAL CAPACITOR NETWORK INCLUDED IN A DIGITAL LOOP.
- AUTOMATIC GAIN ADJUSTMENT OF THE DELAY LINE COMPENSATIONS :
  THIS ADJUSTMENT IS MADE ON THE BURST AND IS REFRESDED EVERY LINE RETRACE
- AUTOMATIC ADJUSTMENT FOR PAL OSCILLATOR :
  THIS OSCILLATOR HAS A DIGITAL AND AN ANALOGIC LOOP. THE PAL FREQUENCIES ARE MEMORIZED IN A ROM CONNECTED TO THE DIGITAL LOOP. THE DIGITAL LOOP GIVES THE RIGHT FREQUENCY AND THE ANALOGIC ONE HOLDS THE PHASE.
- AUTOMATIC ADJUSTMENT OF FoR AND FoB IN SECAM : THESE FREQUENCIES ARE PROGRAMMED IN THE ROM AND ARE SENT TO TWO OTHER DIGITAL LOOPS WHEN SECAM STANDARD IS SELECTED.
- AUTOMATIC DIFFERENCE PHASE ERROR COMPENSATION IN PAL MODE.
  THE PAL VCO IS LOCKED ON THE BURST AND DURING THE LINE, ON THE BLUE PICTURE CONTENT (0° axis color vector).

TYPICAL APPLICATION



E88TEA5640B-02

BLOCK DIAGRAM



S : Secam ; BP : Bandfilter adjustment ; P : Pal ; BG : Burstgate
LP : Line Pulse ; FP : Frame Pulse
A : Amplit. Modul. ; F : Freq. Modul ; K : Identification ; BL : Blanking

E88TEA5640B-03

STANDARD SWITCHING AND INHIBITION

SECAM recognition :

- When SECAM on, pin 12 and pin 17 DC voltages are lower than 5 V.
- For PAL standard, pin 12 and pin 17 DC voltages are regulated V_{CC} (typical 8 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature		– 40 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12 V ; With Normalized Color Bar Pattern Input Signal (75 %) Subcarrier Level : 320 mVPP
Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Supplies					
Vreg	Regulated Voltage I10 = 4 mA	Pins 9 - 18	7.5	8	8.5	V
ICC	Supply Current	Pin 9 + Pin 18		90	120	mA
I9	Supply Current	Pin 9			90	mA
I18	Supply Current	Pin 18			27	mA
VI2L	DC Voltage at I20 = 15 mA	Pin 20		0.8		V
I10	Input Current	Pin 10	2		20	mA
	Transfer Characteristic (I10 = 4.0 mA)			250		mA/V
	Current Reference	Pin 14				
V14	DC Voltage (I14 = 0.77 mA		1.2	1.4	1.6	V
	Internal Bias	Pin 24				
V 24	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2 mA)			90	110	Ω
	Reference Clock Input					
	F = 62.5 kHz ± 6Hz	Pin 15				
I15L	Low Level Input Current (V15 = 2.1 V)		– 20	– 10	– 5	µA
I15H	High Level Input Current (V15 = 3.2 V)			5	10	µA
V15L	Low Level Input Voltage	R Source = 68 kΩ			1	V
V15H	High Level Input Voltage	R Source = 68 kΩ	4			V
	Voltage Threshold			2.8		V
	Super Sandcastle Detector	Pin 7				
VB	Blanking Threshold		0.5	0.75	0.9	V
VL	Line Threshold		1.6	1.8	1.9	V
V6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I7	Input Current (V7 = 1.75 V)		– 20		0	µA
	Max Input Voltage Pin 7				6.0	V

ELECTRICAL CHARACTERISTICS (continued)

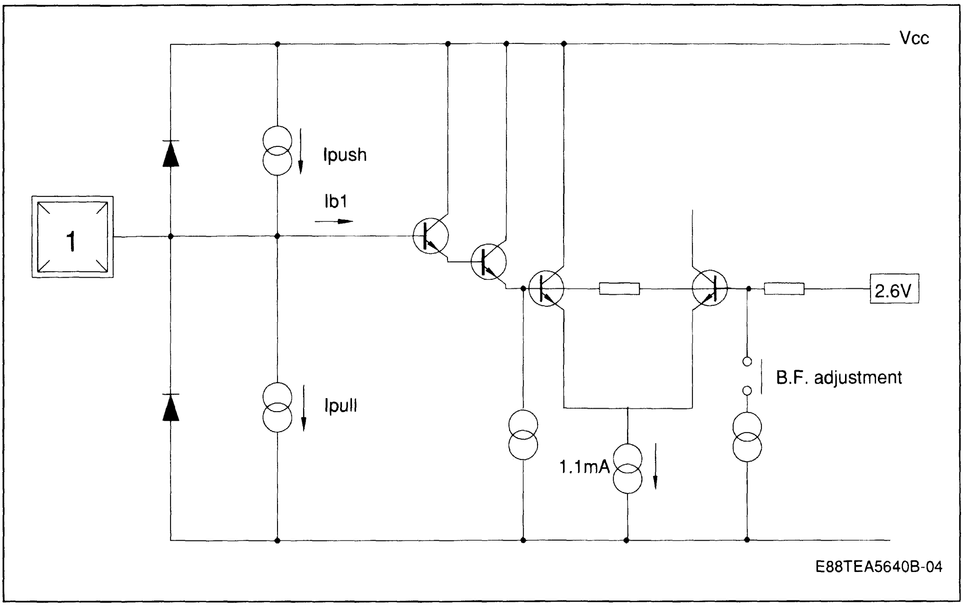
Symbol	Parameter		Min.	Typ.	Max.	Unit
	Chrominance Input	Pin 25				
V25	DC Voltage			5.5		V
	Maximum AC Input Voltage				0.64	Vpp
	Impedance		0.8	1		kΩ
	Automatic Gain Control					
	SECAM MODE					
	• 0 dB Reference Voltage for Measurement on Pins 27 - 28 (chroma input voltage V25 = 320 mVpp)		50	150	250	mVpp
	• AC Voltage Variation on Pins 27 - 28 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 27 -28 (V25 = – 24 dB)		– 5		+ 2	dB
	PAL MODE WITH IDENTIFICATION					
	• 0 dB Reference Voltage for Measurement on Pins 13 -16 (chroma input voltage V25 = 320 mVpp)					
	• AC Voltage Variation on Pins 13 - 16 (V25 = + 6 dB)		– 3		+ 3	dB
	• AC Voltage Variation on Pins 13 - 16 (V25 = – 24 dB)		– 5		+ 2	dB
	Demodulator Part					
	GENERALITIES					
V13	B-Y Output DC Voltage	Pin 13	3	3.5	4	V
V16	R-Y Output DC Voltage	Pin 16	3.2	3.7	4.2	V
	Maximum Sink Current	Pin 13	0.4			mA
	Maximum Sink Current	Pin 16	0.4			mA
	Differential Delay Time Between PAL/SECAM				50	nS
	Delay Diff Tolerance				50	nS
	Delay Between Chroma Output and Luma Signal			450		nS
	B-Y Output AC Impedance (± 50 μA)			250		Ω
	R-Y Output AC Impedance (± 50 μA)			250		Ω
	Blanking Level Offset				± 2	%
	Secam Mode					
VBYS	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYS	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.1		1.45	
	Residual Subcarrier			30		mVpp
	Pal Mode					
VBYP	B-Y AC Voltage		1.0	1.34	1.6	Vpp
VRYP	R-Y AC Voltage		0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio		1.0		1.3	
	Residual Subcarrier			30		mVpp

ELECTRICAL CHARACTERISTICS (continued)

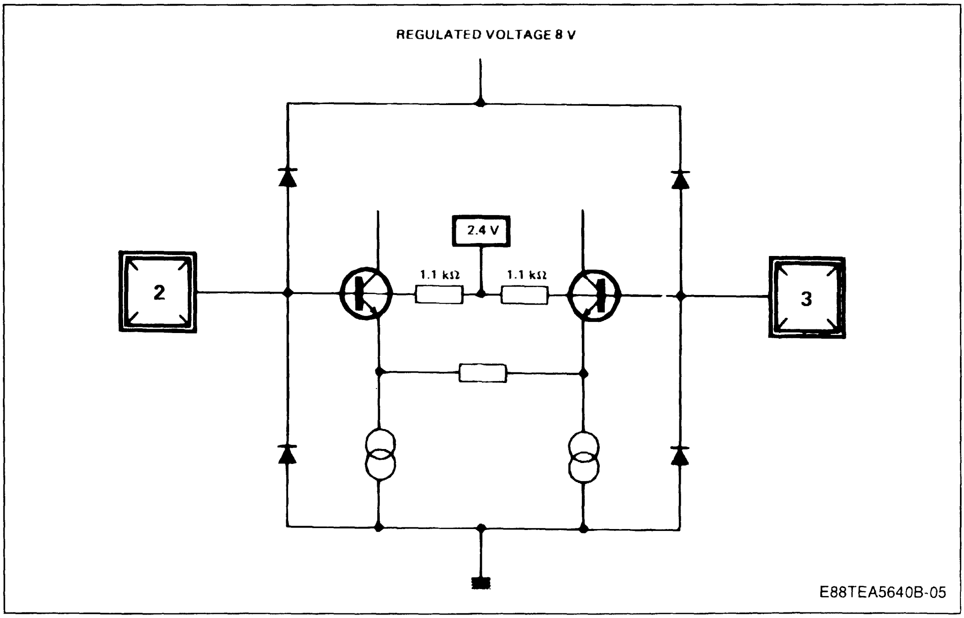
Symbol	Parameter	Min.	Typ.	Max.	Unit
	De-Emphasis Pins 12 - 17				
	SECAM MODE				
	DC Voltage (blanking level)		3.5	4.0	V
	Impedance		11		kΩ
	PAL MODE				
	DC Voltage		VREG		V
	Impedance		70		kΩ
	Reference Oscillator PLL				
	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz
	Band Filter Pin 23				
	Impedance SECAM Mode	3.7	4.7	5.7	kΩ
	PAL Mode	0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)		20		pF
	Maximum Switchable Internal Capacitance (all standards)		50		pF
ΔF	Internal Oscillator Frequency Range for L = 10 µH C = 68 pF	590			kHz
	Frequency Offset, After Automatic Adjustement			± 10	kHz
	Undelayed Signal Outputs Pins 27 - 28				
V27 V28	DC Voltage		1.6		V
I27 I28	Sink Current	1			mA
	Impedance		30		Ω
	Identification				
	Burst Attenuation Range / Nominal Level				
	SECAM Mode (line identification)	30			dB
	Pal Mode	30			dB
	Delayed Signal Input Pins 2 - 3				
	DC Voltage in PAL Mode		2.4		V
	Input Impedance	0.88	1.1	1.32	kΩ
	Delay Line Attenuation Compensation				
	Range of Automatic Attenuation Compensation	– 3	– 9	– 15	dB
	Delay Line Phase Shift Compensation				
	Range of Phase Shift Compensation with a 100KΩ Potentiometer (see application diagram p. 3)	± 30			Degree
	Alternation Line Detection PAL or SECAM Pin 11				
VTHH	High Differential Threshold (VTHH = V11H – V24)	200		350	mV
VTHL	Low Differential Threshold (VTHL = V11L – V24)	– 350		– 200	mV
	Leakage Current Threshold (V11 = V24 + 1V)			0.5	µA

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

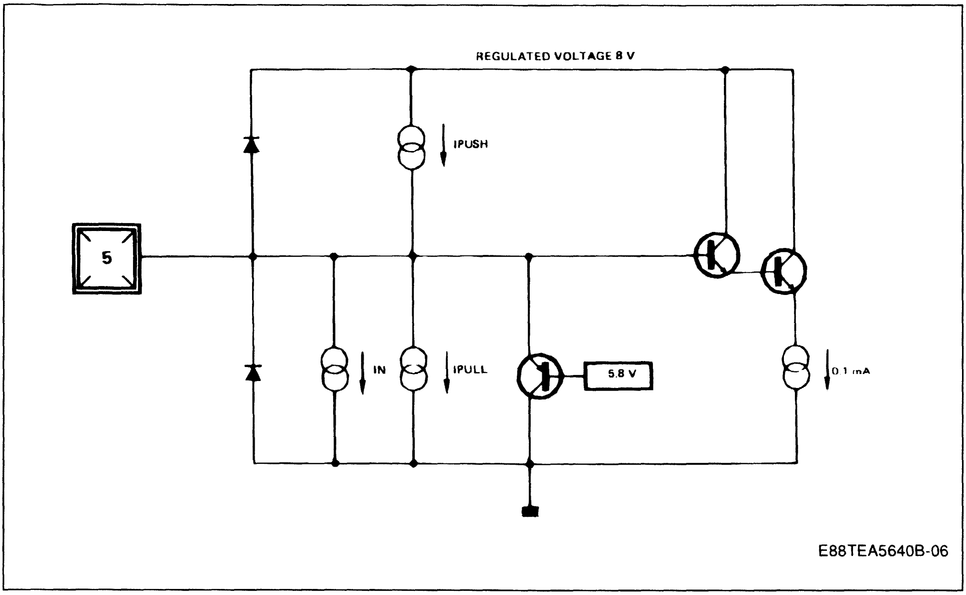
PIN 1



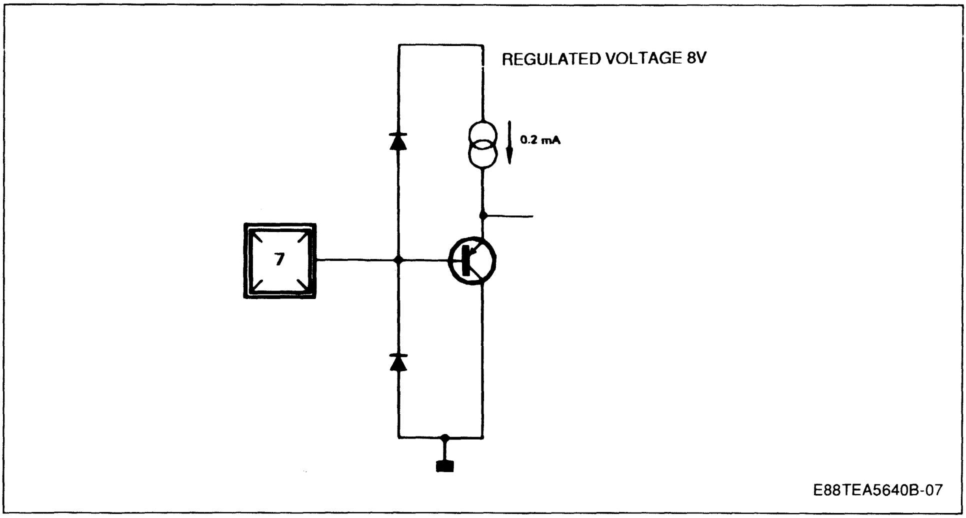
PINS 2 – 3



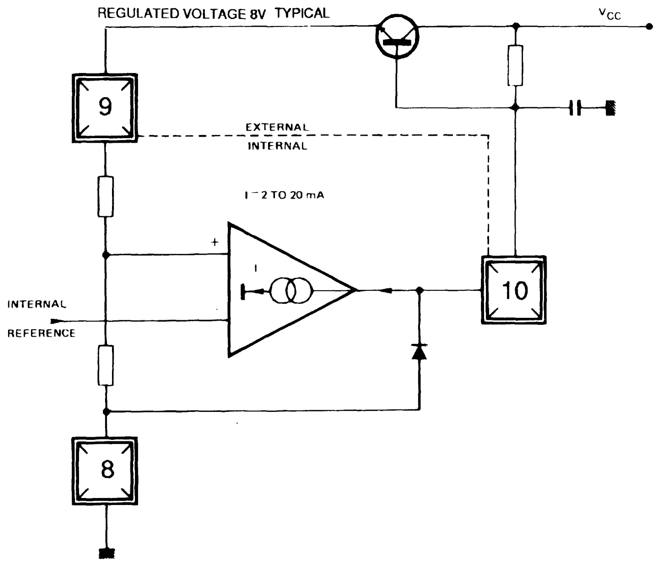
PIN 5


REGULATED VOLTAGE 8 V
IPUSH
5
IN
IPULL
5.8 V
0.1 mA
E88TEA5640B-06

PIN 7

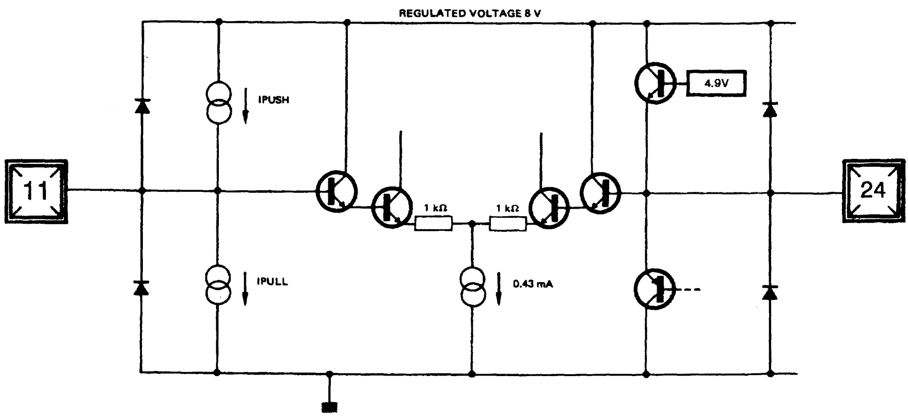

REGULATED VOLTAGE 8V
0.2 mA
7
E88TEA5640B-07

PINS 8 – 9 – 10



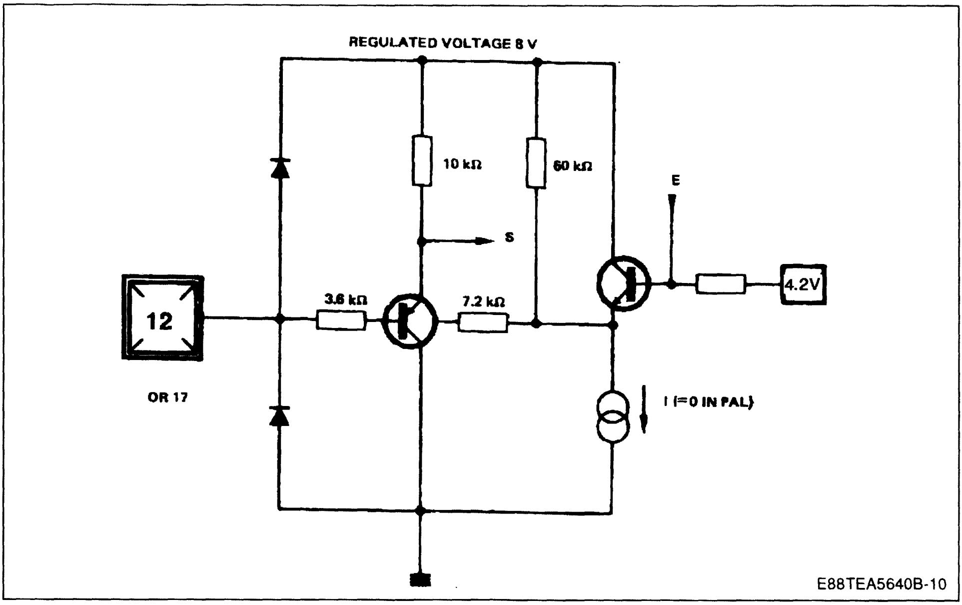
E88TEA5640B-08

PINS 11 – 24

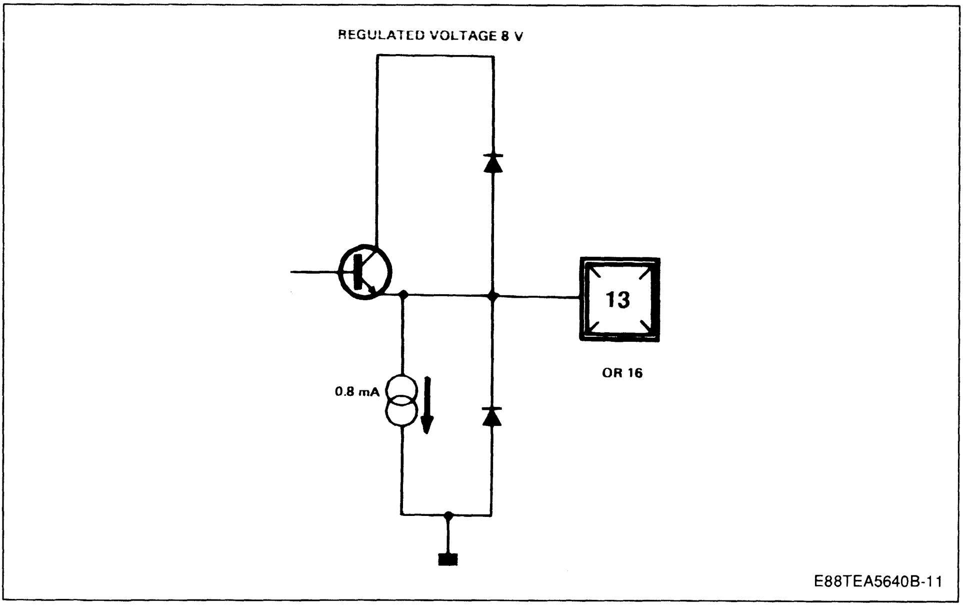


E88TEA5640B-09

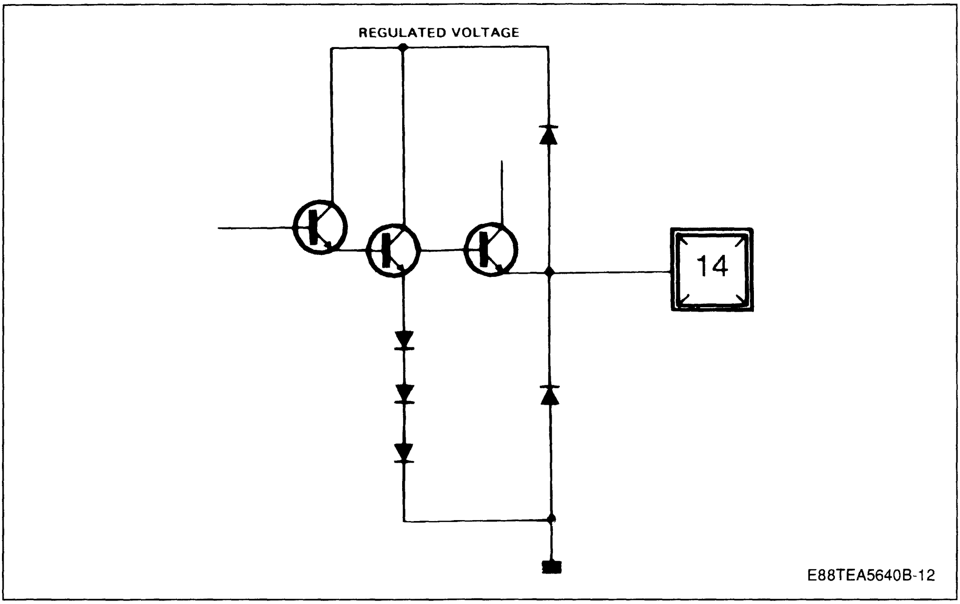
PINS 12 – 17



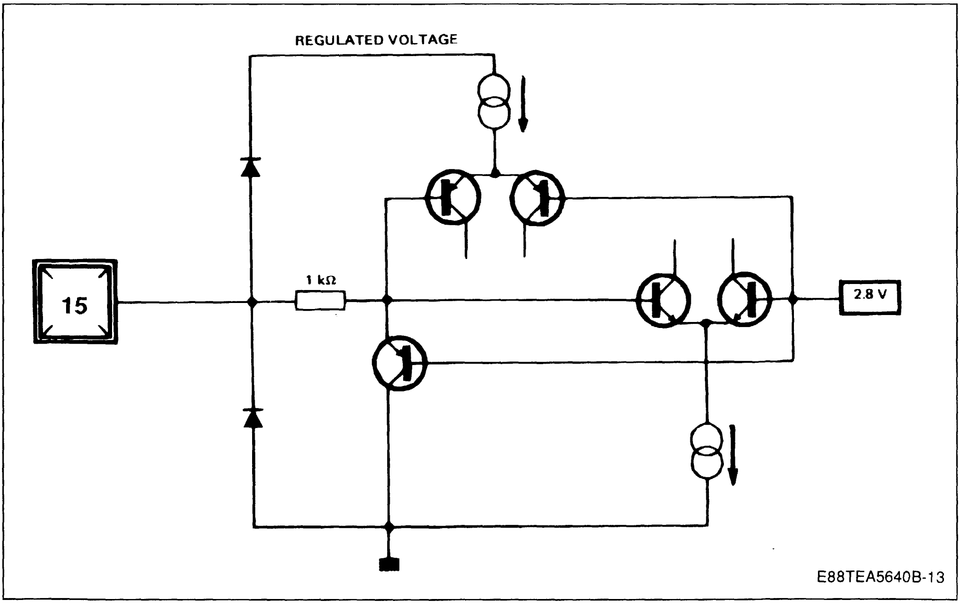
PINS 13 – 16



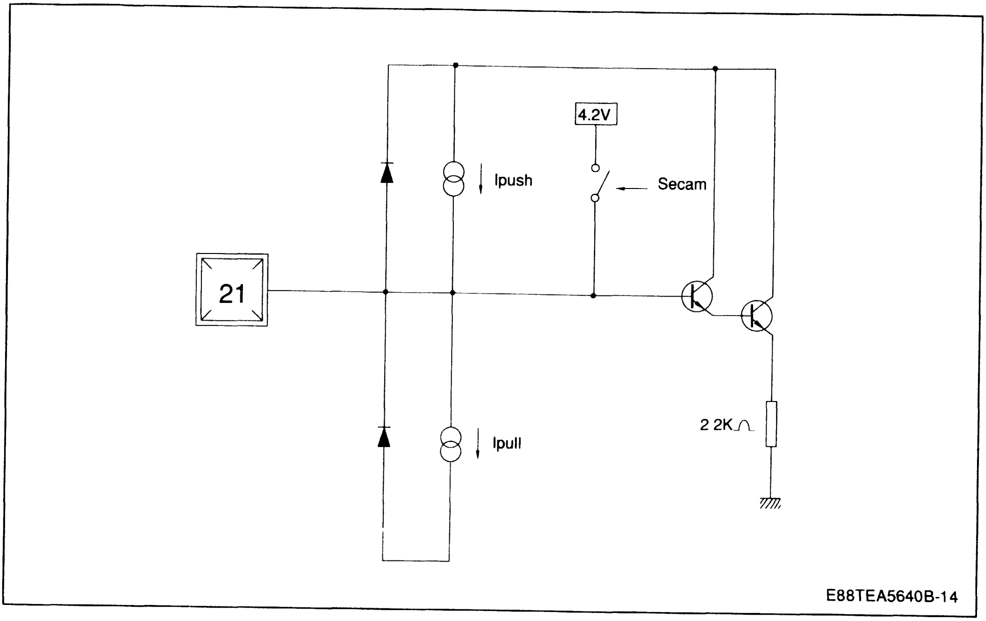
PIN 14


REGULATED VOLTAGE
14
E88TEA5640B-12

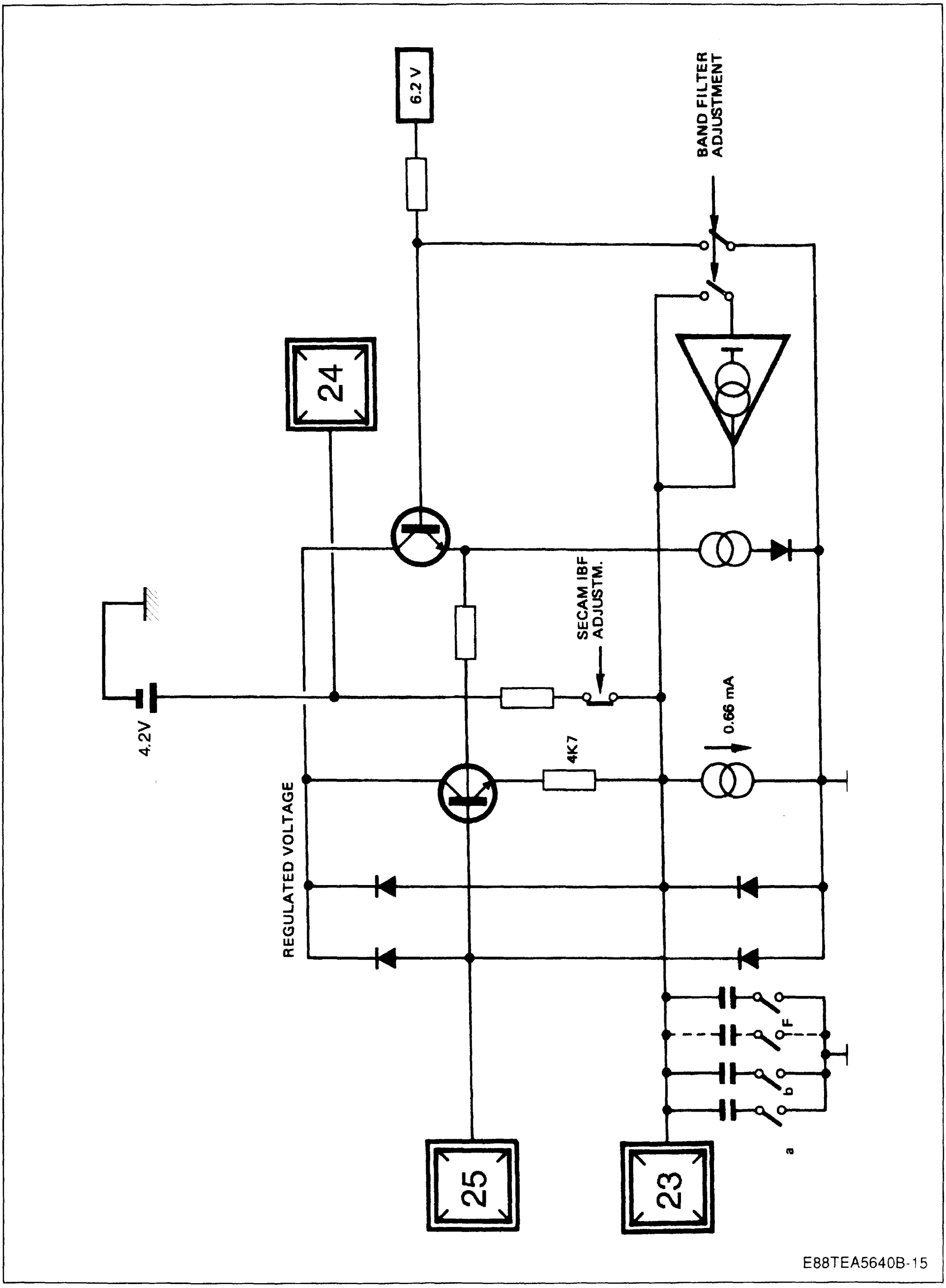
PIN 15


REGULATED VOLTAGE
15
1 kΩ
2.8 V
E88TEA5640B-13

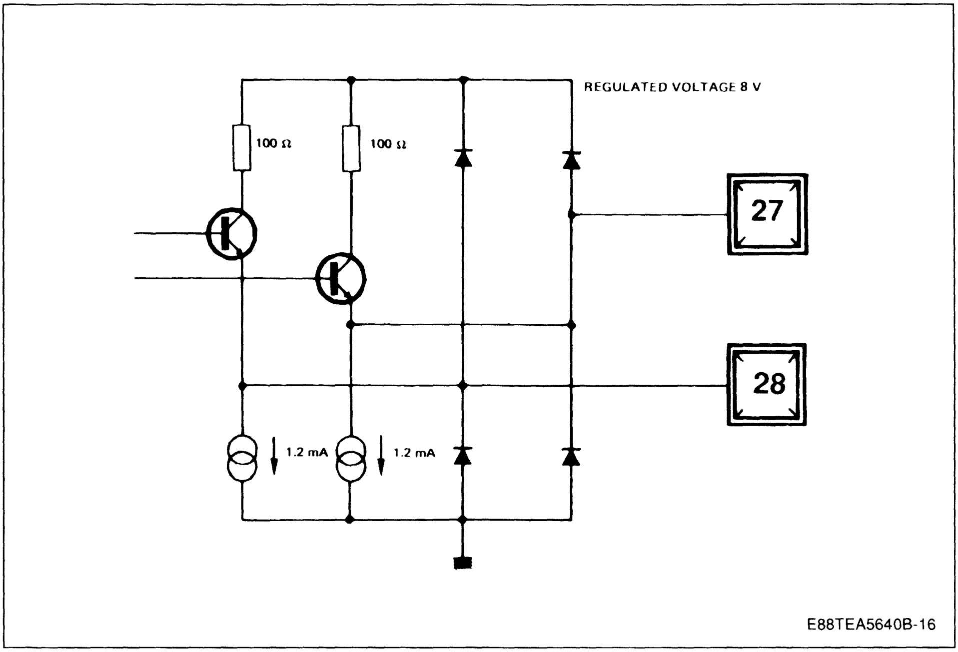
PIN 21



PINS 23 – 24 – 25


6.2 V
BAND FILTER ADJUSTMENT
24
SECAM IBF ADJUSTM.
4.2V
0.66 mA
4K7
REGULATED VOLTAGE
F
b
a
25
23
E88TEA5640B-15

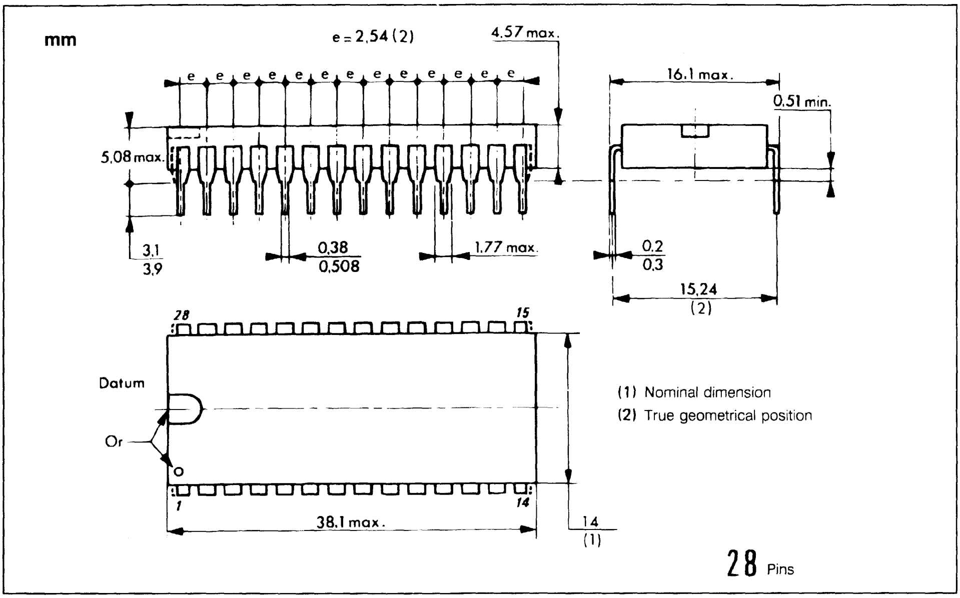
PINS 27 - 28



REGULATED VOLTAGE 8 V
100 Ω
100 Ω
27
28
1.2 mA
1.2 mA
E88TEA5640B-16

PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



SGS-THOMSON MICROELECTRONICS

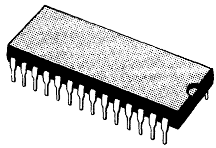
TEA5640C

MULTISTANDARD COLOR TV DECODER

- FULLY AUTOMATIC MULTISTANDARD SWITCHING : THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM USED FOR THE AUTOMATIC STANDARD RECOGNITION
- NO CRYSTALS REQUIRED : ALL THE FREQUENCIES ARE SYNTHESIZED FROM THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz, AND FROM SPECIFIED DATA STORED IN AN INTERNAL ROM
- AUTOMATIC BELL FILTER ADJUSTMENT
- ONLY ONE DELAY LINE COMPENSATION ADJUSTMENT
- AUTOMATIC INTERNAL PAL AND NTSC OSCILLATOR ADJUSTMENT
- AUTOMATIC ADJUSTMENT FOR FOB AND FOR IN SECAM
- POSITIVE R-Y AND B-Y OUTPUTS

DESCRIPTION

The TEA5640C is a multistandard TV decoder for PAL-SECAM NTSC1 (3.58 MHz) and NTSC2 (4.43 MHz). The circuit automatically selects the standard corresponding to the input signal. It produces all the reference frequencies required for decoding, which is achieved by a digital frequency synthesizer. Included on the chip are, four numerical frequency locked loops that allow the elimination of PAL and NTSC crystals. The circuit uses an external reference frequency of 62.5 kHz generally provided by the frequency synthesis tuner of the TV set.



TEA5640C
DIP28
(Plastic Package)

PIN CONNECTIONS

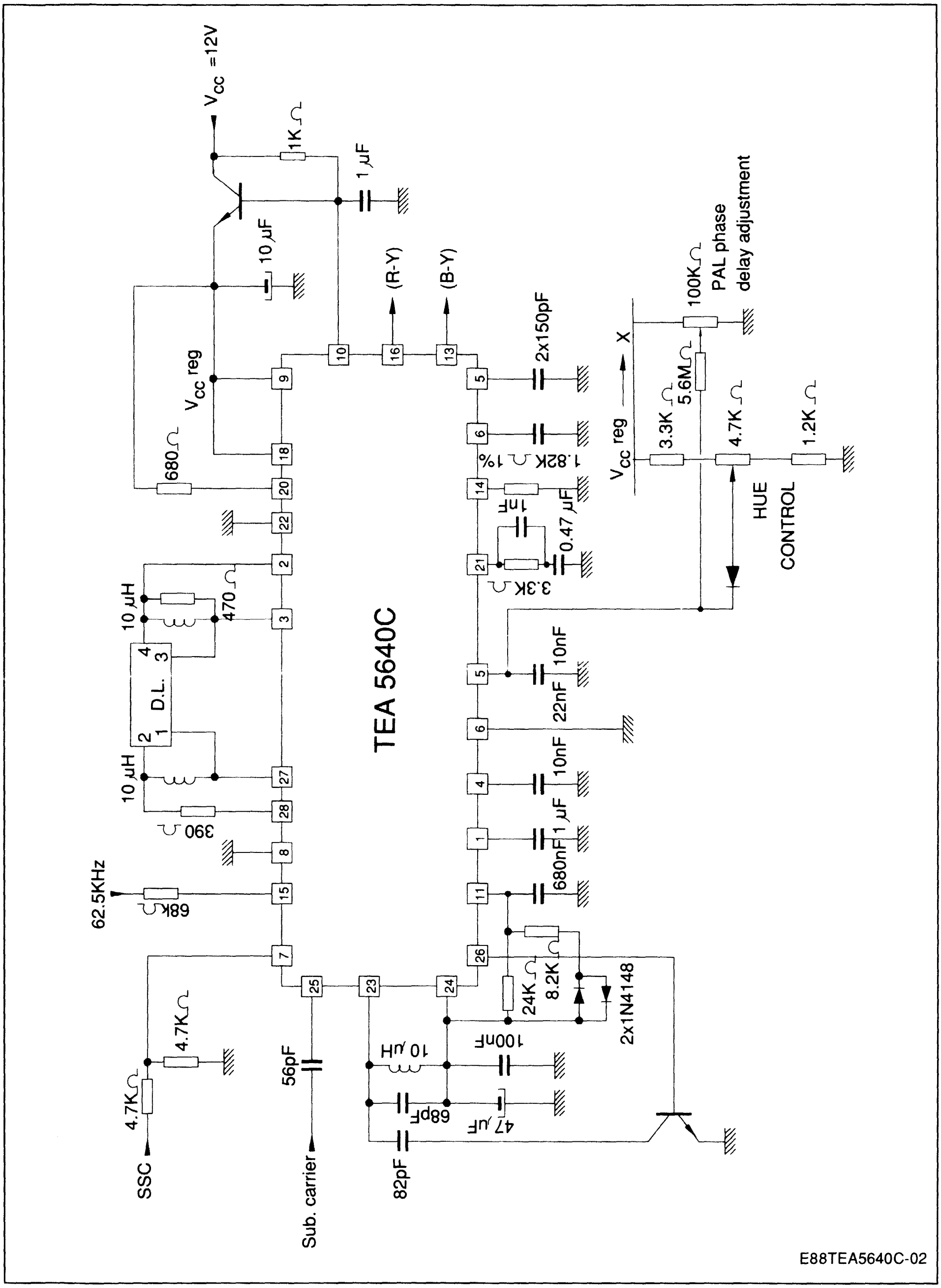
Function	Pin	Pin	Function
AGC filter	1	28	Not delayed signal output
Delayed signal input	2	27	Not delayed signal output
Delayed signal input	3	26	3.58 MHz tuning switch
DL gain compensation	4	25	Chrominance input
DL phase compensation	5	24	Band filter
U identification	6	23	DC decoupling
Super sandcastle input	7	22	Ground
Ground	8	21	PAL VCO filter
Regulated voltage	9	20	Current supply
Regulated control output	10	19	Not to be connected
V identification	11	18	Regulated voltage
B-Y de-emphasis	12	17	R-Y de-emphasis
B-Y output voltage	13	16	R-Y output voltage
D/A current reference	14	15	62.5 kHz reference frequency input

E88TEA5640C-01

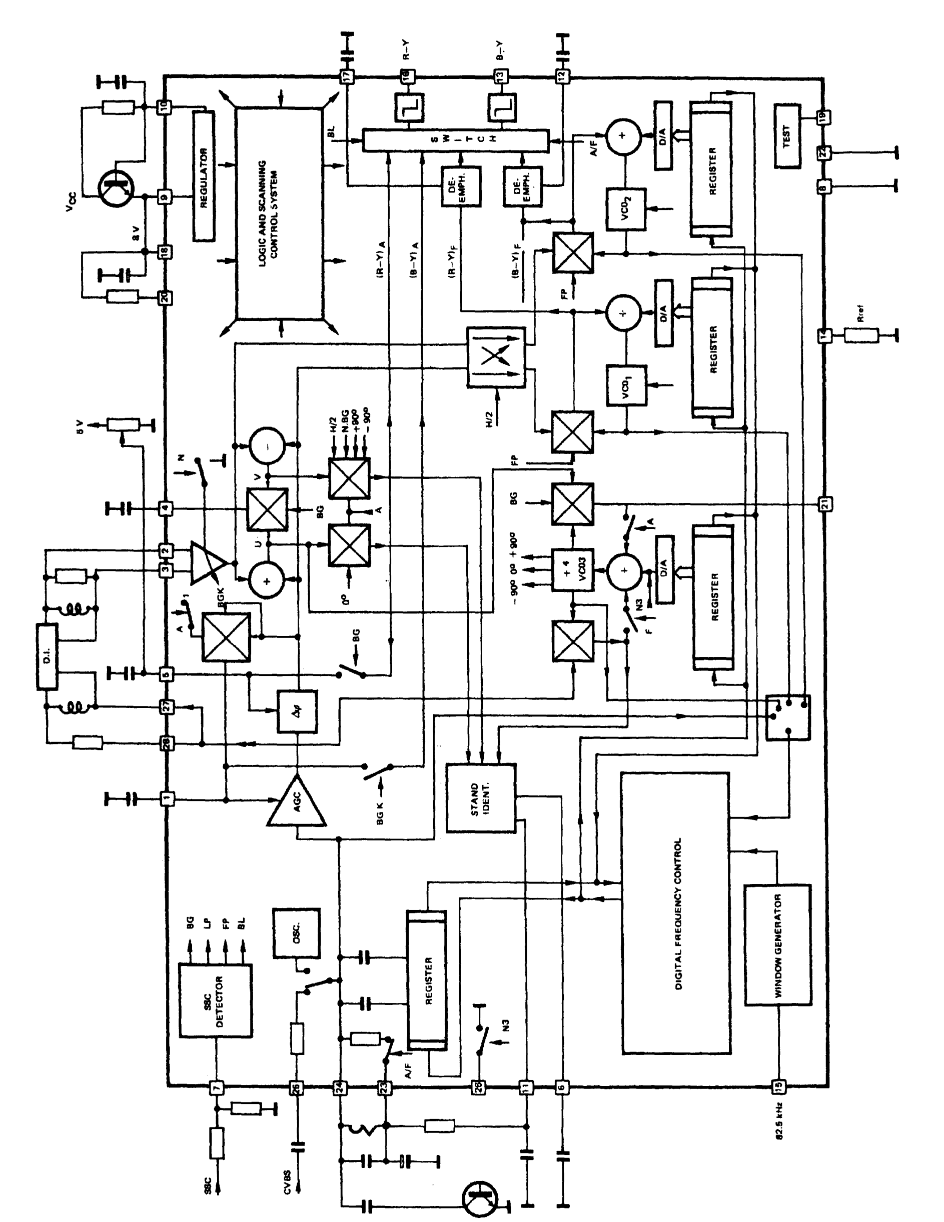
FEATURES

- FULL AUTOMATIC MULTISTANDARD SWITCHING :
- THE CIRCUIT INCLUDES A SCANNING CONTROL SYSTEM THAT PROVIDES ALL THE SWITCHINGS REQUIRED FOR THE AUTOMATIC STANDARD RECOGNITION. THIS SYSTEM IS SYNCHRONIZED BY THE FRAME PULSE.
- NO CRYSTAL REQUIREMENT :
  THE PAL AND NTSC FREQUENCIES ARE SYNTHESIZED ORIGINALLY BY THE EXTERNAL REFERENCE FREQUENCY OF 62.5 kHz AND DATA STORED IN THE ROM.
- AUTOMATIC ADJUSTMENT OF THE BELL FILTER : BY SWITCHING AN INTERNAL CAPACITOR NETWORK INCLUDED IN A DIGITAL LOOP.
- AUTOMATIC GAIN ADJUSTMENT OF THE DELAY LINE COMPENSATIONS :
  THIS ADJUSTMENT IS MADE ON THE BURST AND IS REFRESDED EVERY LINE RETRACE
- AUTOMATIC ADJUSTMENT FOR PAL AND NTSC OSCILLATOR :
  THIS OSCILLATOR HAS A DIGITAL AND AN ANALOGIC LOOP. THE PAL AND NTSC FREQUENCIES ARE MEMORIZED IN A ROM CONNECTED TO THE DIGITAL LOOP. THE DIGITAL LOOP GIVES THE RIGHT FREQUENCY AND THE ANALOGIC ONE HOLDS THE PHASE.
- AUTOMATIC ADJUSTMENT OF FoR AND FoB IN SECAM : THESE FREQUENCIES ARE PROGRAMMED IN THE ROM AND ARE SENT TO TWO OTHER DIGITAL LOOPS WHEN SECAM STANDARD IS SELECTED.
- AUTOMATIC DIFFERENCE PHASE ERROR COMPENSATION IN PAL MODE.
  THE PAL VCO IS LOCKED ON THE BURST AND DURING THE LINE, ON THE BLUE PICTURE CONTENT (0° axis color vector).

TYPICAL APPLICATION



BLOCK DIAGRAM



S : Secam ; BP : Bandfilter adjustment ; P : Pal ; BG : Burstgate
N4 : NTSC 4.43 ; N3 : NTSC 3.58 ; LP : Line Pulse ; FP : Frame Pulse
A : Amplit. Modul. ; F : Freq. Modul ; K : Identification ; BL : Blanking

E88TEA5640C-03

STANDARD SWITCHING AND INHIBITION

NTSC inhibition
NTSC 1 and 2 standards can be inhibited by connecting pin 6 to the ground.

3.58 MHz filter switching :
Pin 26 can be used to switch external filters when NTSC 1 is selected (For example luma filter).

SECAM recognition :

- When SECAM on, pin 12 and pin 17 DC voltages are lower than 5 V.
- For other standards, pin 12 and pin 17 DC voltages are regulated V_{CC} (typical 8 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V	Supply Voltage	Pins 9 - 18	9.5	V
I	Current	Pin 20	200	mA
T_{oper}	Operating Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature		– 40 to 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction Ambient Thermal Resistance (with mini 10 % Cu on board)	55	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C ; V_{CC} = 12 V ; With Normalized Color Bar Pattern Input Signal (75 %) Subcarrier Level : 320 mVPP
Refer to Application Diagram Page (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Supplies					
Vreg	Regulated Voltage I10 = 4 mA	Pins 9 - 18	7.5	8	8.5	V
ICC	Supply Current	Pin 9 + Pin 18		90	120	mA
I9	Supply Current	Pin 9			90	mA
I18	Supply Current	Pin 18			27	mA
VI2L	DC Voltage at I20 = 15 mA	Pin 20		0.8		V
I10	Input Current	Pin 10	2		20	mA
	Transfer Characteristic (I10 = 4.0 mA)			250		mA/V
	Current Reference	Pin 14				
V14	DC Voltage (I14 = 0.77 mA		1.2	1.4	1.6	V
	Internal Bias	Pin 24				
V 24	DC Voltage		3.7	4.2	4.7	V
	Impedance (I_{out} = 2 mA)			90	110	Ω
	Reference Clock Input					
	F = 62.5 kHz ± 6Hz	Pin 15				
I15L	Low Level Input Current (V15 = 2.1 V)		– 20	– 10	– 5	µA
I15H	High Level Input Current (V15 = 3.2 V)			5	10	µA
V15L	Low Level Input Voltage	R Source = 68 kΩ			1	V
V15H	High Level Input Voltage	R Source = 68 kΩ	4			V
	Voltage Threshold			2.8		V
	Super Sandcastle Detector	Pin 7				
VB	Blanking Threshold		0.5	0.75	0.9	V
VL	Line Threshold		1.6	1.8	1.9	V
V6	Burst Gate Threshold		3.2	3.5	3.8	V
	Minimum Frame Blanking Duration		1.15			mS
I7	Input Current (V7 = 1.75 V)		– 20		0	µA
	Max Input Voltage Pin 7				6.0	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Chrominance Input Pin 25				
V25	DC Voltage		5.5		V
	Maximum AC Input Voltage			0.64	Vpp
	Impedance	0.8	1		kΩ
	Automatic Gain Control				
	SECAM MODE				
	• 0 dB Reference Voltage for Measurement on Pins 27 - 28 (chroma input voltage V25 = 320 mVpp)	50	150	250	mVpp
	• AC Voltage Variation on Pins 27 - 28 (V25 = + 6 dB)	– 3		+ 3	dB
	• AC Voltage Variation on Pins 27 -28 (V25 = – 24 dB)	– 5		+ 2	dB
	PAL/NTSC MODE WITH IDENTIFICATION				
	• 0 dB Reference Voltage for Measurement on Pins 13 -16 (chroma input voltage V25 = 320 mVpp)				
	• AC Voltage Variation on Pins 13 - 16 (V25 = + 6 dB)	– 3		+ 3	dB
	• AC Voltage Variation on Pins 13 - 16 (V25 = – 24 dB)	– 5		+ 2	dB
	Demodulator Part				
	GENERALITIES				
V13	B-Y Output DC Voltage Pin 13	3	3.5	4	V
V16	R-Y Output DC Voltage Pin 16	3.2	3.7	4.2	V
	Maximum Sink Current Pin 13	0.4			mA
	Maximum Sink Current Pin 16	0.4			mA
	Differential Delay Time Between PAL/SECAM			50	nS
	Delay Diff Tolerance			50	nS
	Delay Between Chroma Output and Luma Signal		450		nS
	B-Y Output AC Impedance (± 50 µA)		250		Ω
	R-Y Output AC Impedance (± 50 µA)		250		Ω
	Blanking Level Offset			± 2	%
	Secam Mode				
VBYS	B-Y AC Voltage	1.0	1.34	1.6	Vpp
VRYS	R-Y AC Voltage	0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio	1.1		1.45	
	Residual Subcarrier		30		mVpp
	Pal Mode				
VBYP	B-Y AC Voltage	1.0	1.34	1.6	Vpp
VRYP	R-Y AC Voltage	0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio	1.0		1.3	
	Residual Subcarrier		30		mVpp
	NTSC 4.43				
VBYN2	B-Y AC Voltage	1.0	1.34	1.6	Vpp
VBYN2	R-Y AC Voltage	0.8	1.05	1.3	Vpp
	B-Y/R-Y Ratio	1.0		1.3	
	Residual Subcarrier		50		mVpp

ELECTRICAL CHARACTERISTICS (continued)

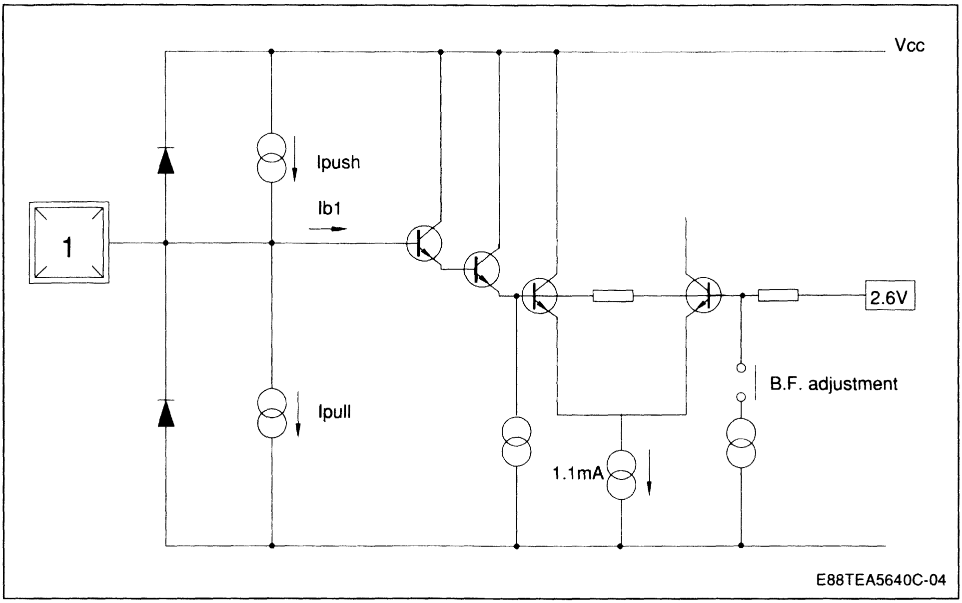
Symbol	Parameter	Min.	Typ.	Max.	Unit
	NTSC 3.58				
VBYN1	B-Y AC Voltage	1.0		1.6	Vpp
VRYN1	R-Y AC Voltage	0.8		1.3	Vpp
	B-Y/R-Y Ratio	1.0		1.3	
	Residual Subcarrier		50		mVpp
	De-Emphasis Pins 12 - 17				
	SECAM MODE				
	DC Voltage (blanking level)		3.5	4.0	V
	Impedance		11		kΩ
	PAL NTSC MODE				
	DC Voltage		VREG		V
	Impedance		70		kΩ
	Reference Oscillator PLL				
	Catching Range in PAL Mode	± 350			Hz
	Holding Range	± 500			Hz
	Band Filter Pin 23				
	Impedance SECAM Mode	3.7	4.7	5.7	kΩ
	PAL NTSC Mode	0.85	1.1	1.35	kΩ
	Minimum Switchable Internal Capacitance (all standards)		20		pF
	Maximum Switchable Internal Capacitance (all standards)		50		pF
ΔF	Internal Oscillator Frequency Range for L = 10 μH C = 68 pF	590			kHz
	Frequency Offset, After Automatic Adjustement			± 10	kHz
	3.58 MHz Switch Output Pin 26				
	NTSC1 (3.58 MHz)				
V26N1	DC Voltage (I26 = 0 mA)	1			V
	Impedance		2		kΩ
	NTSC2 (4.43 MHz) or PAL or SECAM				
V26N2	DC Voltage			0.3	V
	Max Sink Current	0.35			mA
	Undelayed Signal Outputs Pins 27 - 28				
V27 V28	DC Voltage		1.6		V
I27 I28	Sink Current	1			mA
	Impedance		30		Ω
	Identification				
	Burst Attenuation Range / Nominal Level				
	SECAM Mode (line identification)	30			dB
	Pal Mode	30			dB
	NTSC Modes	20			dB

ELECTRICAL CHARACTERISTICS (continued)

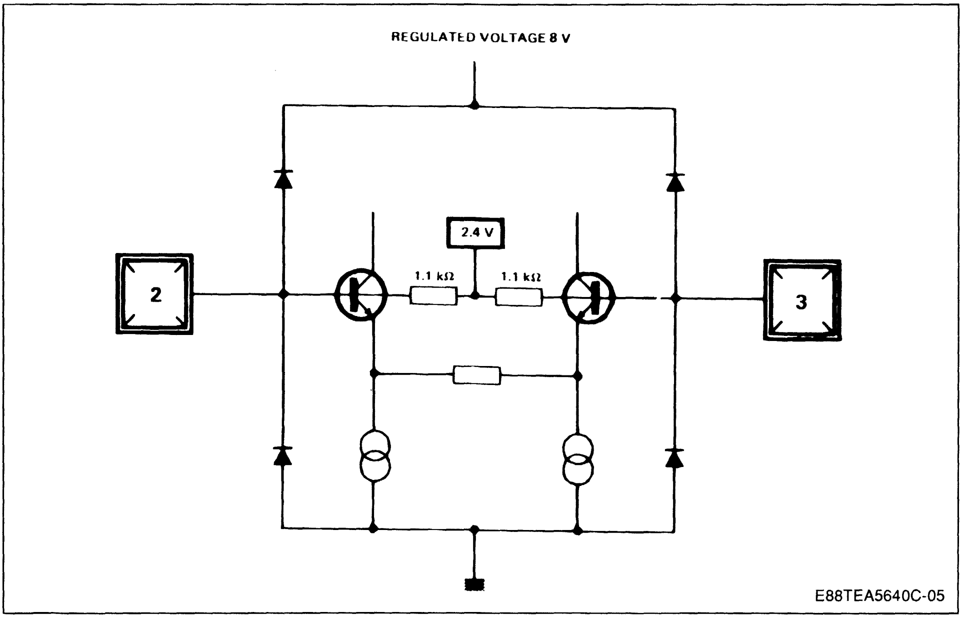
Symbol	Parameter		Min.	Typ.	Max.	Unit
	TINT Control (NTSC Modes)					
	Range of Phase Change For V Pin 5 Changing from 2 to 4.5 V			± 40		Degrees
V5	DC Voltage for 0 Degree TINT Change	Pin 5		3.5		V
I5	Input Current	Pin 5	0.08		0.2	mA
	NTSC Detection					
	Detection Threshold	Pin 6	3	3.5	4	V
	NTSC Mode Inhibition Threshold		0.5		2.5	V
	Leakage Current				0.5	µA
	Delayed Signal Input	Pins 2 - 3				
	DC Voltage in PAL Mode			2.4		V
	Input Impedance		0.88	1.1	1.32	kΩ
	Delay Line Attenuation Compensation					
	Range of Automatic Attenuation Compensation		– 3	– 9	– 15	dB
	Delay Line Phase Shift Compensation					
	Range of Phase Shift Compensation with a 100KΩ Potentiometer (see application diagram p. 3)		± 30			degree
	Alternation Line Detection PAL or SECAM	Pin 11				
VTHH	High Differential Threshold (VTHH = V11H – V24)		200		350	mV
VTHL	Low Differential Threshold (VTHL = V11L – V24)		– 350		– 200	mV
	Leakage Current Threshold (V11 = V24 + 1V)				0.5	µA

INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAMS

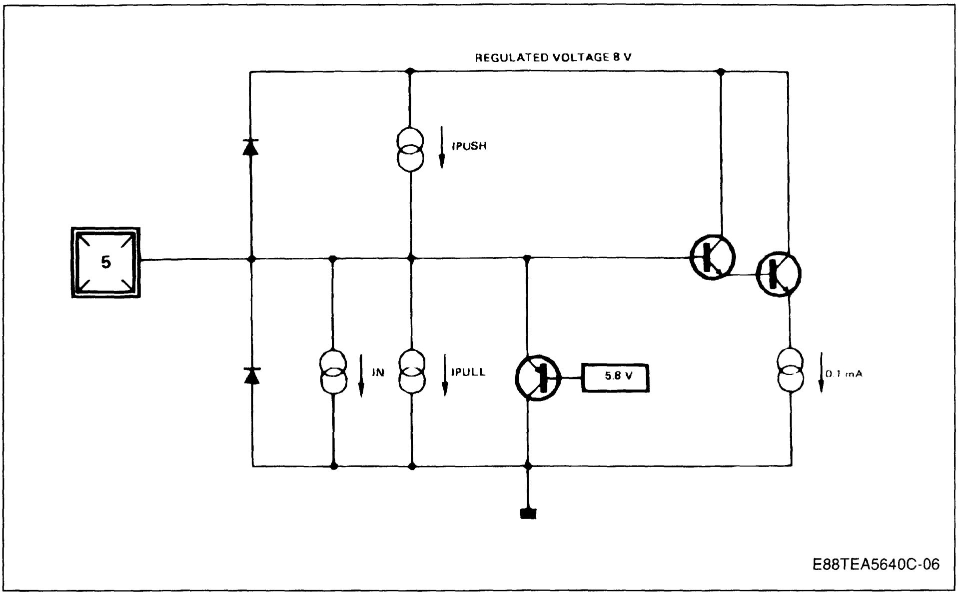
PIN 1



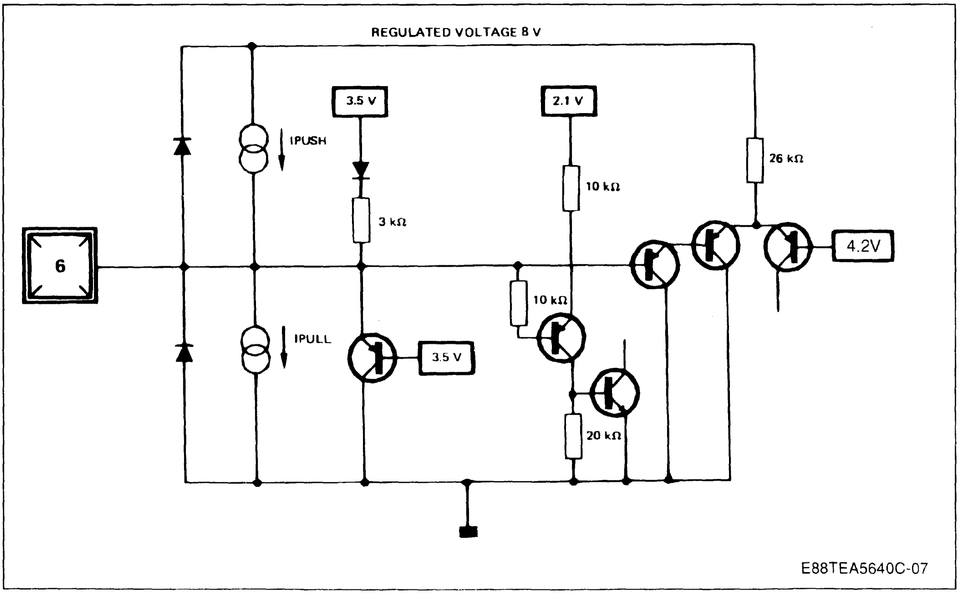
PINS 2 – 3



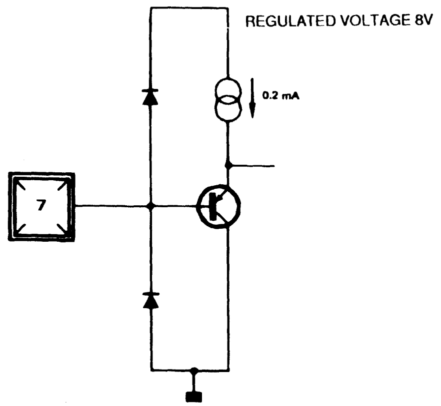
PIN 5


REGULATED VOLTAGE 8 V
IPUSH
5
IN
IPULL
5.8 V
0.1 mA
E88TEA5640C-06

PIN 6

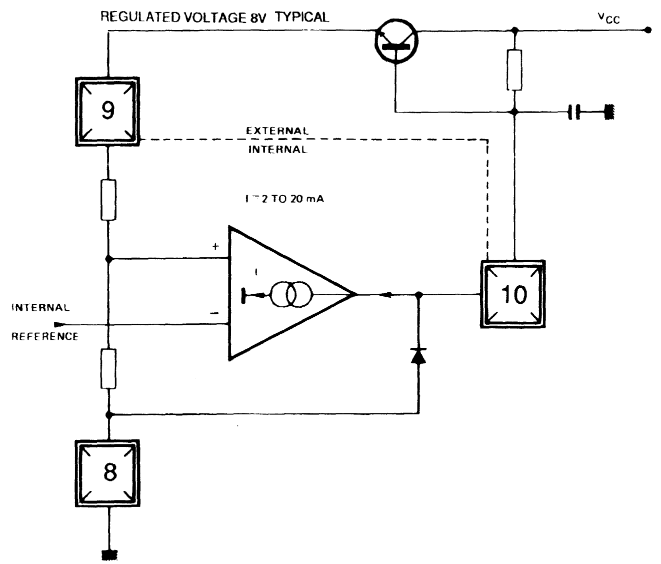

REGULATED VOLTAGE 8 V
3.5 V
2.1 V
IPUSH
3 kΩ
10 kΩ
26 kΩ
6
4.2V
10 kΩ
IPULL
3.5 V
20 kΩ
E88TEA5640C-07

PIN 7



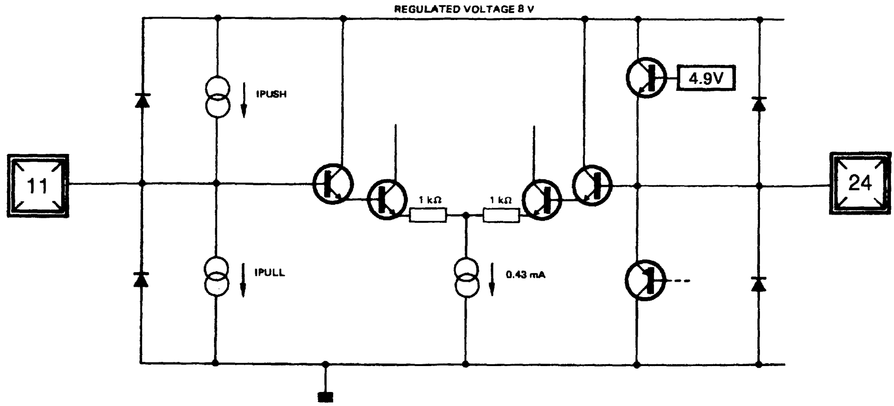
E88TEA5640C-08

PINS 8 – 9 – 10



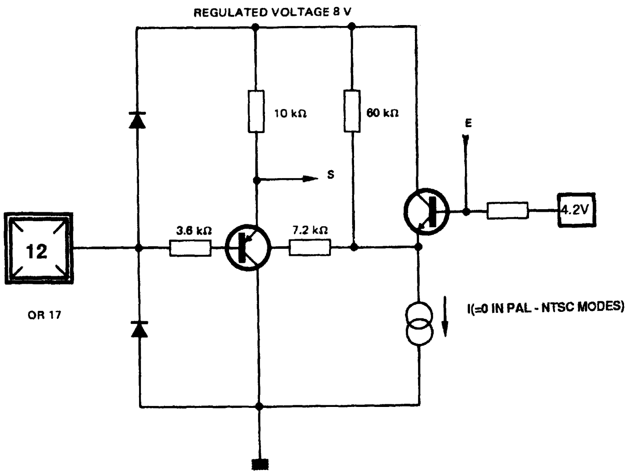
E88TEA5640C-09

PINS 11 – 24



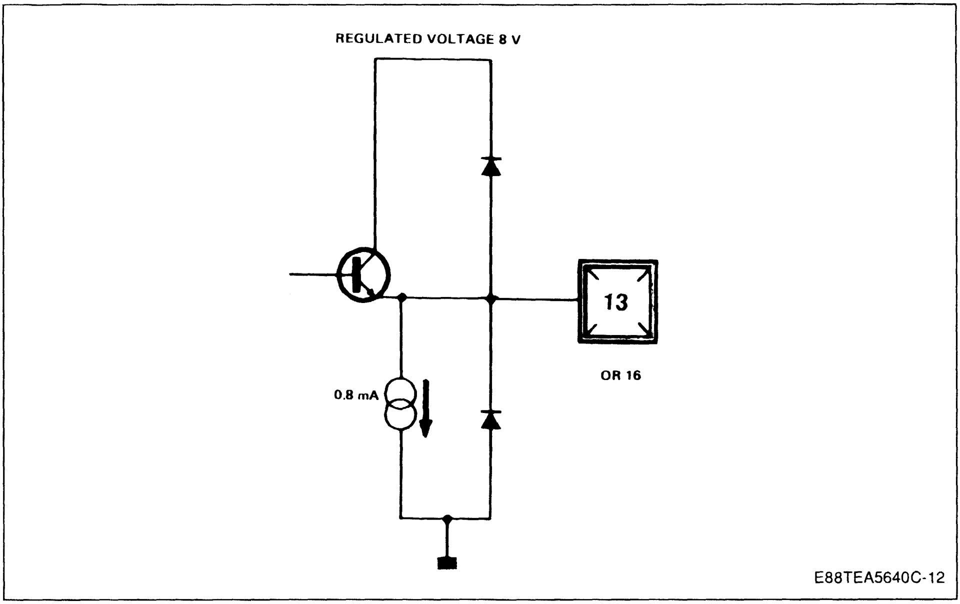
E88TEA5640C-10

PINS 12 – 17

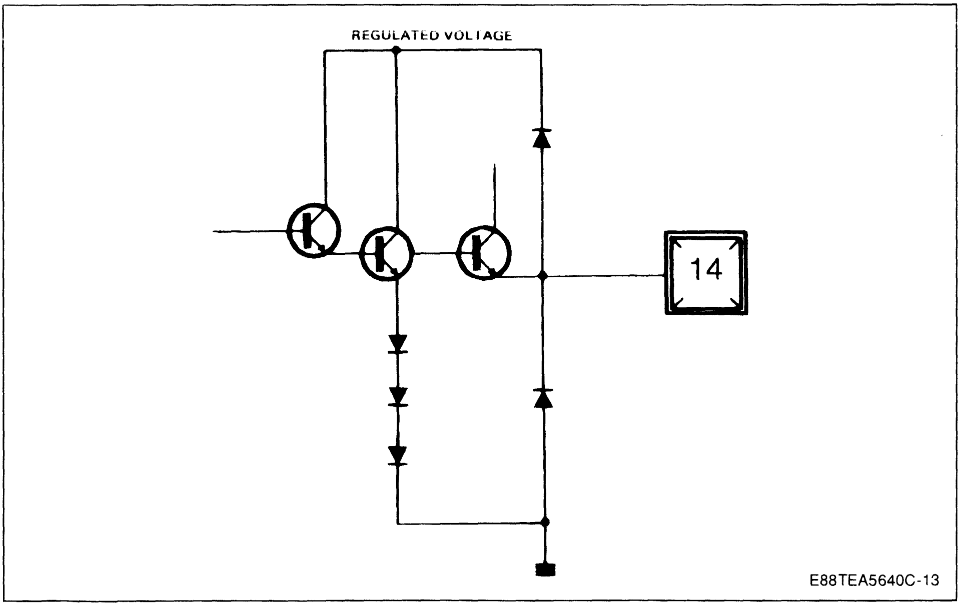


E88TEA5640C-11

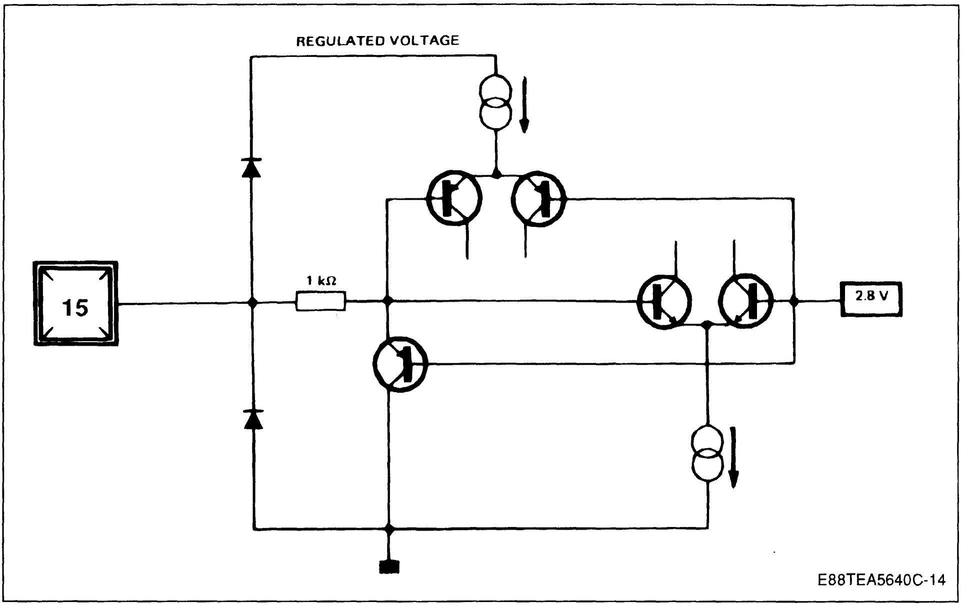
PINS 13 – 16



PIN 14

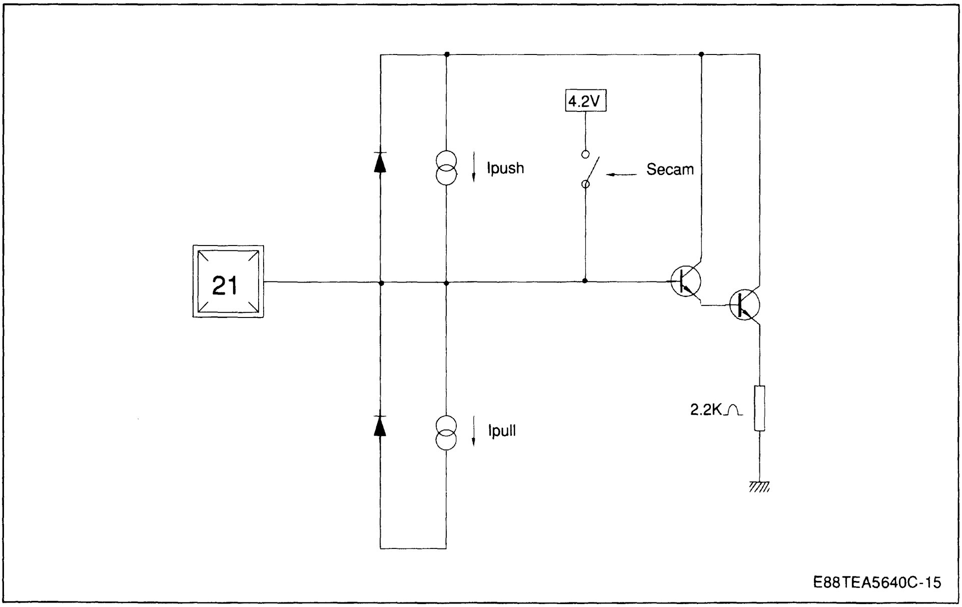


PIN 15



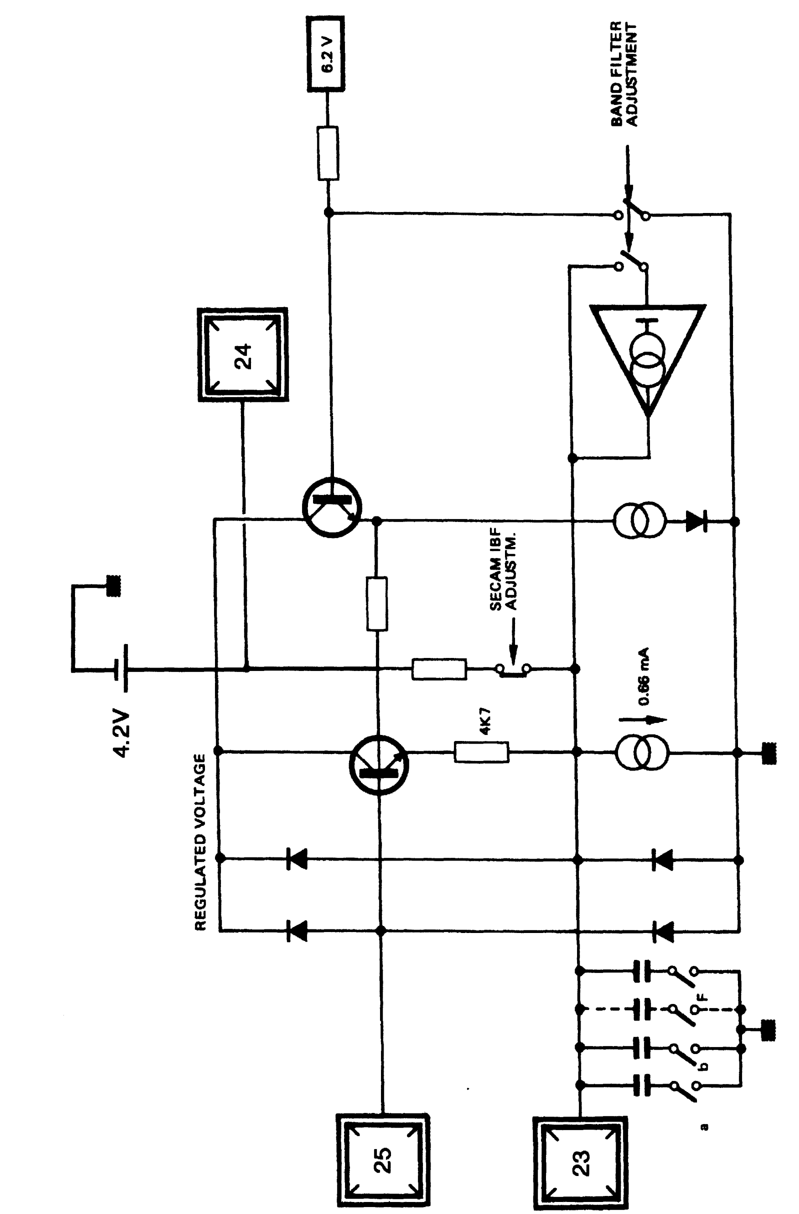
REGULATED VOLTAGE
15
1 kΩ
2.8 V
E88TEA5640C-14

PIN 21



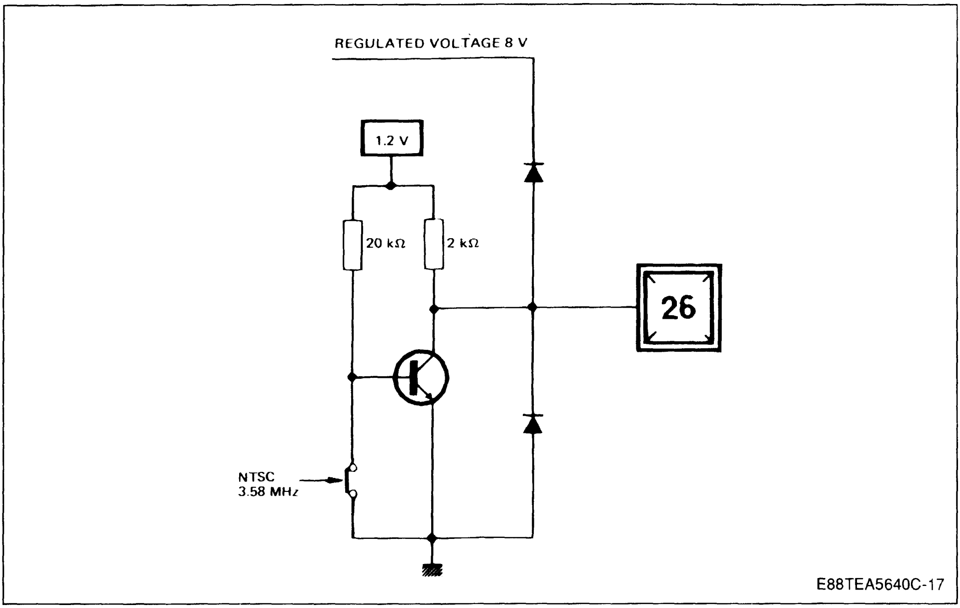
4.2V
Ipush
Secam
21
2.2KΩ
Ipull
E88TEA5640C-15

PINS 23 – 24 – 25

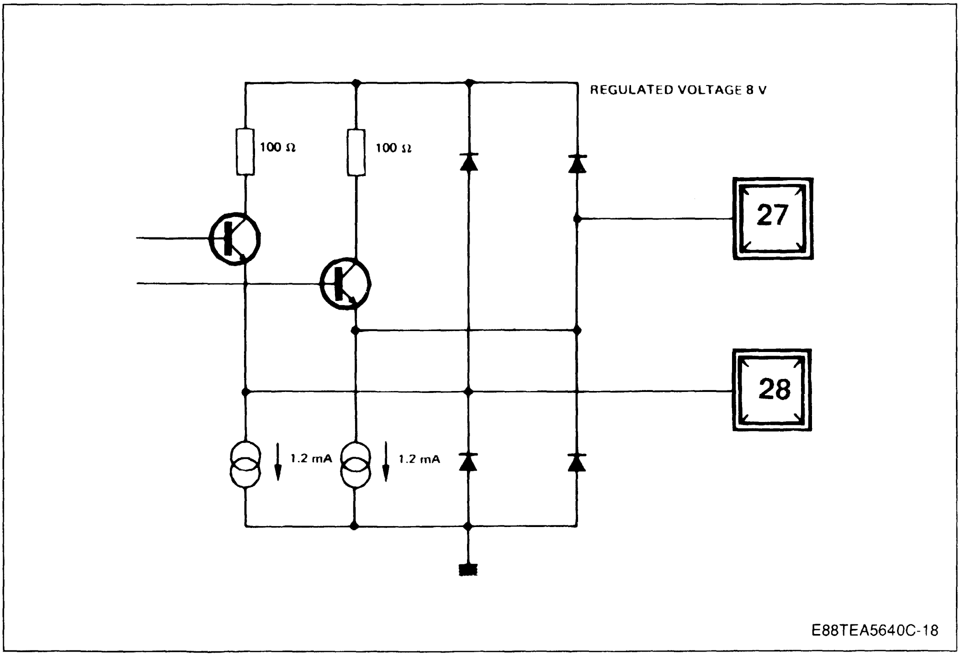


E88TEA5640C-16

PIN 26

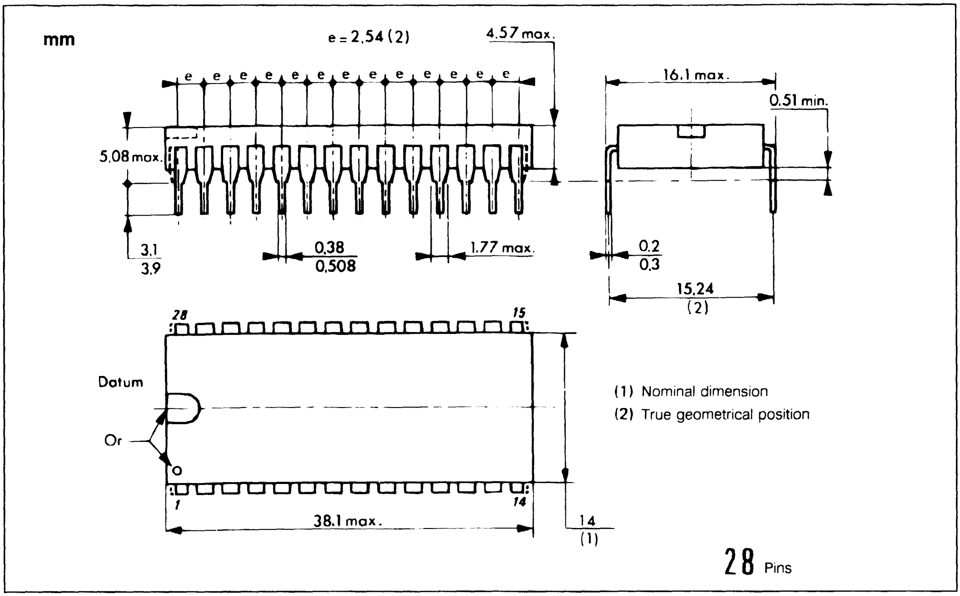


PINS 27 - 28



PACKAGE MECHANICAL DATA

28 PINS – PLASTIC DIP



SGS-THOMSON
MICROELECTRONICS

TEA5701

3 CHANNEL, LARGE BAND HEAD AMPLIFIER FOR VCR

ADVANCE DATA

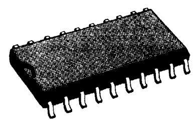
THE TEA5701 IS AN ADVANCED ONE CHIP 3 HEADS RECORD AND PLAY-BACK AMPLIFIER FOR VCR

PLAY-BACK MODE

- LOW NOISE PERFORMANCE
- LARGE BANDWIDTH (SVHS PROCESSING CAPABILITY)
- AUTOMATIC OFFSET CANCELLER BETWEEN TWO SELECTED HEADS
- RECORD AMPLIFIER INHIBITION DURING PLAY-BACK
- DIRECT DRIVE OF COAXIAL CABLE (500 Ω - 100 pF) OF PLAY-BACK OUTPUT

RECORD MODE

- INTEGRATED I/I CONVERTER WITH AUTOMATIC CONTROL OF TRANSCONDUCTANCE
- AUTOMATIC RECORD PLAY-BACK SWITCHING
- PLAY-BACK INHIBITION DURING RECORD MODE
- AUTOMATIC PROTECTION OF RECORD AMPLIFIER AGAINST SHORT CIRCUIT

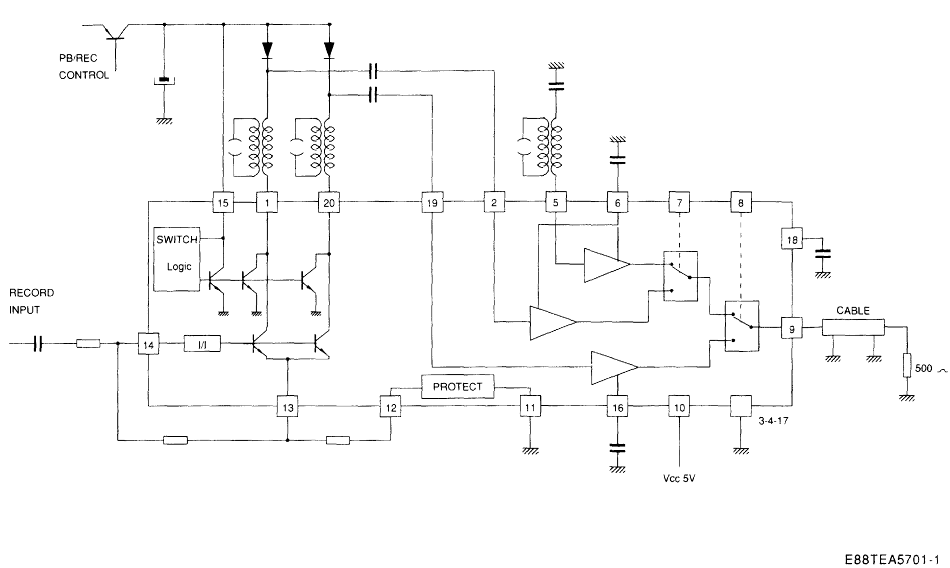


TEA5701
SO20 LARGE
(Plastic Micropackage)

PIN CONNECTION

N°	Function	N°	Function
1	Recording Output Channel 2	11	Ground
2	Play-back Input Channel 2	12	Current Limitation Input
3	Ground	13	Feed-back Output for Recording Mode
4	Ground	14	Recording Input
5	Play-back Input Channel 3	15	Voltage Supply for Recording Mode
6	DC Offset Canceller Channel 2 and 3	16	DC Offset Canceller Channel 1
7	CH2 - CH3 Switch Control	17	Ground
8	CH1 - CH2 or 3 Switch Control	18	Cascode Input Decoupling
9	Play-back Output	19	Play-back Input Channel 1
10	V_{CC} = 5 V	20	Recording Output Channel 1

BLOCK DIAGRAM



DESCRIPTION

TEA5701 is intended for 3 heads VCR applications. It includes all the electrical functions necessary to achieve play-back and record processing for VHS and SVHS applications (9 MHz).

High performance technology allows very low noise levels (current and voltage). In play-back mode a special feature suppresses the DC offset when switching two channels. Optimized play-back output stage gives to the TEA5701 large capability to drive directly a coaxial cable in order to reduce number of external components.

An automatic scanning of recording supply voltage permits that TEA5701 switches automatically in play-back or in record mode. The switching threshold voltage from play-back to record and record to play-back is fixed to a value which forbids high current peaking through the heads.

The recording amplifier includes a protection system which protects the IC and the application board against overheating in case of short circuit on the recording transconductance components.

The TEA5701 is fully protected against ESD.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	6	V
V_{REC}	Supply Voltage	15	V
T_{stg}	Storage Temperature Range	– 40 to + 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

ELECTRICAL OPERATING CHARACTERISTICS

All the operating characteristics are given for ambient temperature 25 °C unless otherwise specified.

PLAY-BACK MODE

General conditions for play-back : VCC = 5 V, no load on play-back output.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5	5.25	V
I_{CC}	Current Supply			45	60	mA
G_{PB}	Play-back Gain	Sine Wave 400 mVpp at 600 khz on Pin 9	56	60	63	dB
$\Delta\ G_{PB}$	Gain Difference Between Three Play-back Channels	Sine Wave 3.8 MHz, 0.4 mVpp on Pins 2 - 5 - 19		0.3		dB
en	Equivalent Input Voltage Noise Level	Measured at 500 KHz – CH1 Via Switching Transistor Pin 20 – CH2 Via Switching Transitor Pin 1 – CH3 Grounded		0.4		$nV/\sqrt{Hz}$
in	Equivalent Input Current Noise Level	Measured at 500 kHz - PB Inputs Pins 2 - 5 - 19 not Connected		3		$pA/\sqrt{Hz}$
CRT	Crosstalk	Sine Wave 3.8 MHz 400 mVpp on Pin 9 For selected channel : – CH1 input, between pins 19 and 20 – CH2 input, between pins 1 and 2 – CH3 input, between pin 5 and ground.			– 40	dB
FLCPB	Play-back Bandwidth Low Cut Off Frequency	Reference Signal Level : Sine Wave 3.8 MHz 400 mVpp – Play-back Input Capacitors 22 nF (pins 2 - 6 - 19) – DC Offset Canceller Capacitor (pins 6 - 16-) 47 nF		20	100	KHz

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
FHCPB	Play-back Bandwidth High Cut Off Frequency	Same Conditions as Above	8	9.5		MHz
C_{in}	Play-back Input Capacitance Pins 2 - 5 - 19			50		pF
R_{in}	Play-back Input Resistance Pins 2 - 5 - 19			600		Ω
VDCPB	DC Level on Play-back Output Pin 9 during Play-back	With 500 Ω Load Resistor Between Pin 9 and Ground	1.9	2.4	2.9	V
ΔVDC	Head Switch Offset Pin 9 (all switches combinations)				50	mV
SM	Second Harmonic on Play-back Output Pin 9	Sine Wave 3.8 MHz 400 mVpp with 500 Ω load Resistor		– 43	– 38	dB
V_{sat}	Maximum Voltage on Pins 1 and 20 at Play-back Mode	Input Current Pins 1 and 20 20 mADC			100	mV

RECORDING MODE

General conditions for recording mode : V_{REC} = 12 V
V_{CC} = 5 V
Load resistor 100 Ω on pins 1 and 20
No load on play-back output pin 9

Transconductance network defined by : R1 = 5.1 Ω 1 % pins 12-13
R2 = 1 kΩ 1 % pins 13-14
R3 = 750 Ω 1 % pin 14

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{REC}	Recording Supply Voltage		9	12	12.6	V
ICCREC	Current Supply from VREC			50	60	mA
ICCI	Current Supply from V_{CC}			30	37.5	mA
VDCREC	DC Level on Play-back Output Pin 9	With 500 Ω Load Resistor Between Pin 9 and Ground	3.1	3.6	4.1	V
	Maximum Recording Current on Each Channel	f = 1.6 MHz	40			mApp
	Maximum Recording Current on Each Channel	f = 3.8 MHz	35			mApp
g	Transconductance	R1 = 5.1 Ω 0 % R2 = 1000 Ω 0 % R3 = 750 Ω 0 % V_{in} = 300 mVpp Measured at 500 KHz		132		mA/V
Δ g	Recording Current Difference Between Pins 1 and 20	Sine Wave 3.8 MHz Irecording = 30 mA_{PP}			0.5	dB
REREC	Equivalent Input Resistance			660		Ω

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
R_s	Output Resistance Pins 1 and 20	R1 = 5.1 Ω		100		kΩ
SHREC	Second Harmonic Pins 1 and 20	Output Current on Each Output : 30 mApp at 3.8 MHz			– 38	dB
FLCREC	Recording Bandwidth Low Cut Off Frequency	Reference Output Current 30 mApp at 3.8 MHz for – 3 dB		20	100	kHz
FHCREC	Recording Bandwidth High Cut Off Frequency	Reference Output Current 30 mApp at 500 KHz for – 3 dB	8	9.5		MHz
	Maximum Input Current Pin 12	Pin 12 Connected to VREC = 12 V			100	mA
	Maximum Saturation Voltage on Pin12	Input Current Pin 12 : 50 mA		100	150	mV
IM	Intermodulation	I Luminance = 30 mApp 3.8 MHz I Chrominance = 7.5 mApp, 600 KHz Measured at 3.8 MHz ± 600 KHz		– 50		dB

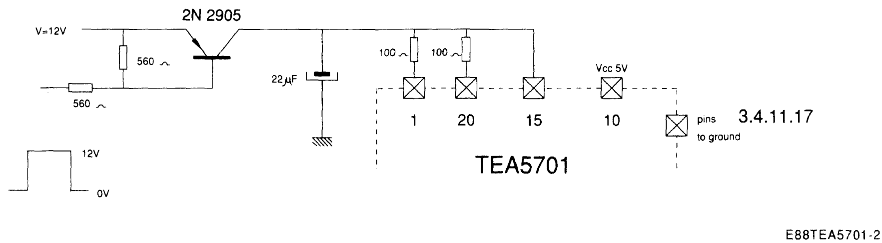
SWITCHING LEVELS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{H8}	Threshold Voltage for Head 1 Selection on Pin 8		2.4		V_{CC}	V
V_{L8}	Threshold Voltage for Head 2 or 3 Selection on Pin 8		0		1.5	V
I_{H8}	Input Current Pin 8 for H1 Selected	Pin 8 Connected to V_{CC}			50	µA
I_{L8}	Output Current Pin 8 for H2 or 3 Selected	Pin 8 Connected to Ground			– 50	µA
V_{H7}	Threshold Voltage for Head 2 Selection on Pin 7		2.4		V_{CC}	V
V_{L7}	Threshold Voltage for Head 3 Selection on Pin 7		0		1.5	V
I_{H7}	Input Current Pin 7 for Head 2 Selected	Pin 7 Connected to V_{CC}			50	µA
I_{L7}	Output Current Pin 7 for Head 3 Selected	Pin 7 Connected to Ground			– 50	µA
	Switching Time from H1 Selected to H2 Selected	Switching Pulse from 5 to 0 V Applied Pin 8		250	500	ns
	Switching Time from H2 Selected to H1 Selected	Switching Pulse from 0 to 5 V Applied Pin 8		250	500	ns

ELECTRICAL CHARACTERITICS (continued)

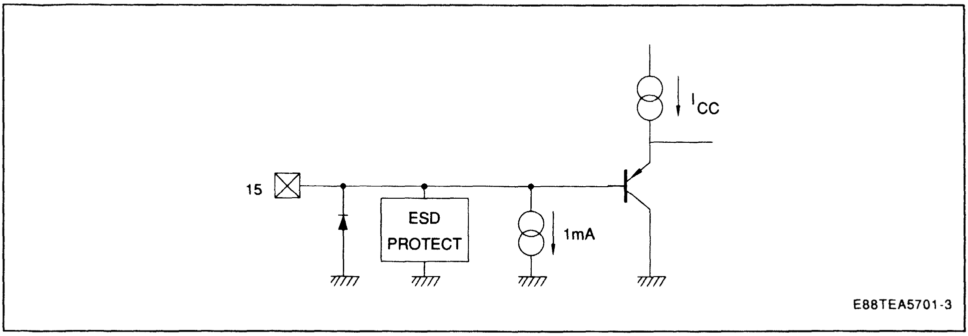
Symbol	Parameter		Min.	Typ.	Max.	Unit
VRPB	Recording Supply Voltage Threshold (pin 15) for Switching from Record to Play-back		0.15	0.3	0.5	V
VPBR	Recording Supply Voltage Threshold (pin 15) for Switching from Play-back to record		0.25	0.4	0.6	V
	Delay Time for Suppression of Play-back Output Signal on Pin 9 (play-back to record)	See Measurement Conditions End of Paragraph		30		µs
	Delay Time for Presence of Play-back Output Signal on Pin 9 (record to play-back)	See Measurements Conditions End of Paragraph		20		ms
	Delay Time for Suppression of Recording Signals Pins 1 and 20 (record to play-back)	See Measurements Conditions End of Paragraph		4		ms
	Delay Time for Suppression of Recording Signals Pin 1 and 20 (play-back to record)	See Measurements Conditions End of Paragraph		200		µs
SVR	Supply Voltage Rejection	Gain Measure Made Between Play-back Output Pin 9 and V_{CC} (0.5 mVpp on pin 10)	15	20	25	dB

Test Conditions for Measuring Delay Times (play-back to record and vice versa)

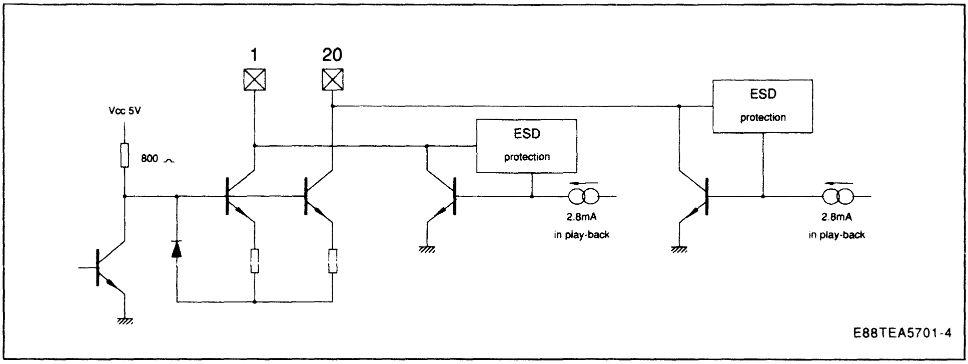


INPUTS/OUTPUTS EQUIVALENT INTERNAL DIAGRAM

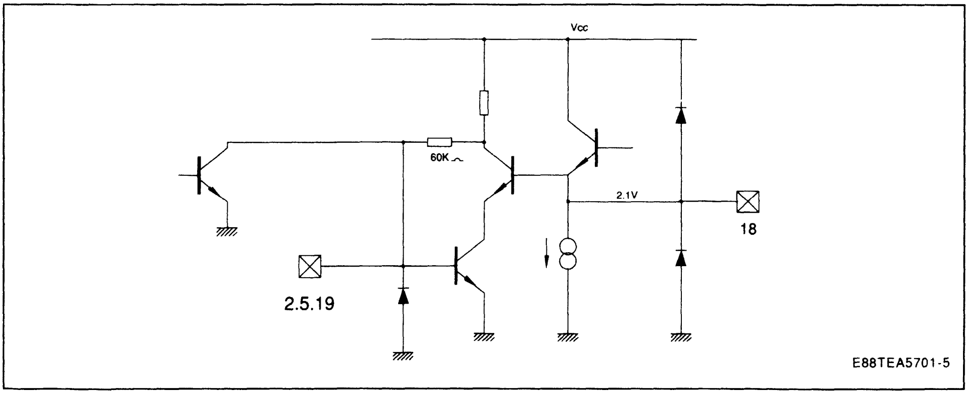
PIN 15



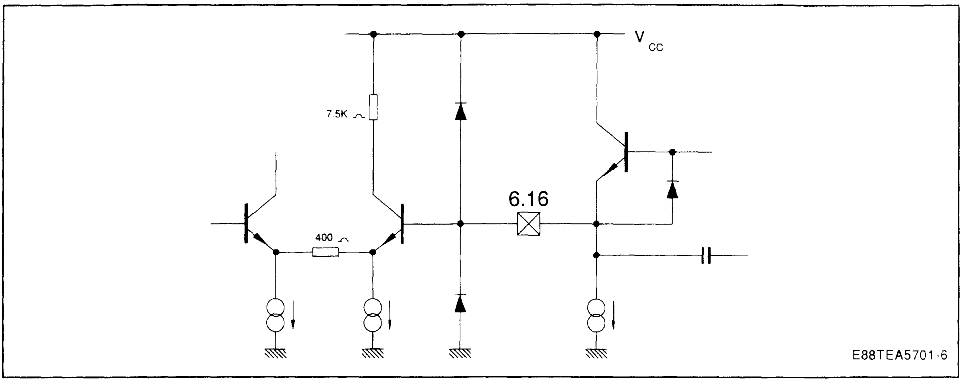
PIN 1 AND 20



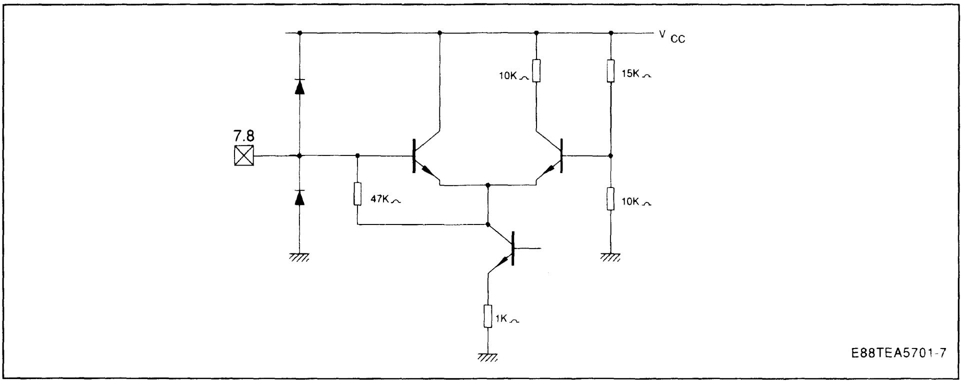
PINS 2 - 5 - 19 - 18



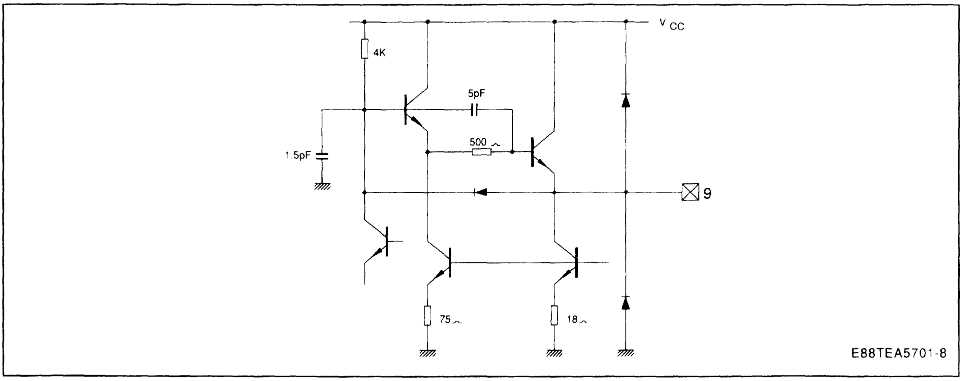
PINS 6 - 16



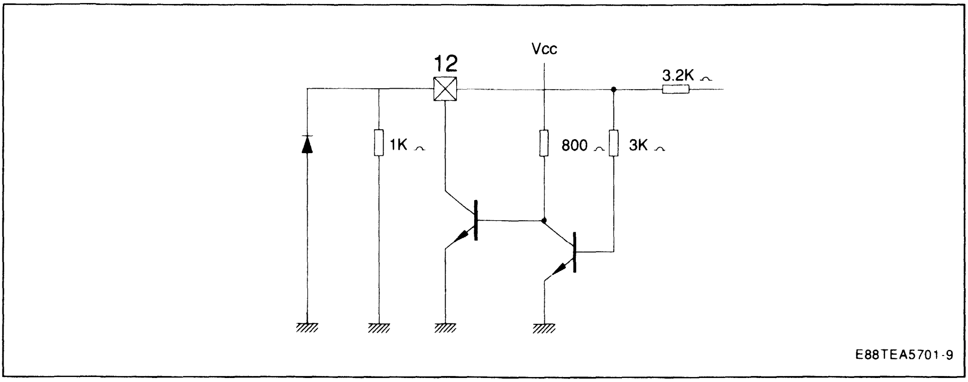
PINS 7 - 8



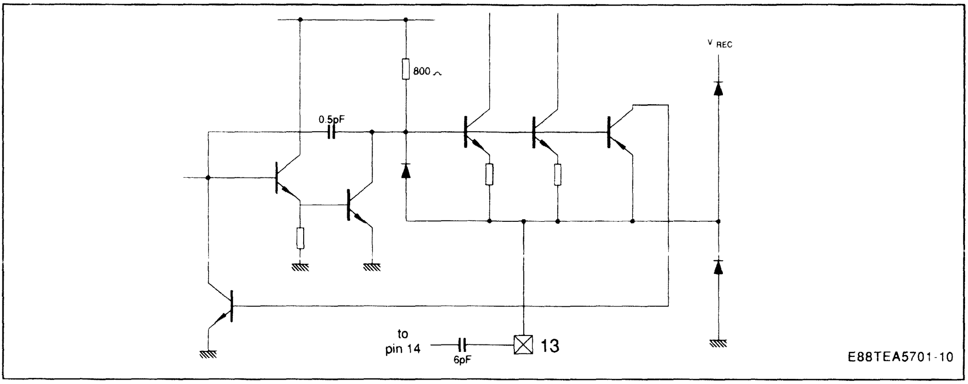
PIN 9



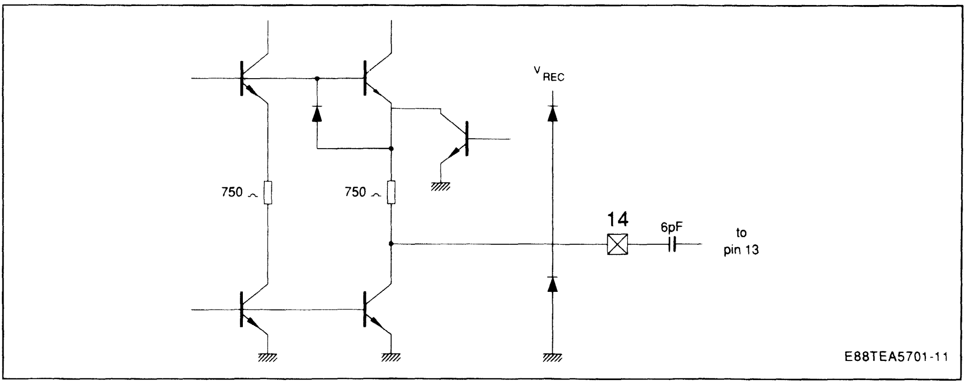
PIN 12



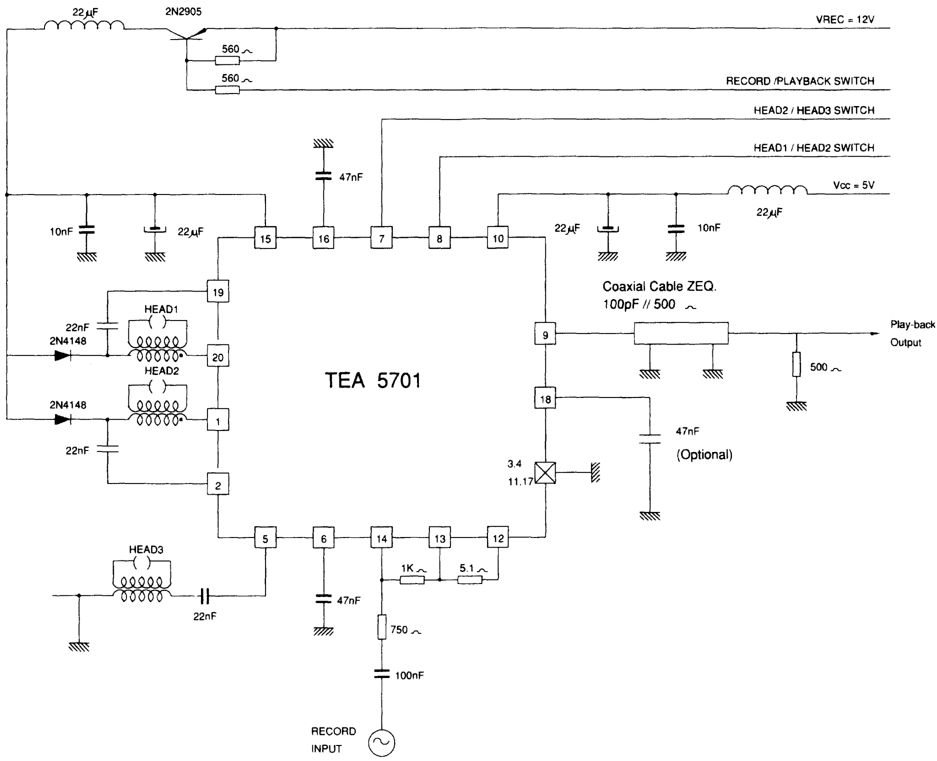
PIN 13



PIN 14

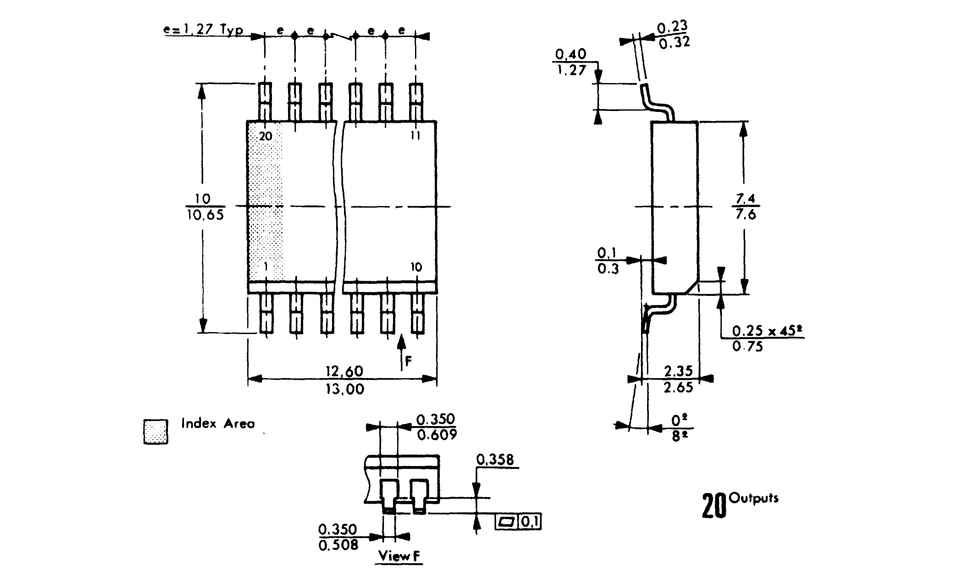


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

SO20 LARGE – PLASTIC MICROPACKAGE



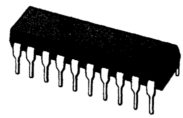
SGS-THOMSON
MICROELECTRONICS

TEA6414

BUS CONTROLLED VIDEO MATRIX SWITCH

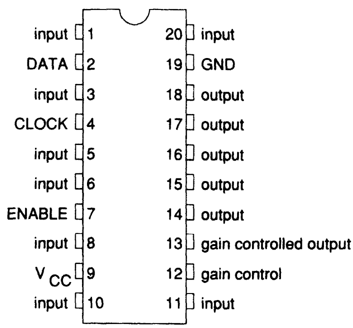
ADVANCE DATA

- 15MHz BANDWIDTH
- 8 INPUTS (CVBS, RGB, MAC, chroma...)
- 6 OUTPUTS (one gain controlled output)
- POSSIBILITY OF MAC SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- – 55dB CROSSTALK AT 5 MHz
- FULLY PROTECTED AGAINST ESD



TEA6414
DIP20
(Plastic Package)

PIN CONNECTIONS

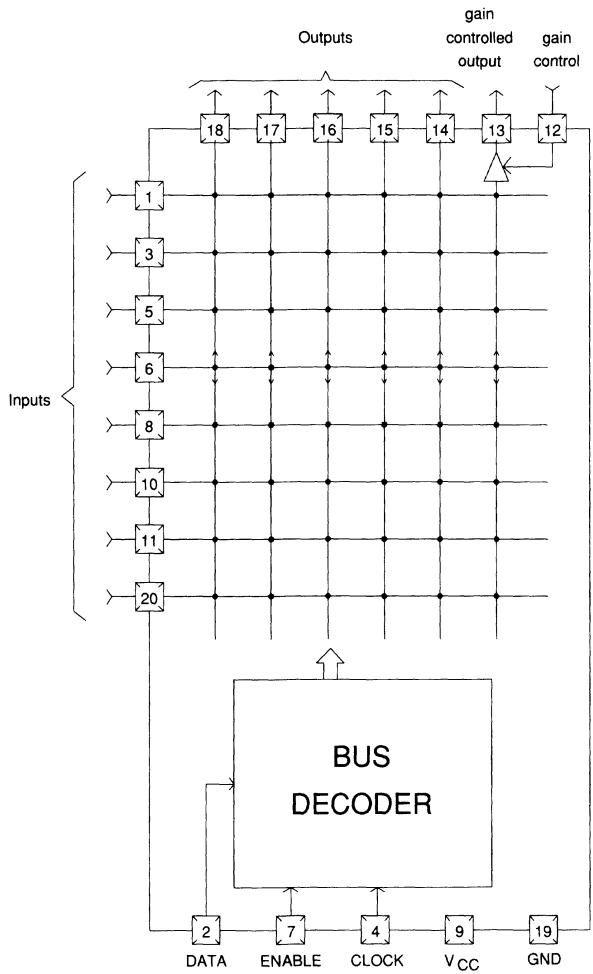


E88TEA6414-01

DESCRIPTION

The TEA6414 switches 8 input VIDEO sources on 6 outputs. Each output can be switched on only one of each input but it is possible to have the same input connected to several outputs. The gain controlled output must be connected to an unclamped input. All the switching possibilities are changed through the 3 Wire-Bus (THOMSON BUS).

BLOCK DIAGRAM



E88TEA6414-02

Note : When any input is not used, it must be bypassed to ground through a 220nF capacitor, so as to avoid degrading the crosstalk.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Pin 9	11.5	V
T_{amb}	Operating Ambient Temperature Range	0 to + 70	°C
T_{stg}	Storage Temperature Range	– 20 to + 150	°C

THERMAL DATA

$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 10V, R_{load} = 10kΩ, C_{load} = 3pF (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage Pin 9	7	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC} = 10V)		37	45	mA

GAIN CONTROLLED OUTPUT (pin 13 ; forced input DC level = 5V with an external resistor bridge on the selected input, see application diagram)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Dynamic Pin 13	3			V_{pp}
	Output Impedance		120	150	Ω
	Min. Gain ($I_{control}$ on pin 12 = – 0.8mA)	– 10	– 9	– 8	dB
	Nominal Gain ($I_{control}$ = 0, V_{in} = 1Vpp)	5.5	6.5	7.5	dB
	Max. Gain ($I_{control}$ on pin 12 = 0.8mA)	12	13	14	dB
	Bandwidth (– 3dB attenuation)	7	10		MHz
	Crosstalk (f = 5MHz)		– 55		dB
	DC Level	5.7	6	6.3	V

GAIN CONTROL

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Nominal Voltage Pin 12	3.7	4	4.3	V
	Impedance	0.8	1	1.2	kΩ
	Max. Gain Control Current (for gain max. – 0.5dB)	0.04	0.1	0.2	mA
	Min. Gain Control Current (for gain min. + 0.5dB)	– 0.3	– 0.2	– 0.14	mA

ELECTRICAL CHARACTERISTICS (continued)

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Max Signal Amplitude (CVBS signal)	2			V_{pp}
	Input Current (per output connected, input voltage = 5VDC) (this current is X6 when all outputs are connected on the input)		1	2	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70°C)			100	mV

OUTPUTS (V_{in} = 1V_{pp} for all dynamic tests)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Dynamic Pin 14-15-16-17-18	4			V_{pp}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth (– 1dB Attenuation)	7	10		MHz
	Crosstalk (f = 5MHz)		– 55		dB
	DC Level	2.9	3.2	3.5	V

GENERAL DESCRIPTION

The main function of the IC is to switch 8 input video sources on 6 outputs.

Each output can be switched on only one of each input. On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB. For D2MAC signal the alignment is switched off by forcing, with an external resistor bridge, 5 V_{DC} on the input.

Each input can be used as a normal input or as a MAC input (with external resistor bridge).

All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

On the output (pin 13) the gain is controlled in the range + 13dB, – 9dB in order to adjust the output level to 2Vpp. The nominal gain (6.5dB) is obtained when pin 12 is DC not connected and AC grounded. The gain is controlled by varying current on pin 12.

It is possible to have the same input connected to several outputs.

The starting configuration (power supply from 0 to 8V) is undetermined.

6 words of 8 bits are necessary to determine one configuration.

BUS SELECTIONS (THOMSON BUS)

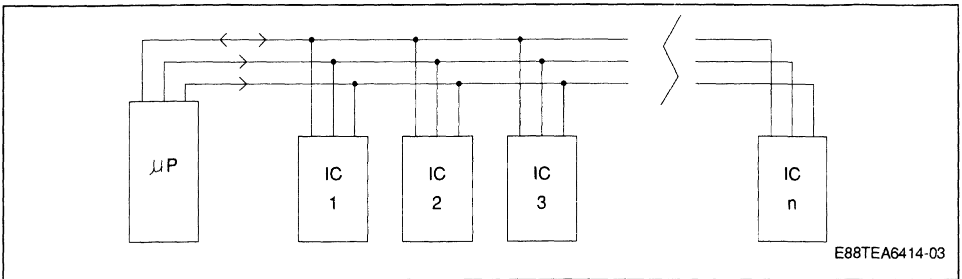
ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	pin 18	Output is selected by address bits
00100	XXX	pin 14	
00010	XXX	pin 15	
00110	---	not used	
00001	XXX	pin 17	
00101	XXX	pin 13	
00011	XXX	pin 15	
00111	---	not used	

ADDRESS MSB	DATA LSB	Selected Input	
00XXX	000	pin 5	Input is selected by data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

Example : 00100 101 connect pin 10 (input) to pin 14 (output).
(equals 25 in hexadecimal).

SPECIFICATION FOR THE THOMSON BIDIRECTIONAL DATA BUS

The bidirectional data bus has three lines (DATA, CLOCK, ENABLE) and operates serially. Transmission on the DATALINE is effected bidirectionally, whilst the ENABLE- and CLOCKLINES are driven only by the microprocessor. It is possible to select several ICs from the µP via the THOMSON BUS.



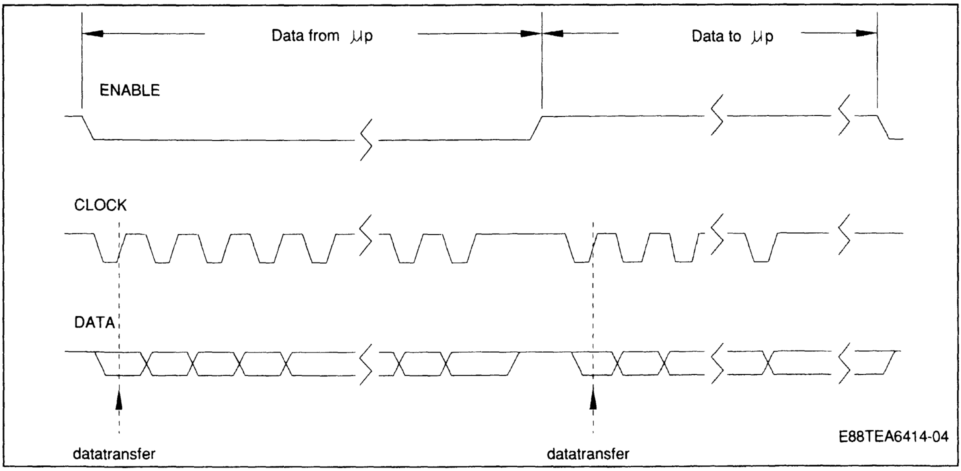
The identification or address of each particular IC is achieved by the length of the word (number of clock pulses), and each IC responds with its own particular word length. The address length is determined only while ENABLE is low, by counting the clock pulses. The rising edge of the ENABLE signal indicates the end of the address sequence.

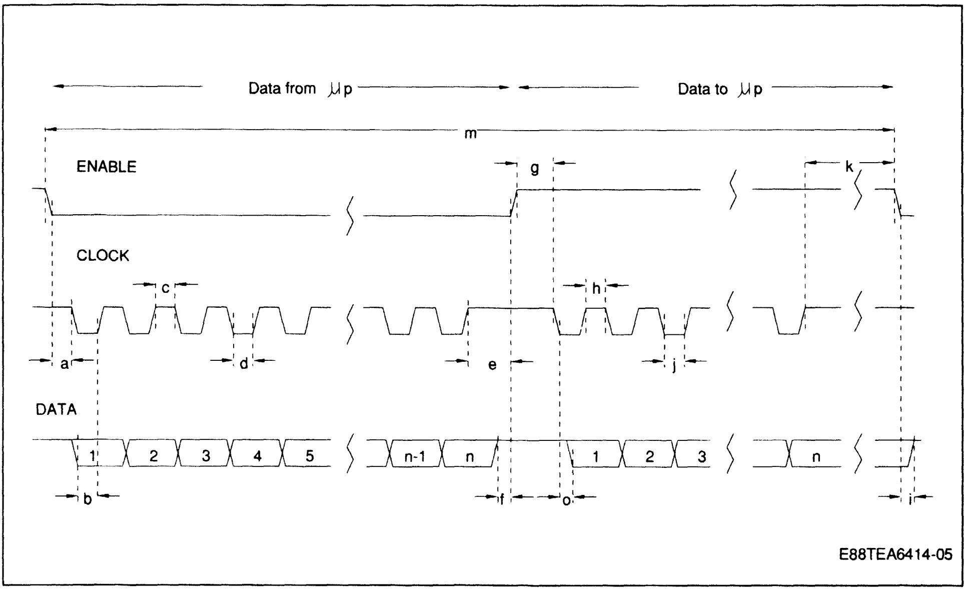
Normally, there are several locations within the same chip, which must be selected individually, the datastream may, therefore be split into subaddress and data. In the case where an IC is not using the complete specified subaddress range it is possible to employ the unused subaddress range with a second or third IC with the same word length. The bitnumber of the subaddress is flexible.

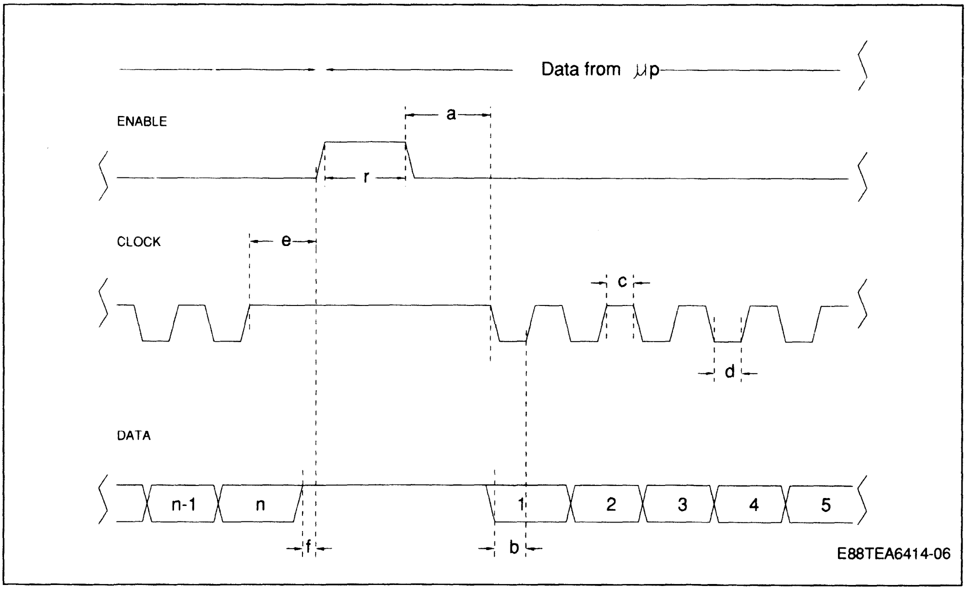
The reply word length from any of the ICs to the µP is also flexible. This bidirectional transmission is possible from the last addressed IC after the positive going edge of the ENABLE signal if the ENABLE signal remains high and the CLOCK impulses are present on the line. The µP in effect clocks out the data from the chip. When an IC is able to send information in the bidirectional way, the µP decides whether to take all information, to suppress completely the information or to stop the transfer after any bit.

This reply word, synchronized to the clock from µP, is sent only once. Should a subsequent clock impulse be present on the clock line, it will switch the IC in question to high impedance.

The register, from which the bidirectional information comes, is addressed with the IC address. When more than one bidirectional register exists, the selection is made by the previously selected subaddress.



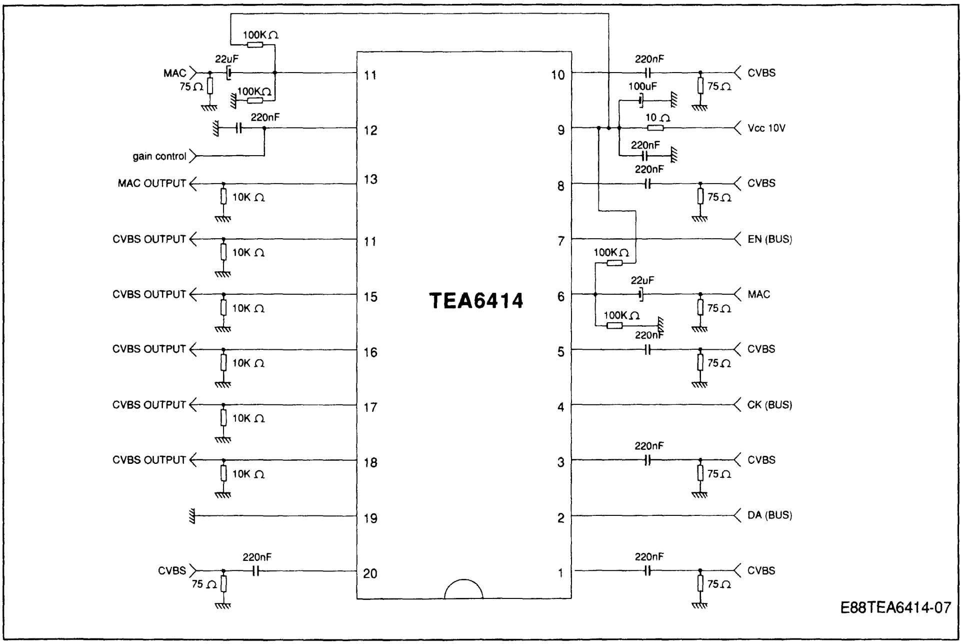

Data from µp
Data to µp
m
ENABLE
g
k
CLOCK
c
h
a
d
e
j
DATA
1
2
3
4
5
n-1
n
1
2
3
n
b
f
o
i
E88TEA6414-05


Data from µp
ENABLE
a
r
CLOCK
e
c
d
DATA
n-1
n
1
2
3
4
5
f
b
E88TEA6414-06

TIMING FOR THOMSON BUS

Parameter	Min.	Typ.	Max.	Unit
a	1			µs
b	1			µs
c	1			µs
d	1			µs
e	2			µs
f	1			µs
r	2			µs

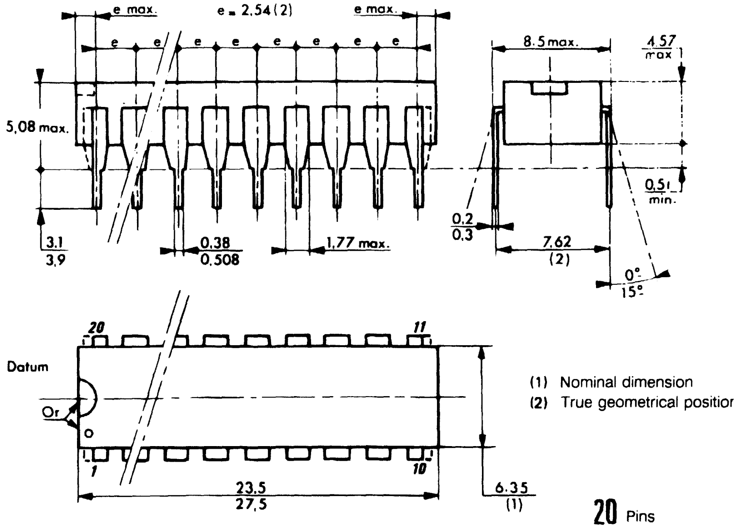
TYPICAL APPLICATION



Note : When any input is not used, it must be bypassed to ground through a 220nF capacitor, so as to avoid degrading the crosstalk.

PACKAGE MECHANICAL DATA

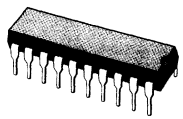
20 PINS – PLASTIC DIP



BUS CONTROLLED VIDEO MATRIX SWITCH

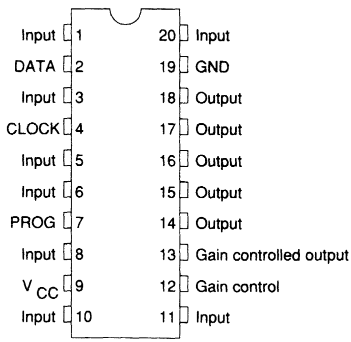
ADVANCE **DATA**

- 15MHz BANDWIDTH
- CASCADABLE WITH ANOTHER TEA6415 (internal address can be changed by pin 7 voltage)
- 8 INPUTS (CVBS, RGB, MAC, chroma...)
- 6 OUTPUTS (one gain controlled output)
- POSSIBILITY OF MAC SIGNAL FOR EACH INPUT BY SWITCHING-OFF THE CLAMP WITH AN EXTERNAL RESISTOR BRIDGE
- BUS CONTROLLED
- 6.5dB GAIN BETWEEN ANY INPUT AND OUTPUT
- - 55dB CROSSTALK AT 5MHz
- FULLY PROTECTED AGAINST ESD



TEA6415
DIP20
(Plastic Package)

PIN CONNECTIONS

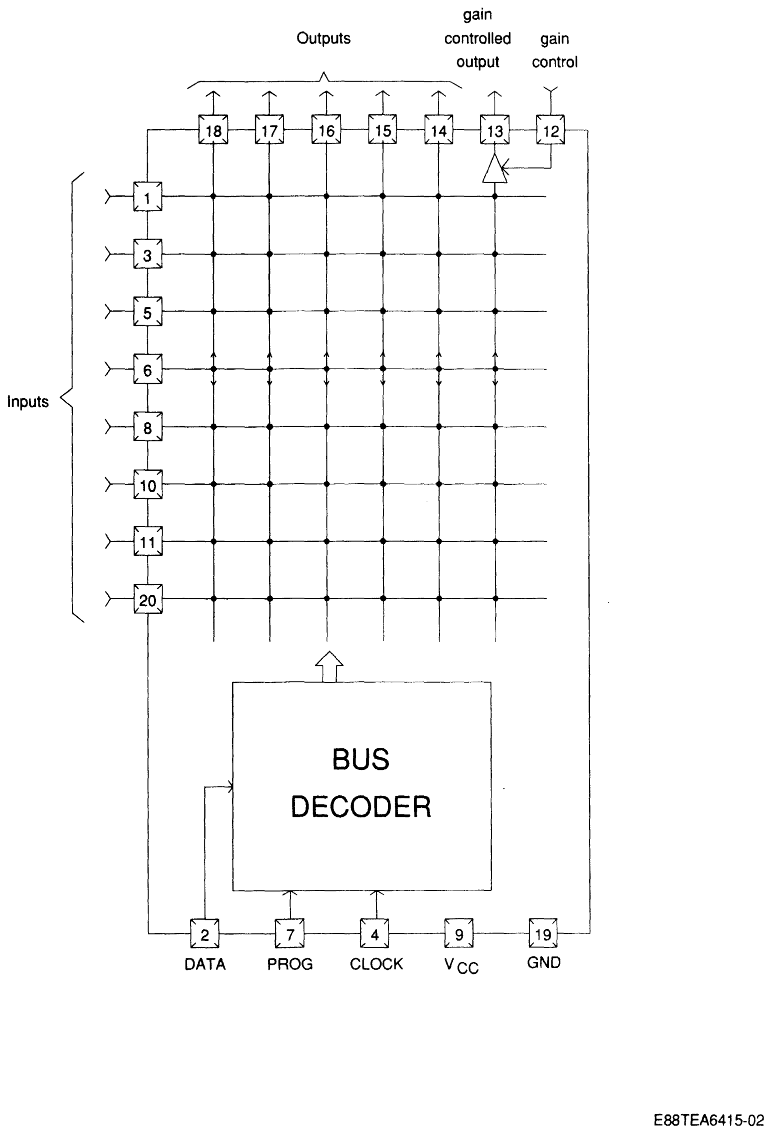


E88TEA6415-01

DESCRIPTION

The TEA6415 switches 8 input VIDEO sources on 6 outputs. Each output can be switched on only one of each input but it is possible to have the same input connected to several outputs. The gain controlled output must be connected to an unclamped input. All the switching possibilities are changed through the S–Bus.

BLOCK DIAGRAM



Note : When any input is not used, it must be bypassed to ground through a 220nF capacitor, so as to avoid degrading the crosstalk.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage	Pin 9	11.5	V
T_{amb}	Operating Ambient Temperature Range		0 to 70	°C
T_{stg}	Storage Temperature Range		– 20 to 150	°C

THERMAL DATA

$R_{th\ (J-a)}$	Junction-ambient Thermal Resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{CC} = 10V, R_{load} = 10kΩ, C_{load} = 3pF (unless otherwise specified)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	Pin 9	7	10	11	V
I_{CC}	Power Supply Current (without load on outputs ; V_{CC} = 10V)			37	45	mA

GAIN CONTROLLED OUTPUT (pin 13 ; forced input DC level = 5V with an external resistor bridge on the selected input ; see application diagram)

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Dynamic	Pin 13	3			V_{pp}
	Output Impedance			120	150	Ω
	Minimum Gain ($I_{control}$ on pin 12 = – 0.8mA)		– 10	– 9	– 8	dB
	Nominal Gain ($I_{control}$ = 0 ; V_{in} = 1Vpp)		5.5	6.5	7.5	dB
	Maximum Gain ($I_{control}$ on pin 12 = 0.8mA)		12	13	14	dB
	Bandwidth (– 3dB attenuation)		7	10		MHz
	Crosstalk (f = 5MHz)			– 55		dB
	DC Level		5.7	6	6.3	V

GAIN CONTROL

Symbol	Parameter		Min.	Typ.	Max.	Unit
	Nominal Gain Voltage	Pin 12	3.7	4	4.3	V
	Impedance		0.8	1	1.2	kΩ
	Max. Gain Control Current (for gain max. – 0.5dB)		0.04	0.1	0.2	mA
	Min. Gain Control Current (for gain min. + 0.5dB)		– 0.3	– 0.2	– 0.14	mA

ELECTRICAL CHARACTERISTICS (continued)

INPUTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Max. Signal Amplitude (CVBS signal)	2			V_{pp}
	Input Current (per output connected, input voltage = $5V_{DC}$) (this current is X6 when all outputs are connected on the input)		1	2	µA
	DC Level	3.3	3.6	3.9	V
	DC Level Shift (temperature from 0 to 70°C)			100	mV

OUTPUTS (V_{in} = $1V_{pp}$ for all dynamic tests)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Dynamic Pins 14-15-16-17-18	4			V_{pp}
	Output Impedance		25	50	Ω
	Gain	5.5	6.5	7.5	dB
	Bandwidth (– 1dB attenuation)	7	10		MHz
	Crosstalk (f = 5MHz)		– 55		dB
	DC Level	2.9	3.2	3.5	V

PROGRAMMATION INPUT (pin 7)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Threshold Voltage		2		V

GENERAL DESCRIPTION

The main function of the IC is to switch 8 input video sources on 6 outputs.

Each output can be switched on only one of each input.

On each input an alignment of the lowest level of the signal is made (bottom of synch. top for CVBS or black level for RGB signals).

Each nominal gain between any input and output is 6.5dB. For D2MAC signal the alignment is switched off by forcing with an external resistor bridge, 5 VDC on the input.

Each input can be used as a normal input or as a MAC input (with external resistor bridge).

All the switching possibilities are changed through the BUS.

Driving 75Ω load needs an external transistor.

On the output (pin 13) the gain is controlled in the range + 13dB - 9dB in order to adjust the output level to 2 Vpp. The nominal gain (6.5dB) is obtained when pin 12 is DC not connected and AC grounded. The gain is controlled by varying current on pin 12.

It is possible to have the same input connected to several outputs.

The starting configuration (power supply from 0 to 8V) is undetermined.

6 words of 8 bits are necessary to determine one configuration.

BUS SELECTIONS (S–Bus)

2nd byte of transmission

ADDRESS MSB	DATA LSB	Selected Output	
00000	XXX	pin 18	Output is selected by address bits
00100	XXX	pin 14	
00010	XXX	pin 15	
00110	---	not used	
00001	XXX	pin 17	
00101	XXX	pin 13	
00011	XXX	pin 15	
00111	---	not used	

ADDRESS MSB	DATA LSB	Selected Input	
00XXX	000	pin 5	Input is selected by data bits
00XXX	100	pin 8	
00XXX	010	pin 3	
00XXX	110	pin 20	
00XXX	001	pin 6	
00XXX	101	pin 10	
00XXX	011	pin 1	
00XXX	111	pin 11	

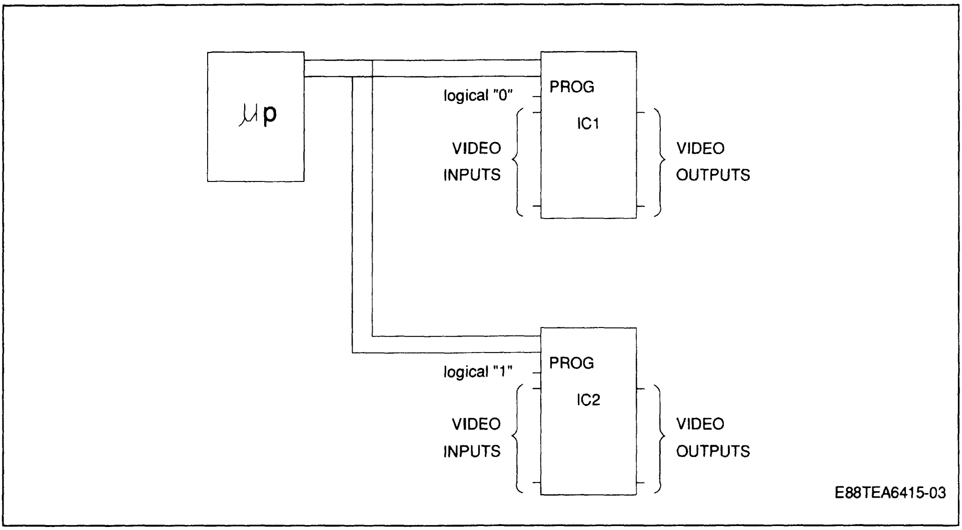
Example : 00100 101 connect pin 10 (input) to pin 14 (output).
(Equals 25 in hexadecimal).

Adress byte (1st byte of transmission)

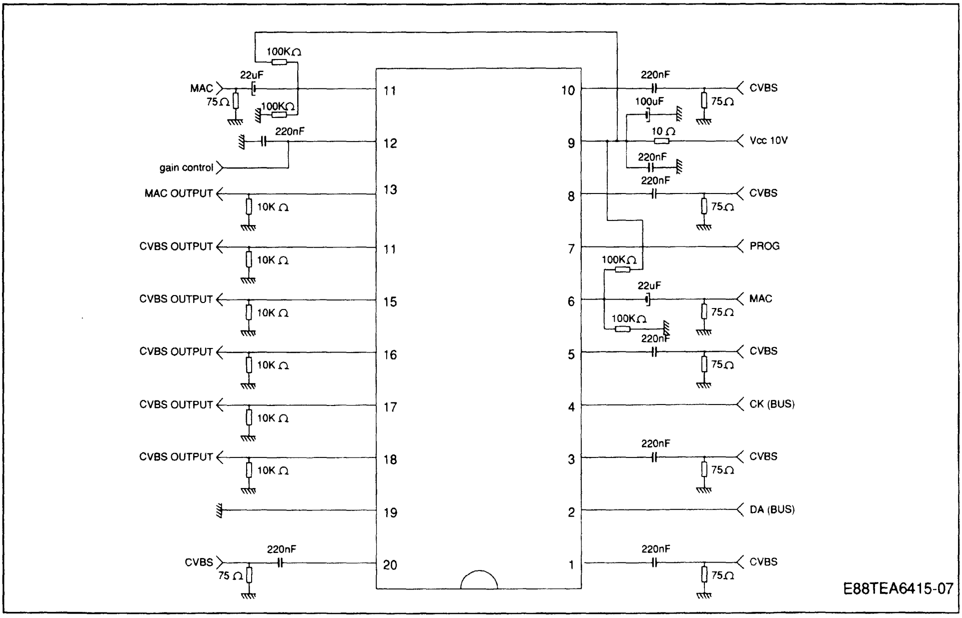
86	1000	0110	when pin PROG is connected to V_{CC}
06	0000	0110	when pin PROG is connected to GROUND

USE WITH ANOTHER TEA6415

The programmation input (PROG) permits to operate with two TEA6415 in parallel and to select them indepently through the S–Bus without modifying the address byte. Consequently, the switch capabilities are doubled or IC1 and IC2 can be cascaded.



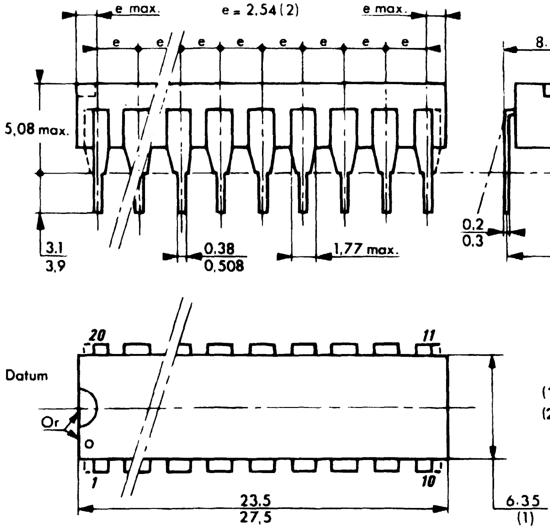
TYPICAL APPLICATION



Note : When any input is not used, it must be bypassed to ground through a 220nF capacitor, so as to avoid degrading the crosstalk.

PACKAGE MECHANICAL DATA

20 PINS - Plastic Dip



(1) Nominal dimension
(2) True geometrical positior

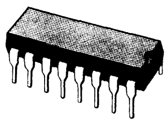
20 Pins

SGS-THOMSON MICROELECTRONICS

TEA7105

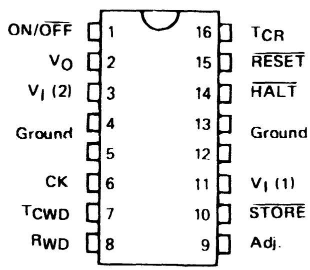
VOLTAGE REGULATOR FOR CMOS MICROPROCESSOR BASED SYSTEMS

- OUTPUT CURRENT : 100 mA
- ON-CHIP CURRENT LIMIT AND THERMAL PROTECTION
- $\overline{RESET}$ GENERATOR WITH EXTERNALLY ADJUSTABLE DELAY
- REGULATOR INPUT VOLTAGE LEVEL DETECTION SYSTEM (level adjusted externally)
- WATCH DOG TIMER
- INPUT VOLTAGE FAILURE DETECTION SYSTEM DELIVERS A $\overline{STORE}$ SIGNAL IN CASE OF INPUT VOLTAGE DISCONTINUITY
- REGULATOR ON/$\overline{OFF}$ CONTROL SIGNAL ALSO SETS THE OUTPUT TO HIGH IMPEDANCE STATE



TEA7105
BATWING DIP-16
(Plastic Package)

PIN CONNECTIONS



E88TEA7105-01

DESCRIPTION

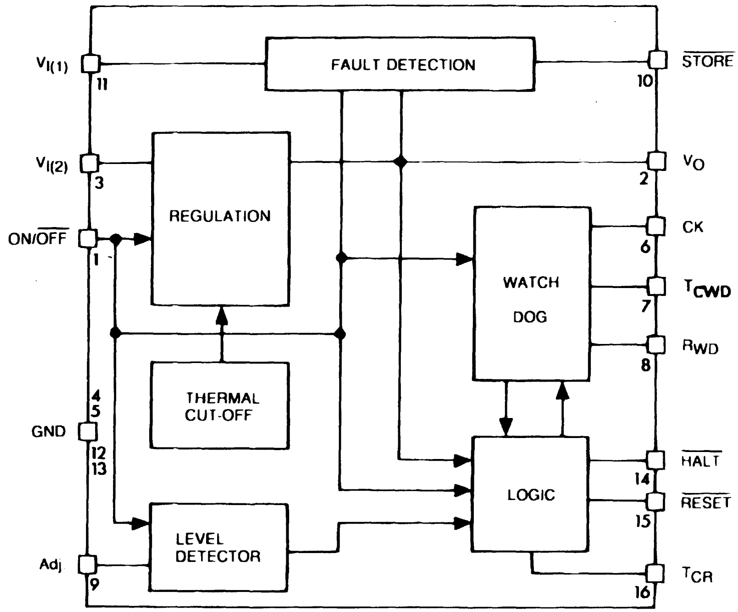
The TEA7105 is a voltage regulator especially suited to all microprocessor-based digital systems. Upon initial power on, the circuit delivers a RESET signal with programmable delay. This signal is disabled under three conditions :

- When supply voltage falls below a certain threshold level adjusted externally
- When output voltage falls below a preset level
- In the absence of trigger pulses on WATCH DOG input

The regulator features a WATCH DOG function with timing requirements met by a wide range of frequencies. The device detects the occurance of input voltage DROP and delivers a $\overline{STORE}$ signal whitebeing powered by the energy stored in the input capacitor.

An ON/$\overline{OFF}$ function is provided enabling the circuit to be put in standby mode and also to set the regulated output to high impedance state. In this mode, the power consumption is extremely low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{I(1)}$. $V_{I(2)}$	Supply Voltage	+ 40	V
	CK Input Voltage	– 0.3 to V_O	V
	ON/$\overline{\text{OFF}}$ Input Voltage	– 0.3 to $V_{I(2)}$	V
	Adj. Pin Input Voltage	– 0.3 to $V_{I(2)}$	V
P_{tot}	Power Dissipation	Internally Limited	–
T_{oper}	Operating Ambient Temperature Range	– 40 to + 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

THERMAL DATA

$R_{th\ (j\text{-}a)}$	Maximum Junction-ambient Thermal Resistance	45	°C/W
$R_{th\ (j\text{-}c)}$	Maximum Junction-case Thermal Resistance	11	°C/W

$R_{th(j\text{-}a)}$ is measured on packages soldered on a printed circuit board with a copper area of 20 cm^2.

ELECTRICAL CHARACTERISTICS T_{amb} = + 25 °C, $V_{I(1)} = V_{I(2)}$ = + 12 V
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOLTAGE REGULATOR					
V_O	Output Voltage (+ 7 V ≤ V_I ≤ + 36 V, 1 ≤ I_O ≤ 100 mA)	4.85	–	5.15	V
K_{VI}	Line Regulation (+ 7 V ≤ V_I ≤ + 36 V, I_O = 50 mA)	–	30	100	mV
K_{VO}	Load Regulation (V_I = + 10 V, 5 mA < I_O < 100 mA)	–	10	75	mV
I_{SC}	Short-circuit Current (V_I = + 10 V, 0 ≤ V_O ≤ + 5 V)	–	200	–	mA
$\overline{RESET}$ FUNCTION					
	Minimum Output Voltage to Activate $\overline{RESET}$	4.5	–	4.8	V
	Output Voltage Hysteresis to Disable $\overline{RESET}$	–	50	–	mV
$V_{(ref)}$	Internal Reference for the Adj. Detection	–	2.5	–	V
$I_{(adj)}$	Maximum Adj. Pin Current ($V_{(adj)}$ = 0 V)	–	–	1	µA
$V_{L(\overline{reset})}$	Low Level $\overline{RESET}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{reset})}$	High Level $\overline{RESET}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
CK AND ON/$\overline{OFF}$ INPUTS					
V_{IL}	Maximum Low Level Input Voltage	–	–	0.8	V
I_{IL}	Maximum Low Level Input Current (V_{IL} = 0 V)	– 120	– 60	–	µA
V_{IH}	Minimum High Level Input Voltage	2.4	–	–	V
I_{IH}	Maximum High Level Input Current (V_{IH} = + 2.4 V)	–	–	100	µA
ALARM /$\overline{STORE}$ FUNCTION					
$V_{H(min)}$	Minimum Input Voltage to Activate $\overline{STORE}$ Signal	5	5.7	6.4	V
$V_{L(\overline{store})}$	Low Level $\overline{STORE}$ Output (I_O = 2 mA)	–	–	0.4	V
$V_{H(\overline{store})}$	High Level $\overline{STORE}$ Output (I_{OH} = – 100 µA)	V_O – 1	–	V_O	V
ON/$\overline{OFF}$ FUNCTION					
$I_{(sb)}$	Standby Current $V_{(ON/\overline{OFF})}$ = 2.4 V $V_{(ON/\overline{OFF})}$ = 0 V	 – –	 4 0.5	 8 –	mA
$I_{O(dis)}$	V_O Pin Discharge Current ($V_{ON/\overline{OFF}}$ = 0, V_O = + 5 V)	–	–	2	µA

ELECTRICAL CHARACTERISTICS (continued)

TIMING (see timing diagrams)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	CWD	–	–	33	nF
	C_R	–	–	220	nF
t_{init}	t_{init} (C_R = 100 nF) Note 1	–	30	–	ms
t_d	t_d (CWD = 33 nF) Note 2	–	7	–	ms
t_{reset}	t_{reset} (CWD = 33 nF, C_R = 100 nF) Note 3	–	6	–	ms
t_{cycle}	t_{cycle} (CWD = 33 nF, C_R = 100 nF) Note 4	–	13	–	ms
T_{CK}	Pulse Width at Input CK	20	–	t_d	µs

Notes : 1. This is the period at the end of which $\overline{\text{RESET}}$ signal appears after V_{OUT} rises up and when switch S1 has been closed, this is given by the following relationship.
$t_{init} = 0.3 \cdot CR \cdot 10^6$.
2. This is the maximal clock period determined by the value of CWD.
$t_d = \frac{2.7}{11.6} \cdot CWD \cdot 10^6$.
3. This is the time required for micorcomputer reinitialisation.
$t_{reset} = \frac{1}{11.6} \cdot CWD \cdot 10^6 + \frac{5}{125} \cdot CR \cdot 10^6$.
4. This is the time required by the microcomputer during a restart to generate at least one clock pulse.
$t_{cycle} = t_d + t_{reset}$.

Remark : For more important clock period see specifiic application figure 10.

PIN DESCRIPTION

$V_{I(1)}$

Input connected directly to power supply to detect any supply failure.

$V_{I(2)}$

Regulator's power input. This input is separated from power supply through a diode.

A decoupling capacitor is connected to this input.

An inadequate supply voltage level is detected at this input.

Adj

In order to detect the level of $V_{I(2)}$ a resistance inserted between Adj pin and $V_{I(2)}$ and another between Adj pin and GND are necessary.

ON/$\overline{\text{OFF}}$

Logic input. A logic 1 applied to this input will cause the TEA7105 to become fully operational ; whereas a logic O will set the circuit to standby mode.

V_O

Powercutput to microprocessor and digital systems.

Two different output voltage levels are detected according to whether the transition is from low voltage to high voltage or the inverse (Refer to timing diagram - figure 4).

High impedance output when the circuit is in standby mode.

T_{CR}

Combination of a grounded capacitor and the internal current generator will implement the $\overline{\text{RESET}}$ signal delay upon the initial power on.

T_{CWD}

A relaxation oscillator is implemented by combining a grounded capacitor and the internal current generator

R_{WD}

A resistance inserted between this pin and ground will cause the flow of additional charging current to capacitor C_{WD} thereby modifying the slope of the local oscillator and improving the choice of C_{WD} values.

C_K

This is the WATCH DOG function input. The clock signal resets the ramp of the relaxation oscillator. The circuit is triggerred on rising edge of the clock.

$\overline{RESET}$

During the initialization, TEA7105 detects at the output V_O a voltage level V_{C1} and generates a $\overline{RESET}$ signal (see timing diagrams - figure 5).

The following three conditions cause $\overline{RESET}$ signal to be forced to zero level :

- If the output voltage level falls below V_{C1} by a hysteresis of ΔV_{C1} (see timing diagrams - figure 5).
- If no signal arrives at input CK for a minimal period to 20 µs and maximal period equal to td (see timing diagrams - figure 6).
- If the input voltage falls below the adjustable threshold level (see timing diagrams - figure 4).

$\overline{HALT}$

Fonction and electrical characteristics are the same as the $\overline{RESET}$ pin.

$\overline{STORE}$

If input voltage $V_{I(1)}$ falls below V_{C2} level, TEA7105 will use the energy stored in the input capacitor to generate the $\overline{STORE}$ signal for the microprocessor data protection (see timing diagrams - figure 4).

Figure 1 : Maximum Power Dissipation Versus Junction-ambient Temperature.

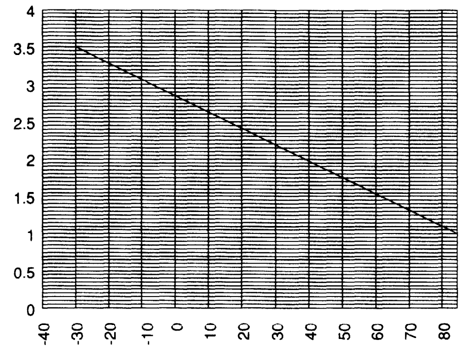
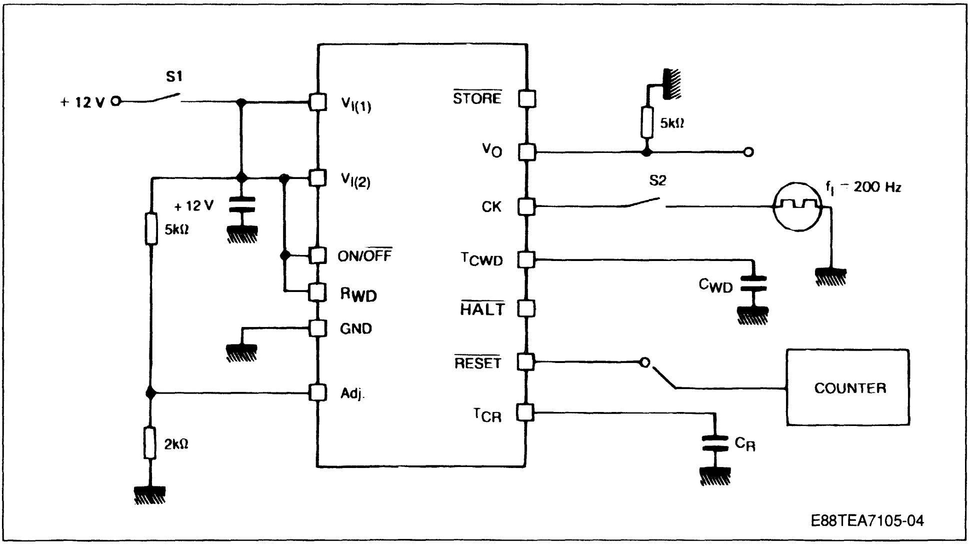


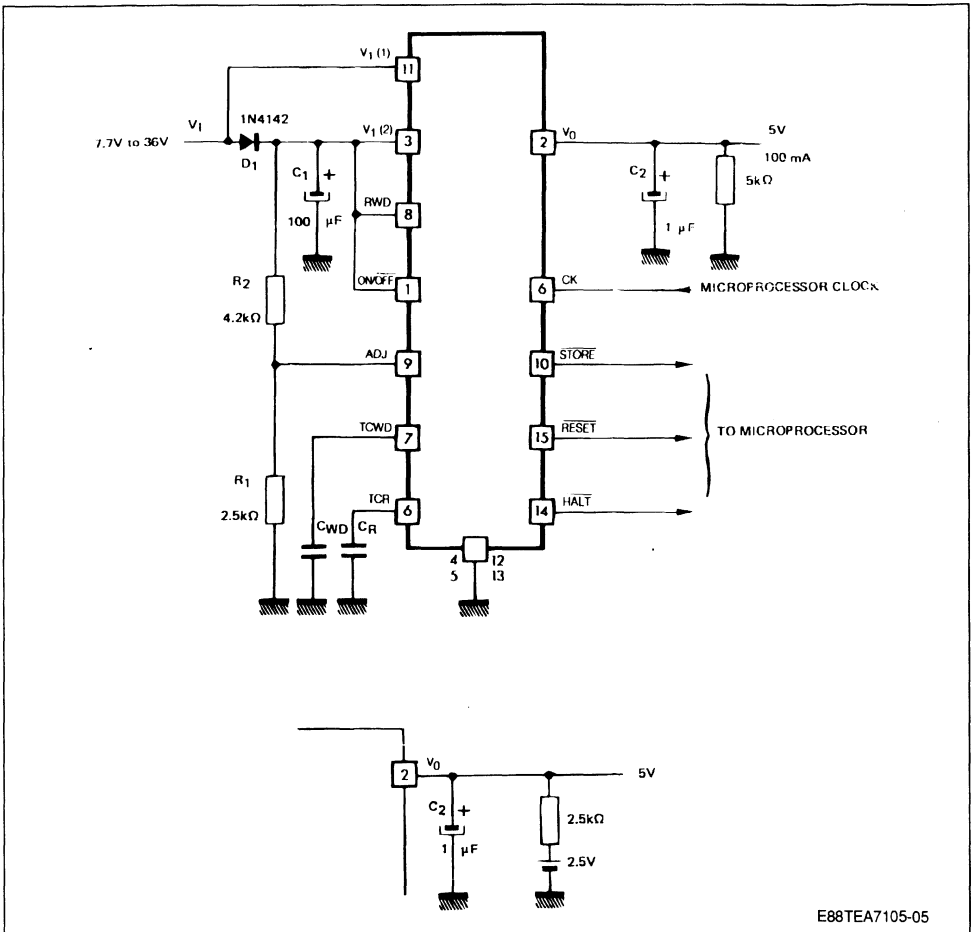
Figure 2 : Test Circuit.



TYPICAL APPLICATION

A minimum current of 1 mA should be delivered by the TEA7105 for effective voltage control. This is why a 5 KΩ resistor (or an equivalent load if a backup battery is used) shall be connected between V_O and the ground.

Figure 3 : Typical Application.



OPERATING PRINCIPLE (see block diagram)

Output V_O(+ 5 V) is supplied by voltage V_I(2) (7 to 36 V).

Input V_I(1) may be used to detect input voltage drop and to generate a STORE signal.

Warning signals $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ are generated when :

- the circuit is being powered, for a time t_{init},
- the level detector detects insufficient voltage across power supply V_I(2),
- voltage V_O drops below a given threshold,
- the watch dog detects that pulses are no more generated by the microcomputer when running a program.

The thermal protection device may produce a high impedance at the voltage regulator output.

The impedance of the complete circuit becomes high when $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V or by acting on the ON/OFF input.

External capacitors allow inputs t_{CWD} and t_{CR} to define the t_{init}, t_{reset}, t_{cycle}, td times (figures 5 and 7) which are characteristic of the $\overline{HALT}$ and $\overline{RESET}$ signals.

It's possible to inhibit the watch dog function by grounding the pin 7 (CWD).

If store function is not used the diode D1 is not accessary.

WHEN POWERING (figures 4,5,6)

Outputs $\overline{HALT}$ and $\overline{RESET}$ are (at logic level O) during a time t_{init} following voltage V_O build up, which is used for microcomputer initialization.

t_{init} (ms) = 0.3 CR (nF).

WHEN NO INPUT VOLTAGE IS PRESENT (figure 4)

The TEA7105 regulates the power supply voltage $V_I(1)$. As soon as it drops below $V_I(2)$ diode D1 is blocked. The energy is delivered by capacitor C1 to supply the internal logics of the circuit and the microcomputer.

If $V_I(1)$ drops below a fixed threshold, 5 V < V threshold < 6.4 V, a $\overline{STORE}$ signal is generated to indicate to the supplied system to save the required data.

If $V_I(2)$ drops below an externally programmed threshold (7 V < V threshold < 36 V).

$V_{threshold} = (2.5\ (R1 + R2)/R1) + V_d$.

Outputs $\overline{HALT}$ and $\overline{RESET}$ switch to logic state 0.

If $V_I(2)$ drops below a fixed threshold, 4.5 V < V threshold < 4.8 V, the circuit impedance reaches a high value.

WHEN THE OUTPUT VOLTAGE DROPS (figure 4)

When voltage V_O drops below a fixed threshold, 4.5 V < $V_{threshold}$ < 4.8 V outputs $\overline{HALT}$ and $\overline{RESET}$ switch to logic state 0.

WHEN NO CLOCK SIGNAL IS PRESENT (figure 6)

The microcomputer when in operation will generate a clock signal whose period t will be between t min = 20 µs and t max = td

When this signal is not generated, or if the clock period is larger than td, this means that the microcomputer does not operate correctly.

The TEA7105 thus generates the $\overline{HALT}$ and $\overline{RESET}$ signals after a time td from the last rising edge.

In this case signals HALT and RESET are activated periodically, t reset and t cycle being fixed by capacitors Cr and CWD.

td may be adjusted by a resistor RWD connected between pin 8 and the ground (figure 9).

In normal condition the maximal clock period is to 7 ms.

It's possible to increase this value in adding some external components (figure 10).

INCREASE OF THE OUTPUT CURRENT (figure 7)

The TEA7105 can deliver a 100 mA current which can be increased by using an external transistor, which maintains the circuit characteristics. The setup illustrated in figure 10 an used in our laboratory circuit gives a 7 mV output variation for a load current varying from 0 to 1A. In this case $V_{threshold} \approx V_S + 3\ V_D + R_S.I_S$. The maximum value of power supply voltage is determined by $V_{min} \approx V_S + 3\ V_D + R_S.I_S$.

OPERATION

For small currents the V_{BE} voltage is lower than 0.6 V ; the transistor is blocked, only the regulator delivers current.

When V_{BE} reaches 0.6 V ($I = V_{BE}/R_b = 0.6/33 = 20$ mA) the transistor starts conduction. The transistor current gain is high enough to provide a very small current drift of the controller with respect to the load, which improves voltage control.

When short-circuited the current is limited by resistor R_S.

$I_{SC} = (V_I - 2.V_d - V_{sat})\ R_S$

CONCLUSION

The TEA7105 is a new generation voltage regulator giving a simple answer to microcomputer power supply problems.

It prevents untimely interruption of microcomputers and makes it possible to return to current program without any trouble.

This regulator may be used in its original version to power a microcomputer or any system with a maximum current requirement of 100 mA. A current extension is available for more powerful systems.

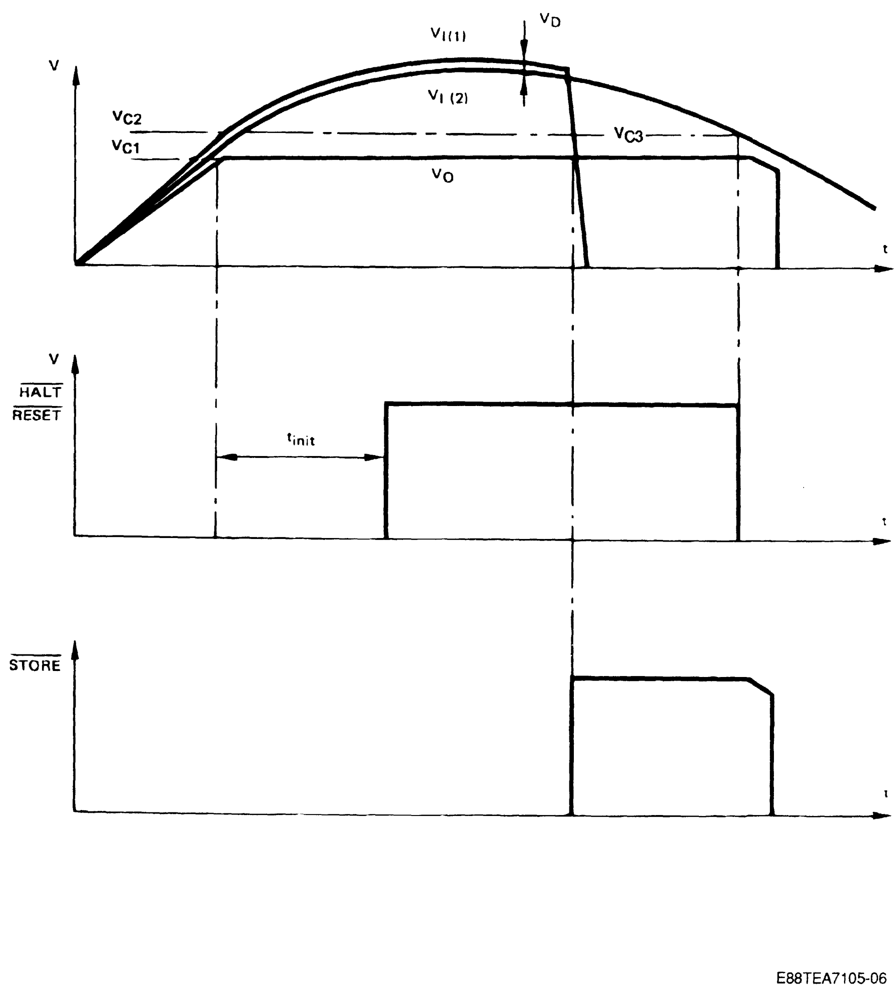
The TEA7105 provides a simple, reliable, economical and high performance power supply.

When V_I (1) becomes lower than a fixed threshold 5V < VC3 < 6.4 the $\overline{STORE}$ output switches to logic state 1. This threshold may be modified by using an external potential divider.

When V_I (2) becomes lower than an externally adjustable threshold signals $\overline{HALT}$ and $\overline{RESET}$ switch to logic state O (V_{C2} = 2.5 (R1 + R2) / R1).

When V_I (2) becomes lower than a fixed threshold 4.5 V < V threshold < 5.5 V the circuit impedance becomes high.

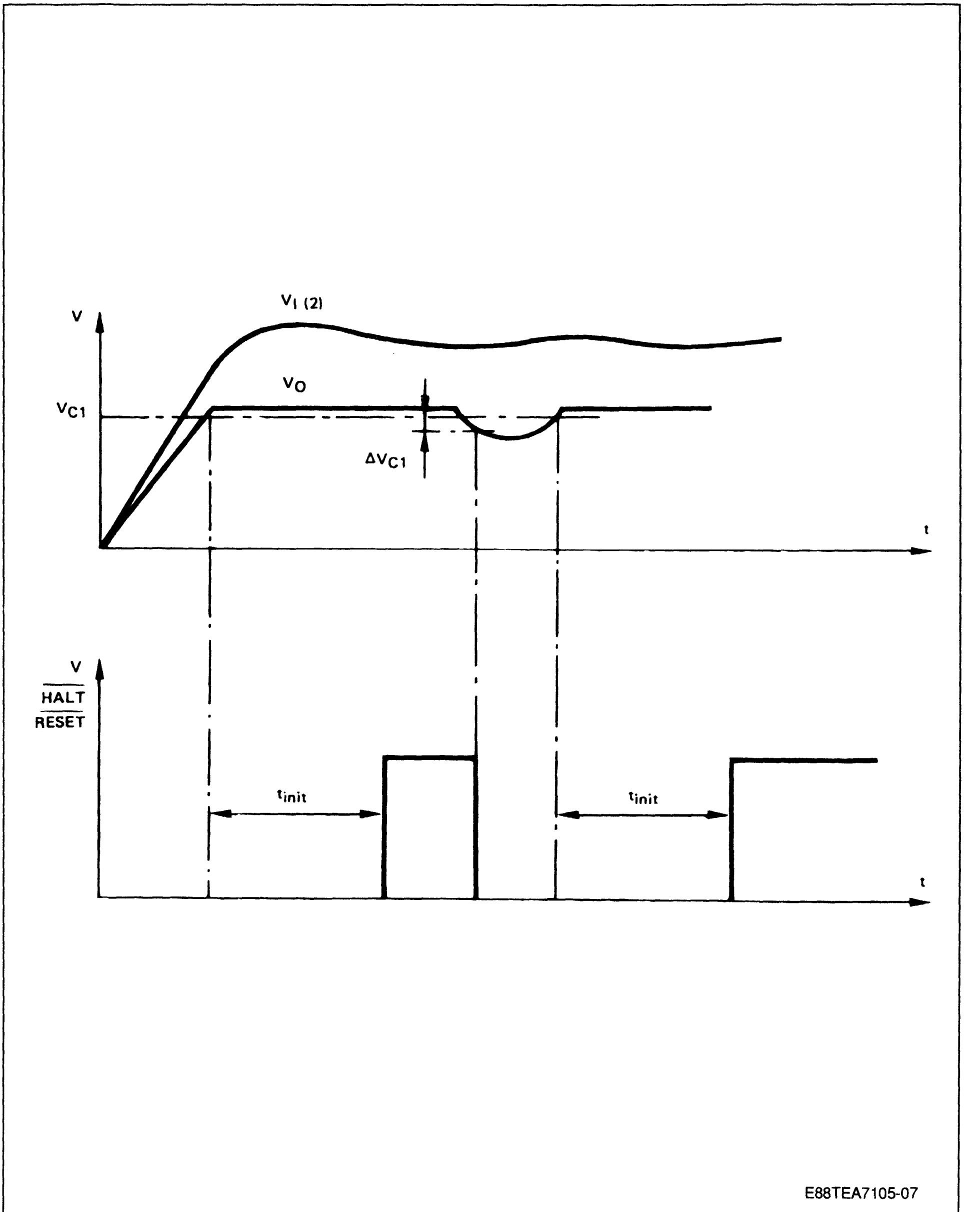
Figure 4 : Detection of Input Voltage Drop.



When the output voltage becomes lower than V threshold (4.5 < threshold < 4.8 V) the warning signals $\overline{HALT}$ and $\overline{RESET}$ switch to logic state O.

These signals become active as soon as V_O reaches the threshold to reinitialize and block the microcomputer during t_{init}.

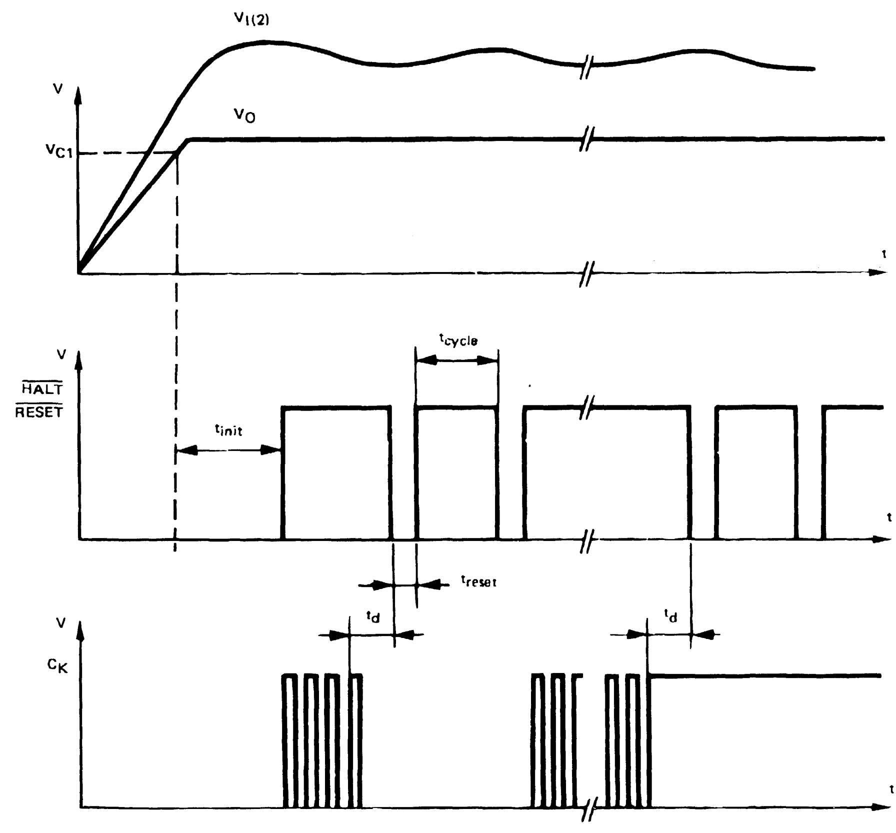
Figure 5 : Detection of Output Voltage Drop.



Signals $\overline{HALT}$ and $\overline{RESET}$ become active after a time t_d from the last clock signal rising edge.

t_d and t_{reset} depend on capacitors C_{WD} and C_R, preset curves are given in figure 8.

Figure 6 : Interruption of Clock Pulses.

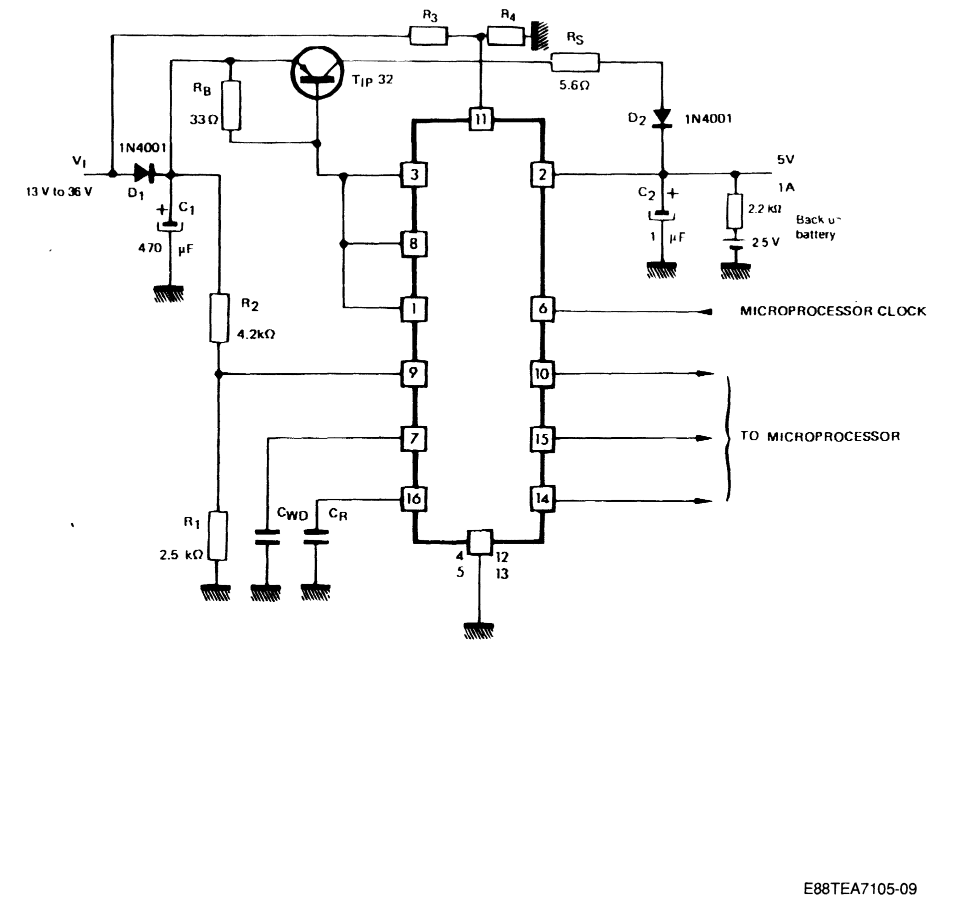


E88TEA7105-08

This application is used to deliver a 1 A current with excellent voltage control. The D2 diode avoids the discharge of the back up battery in the TEA7105 when it' s in hight impedance output in stand by mode.

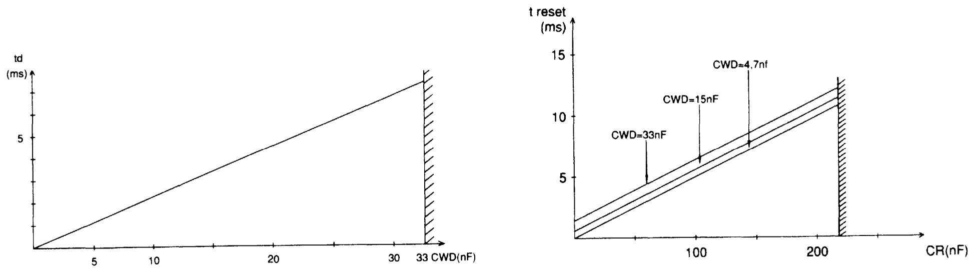
The value of $V_{I(1)}$ activing $\overline{STORE}$ signal is determined by ($V_{I(1)}$ store = (5.7 (R3 + R4)/ R4).

Figure 7 : Current Extension.



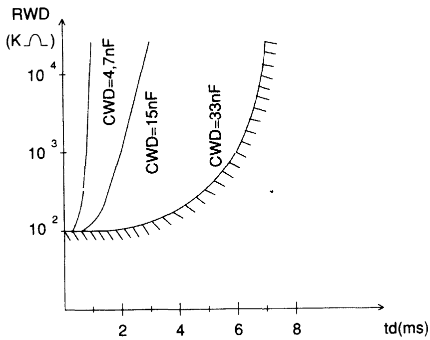
We see that C_r and C_{WD} actions are not fully independent. It is possible to adjust td more finely by using an external resistor connected between pin R_{WD} and the ground (figure 9).

Figure 8 : Determination of t_d and t_{reset} in relation to C_{WD} and C_R.



E88TEA7105-10

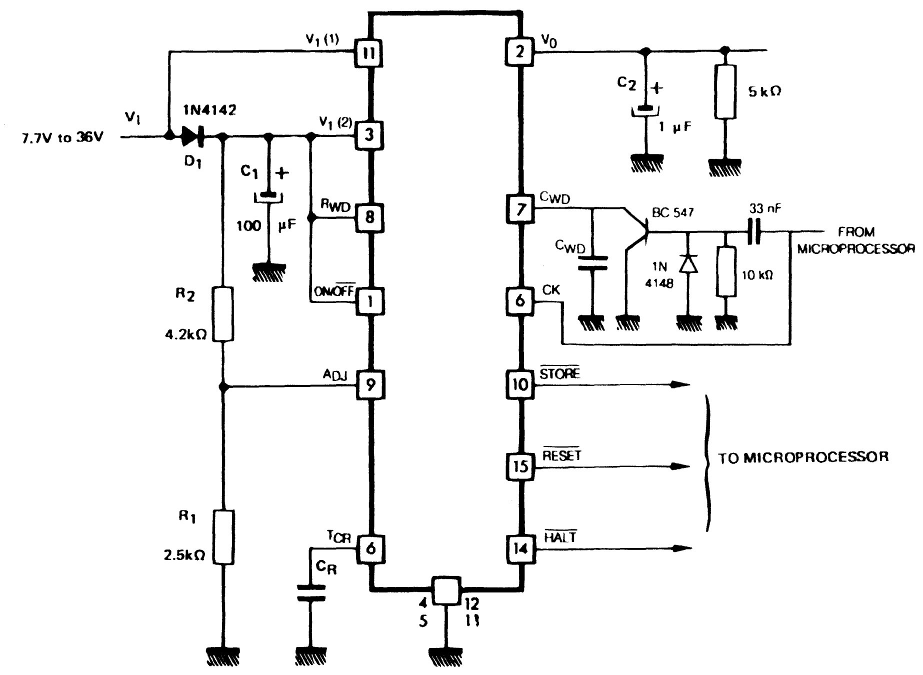
Figure 9 : Determination of t_{CK} max = t_d in relation to R_{WD} and C_{WD}.



E88TEA7105-11

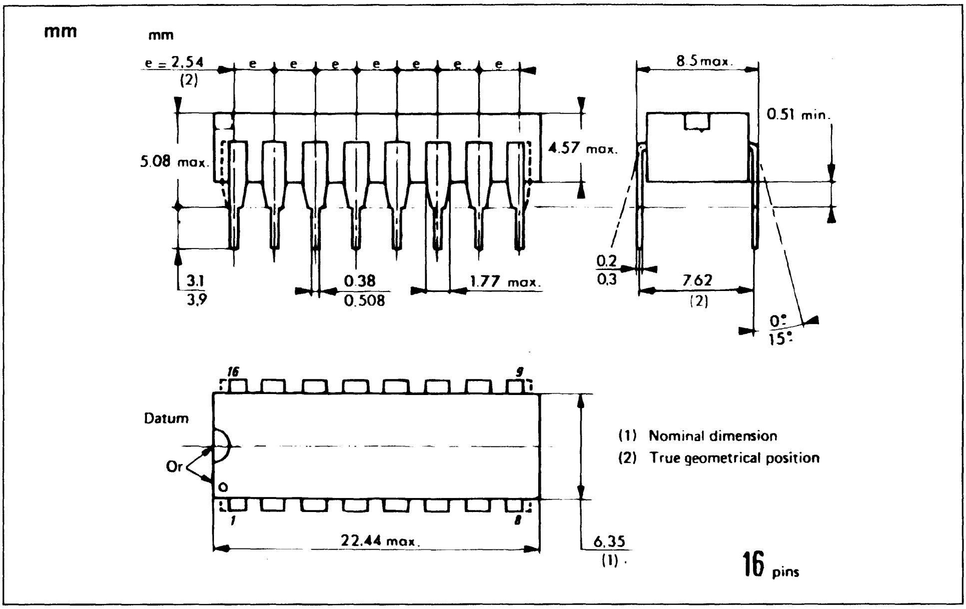
For applications using very long clock period it's possible to use an external transistor. In this case the maximal clock period, in relation to C_{WD}, may be longer than 500 ms. The relationship to define t_{init}, t_d, t_{reset} are same that in typical application.

Figure 10 : Very Long Clock Period.



PACKAGE MECHANICAL DATA

16 PINS – PLASTIC DIP

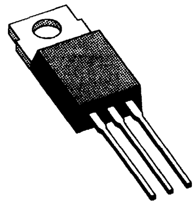


SGS-THOMSON MICROELECTRONICS

TEA7605

LOW-DROP VOLTAGE REGULATOR

- $V_O = 5\ V \pm 4\ \%$ ($I_O = 5\ mA$)
- $I_{OS} \geq 500\ mA$
- $V_I - V_O \leq 0.6\ V$ ($I_O = 500\ mA$)
- V_I (surge) = ± 80 V
- THERMAL AND SHORT-CIRCUIT PROTECTION



TEA7605 SP
TO220
(Plastic Package)

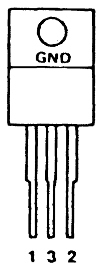
DESCRIPTION

TEA7605 is a low-drop 5 V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible quiescent current (250 µA).
- Lowest possible output capacitor (1 µF).

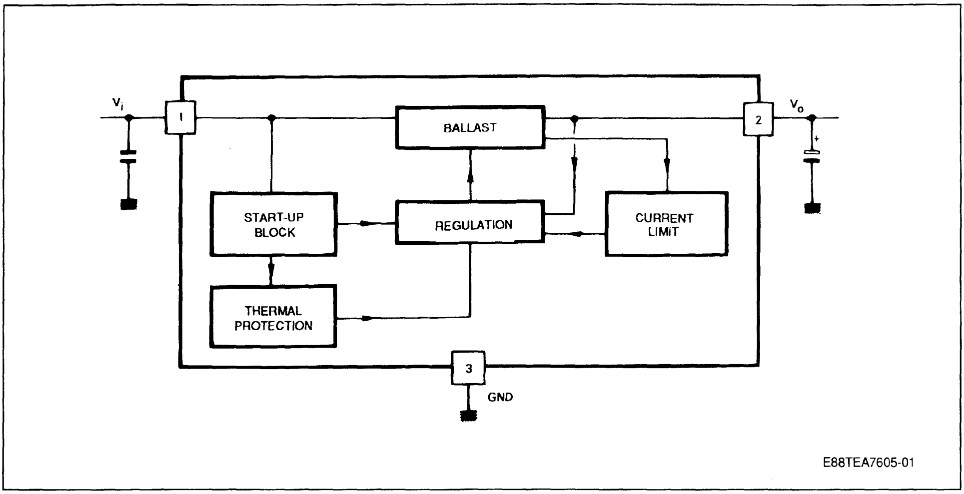
PIN CONNECTIONS



E88TEA7605-02

1 = V_i
2 = V_O
3 = GND

BLOCK DIAGRAM



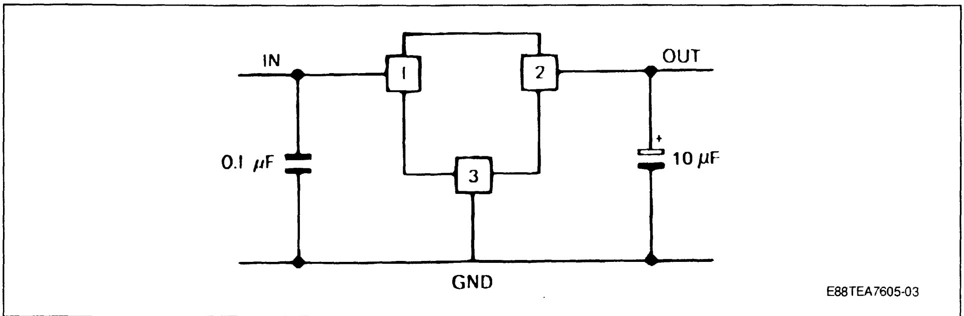
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage - Continuous - $\tau = 300$ ms	 30 80	 V V
V_i	Reverse Input Voltage - Continuous - $\tau = 120$ ms	 – 18 – 80	 V V
T_J	Operating Junction Temperature Range	– 45 to 150	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C

THERMAL DATA

$R_{th\ (j-c)}$	Junction-case Thermal Resistance	3	°C/W
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	70	°C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25 °C, V_i = 14.4 V (unless otherwise specified) Output Capacitor = 10 µF (see note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500 mA)	4.875	5	5.125	V
V_i	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_o = 0 mA I_o = 150 mA I_o = 500 mA		0.25 10 75	0.35 20 100	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26 V ; I_o = 5 mA)		5	10	mV
kV_o	Load Regulation (I_o = 5 to 500 mA)		40	60	mV
V_i - V_o	Drop-out Voltage I_o = 150 mA I_o = 500 mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350 mA, f = 120 Hz, C_o = 1 µF, V_1 = 12 ± 5 V)		60		dB
I_{os}	Short-circuit Output Current	0.5	0.7		A

NOTE : APPLICATIONS HINTS

The output capacitor has a direct influence on output voltage stability. A 10 µF capacitor will provide satisfactory results ; there is no upper limit.

If necessary, this value can be reduced down to 1 µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance, 400 mA to < 1 mA).

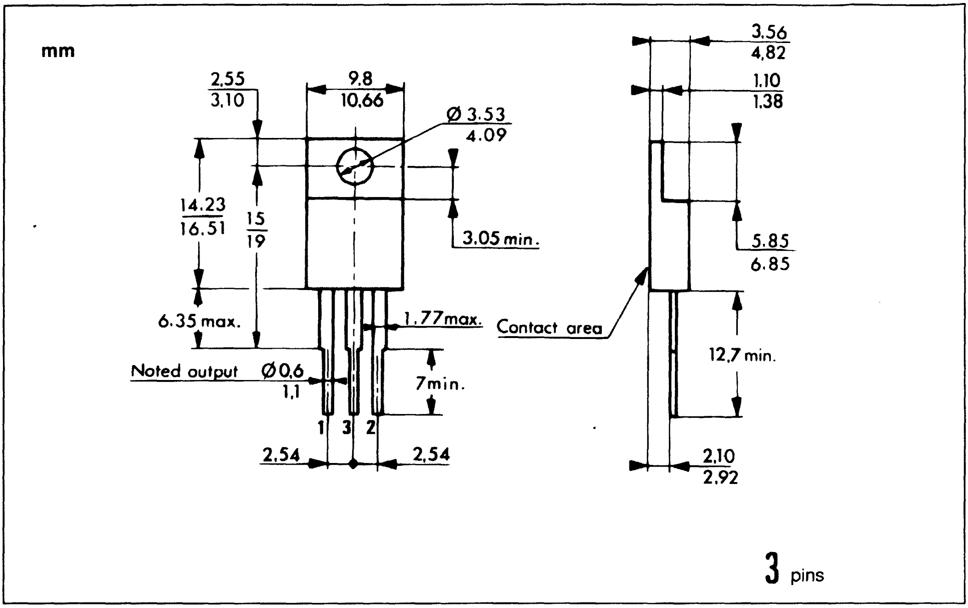
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45 °C to + 125 °C, V_i = 14 .4 V (unless otherwise specified) Output Capacitor = 10 µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500 mA)	4.8	5	5.2	V
$\frac{d_{V_o}}{d_t}$	Output Voltage Drift – 45 to 25 °C 25 to 125 °C	– 0.4 – 0.6			mV/°C
I_{CC}	Current Consumption I_o = 0 mA I_o = 150 mA I_o = 500 mA			0.4 25 120	mA mA mA
KV_i	Line Regulation (V_i = 6 to 26 V I_o = 5 mA)			20	mV
KV_o	Load Regulation (I_o = 5 to 500 mA)			80	mV
V_i - V_o	Drop-out Voltage I_o = 150 mA I_o = 500 mA		0.2 	 0.8	V V
I_{os}	Short Circuit Output Current	0.5			A

PACKAGE MECHANICAL DATA

TO220 – PLASTIC PACKAGE

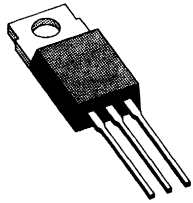


SGS-THOMSON MICROELECTRONICS

TEA7610

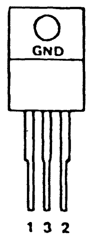
LOW-DROP VOLTAGE REGULATOR

- $V_O = 10V \pm 4\%$ ($I_O = 5mA$)
- I_O = 5 TO 500mA
- $V_i - V_O = 0.6V$ ($I_O = 500mA$)
- V_i (surge) = $\pm 80V$
- THERMAL AND SHORT CIRCUIT PROTECTION



TEA7610 SP
TO220
(Plastic Package)

PIN CONNECTIONS



1 = V_I
2 = V_O
3 = GND

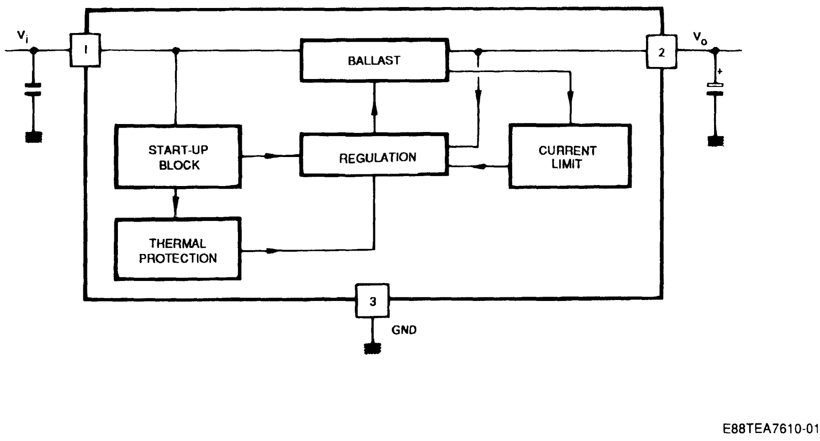
DESCRIPTION

TEA 7610 is a low-drop regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



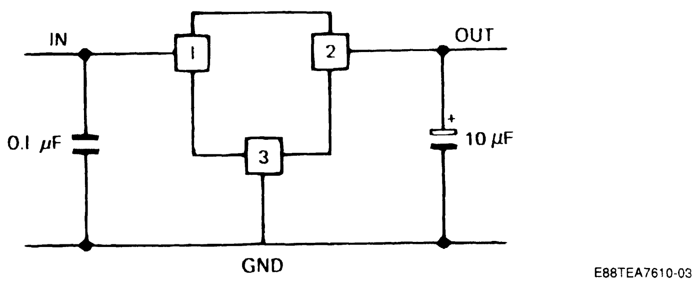
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage - Continuous - τ = 300mS	30 80	V V
V_i	Reverse Input Voltage - Continuous - τ = 120mS	– 18 – 80	V V
T_{oper}	Operating Junction Temperature	45 to 150	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

THERMAL DATA

$R_{th\ (j\text{-}c)}$ $R_{th\ (j\text{-}a)}$	Maximum Junction-case Thermal Resistance Maximum Junction-ambient Thermal Resistance	3 70	°C/W °C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_i = 14.4V (unless otherwise specified), Output Capacitor = 10µF (note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	9.7	10	10.3	V
V_i	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA		1.5 10 75	2 20 100	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)		5	20	mV
kV_o	Load Regulation (I_o = 5 to 500mA)		40	80	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350mA, f = 120Hz, C_o = 1µF, V_1 = 12 ± 5V)		60		dB
I_{os}	Short-circuit Output Current	0.5	0.7		A

NOTE : APPLICATION HINTS

The output capacitor has a direct influence on ouptut voltage stability. A 10µF capacitor will provide satisfactory results ; there is no upper limit.

If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

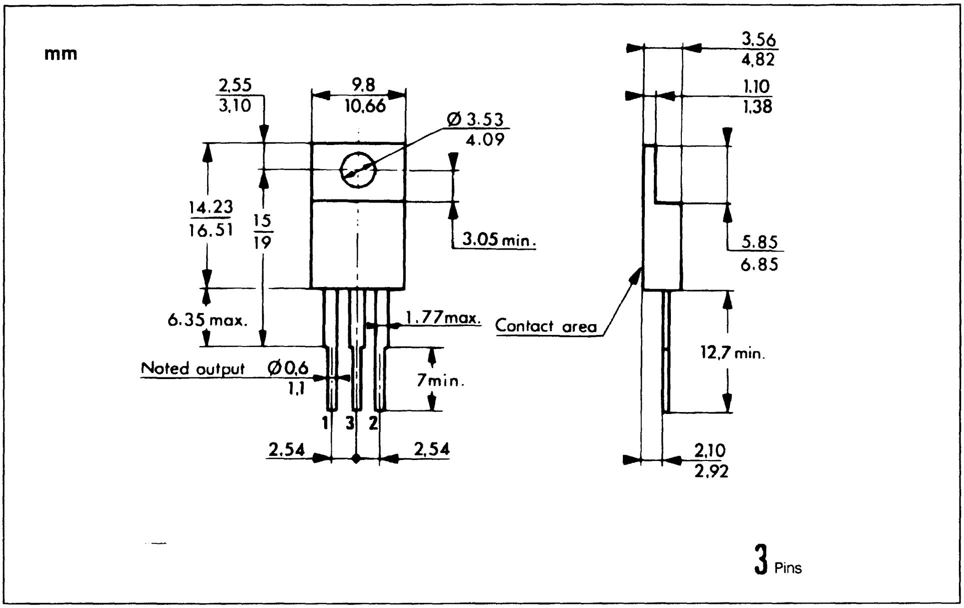
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to 125°C, V_i = 14.4V (unless otherwise specified), Output Capacitor = 10µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	9.6	10	10.4	V
$\frac{dV_o}{d_t}$	Output Voltage Drift – 45 to 25°C 25 to 125°C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA			2.5 25 120	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)			30	mV
kV_o	Load Regulation (I_o = 5 to 500mA)			100	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.20 	 0.8	V V
I_{os}	Short-circuit Output Current	0.5			A

PACKAGE MECHANICAL DATA

TO220 – PLASTIC PACKAGE

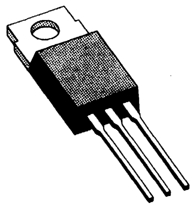


SGS-THOMSON MICROELECTRONICS

TEA7685

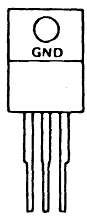
LOW-DROP VOLTAGE REGULATOR

- Vo = 8.5V ± 4% (Io = 5mA)
- Io = 5 TO 500mA
- Vi - Vo = 0.6V (Io = 500mA)
- Vi (surge) = ± 80V
- THERMAL AND SHORT CIRCUIT PROTECTION



TEA7685
TO220
(Plastic Package)

PIN CONNECTIONS



E88TEA7685-02

1 = V_I
2 = V_O
3 = GND

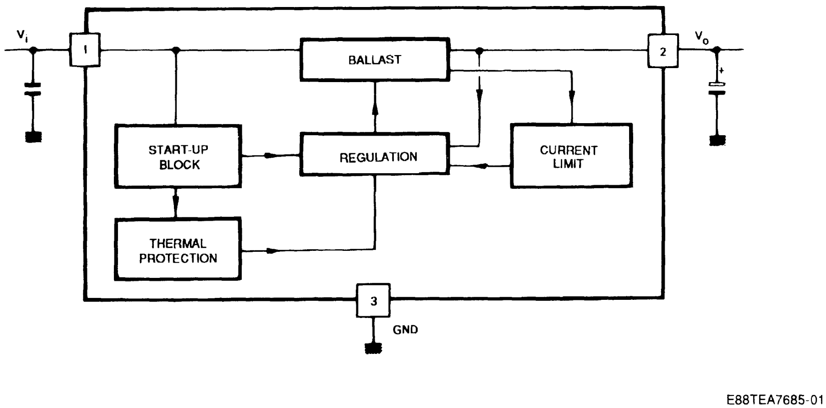
DESCRIPTION

TEA 7685 is a low-drop 8.5V regulator well suited to supplying stabilized voltage to µPs in harsh industrial environment.

Special care was taken to keep :

- Lowest possible output capacitor (1µF).

BLOCK DIAGRAM



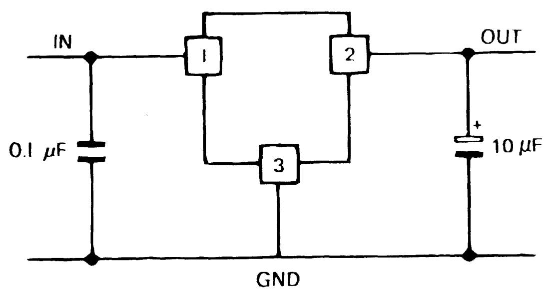
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage - Continuous - τ = 300mS	30 80	V V
V_i	Reverse Input Voltage - Continuous - τ = 120mS	– 18 – 80	V V
T_{oper}	Operating Junction Temperature	45 to + 150	°C
T_{stg}	Storage Temperature	– 55 to + 150	°C

THERMAL DATA

$R_{th(j-c)}$ $R_{th(j-a)}$	Maximum Junction-case Thermal Resistance Maximum Junction-ambient Thermal Resistance	3 70	°C/W °C/W

APPLICATION DIAGRAM



ELECTRICAL OPERATING CHARACTERISTICS

T_j = 25°C, V_i = 14.4V (unless otherwise specified) Output Capacitor = 10µF (note)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	8.26	8.5	8.74	V
V_i	Input Supply Voltage (permanent)			28	V
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA		1.5 10 75	2 20 100	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)	– 15	5	15	mV
kV_o	Load Regulation (I_o = 5 to 500mA)	– 70	– 40	70	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.18 0.4	 0.6	V V
SVRR	Supply Voltage Rejection (I_o = 350mA, f = 120Hz, C_o = 1µF, V_1 = 12 ± 5V)		60		dB
I_{os}	Short-circuit Output Current	0.5	0.7		A

NOTE : APPLICATION HINTS

The output capacitor has a direct influence on ouptut voltage stability. A 10µF capacittor will provide satisfactory results : there is no upper limit.

If necessary, this value can be reduced down to 1µF ; however, in such case, it should be checked that output capacitor keeps sufficiently high capacitance and low equivalent series resistance in the whole temperature range.

Such low capacitor value is not recommended either, if output current is to switch abruptly from very high to very low values (for instance 400mA to < 1mA).

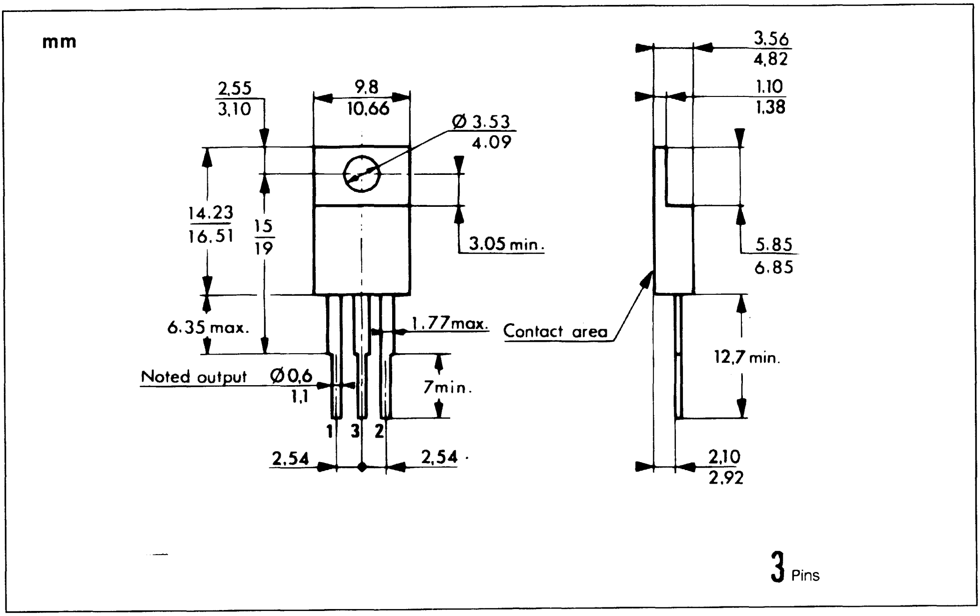
ELECTRICAL OPERATING CHARACTERISTICS

T_j = – 45°C to + 125°C, V_i = 14.4V (unless otherwise specified) Output Capacitor = 10µF

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_o	Output Voltage (I_o = 5 to 500mA)	8.16	8.5	8.84	V
$\frac{d_{Vo}}{d_t}$	Output Voltage Drift – 45 to 25°C 25 to 125°C	– 1 – 1.2		0 0	mV/°C
I_{CC}	Current Consumption I_o = 0mA I_o = 150mA I_o = 500mA			2.5 25 120	mA mA mA
kV_i	Line Regulation (V_i = 6 to 26V ; I_o = 5mA)	– 25		25	mV
kV_o	Load Regulation (I_o = 5 to 500mA)	– 90		90	mV
V_i - V_o	Drop-out Voltage I_o = 150mA I_o = 500mA		0.20	 0.8	V V
I_{os}	Short-circuit Output Current	0.5			A

PACKAGE MECHANICAL DATA

TO220 – PLASTIC PACKAGE



SGS-THOMSON MICROELECTRONICS

UAA4000

REMOTE CONTROL TRANSMITTER

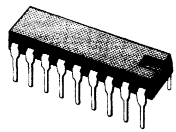
- ULTRASONIC OR INFRA-RED TRANSMISSION
- DIRECT DRIVE FOR ULTRASONIC TRANSDUCER
- DIRECT DRIVE OF VISIBLE LED WHEN USING INFRA-RED
- VERY LOW POWER REQUIREMENTS
- PULSE POSITION MODULATION GIVES EXCELLENT IMMUNITY FROM NOISE AND MULTIPATH REFLECTIONS
- SINGLE POLE KEY MATRIX
- SWITCH RESISTANCE UP TO 1 KΩ TOLERATED
- FEW EXTERNAL COMPONENTS
- ANTI-BOUNCE CIRCUITRY ON CHIP

QUICK REFERENCE DATA

- POWER SUPPLY : 9 V, STANDBY 6 µA, OPERATING 8 mA
- MODULATION : PULSE POSITION WITH OR WITHOUT CARRIER
- CODING : 5 BITS WORD GIVING A PRIMARY COMMAND SET OF 32 COMMANDS
- KEY ENTRY : 8 x 4 SINGLE POLE KEY MATRIX
- DATE RATE : SELECTABLE 1 BIT/SEC TO 10 K BIT/SEC
- CARRIER FREQUENCY : SELECTABLE 0 HZ (no carrier) TO 200 KHz

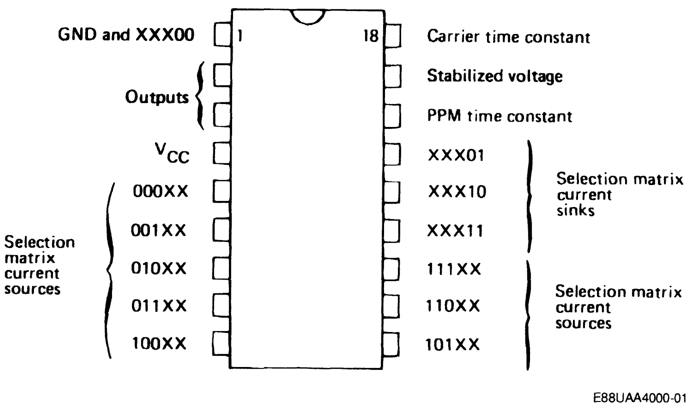
DESCRIPTION

The UAA4000 is an easily expandable, 32 command, pulse position modulation transmitter drawing zero standby current.

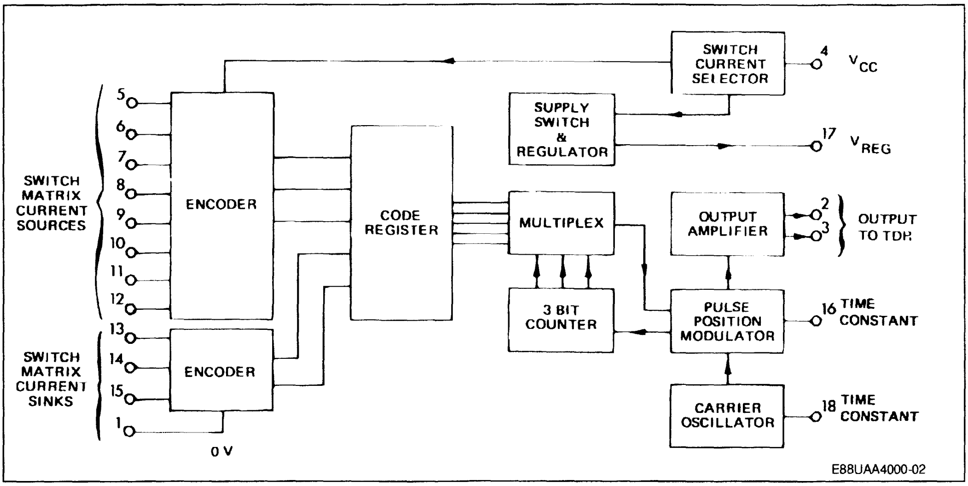


UAA4000
DIP18
(Plastic Package)

PIN CONNECTIONS



BLOCK DIAGRAM



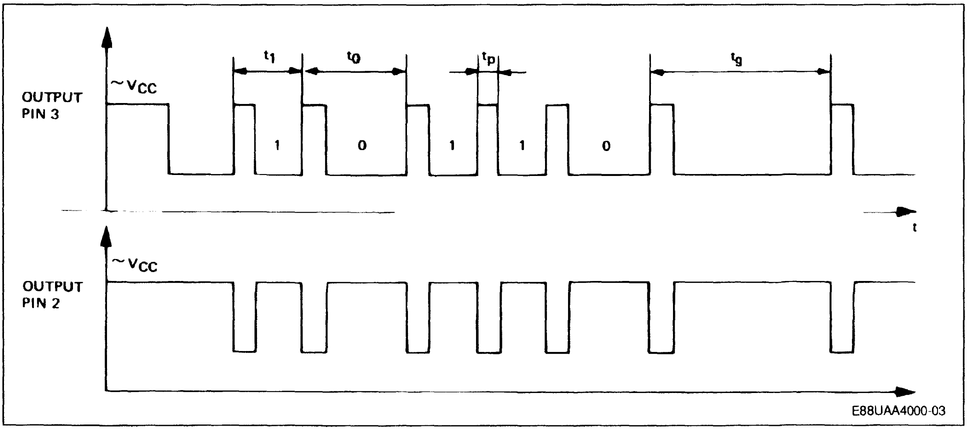
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Pin 4	11	V
P_{tot}	Maximum Power Dissipation	600	mW
I_C	Maximum Output Current Pin 3	5	mA
T_{oper}	Operating Temperature Range	– 10 to 65	°C
T_{stg}	Storage Temperature Range	– 55 to 125	°C

THERMAL DATA

R_{th}(j–a)	Junction–ambient Thermal Resistance	70	°C/W

OUTPUT WAVEFORMS (PPM word notation).

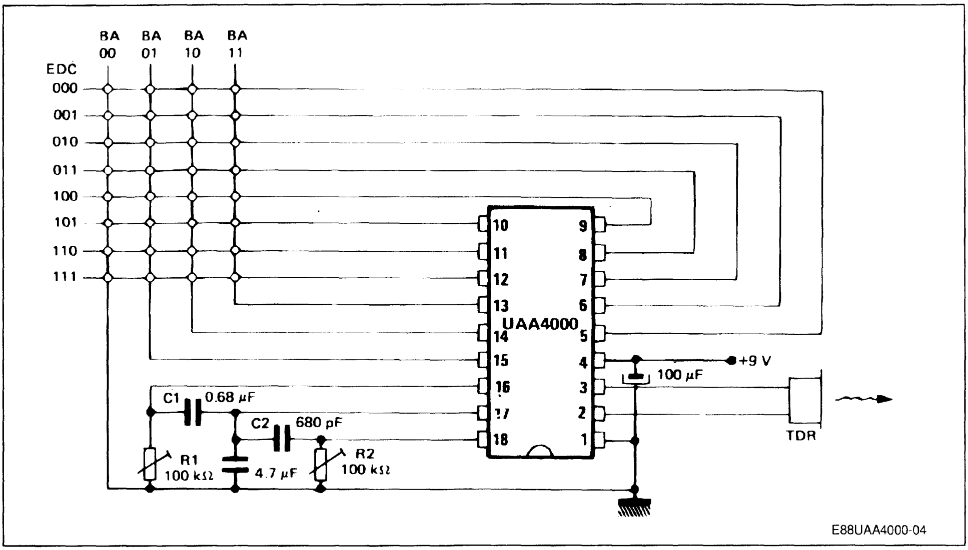


ELECTRICAL CHARACTERISTICS (see test circuit next page)
T_{amb} = 25 °C, V_{CC} = 9 V, f_o = 40 kHz, t_1 = 18 ms
4.7 µF Capacitor on Pin 17 (unless otherwise specified)

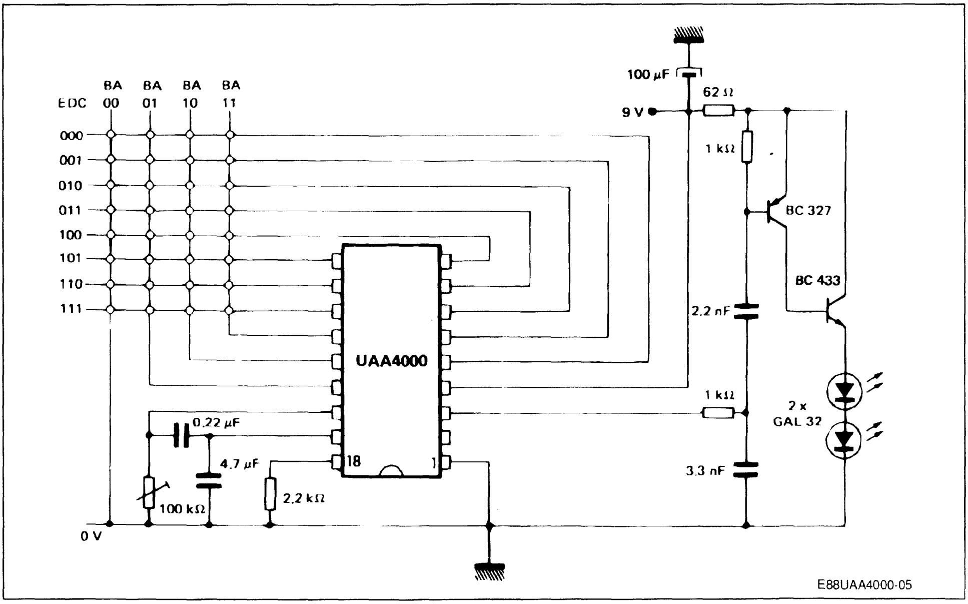
Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage	Pin 4	7	9	11	V
	Operating Supply Current	Pin 4		8	16	mA
	Standby Supply Current	Pin 4			30	µA
	Stabilized Voltage	Pin 17	3.9	4.2	4.5	V
	Output Current Available	Pin 17			1	mA
	Output Voltage Swing (unloaded)	Pins 2, 3		8	V_{CC}	V
	Output Current (peak value)	Pins 2, 3			5	mA
	External Switch Resistance				1	kΩ
	External Switch Closing Time		6			ms
	External Carrier Oscillator (R2 required, C_2 = 680 pF)	Pin 18	20	40	80	kΩ
	External PPM Resistor (R1 required, C_1 = 0.68 µF)	Pin 16	15	30	60	kΩ
	Ratio t0/t1	Pins 2, 3	1.4	1.5	1.6	
t_p	Pulse Width	Pins 2, 3	2	3	4	ms
t_g	Inter–word Gap	Pins 2, 3	50	54	58	ms

APPLICATION CIRCUITS

TEST AND ULTRASONIC APPLICATION CIRCUIT

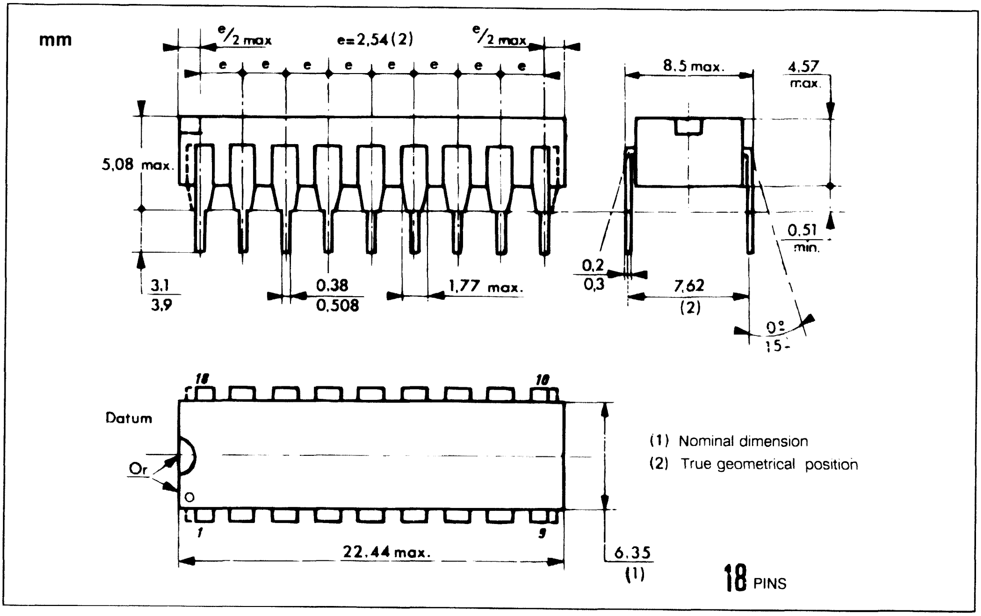


INFRA-RED APPLICATION CIRCUIT



PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP



SGS-THOMSON
MICROELECTRONICS

UAA4009

REMOTE CONTROL RECEIVER

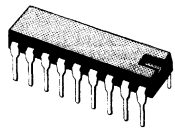
- ON-CHIP OSCILLATOR
- USED WITH IR OR ULTRASONIC TRANSMISSION SYSTEM
- 5 BITS PPM MODULATION, FIRST TRANSMITTED MUST BE ZERO
- 2 SUCCESSIVE CODEWORDS COMPARISON
- 12 CHANNELS SET EITHER BY REMOTE CONTROL OR OUTPUT PIN GROUNDING
- MUTING DURING CHANNEL CHANGE
- PRIORITY CHANNEL SET BY EXTERNAL CAPACITOR
- V_{CC} = 12 V
- I_{CC} = 15 mA
- PPM PULSES :

- CHANNEL OUTPUT : OPEN NPN COLLECTOR WITH FEED-BACK INFORMATION
- STAND-BY OUTPUT : OPEN NPN COLLECTOR
- V_{max}, OUTPUT : 35 V

DESCRIPTION

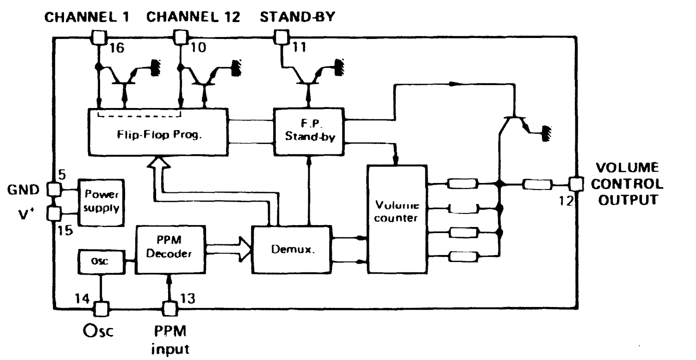
UAA4009 is an I2L/BIPOLAR circuit for use as a receiver of remote control signals for television control applications.

- This device :
- receives 15 of the 32 codes transmitted by the UAA4000 (PPM)
- commutes tuning voltage for 12 TV channels
- provides 0 to 6 V voltage (16 steps) for one electronic potentiometer
- gives "stand-by" information



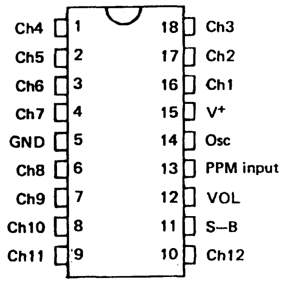
UAA4009
DIP18
(Plastic Package)

BLOCK DIAGRAM



E88UAA4009-01

PIN CONNECTIONS



GENERAL DESCRIPTION

PPM DEMODULATION

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. Frequency is linked with transmission rate.

Following numerical values are given at f = 5.1 KHz.

For example, 5.1 KHz ensures potentiometer up or down travelling to be completed in about 5.5 s and channel 1 is set in 120 ms.

Each pulse that is received starts a counter. Input is masked for first 3.5 ms. Windows from 3.5 to 7 ms and from 7 to 13 ms determine whether a 1 or a 0 is present. Periods between pulses of 13 to 25.5 ms are recognized as word intervals.

Checks are made to ensure 5 bits are received for a word to be valid ; two consecutive and identical words allow corresponding function activation, 13 ms after receiving last pulse of the 2nd word (max 109 ms after first pulse of the first word).

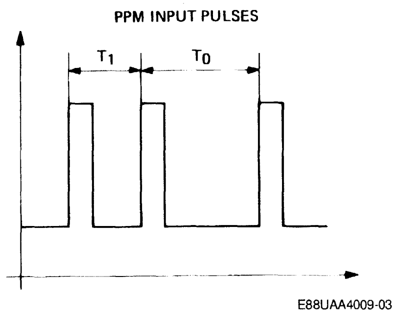
CODES

00001	Channel 1
00010	Channel 2
00011	Channel 3
00100	Channel 4
00101	Channel 5
00110	Channel 6
00111	Channel 7
01000	Channel 8
01001	Channel 9
01010	Channel 10
01011	Channel 11
01100	Channel 12
01101	Stand-by ON
01110	Volume UP
01111	Volume DOWN

NOTES : • 00001
(↑ 1st ... ↑ last to be transmitted.)

• Other codes are ignored

PPM INPUT PULSES



CHANNELS

Channel activation is achieved either by remote control, or directly by momentary grounding corresponding pin of the circuit. This allows local push-button control without external components.

OUTPUTS : an open collector transistor grounds desired pin while others are high impedance (V_{max} = 35 V). The typical current grounded is 10 mA.

STAND-BY

S – B is activated (S – B ON) only by remote control ; it is disabled by activation of any channel either by remote control or front-panel switches.

S – B ON activates muting.

OUTPUT : Open collector S – B ON : high impedance
S – B OFF : grounded

MUTING

During channel change or while S – B is on, volume is reduced to minimum by grounding external capacitor. When muting is released, volume goes back to previous value by charging capacitor with RC constant to be adjusted at desired value (R is 2 KΩ typ.).

VOLUME

A four bits binary counter drives a resistors array. It provides 0 to 6 V variation in 16 steps. Output impedance is 2 KΩ (50 Ω if muting is on).

Increment is inhibited when S – B is ON.

BEHAVIOUR AT START

When power is switched on :

- volume is preset at 0111 digital state, that is 2.8 V on volume output
- channel with greatest capacitor to the ground is activated

Ex. : on "typ. app. fig.", 22 nF has been connected to channel N

OSCILLATOR

The minimum resistor value on pin 14 is 30 KΩ.

T = C (160 R+ 1660) for V_{CC} = 12 V.
T = oscillator period (µs)
C = capacitance (µF)
R = resistance (KΩ)

NB (important) :

- When S – B is ON, 33 V tuning voltage must keep present. Otherwise all outputs are going to ground and consequently S – B is disabled.
- V^+ 12 V must be present to ensure output can accept 33 V.
- In any case, V_{CC} must be present on the circuit when V_{CHoff} is present (typically 33 V).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	10 → 15	V
V_{CHoff}	Voltage on "Channel off" Pins	35	V
I_{CHon}	Current on "Channel on" Pins	20	mA
V_{in}	PPM Input High Voltage	20	V
V_{SBon}	Stand–by on Voltage	15	V
I_{SBoff}	Stand–by off Current	2	mA
I_{VOL}	Volume Output Current (available)	2	mA
T_{oper}	Operating Ambient Temperature	0 to 70	°C
P_{tot}	Max Power Dissipation	500	mW

THERMAL DATA

Symbol	Parameter	Value	Unit
R_{th}(j–a)	Junction–ambient Thermal Resistance	70	°C/W

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V ; T_{amb} = + 25 °C (unless otherwise noted)

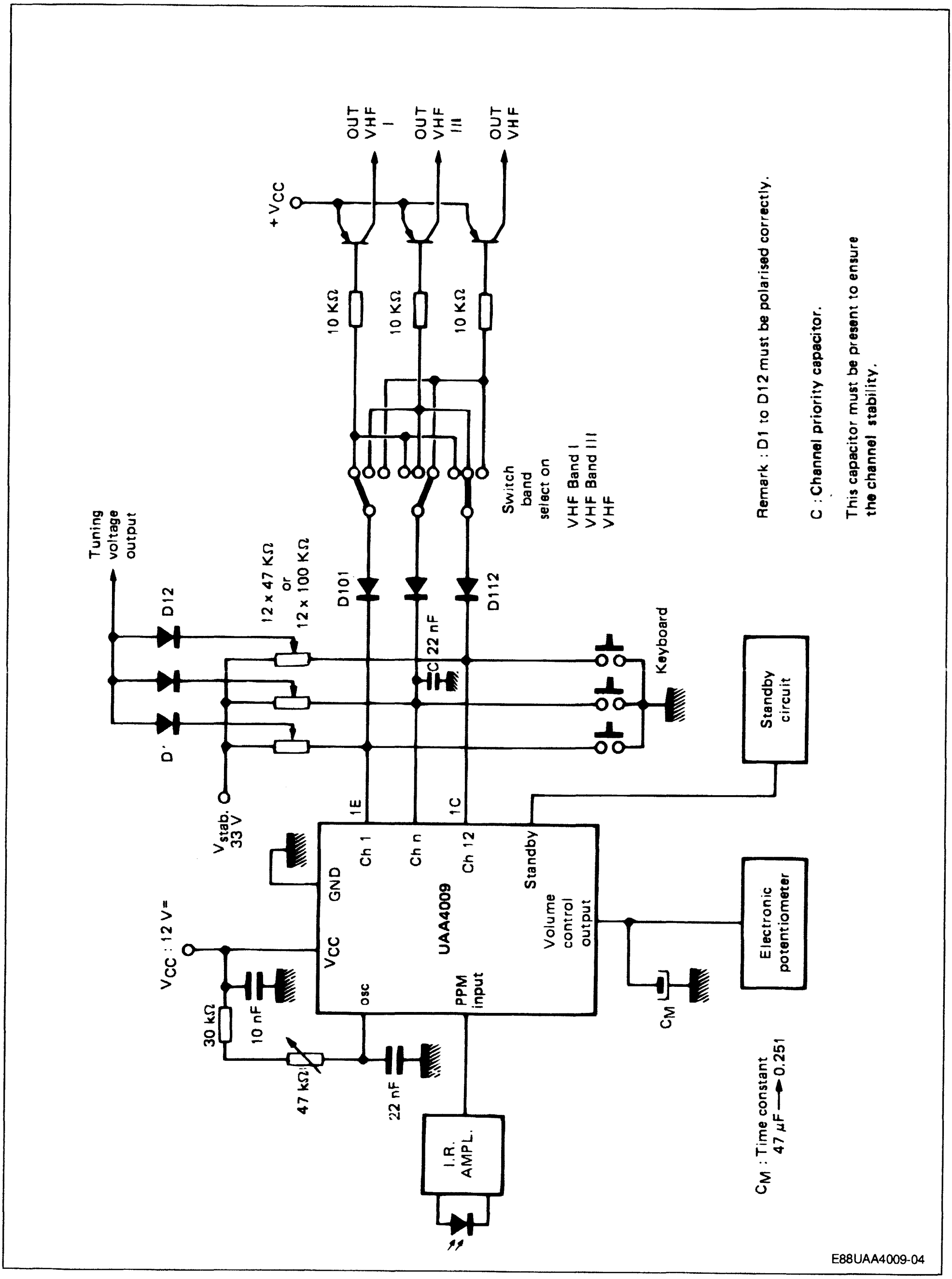
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	10	15	30	mA
V_{CHoff}	Voltage on "Channel off" Pins		33	35	V
I_{CHoff}	Current on "Channel off" Pins (V_{CHoff} = 33 V)			1	µA
V_{CHon}	Voltage on "Channel on" Pins (I_{CHon} = 10 mA)		50	80	mV
I_{CHon}	Current on "Channel on" PIns		10	20	mA
$\frac{\Delta V_{CHon}}{\Delta\theta}$	Temperature coefficient		150	300	µV/°C
V_{in}	PPM Input Low Voltage		0 to 3		V
I_{in}	PPm Input Low Current (V_{in} = 0 V)		– 30		µA
V_{in}	PPM Input High Voltage		5	20	V
I_{in}	PPM Input High Current (V_{in} = V_{CC} = 12 V)		2		µA
V_{SBon}	Stand–by on Voltage		V_{CC}	15	V
I_{SBon}	Stand–by on Current (V_{SBon} = 12 V)			1	µA
V_{SBoff}	Stand–by off Voltage (at I_{SBoff} = 1 mA)			0.15	V
I_{SBoff}	Stand–by off Current		1	2	mA
ΔV_{VOL}	Volume Voltage Swing (unloaded)	4.9	6	7	V
V_{VOL}	Volume Voltage (step zero)		50	100	mV
V_{VOLst}	Starting Volume Voltage		2.8		V
R_{OUTvol}	Volume Output Impedance (S–B off)	1.4	2	2.6	kΩ
R_{OUTVOL}	(S–B on)	35	50	65	Ω
I_{VOL}	Volume Output Current (available)			2	mA
$\frac{\Delta V_{VOL}}{\Delta\theta}$	Temp. Coefficient Volume–voltage (Load = 20 kΩ)		2		mV/°C
	V_{CC} Ripple Rejection (100 Hz)	30	40		dB
F_{osc}	Oscillator Frequency	0.5	5.1	10	kHz
T*	Optimum Oscillator Adjustement with UAA4000 Transmitter		1/29		t"1" transmitted
	Input Pulse Width	10			µs
t"1"	PPM Window for "1"	19.5		34.5	T*
t"0"	for "0"	35.5		66.5	T*
t"s"	for "synchro"	67.5		130.5	T*
f_{osc}	Oscillator Max Allowable Dispersion (transmitter f_{osc} = cst)			± 20	%
T_{ch}	Channel change delay		2 words+ 67 T*		
T_{VOL}	Volume Swing Average Delay	2.8	2.8x10[4]T*		s

T* : Receiver oscillator period at optimal frequency matching between transmitter and receiver.

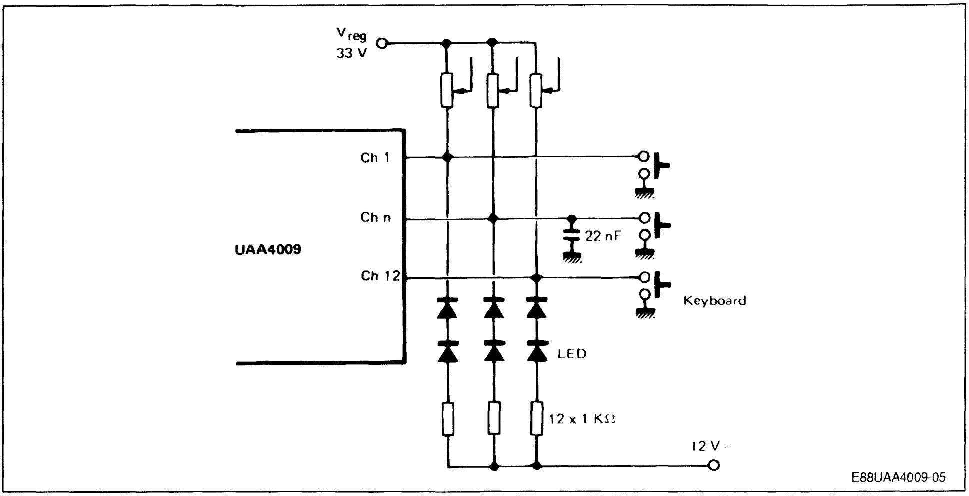
EXTERNAL FORCED SWITCHING

Symbol	Parameter	Min.	Typ.	Max.	Unit
	External Channel Activating Level			3.5	V
	Minimum Switching Time		20		µs

TYPICAL APPLICATION

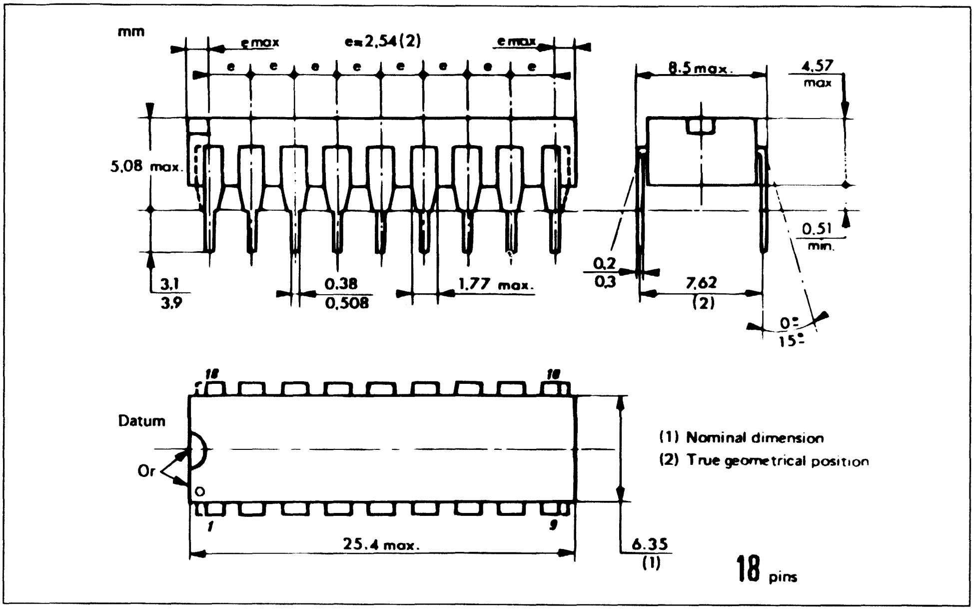


APPLICATION WITH LED DISPLAY



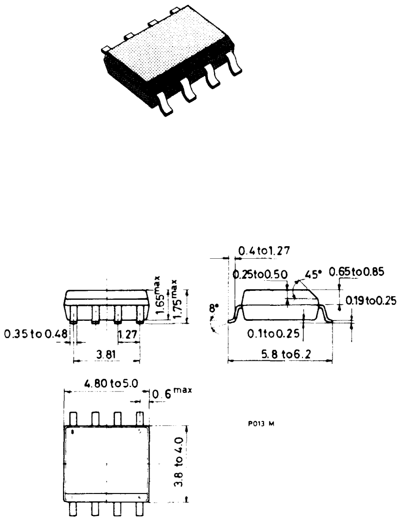
PACKAGE MECHANICAL DATA

18 PINS – PLASTIC DIP

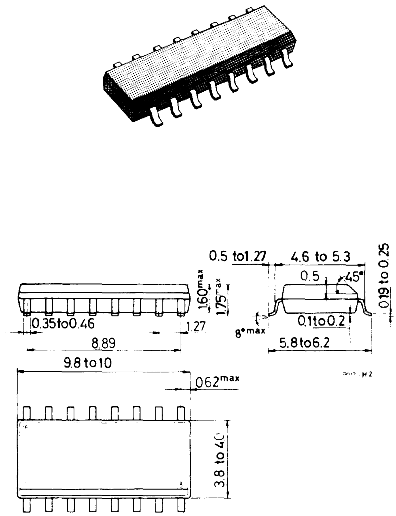


PACKAGES

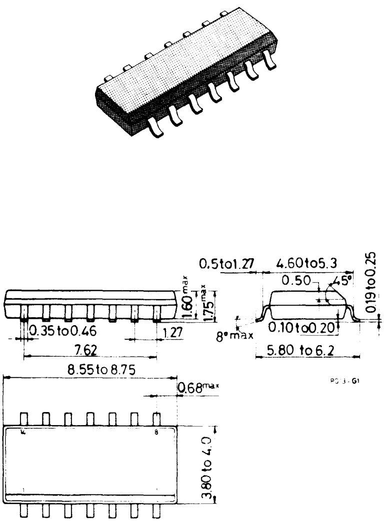
SO-8J



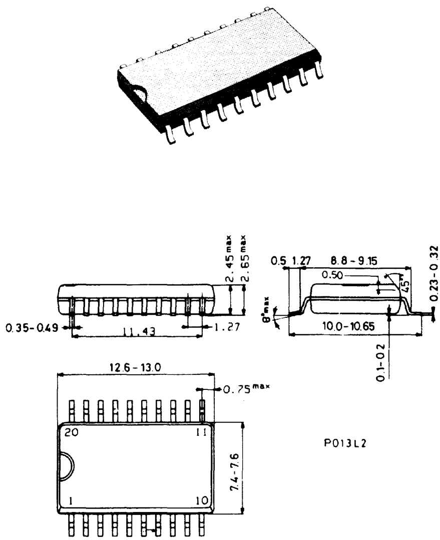
SO-16J



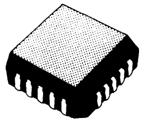
SO-14J

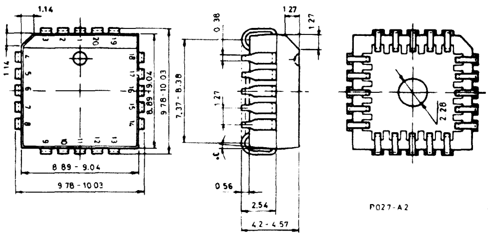


SO-20L
SO-20 (12+4+4)

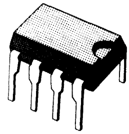


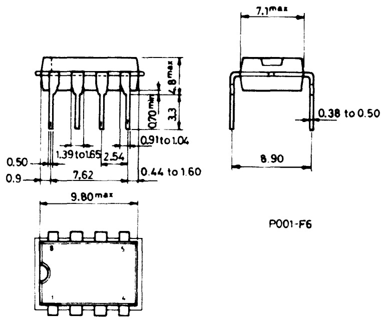
PLCC - 20 Plastic Chip Carrier
PLCC 15 +5



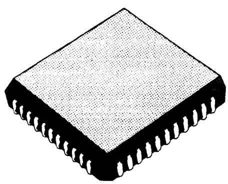


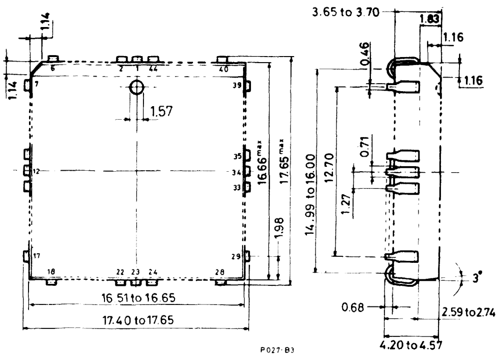
8 lead Plastic Minidip
4 + 4 lead Powerdip



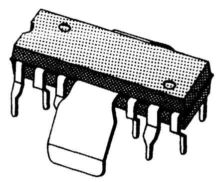


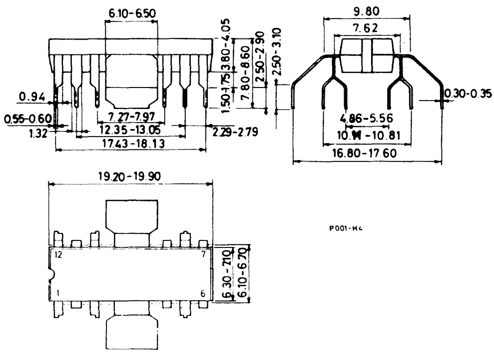
PLCC - 44 Plastic Chip Carrier





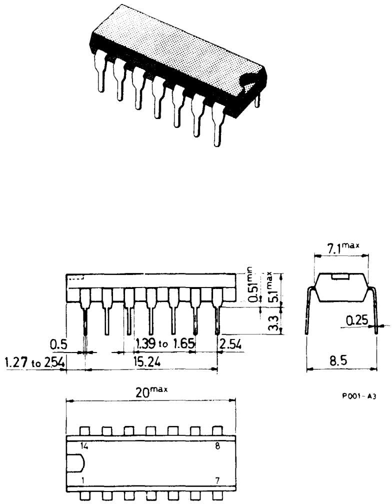
Findip



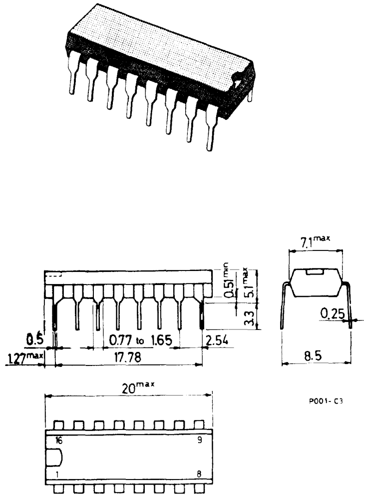


PACKAGES

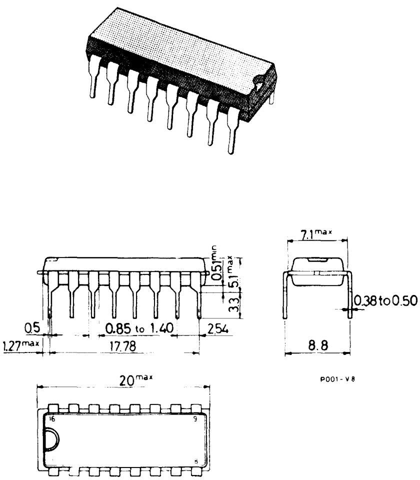
14 lead Plastic Dip



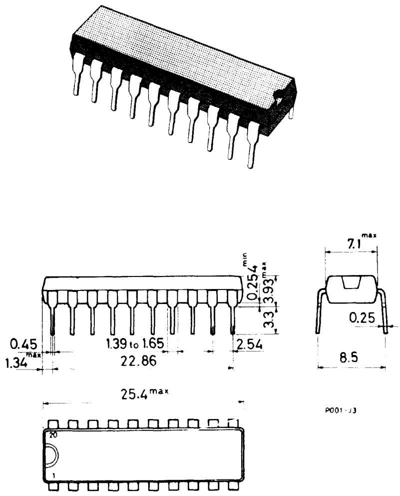
16 lead Plastic Dip (0.25)



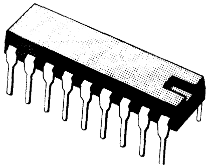
16 lead Plastic Dip (0.4)
8 + 8 lead Powerdip
12 + 2 + 2 lead Powerdip

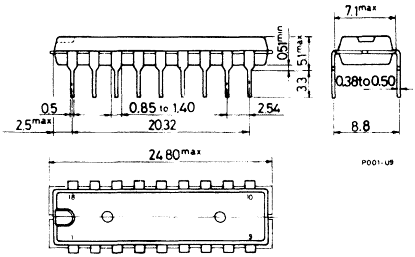


20 lead Plastic Dip (0.25)

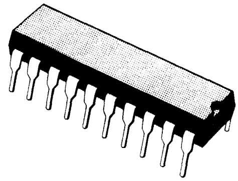


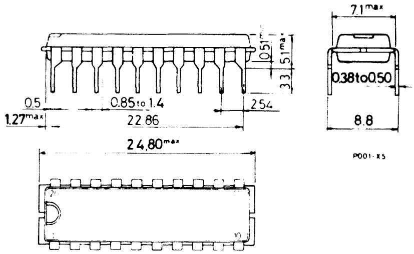
18 lead Plastic Dip
12 + 3 + 3 lead Powerdip
9 + 9 lead Powerdip



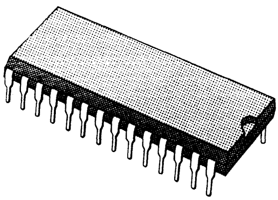


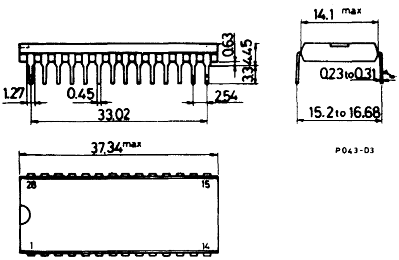
20 lead Plastic Dip (0.4)
16 + 2 + 2 Powerdip



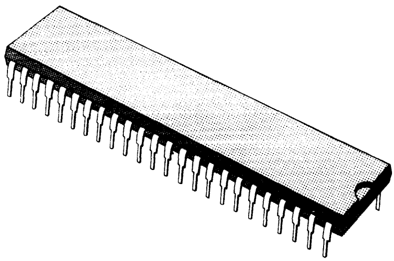


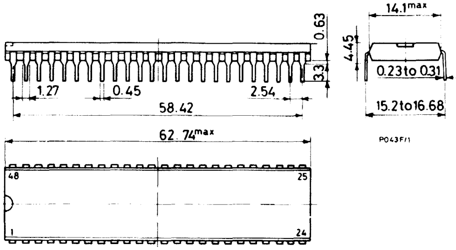
28 lead Plastic Dip



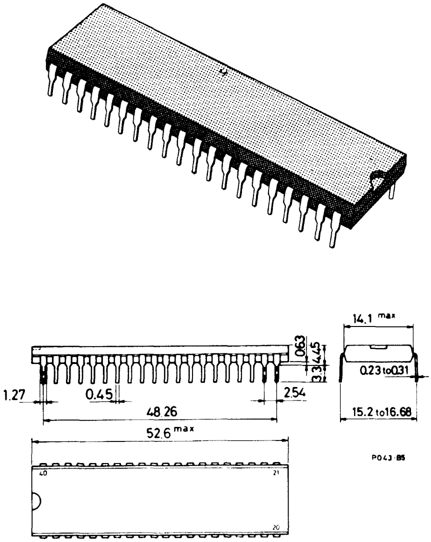


48 lead Plastic Dip

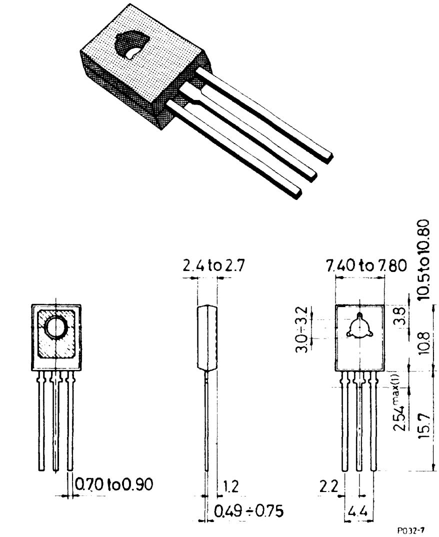




40 lead Plastic Dip

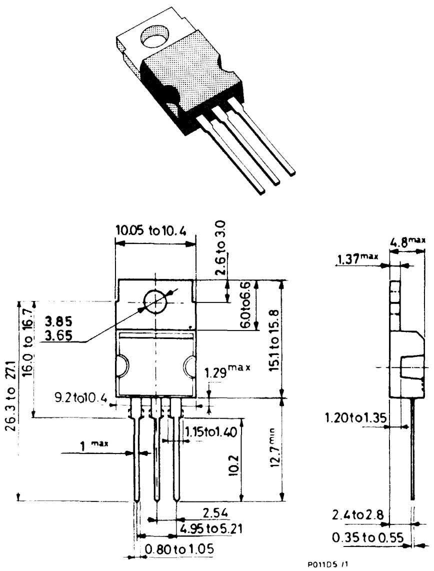


SOT-32 (TO-126)

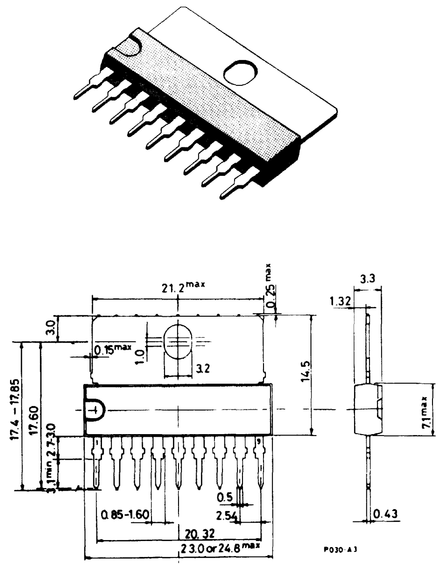


(1) Within this region the cross-section of the leads is uncontrolled

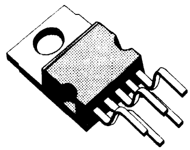
TO-220



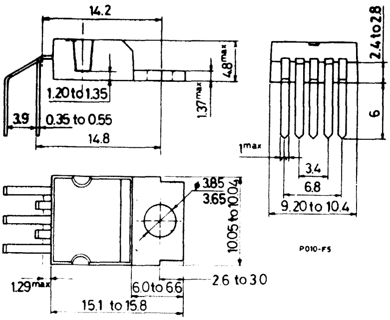
SIP-9
SIP-10



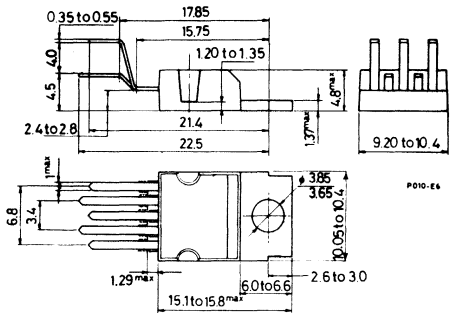
PENTAWATT



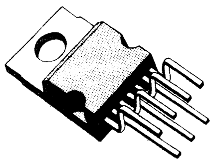
Horizontal Version



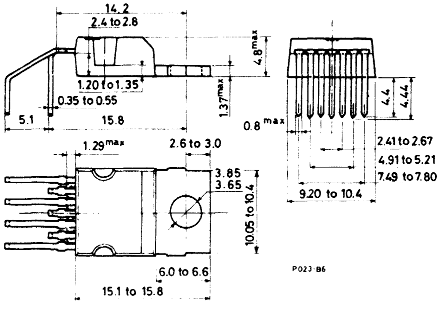
Vertical Version



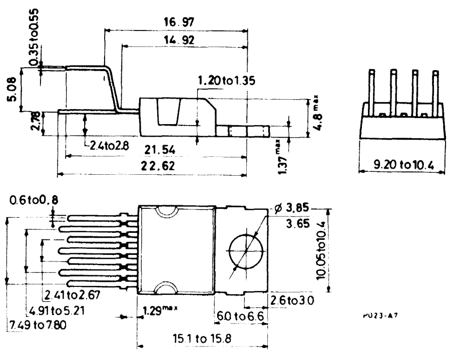
HEPTAWATT



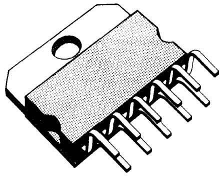
Horizontal Version

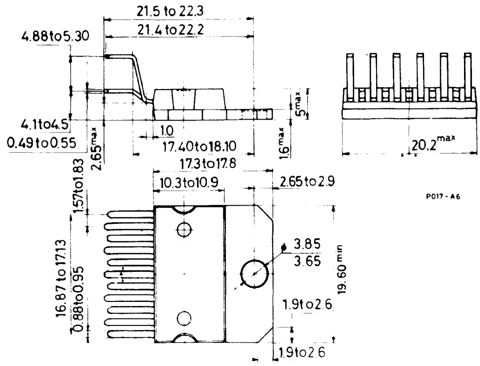


Vertical Version

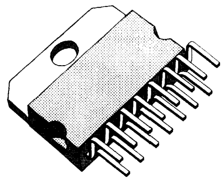


MULTIWATT-11

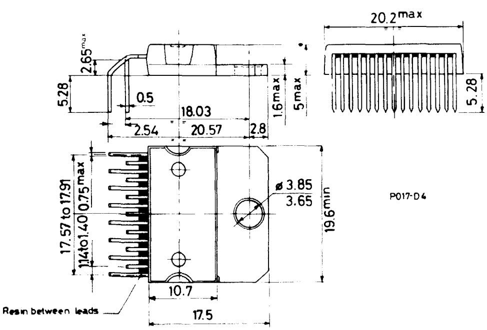




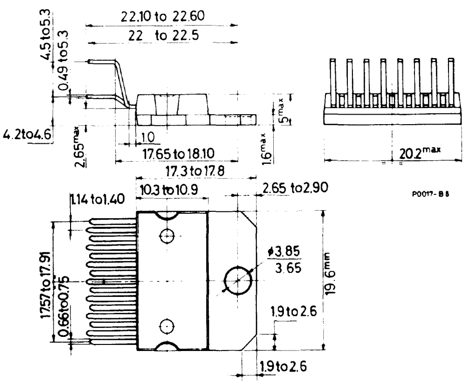
MULTIWATT-15



Horizontal Version



Vertical Version



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